Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!

Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

Si823x Data Sheet

0.5 and 4.0 Amp ISOdrivers (2.5 and 5 kV_{RMS})

The Si823x isolated driver family combines two independent, isolated drivers into a single package. The Si8230/1/3/4 are high-side/low-side drivers, and the Si8232/5/6/7/8 are dual drivers. Versions with peak output currents of 0.5 A (Si8230/1/2/7) and 4.0 A (Si8233/4/5/6/8) are available. All drivers operate with a maximum supply voltage of 24 V.

The Si823x drivers utilize Silicon Labs' proprietary silicon isolation technology, which provides up to 5 kV_{RMS} withstand voltage per UL1577 and fast 60 ns propagation times. Driver outputs can be grounded to the same or separate grounds or connected to a positive or negative voltage. The TTL level compatible inputs with >400 mV hysteresis are available in individual control input (Si8230/2/3/5/6/7/8) or PWM input (Si8231/4) configurations. High integration, low propagation delay, small installed size, flexibility, and cost-effectiveness make the Si823x family ideal for a wide range of isolated MOSFET/IGBT gate drive applications.

Applications

- Power delivery systems
- Motor control systems
- Isolated dc-dc power supplies
- Lighting control systems
- Plasma displays
- Solar and industrial inverters

Safety Approval

- UL 1577 recognized
  - Up to 5000 Vrms for 1 minute
- CSA component notice 5A approval
  - IEC 60950-1, 61010-1, 60601-1 (reinforced insulation)
- VDE certification conformity
  - IEC 60747-5-5 (VDE 0884 Part 5)
  - EN 60950-1 (reinforced insulation)
- CQC certification approval
  - GB4943.1

KEY FEATURES

- Two completely isolated drivers in one package
  - Up to 5 kV_{RMS} input-to-output isolation
  - Up to 1500 V_{DC} peak driver-to-driver differential voltage
- HS/LS and dual driver versions
- Up to 8 MHz switching frequency
- 0.5 A peak output (Si8230/1/2/7)
- 4.0 A peak output (Si8233/4/5/6/8)
- High electromagnetic immunity

1. Feature List

The Si823x highlighted features are listed below.

- Two completely isolated drivers in one package:
  - Up to 5 kV_{RMS} input-to-output isolation
  - Up to 1500 V_{DC} peak driver-to-driver differential voltage
- HS/LS and dual driver versions
- Up to 8 MHz switching frequency
- 0.5 A peak output (Si8230/1/2/7)
- 4.0 A peak output (Si8233/4/5/6/8)
- High electromagnetic immunity
- 60 ns propagation delay (max)
- Independent HS and LS inputs or PWM input versions
- Transient immunity > 45 kV/µs
- Overlap protection and programmable dead time
- AEC-Q100 qualification
- Wide operating range:
  - –40 to +125 °C
- RoHS-compliant packages:
  - SOIC-16 wide body
  - SOIC-16 narrow body
  - LGA-14

2. Ordering Guide

Table 2.1. Si823x Ordering Guide [1, 2]

Ordering Part Number (OPN)	Inputs	Configuration	Peak Current	UVLO Voltage	Isolation Rating	Temp Range	Package Type	Legacy Ordering Part Number (OPN) 2.5 kV Only
Wide Body (WB) Package Options								
Si8230BB-D-IS	VIA, VIB	High Side/ Low Side	0.5 A	8 V	2.5 kVrms	–40 to +125 °C	SOIC-16 Wide Body	Si8230-A-IS
Si8231BB-D-IS	PWM	High Side/ Low Side						Si8231-A-IS
Si8232BB-D-IS	VIA,VIB	Dual Driver						Si8232-A-IS
Si8234CB-D-IS	PWM	High Side/ Low Side	4.0 A	10 V				N/A
Si8233BB-D-IS	VIA,VIB	High Side/ Low Side		8 V				Si8233-B-IS
Si8234BB-D-IS	PWM	High Side/ Low Side						Si8234-B-IS
Si8235BB-D-IS	VIA,VIB	Dual Driver						Si8235-B-IS
Si8230AB-D-IS	VIA, VIB	High Side/ Low Side	0.5 A	5 V	2.5 kVrms	–40 to +125 °C	SOIC-16 Wide Body	N/A
Si8231AB-D-IS	PWM							N/A
Si8232AB-D-IS	VIA,VIB	Dual Driver						N/A
Si8233AB-D-IS	VIA,VIB	High Side/ Low Side	4.0 A	5 V				N/A
Si8234AB-D-IS	PWM							N/A
Si8235AB-D-IS	VIA,VIB	Dual Driver						N/A
Narrow Body (NB) Package Options								
Si8230BB-D-IS1	VIA,VIB	High Side/ Low Side	0.5 A	8 V	2.5 kVrms	–40 to +125 °C	SOIC-16 Narrow Body	N/A
Si8231BB-D-IS1	PWM	High Side/ Low Side						
Si8232BB-D-IS1	VIA,VIB	Dual Driver						
Si8233BB-D-IS1	VIA,VIB	High Side/ Low Side	4.0 A	8 V				
Si8234BB-D-IS1	PWM	High Side/ Low Side						
Si8235BB-D-IS1	VIA,VIB	Dual Driver						
Si8235BA-D-IS1	VIA,VIB	Dual Driver			1.0 kVrms			

Ordering Part Number (OPN)	Inputs	Configuration	Peak Current	UVLO Voltage	Isolation Rating	Temp Range	Package Type	Legacy Ordering Part Number (OPN) 2.5 kV Only
Si8230AB-D-IS1	VIA,VIB	High Side/ Low Side	0.5 A	5 V	2.5 kVrms	–40 to +125 °C	SOIC-16 Narrow Body	N/A
Si8231AB-D-IS1	PWM							N/A
Si8232AB-D-IS1	VIA,VIB	Dual Driver						N/A
Si8233AB-D-IS1	VIA,VIB	High Side/ Low Side	4.0 A	5 V				N/A
Si8234AB-D-IS1	PWM							N/A
Si8235AB-D-IS1	VIA,VIB	Dual Driver						N/A
LGA Package Options								
Si8233CB-D-IM	VIA,VIB	High Side/ Low Side	4.0 A	10 V	2.5 kVrms	–40 to +125 °C	LGA-14 5x5 mm	N/A
Si8233BB-D-IM				8 V				Si8233-B-IM
Si8233AB-D-IM				5 V				N/A
Si8234BB-D-IM	PWM			8 V				Si8234-B-IM
Si8234AB-D-IM				5 V				N/A
Si8235BB-D-IM	VIA,VIB	Dual Driver		8 V				Si8235-B-IM
Si8235AB-D-IM				5 V				N/A
Si8236BA-D-IM				8 V	1.0 kVrms		LGA-14 5x5 mm with Thermal Pad	Si8236-B-IM
Si8236AA-D-IM				5 V				N/A
5 kV Ordering Options								
Si8230BD-D-IS	VIA, VIB	High Side/ Low Side	0.5 A	8 V	5.0 kVrms	–40 to +125 °C	SOIC-16 Wide Body	N/A
Si8231BD-D-IS	PWM	High Side/ Low Side						
Si8232BD-D-IS	VIA, VIB	Dual Driver						
Si8233BD-D-IS	VIA, VIB	High Side/ Low Side	4.0 A					
Si8234BD-D-IS	PWM	High Side/ Low Side						
Si8235BD-D-IS	VIA, VIB	Dual Driver						
Si8230AD-D-IS	VIA, VIB	High Side/ Low Side	0.5 A	5 V	5.0 kVrms	–40 to +125 °C	SOIC-16 Wide Body	N/A
Si8231AD-D-IS	PWM							N/A
Si8232AD-D-IS	VIA, VIB	Dual Driver						N/A
Si8233AD-D-IS	VIA, VIB	High Side/ Low Side	4.0 A	5 V				N/A
Si8234AD-D-IS	PWM							N/A
Si8235AD-D-IS	VIA, VIB	Dual Driver						N/A
3 V VDDI Ordering Options								

Ordering Part Number (OPN)	Inputs	Configuration	Peak Current	UVLO Voltage	Isolation Rating	Temp Range	Package Type	Legacy Ordering Part Number (OPN) 2.5 kV Only
Si8237AB-D-IS1	VIA, VIB	Dual Driver	0.5 A	5 V	2.5 kVrms	–40 to +125 °C	SOIC-16 Narrow Body	N/A
Si8237BB-D-IS1	VIA, VIB	Dual Driver		8 V				
Si8238AB-D-IS1	VIA, VIB	Dual Driver	4.0 A	5 V				
Si8238BB-D-IS1	VIA, VIB	Dual Driver		8 V				
Si8237AD-D-IS	VIA, VIB	Dual Driver	0.5 A	5 V	5.0 kVrms		SOIC-16 Wide Body	
Si8237BD-D-IS	VIA, VIB	Dual Driver		8 V				
Si8238AD-D-IS	VIA, VIB	Dual Driver	4.0 A	5 V				
Si8238BD-D-IS	VIA, VIB	Dual Driver		8 V				

1. All packages are RoHS-compliant with peak reflow temperatures of 260 °C according to the JEDEC industry standard classifications and peak solder temperatures.
2. “Si” and “SI” are used interchangeably.

3. System Overview

3.1 Top Level Block Diagrams

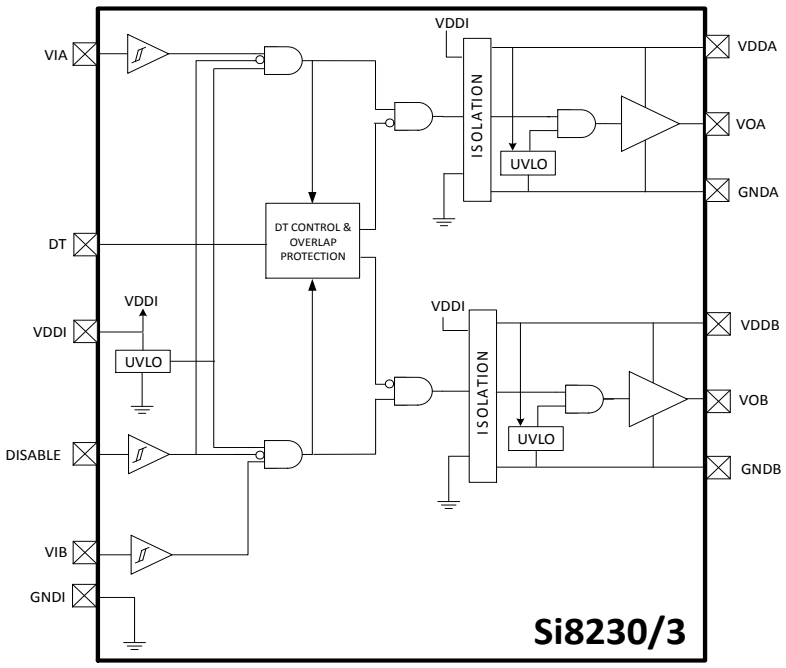


Figure 3.1. Si8230/3 Two-Input High-Side/Low-Side Isolated Drivers

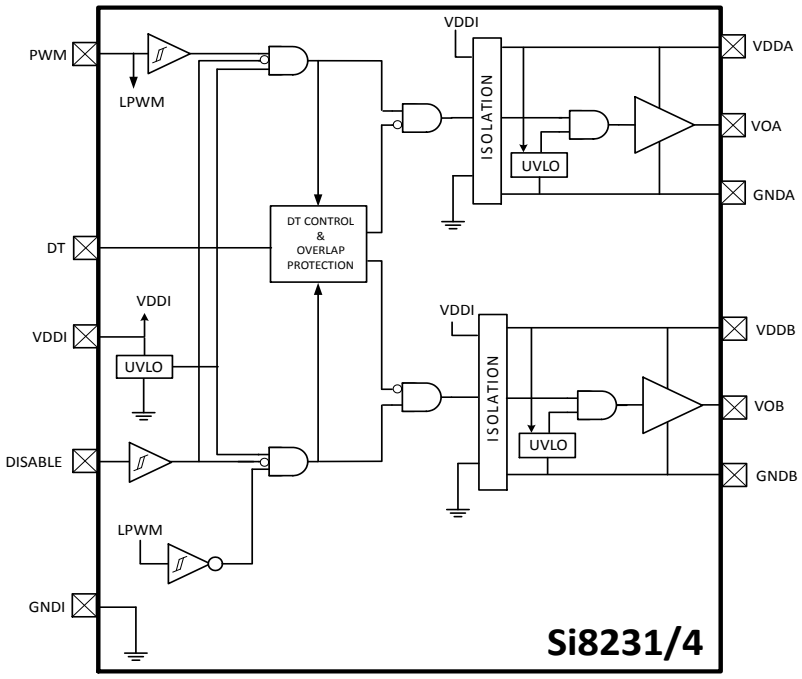


Figure 3.2. Si8231/4 Single-Input High-Side/Low-Side Isolated Drivers

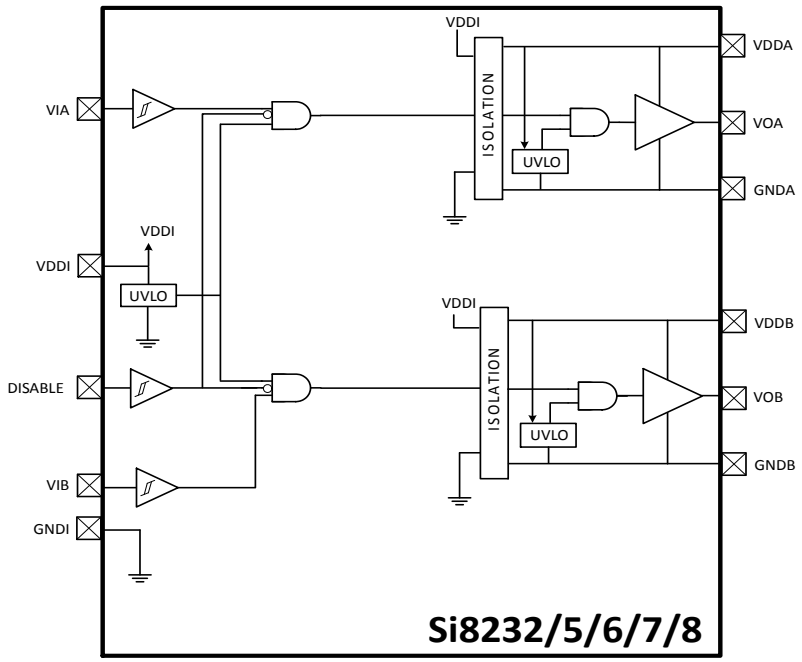


Figure 3.3. Si8232/5/6/7/8 Dual Isolated Drivers

3.2 Functional Description

The operation of an Si823x channel is analogous to that of an optocoupler and gate driver, except an RF carrier is modulated instead of light. This simple architecture provides a robust isolated data path and requires no special considerations or initialization at start-up. A simplified block diagram for a single Si823x channel is shown in the figure below.

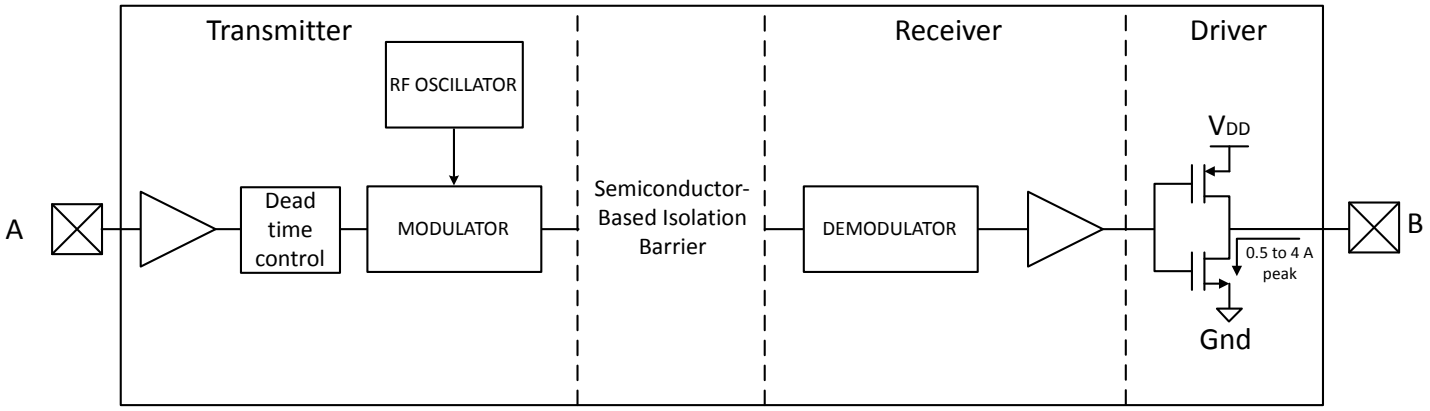


Figure 3.4. Simplified Channel Diagram

A channel consists of an RF Transmitter and RF Receiver separated by a semiconductor-based isolation barrier. Referring to the Transmitter, input A modulates the carrier provided by an RF oscillator using on/off keying. The Receiver contains a demodulator that decodes the input state according to its RF energy content and applies the result to output B via the output driver. This RF on/off keying scheme is superior to pulse code schemes as it provides best-in-class noise immunity, low power consumption, and better immunity to magnetic fields. See the figure below for more details.

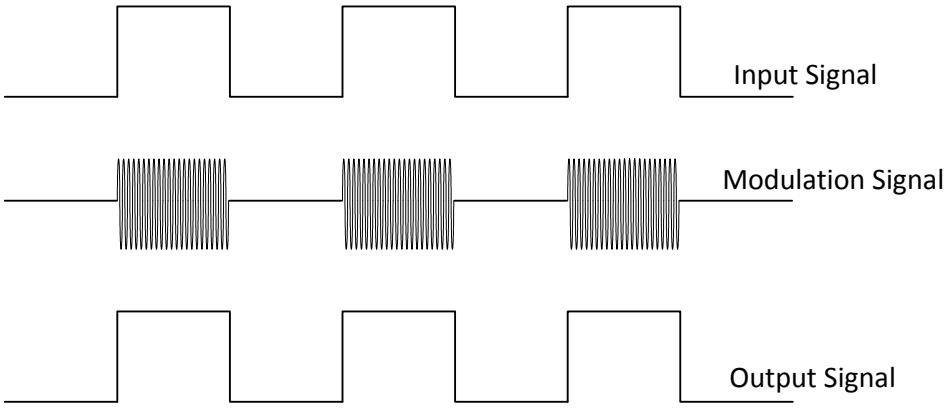


Figure 3.5. Modulation Scheme

3.3 Typical Operating Characteristics (0.5 Amp)

The typical performance characteristics depicted in Figure 3.6 Rise/Fall Time vs. Supply Voltage on page 8 through Figure 3.15 Output Source Current vs. Temperature on page 9 are for information purposes only. Refer to Table 4.1 Electrical Characteristics[1] on page 21 for actual specification limits.

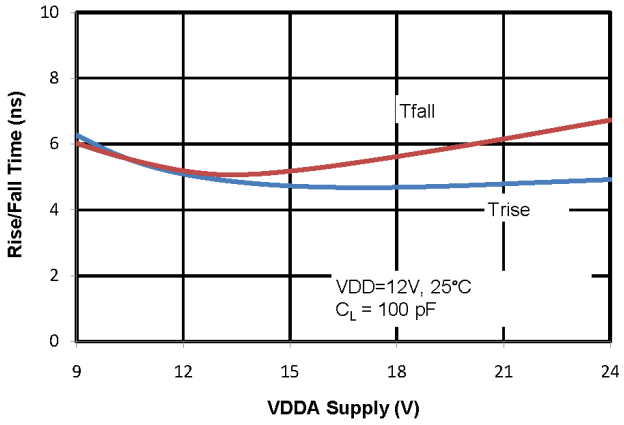


Figure 3.6. Rise/Fall Time vs. Supply Voltage

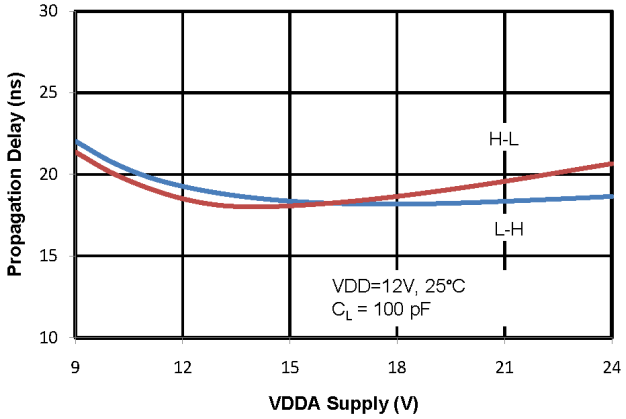


Figure 3.7. Propagation Delay vs. Supply Voltage

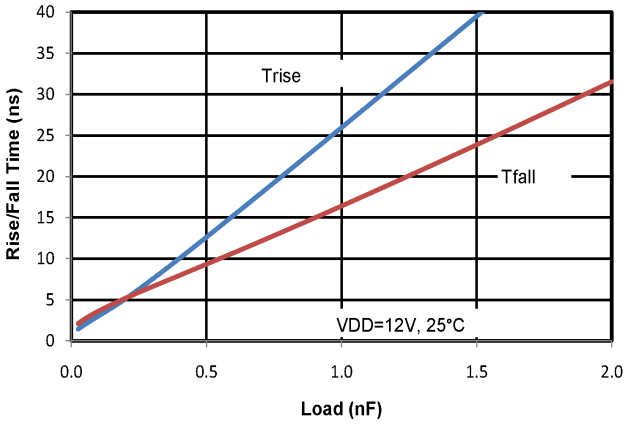


Figure 3.8. Rise/Fall Time vs. Load

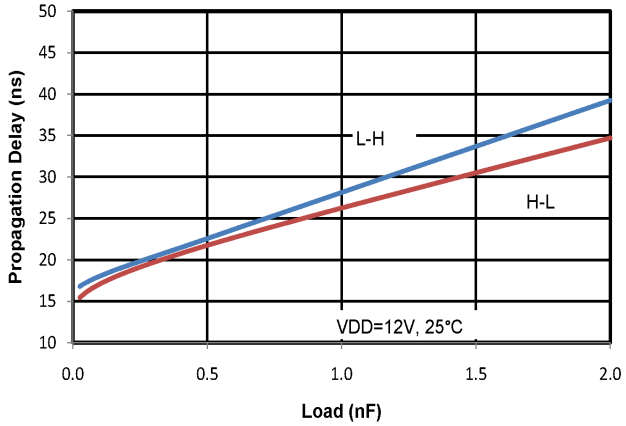


Figure 3.9. Propagation Delay vs. Load

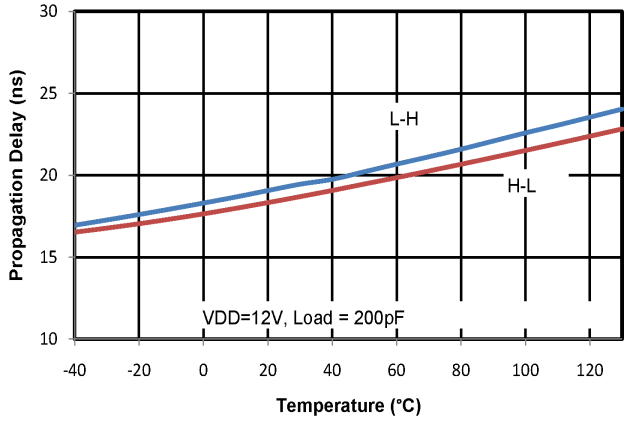


Figure 3.10. Propagation Delay vs. Temperature

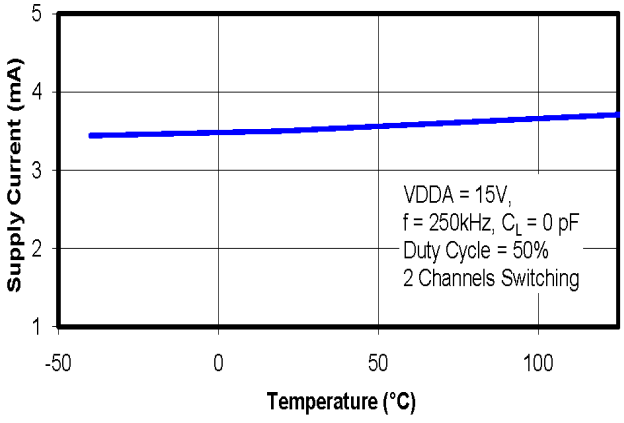


Figure 3.11. Supply Current vs. Temperature

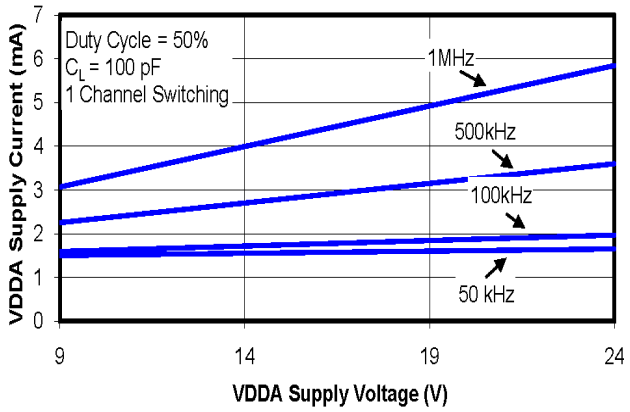


Figure 3.12. Supply Current vs. Supply Voltage

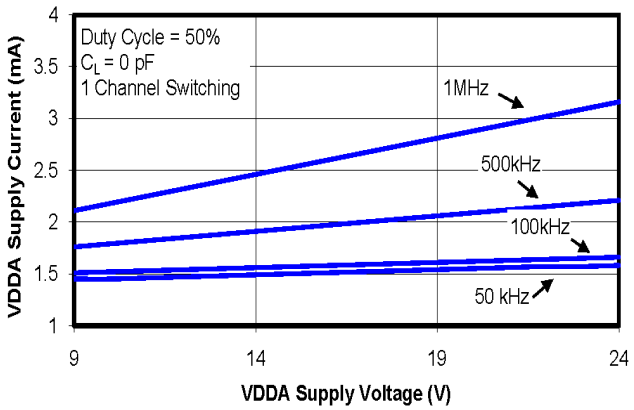


Figure 3.13. Supply Current vs. Supply Voltage

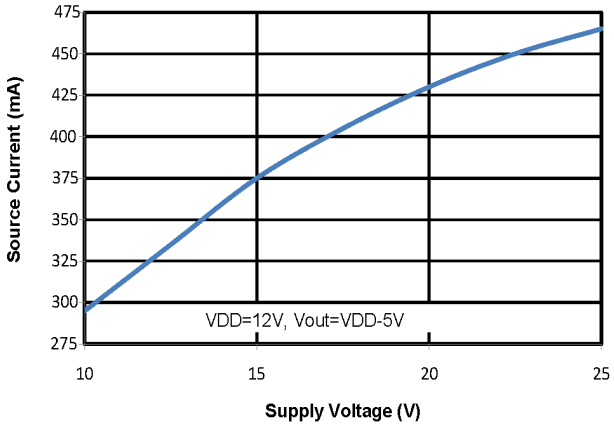


Figure 3.14. Output Source Current vs. Supply Voltage

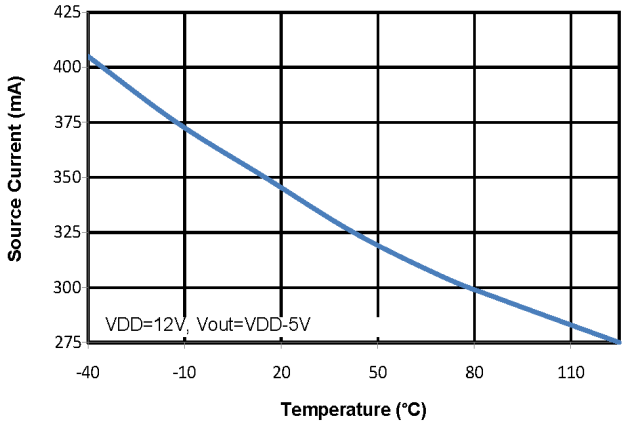


Figure 3.15. Output Source Current vs. Temperature

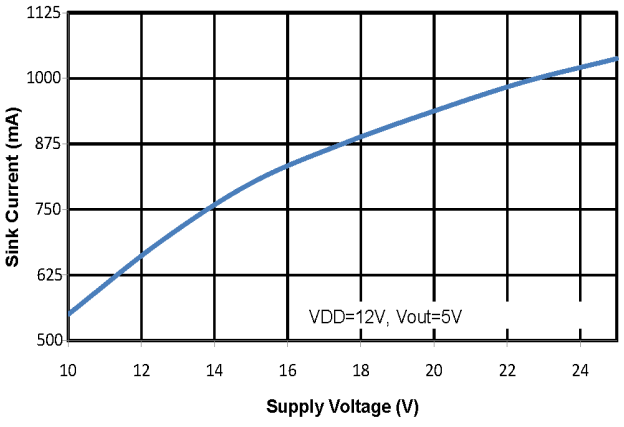


Figure 3.16. Output Sink Current vs. Supply Voltage

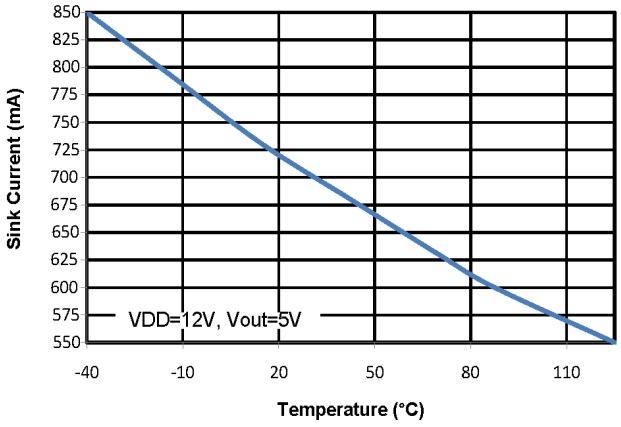


Figure 3.17. Output Sink Current vs. Temperature

3.4 Typical Operating Characteristics (4.0 Amp)

The typical performance characteristics depicted in Figure 3.18 Rise/Fall Time vs. Supply Voltage on page 10 through Figure 3.27 Output Source Current vs. Temperature on page 11 are for information purposes only. Refer to Table 4.1 Electrical Characteristics[1] on page 21 for actual specification limits.

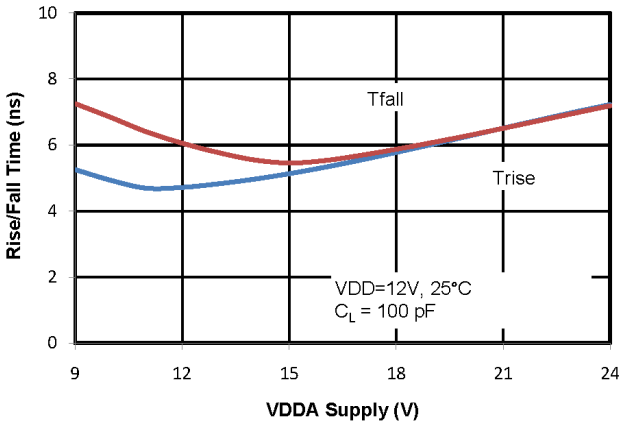


Figure 3.18. Rise/Fall Time vs. Supply Voltage

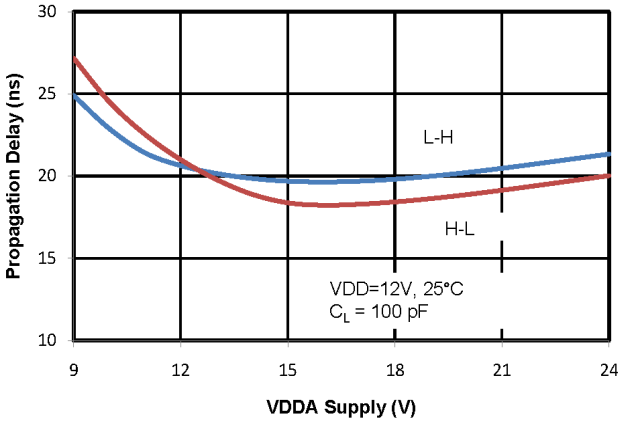


Figure 3.19. Propagation Delay vs. Supply Voltage

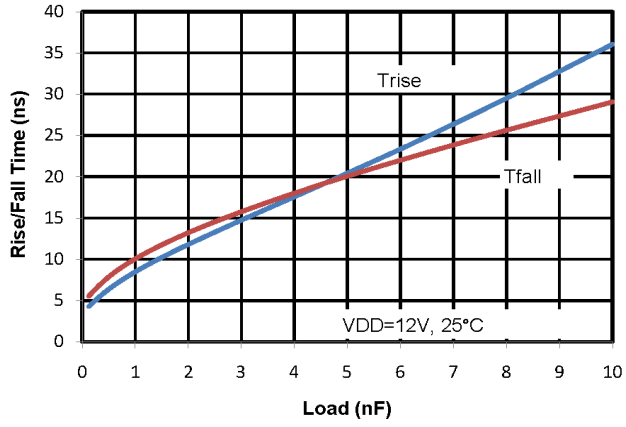


Figure 3.20. Rise/Fall Time vs. Load

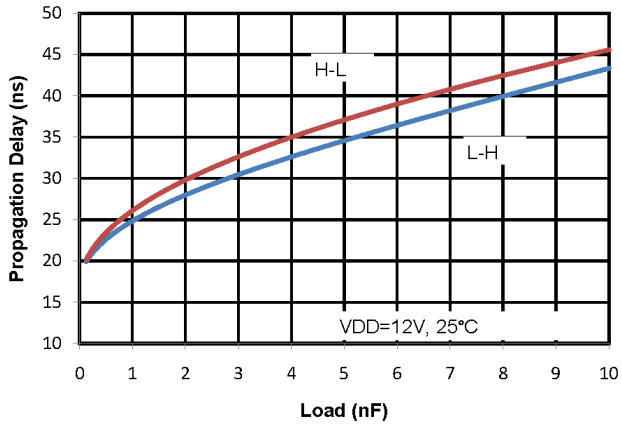


Figure 3.21. Propagation Delay vs. Load

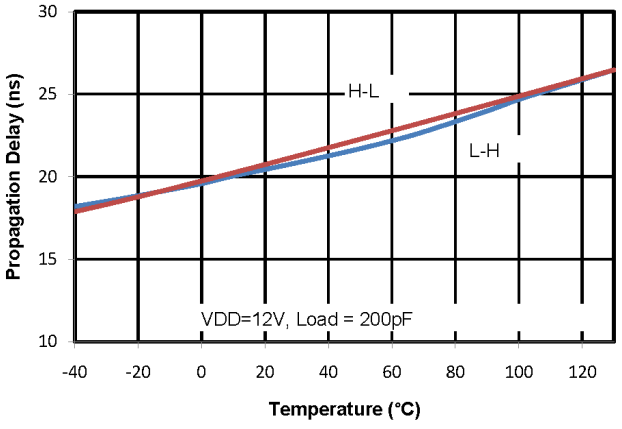


Figure 3.22. Propagation Delay vs. Temperature

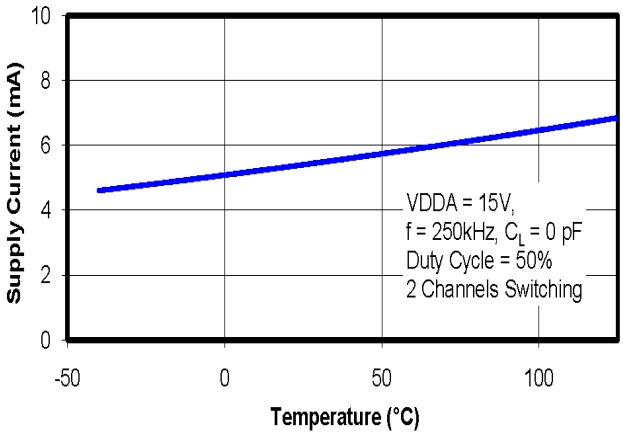


Figure 3.23. Supply Current vs. Temperature

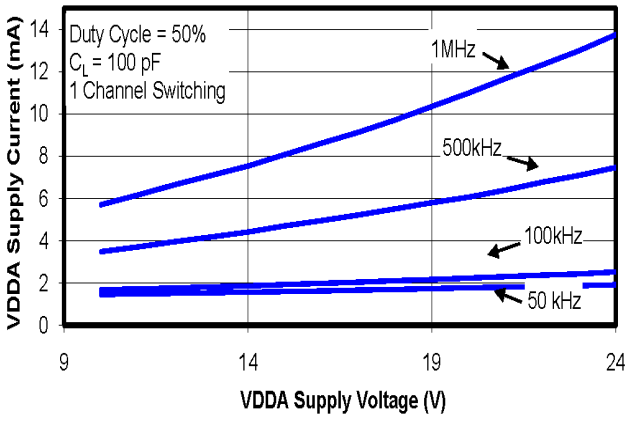


Figure 3.24. Supply Current vs. Supply Voltage

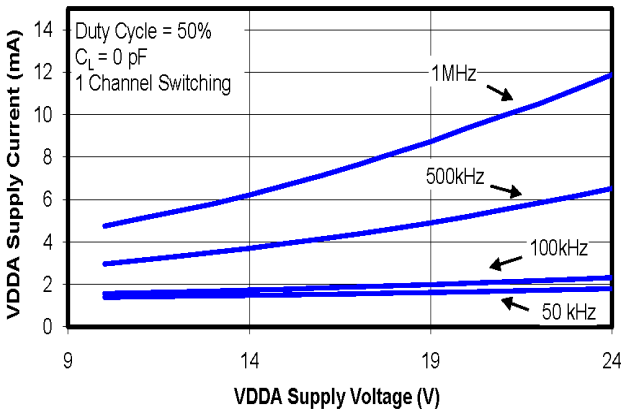


Figure 3.25. Supply Current vs. Supply Voltage

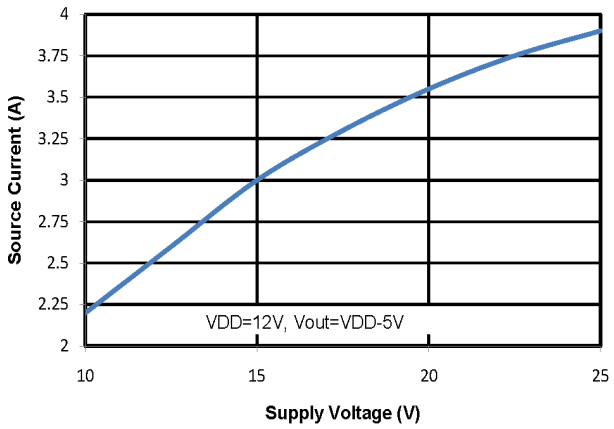


Figure 3.26. Output Source Current vs. Supply Voltage

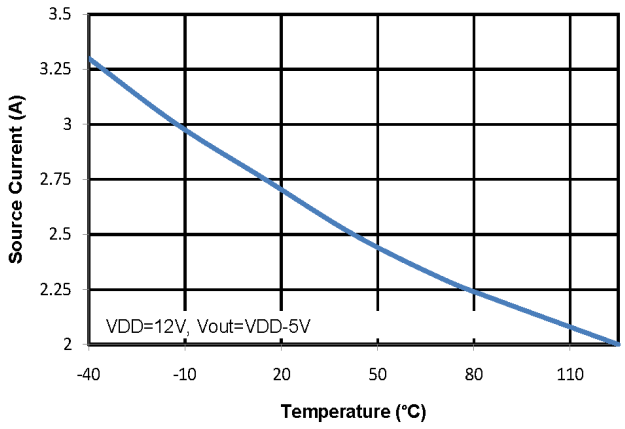


Figure 3.27. Output Source Current vs. Temperature

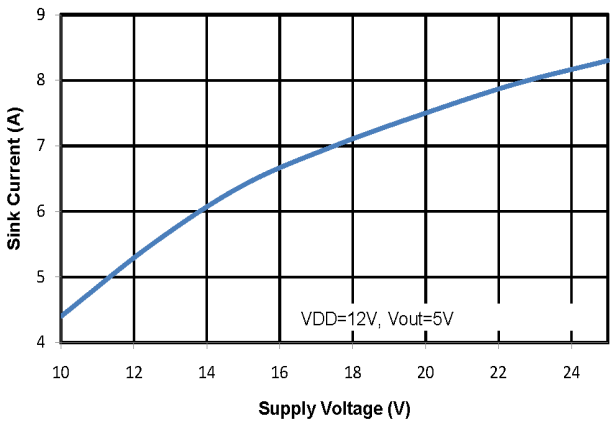


Figure 3.28. Output Sink Current vs. Supply Voltage

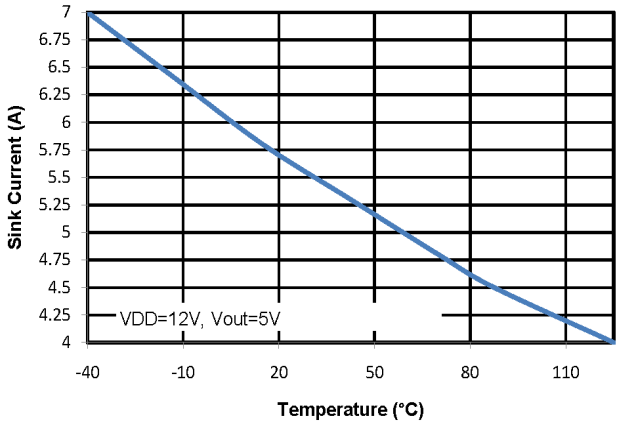


Figure 3.29. Output Sink Current vs. Temperature

3.5 Family Overview and Logic Operation During Startup

The Si823x family of isolated drivers consists of high-side, low-side, and dual driver configurations.

3.5.1 Products

The table below shows the configuration and functional overview for each product in this family.

Table 3.1. Si823x Family Overview

Part Number	Configuration	Overlap Protection	Programmable Dead Time	Inputs	Peak Output Current (A)
Si8230	High-Side/Low-Side	√	√	VIA, VIB	0.5
Si8231	High-Side/Low-Side	√	√	PWM	0.5
Si8232/7	Dual Driver	—	—	VIA, VIB	0.5
Si8233	High-Side/Low-Side	√	√	VIA, VIB	4.0
Si8234	High-Side/Low-Side	√	√	PWM	4.0
Si8235/6/8	Dual Driver	—	—	VIA, VIB	4.0

3.5.2 Device Behavior

The table below consists of truth tables for the Si8230/3, Si8231/4, and Si8232/5/6 families.

Table 3.2. Si823x Family Truth Table[1]

Si8230/3 (High-Side/Low-Side) Truth Table						
Inputs		**VDDI State**	**Disable**	**Output**		**Notes**
VIA	**VIB**			**VOA**	**VOB**	
L	L	Powered	L	L	L	Output transition occurs after internal dead time expires.
L	H	Powered	L	L	H	Output transition occurs after internal dead time expires.
H	L	Powered	L	H	L	Output transition occurs after internal dead time expires.
H	H	Powered	L	L	L	Invalid state. Output transition occurs after internal dead time expires.
X[2]	X[2]	Unpowered	X	L	L	Output returns to input state within 7 µs of VDDI power restoration.
X	X	Powered	H	L	L	Device is disabled.
Si8231/4 (PWM Input High-Side/Low-Side) Truth Table						
PWM Input		**VDDI State**	**Disable**	**Output**		**Notes**
				VOA	**VOB**	
H		Powered	L	H	L	Output transition occurs after internal dead time expires.
L		Powered	L	L	H	Output transition occurs after internal dead time expires.
X[2]		Unpowered	X	L	L	Output returns to input state within 7 µs of VDDI power restoration.
X		Powered	H	L	L	Device is disabled.
Si8232/5/6/7/8 (Dual Driver) Truth Table						
Inputs		**VDDI State**	**Disable**	**Output**		**Notes**
VIA	**VIB**			**VOA**	**VOB**	
L	L	Powered	L	L	L	Output transition occurs immediately (no internal dead time).
L	H	Powered	L	L	H	Output transition occurs immediately (no internal dead time).
H	L	Powered	L	H	L	Output transition occurs immediately (no internal dead time).
H	H	Powered	L	H	H	Output transition occurs immediately (no internal dead time).
X[2]	X[2]	Unpowered	X	L	L	Output returns to input state within 7 µs of VDDI power restoration.
X	X	Powered	H	L	L	Device is disabled.

Notes:

1. This truth table assumes VDDA and VDDB are powered. If VDDA and VDDB are below UVLO, see 3.9 Undervoltage Lockout Operation for more information.
2. Note that an input can power the input die through an internal diode if its source has adequate current.

3.6 Power Supply Connections

Isolation requirements mandate individual supplies for VDDI, VDDA, and VDDB. The decoupling caps for these supplies must be placed as close to the VDD and GND pins of the Si823x as possible. The optimum values for these capacitors depend on load current and the distance between the chip and the regulator that powers it. Low effective series resistance (ESR) capacitors, such as Tantalum, are recommended.

3.7 Power Dissipation Considerations

Proper system design must assure that the Si823x operates within safe thermal limits across the entire load range.The Si823x total power dissipation is the sum of the power dissipated by bias supply current, internal parasitic switching losses, and power dissipated by the series gate resistor and load. Equation 1 shows total Si823x power dissipation.

$$P_D = (V_{DDI})(I_{DDI}) + 2(I_{DD2})(V_{DD2}) + \left(f\right)\left(Q_{TL}\right)\left(V_{DD2}\right)\left[\frac{R_p}{R_p + R_g}\right] + \left(f\right)\left(Q_{TL}\right)\left(V_{DD2}\right)\left[\frac{R_p}{R_p + R_g}\right] + 2fCintV_{DD2}{}^2$$

where:

P_D is the total Si823x device power dissipation (W)

I_{DDI} is the input-side maximum bias current (3 mA)

I_{DD2} is the driver die maximum bias current (2.5 mA)

C_{int} is the internal parasitic capacitance (75 pF for the 0.5 A driver and 370 pF for the 4.0 A driver)

VDDI is the input-side VDD supply voltage (2.7 to 5.5 V)

V_{DD2} is the driver-side supply voltage (10 to 24 V)

f is the switching frequency (Hz)

Q_{TL} is the gate charge of the FET being driven

R_G is the external gate resistor

R_P is the $R_{DS(ON)}$ of the driver pull-up switch: (Rp = 15 Ω for the 0.5 A driver; Rp = 2.7 Ω for the 4.0 A driver)

R_n is the $R_{DS(ON)}$ of the driver pull-down switch: (Rn = 5 Ω for the 0.5 A driver and 1 Ω for the 4.0 A driver)

Equation 1.

Power dissipation example for 0.5 A driver using Equation 1 with the following givens:

V_{DDI} = 5.0 V

V_{DD2} = 12 V

f = 350 kHz

R_G = 22 Ω

Q_G = 25 nC

$$Pd = 0.015 + 0.060 + \left(350 \times 10^3\right)\left(25 \times 10^{-9}\right)\left(12\right)\left[\frac{5}{5 + 22}\right] + 2\left[\left(350 \times 10^3\right)\left(75 \times 10^{-12}\right)(144)\right] = 145\ \text{mW}$$

From which the driver junction temperature is calculated using Equation 2, where:

Pd is the total Si823x device power dissipation (W)

θja is the thermal resistance from junction to air (105 °C/W in this example)

T_A is the ambient temperature

$$T_j = P_d \times \Theta_{ja} \times T_A = (0.145)(105) + 20 = 35.2^oC$$

The maximum power dissipation allowable for the Si823x is a function of the package thermal resistance, ambient temperature, and maximum allowable junction temperature, as shown in Equation 2:

$$P_{Dmax} \leq \frac{T_{jmax} - T_A}{\Theta ja}$$

where:

P_{Dmax} = Maximum Si823x power dissipation (W)

T_{jmax} = Si823x maximum junction temperature (150 °C)

T_A = Ambient temperature (°C)

Θja = Si823x junction-to-air thermal resistance (105 °C/W)

f = Si823x switching frequency (Hz)

Equation 2.

Substituting values for P_{Dmax} T_{jmax}, T_A, and θ_{ja} into Equation 2 results in a maximum allowable total power dissipation of 1.19 W. Maximum allowable load is found by substituting this limit and the appropriate data sheet values from Table 4.1 Electrical Characteristics[1] on page 21 into Equation 1 and simplifying. The result is Equation 3 (0.5 A driver) and Equation 4 (4.0 A driver), both of which assume VDDI = 5 V and VDDA = VDDB = 18 V.

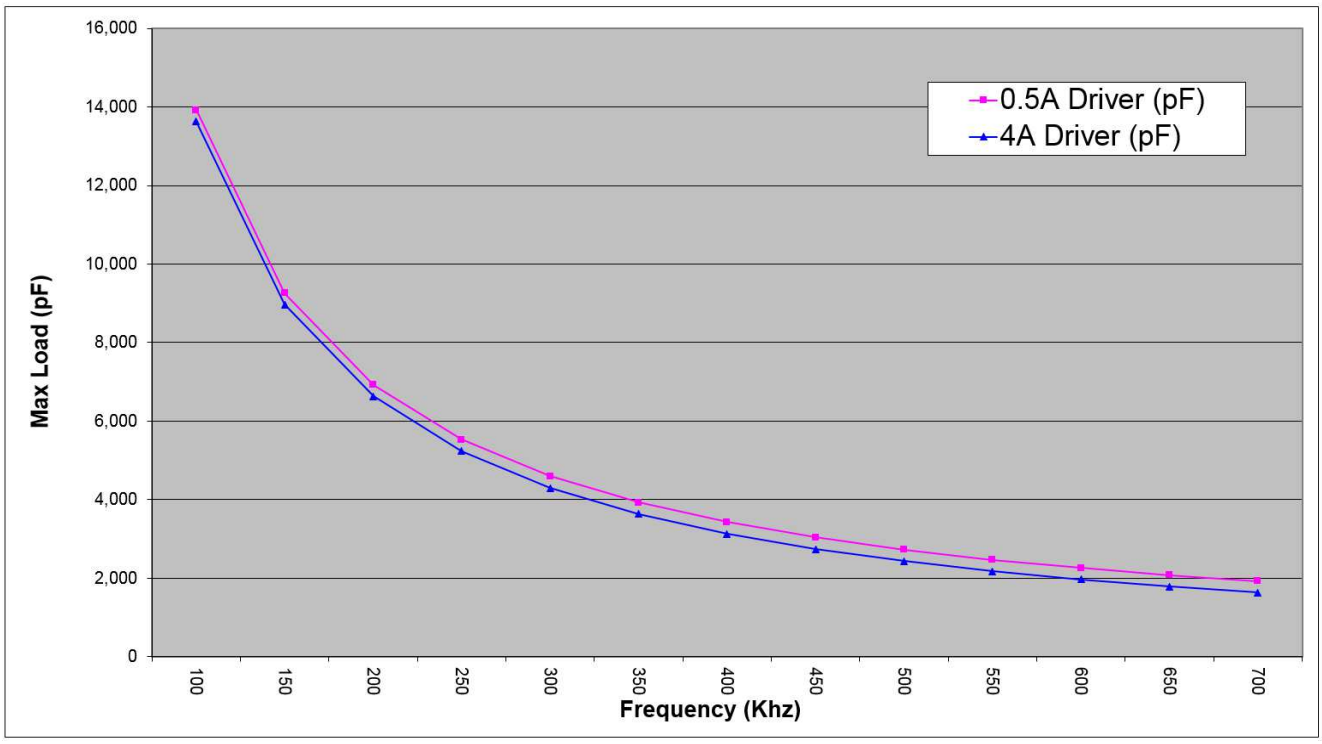
$$C_{L(MAX)} = \frac{1.4 \times 10^{-3}}{f} - 7.5 \times 10^{-11}$$

Equation 3.

$$C_{L(MAX)} = \frac{1.4 \times 10^{-3}}{f} - 3.7 \times 10^{-10}$$

Equation 4.

Equation 3 and Equation 4 are graphed in the figure below, where the points along the load line represent the package dissipation-limited value of CL for the corresponding switching frequency.



3.8 Layout Considerations

It is most important to minimize ringing in the drive path and noise on the Si823x VDD lines. Care must be taken to minimize parasitic inductance in these paths by locating the Si823x as close to the device it is driving as possible. In addition, the VDD supply and ground trace paths must be kept short. For this reason, the use of power and ground planes is highly recommended. A split ground plane system having separate ground and VDD planes for power devices and small signal components provides the best overall noise performance.

3.9 Undervoltage Lockout Operation

Device behavior during start-up, normal operation and shutdown is shown in Figure 3.30 Device Behavior during Normal Operation and Shutdown on page 17, where UVLO+ and UVLO- are the positive-going and negative-going thresholds respectively. Note that outputs VOA and VOB default low when input side power supply (VDDI) is not present.

3.9.1 Device Startup

Outputs VOA and VOB are held low during power-up until VDD is above the UVLO threshold for time period tSTART. Following this, the outputs follow the states of inputs VIA and VIB.

3.9.2 Undervoltage Lockout

Undervoltage Lockout (UVLO) is provided to prevent erroneous operation during device startup and shutdown or when VDD is below its specified operating circuits range. The input (control) side, Driver A and Driver B, each have their own undervoltage lockout monitors.

The Si823x input side enters UVLO when VDDI $\leq$ $VDDI_{UV-}$, and exits UVLO when VDDI > $VDDI_{UV+}$. The driver outputs, VOA and VOB, remain low when the input side of the Si823x is in UVLO and their respective VDD supply (VDDA, VDDB) is within tolerance. Each driver output can enter or exit UVLO independently. For example, VOA unconditionally enters UVLO when VDDA falls below $VDDA_{UV-}$ and exits UVLO when VDDA rises above $VDDA_{UV+}$.

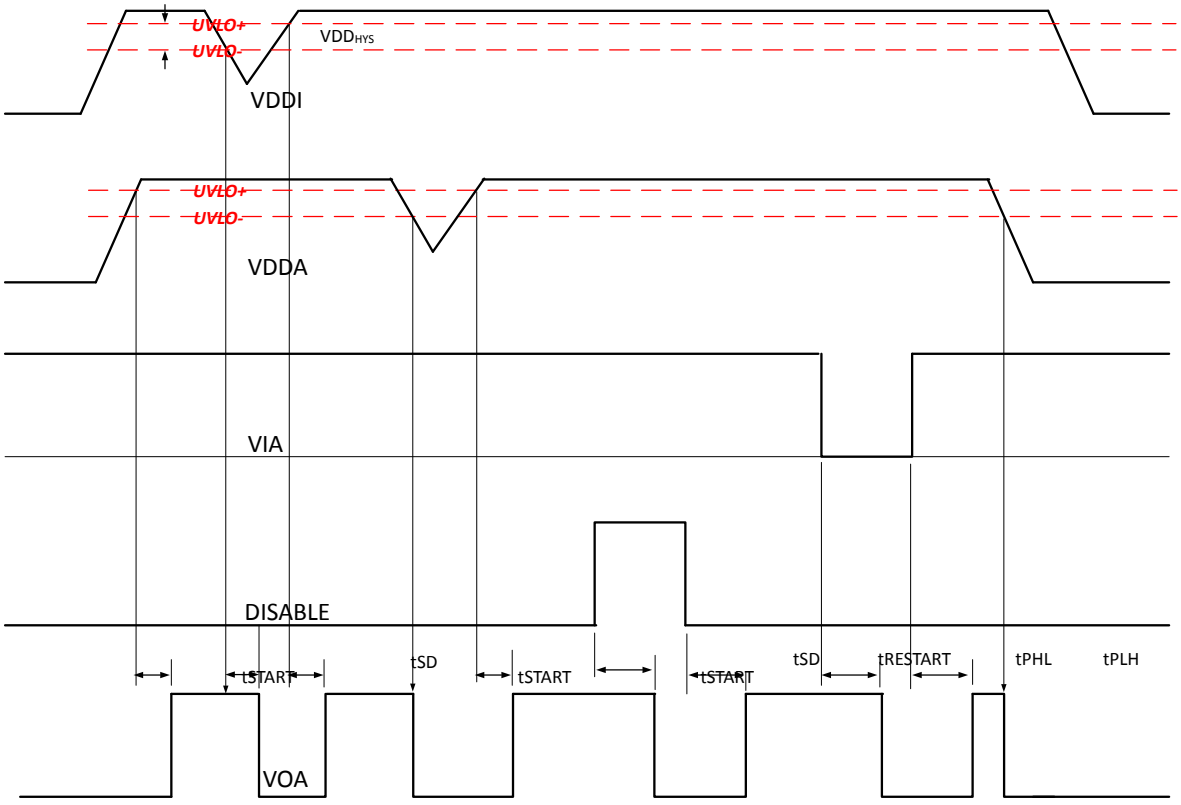


Figure 3.30. Device Behavior during Normal Operation and Shutdown

3.9.3 Undervoltage Lockout (UVLO)

The UVLO circuit unconditionally drives VO low when VDD is below the lockout threshold. Referring to Figure 3.31 Si823x UVLO Response (5 V) on page 18 through Figure 3.34 Si823x UVLO Response (12.5 V) on page 18, upon power up, the Si823x is maintained in UVLO until VDD rises above VDD_{UV+}. During power down, the Si823x enters UVLO when VDD falls below the UVLO threshold plus hysteresis (i.e., VDD ≤ VDD_{UV+} – VDD_{HYS}).

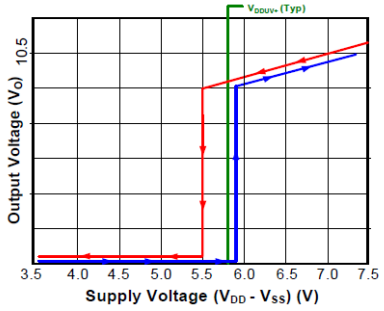


Figure 3.31. Si823x UVLO Response (5 V)

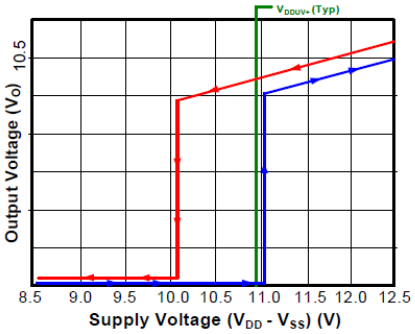


Figure 3.32. Si823x UVLO Response (10 V)

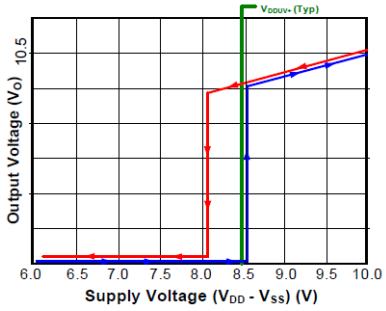


Figure 3.33. Si823x UVLO Response (8 V)

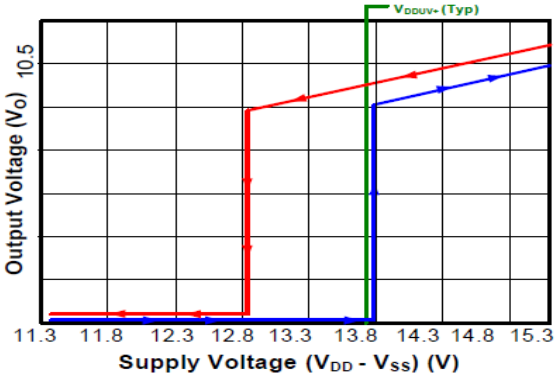


Figure 3.34. Si823x UVLO Response (12.5 V)

3.9.4 Control Inputs

VIA, VIB, and PWM inputs are high-true, TTL level-compatible logic inputs. A logic high signal on VIA or VIB causes the corresponding output to go high. For PWM input versions (Si8231/4), VOA is high and VOB is low when the PWM input is high, and VOA is low and VOB is high when the PWM input is low.

3.9.5 Disable Input

When brought high, the DISABLE input unconditionally drives VOA and VOB low regardless of the states of VIA and VIB. Device operation terminates within tSD after DISABLE =V_{IH} and resumes within tRESTART after DISABLE = V_{IL}. The DISABLE input has no effect if VDDI is below its UVLO level (i.e., VOA, VOB remain low).

3.10 Programmable Dead Time and Overlap Protection

All high-side/low-side drivers (Si8230/1/3/4) include programmable overlap protection to prevent outputs VOA and VOB from being high at the same time. These devices also include programmable dead time, which adds a user-programmable delay between transitions of VOA and VOB. When enabled, dead time is present on all transitions, even after overlap recovery. The amount of dead time delay (DT) is programmed by a single resistor (RDT) connected from the DT input to ground per Equation 5. Note that the dead time pin can be tied to VDDI or left floating to provide a nominal dead time at approximately 400 ps.

$$DT \approx 10 \times RDT$$

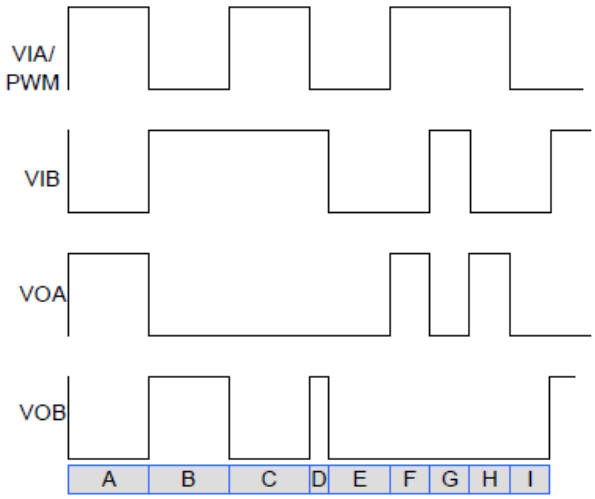
where:

DT = dead time (ns) and

RDT = dead time programing resistor (kΩ)

Equation 5.

The device driving VIA and VIB should provide a minimum dead time of TDD to avoid activating overlap protection. Input/output timing waveforms for the two-input drivers are shown in Figure 3.35 Input / Output Waveforms for High-Side / Low-Side Two-Input Drivers on page 19, and dead time waveforms are shown in Figure 3.36 Dead Time Waveforms for High-Side / Low-Side Two-input Drivers on page 20.



Ref	Description
A	Normal operation: VIA high, VIB low.
B	Normal operation: VIB high, VIA low.
C	Contention: VIA = VIB = high.
D	Recovery from contention: VIA transitions low.
E	Normal operation: VIA = VIB = low.
F	Normal operation: VIA high, VIB low.
G	Contention: VIA = VIB = high.
H	Recovery from contention: VIB transitions low.
I	Normal operation: VIB transitions high.

Figure 3.35. Input / Output Waveforms for High-Side / Low-Side Two-Input Drivers

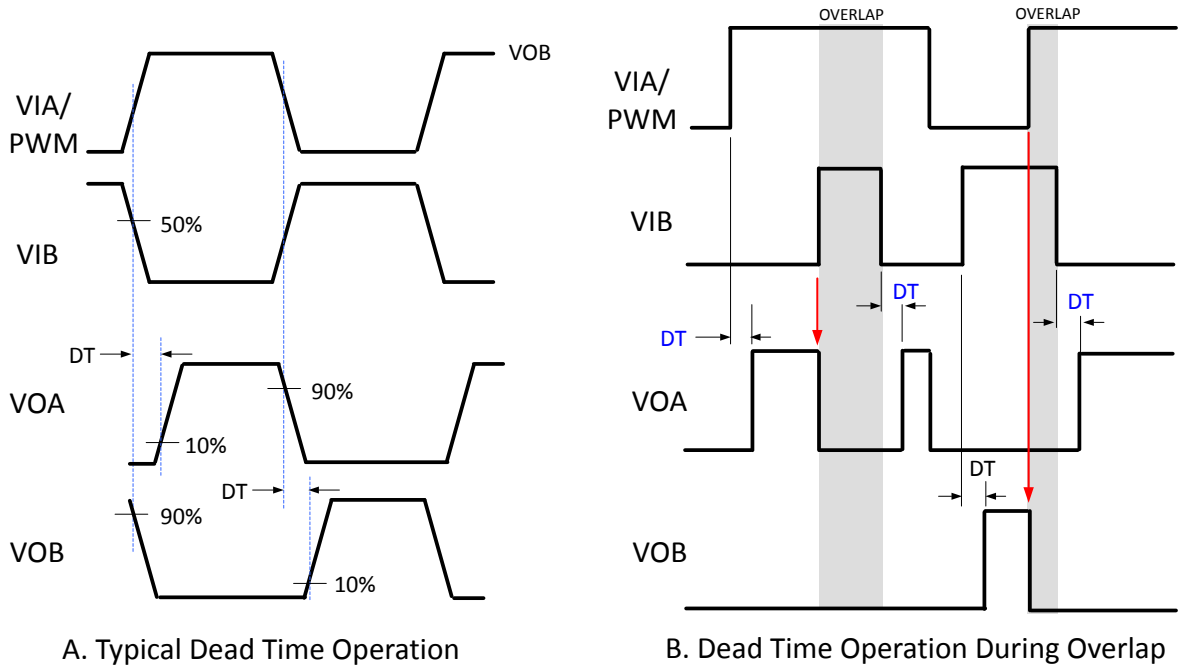


Figure 3.36. Dead Time Waveforms for High-Side / Low-Side Two-input Drivers

4. Electrical Specifications

Table 4.1. Electrical Characteristics[1]

2.7 V < VDDI < 5.5 V, VDDA = VDDB = 12 V or 15 V. TA = –40 to +125 °C. Typical specs at 25 °C

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
DC Specifications						
Input-side Power Supply Voltage	VDDI	Si8230/1/2/3/4/5/6 Si8237/8	4.5 2.7	— —	5.5 5.5	V
Driver Supply Voltage	VDDA, VDDB	Voltage between VDDA and GNDA, and VDDB and GNDB (See 2. Ordering Guide)	6.5	—	24	V
Input Supply Quiescent Current	IDDI(Q)	Si8230/2/3/5/6/7/8	—	2	3	mA
		Si8231/4	—	3.5	5	mA
Output Supply Quiescent Current	IDDA(Q), IDDB(Q)	Current per channel	—	—	3.0	mA
Input Supply Active Current	IDDI	Input freq = 500 kHz, no load	—	3.5	—	mA
Output Supply Active Current	IDDA IDDB	Current per channel with Input freq = 500 kHz, no load	—	6	—	mA
Input Pin Leakage Current	IVIA, IVIB, IPWM		–10	—	+10	µA dc
Input Pin Leakage Current (Si8230/1/2/3/4/5/6)	IDISABLE		–10	—	+10	µA dc
Input Pin Leakage Current (Si8237/8)			-1000	+1000		
Logic High Input Threshold	VIH		2.0	—	—	V
Logic Low Input Threshold	VIL		—	—	0.8	V
Input Hysteresis	VI_{HYST}	Si8230/1/2/3/4/5/6/7/8	400	450	—	mV
Logic High Output Voltage	VOAH, VOBH	IOA, IOB = –1 mA	(VDDA / VDDB) — 0.04	—	—	V
Logic Low Output Voltage	VOAL, VOBL	IOA, IOB = 1 mA	—	—	0.04	V
Output Short-Circuit Pulsed Sink Current	IOA(SCL), IOB(SCL)	Si8230/1/2/7, Figure 4.1 IOL Sink Current Test Circuit on page 24	—	0.5	—	A
		Si8233/4/5/6/8, Figure 4.1 IOL Sink Current Test Circuit on page 24	—	4.0	—	A
Output Short-Circuit Pulsed Source Current	IOA(SCH), IOB(SCH)	Si8230/1/2/7, Figure 4.2 IOH Source Current Test Circuit on page 24	—	0.25	—	A
		Si8233/4/5/6/8, Figure 4.2 IOH Source Current Test Circuit on page 24	—	2.0	—	A
Output Sink Resistance	$R_{ON(SINK)}$	Si8230/1/2/7	—	5.0	—	Ω
		Si8233/4/5/6/8	—	1.0	—	Ω

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Output Source Resistance	$R_{ON(SOURCE)}$	Si8230/1/2/7	—	15	—	Ω
		Si8233/4/5/6/8	—	2.7	—	Ω
VDDI Undervoltage Threshold	$VDDI_{UV+}$	VDDI rising (Si8230/1/2/3/4/5/6)	3.60	4.0	4.45	V
VDDI Undervoltage Threshold	$VDDI_{UV-}$	VDDI falling (Si8230/1/2/3/4/5/6)	3.30	3.70	4.15	V
VDDI Lockout Hysteresis	$VDDI_{HYS}$	(Si8230/1/2/3/4/5/6)	—	250	—	mV
VDDI Undervoltage Threshold	$VDDI_{UV+}$	VDDI rising (Si8237/8)	2.15	2.3	2.5	V
VDDI Undervoltage Threshold	$VDDI_{UV-}$	VDDI falling (Si8237/8)	2.10	2.22	2.40	V
VDDI Lockout Hysteresis	$VDDI_{HYS}$	(Si8237/8)	—	75	—	mV
VDDA, VDDB Undervoltage Threshold	$VDDA_{UV+}$, $VDDB_{UV+}$	VDDA, VDDB rising				
5 V Threshold		See Figure 3.31 Si823x UVLO Response (5 V) on page 18.	5.20	5.80	6.30	V
8 V Threshold		See Figure 3.33 Si823x UVLO Response (8 V) on page 18.	7.50	8.60	9.40	V
10 V Threshold		See Figure 3.32 Si823x UVLO Response (10 V) on page 18.	9.60	11.1	12.2	V
12.5 V Threshold		See Figure 3.34 Si823x UVLO Response (12.5 V) on page 18.	12.4	13.8	14.8	V
VDDA, VDDB Undervoltage Threshold	$VDDA_{UV-}$, $VDDB_{UV-}$	VDDA, VDDB falling				
5 V Threshold		See Figure 3.31 Si823x UVLO Response (5 V) on page 18.	4.90	5.52	6.0	V
8 V Threshold		See Figure 3.33 Si823x UVLO Response (8 V) on page 18.	7.20	8.10	8.70	V
10 V Threshold		See Figure 3.32 Si823x UVLO Response (10 V) on page 18.	9.40	10.1	10.9	V
12.5 V Threshold		See Figure 3.34 Si823x UVLO Response (12.5 V) on page 18.	11.6	12.8	13.8	V
VDDA, VDDB Lockout Hysteresis	$VDDA_{HYS}$, $VDDB_{HYS}$	UVLO voltage = 5 V	—	280	—	mV
VDDA, VDDB Lockout Hysteresis	$VDDA_{HYS}$, $VDDB_{HYS}$	UVLO voltage = 8 V	—	600	—	mV
VDDA, VDDB Lockout Hysteresis	$VDDA_{HYS}$, $VDDB_{HYS}$	UVLO voltage = 10 V or 12.5 V	—	1000	—	mV
AC Specifications						
Minimum Pulse Width			—	10	—	ns
Propagation Delay	t_{PHL}, t_{PLH}	CL = 200 pF	—	30	60	ns
Pulse Width Distortion $\lvert t_{PLH} - t_{PHL} \rvert$	PWD		—	—	5.60	ns
Minimum Overlap Time[2]	TDD	DT = VDDI, No-Connect	—	0.4	—	ns

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Programmed Dead Time[3]	DT	Figure 3.36 Dead Time Waveforms for High-Side / Low-Side Two-input Drivers on page 20, RDT = 100 k	—	900	—	ns
		Figure 3.36 Dead Time Waveforms for High-Side / Low-Side Two-input Drivers on page 20, RDT = 6 k	—	70	—	ns
Output Rise and Fall Time	t_R,t_F	C_L = 200 pF (Si8230/1/2/7)	—	—	20	ns
		C_L = 200 pF (Si8233/4/5/6/8)	—	—	12	ns
Shutdown Time from Disable True	t_{SD}		—	—	60	ns
Restart Time from Disable False	$t_{RESTART}$		—	—	60	ns
Device Start-up Time	t_{START}	Time from VDD_ = VDD_UV+ to VOA, VOB = VIA, VIB	—	—	40	µs
Common Mode Transient Immunity	CMTI	VIA, VIB, PWM = VDDI or 0 V V_{CM} = 1500 V (see Figure 4.3 Common Mode Transient Immunity Test Circuit on page 25)	20	45	—	kV/µs

Notes:

1. VDDA = VDDB = 12 V for 5, 8, and 10 V UVLO devices; VDDA = VDDB = 15 V for 12.5 V UVLO devices.
2. TDD is the minimum overlap time without triggering overlap protection (Si8230/1/3/4 only).
3. The largest RDT resistor that can be used is 220 kΩ.

4.1 Test Circuits

Figures Figure 4.1 IOL Sink Current Test Circuit on page 24, Figure 4.2 IOH Source Current Test Circuit on page 24, and Figure 4.3 Common Mode Transient Immunity Test Circuit on page 25 depict sink current, source current, and common-mode transient immunity test circuits, respectively.

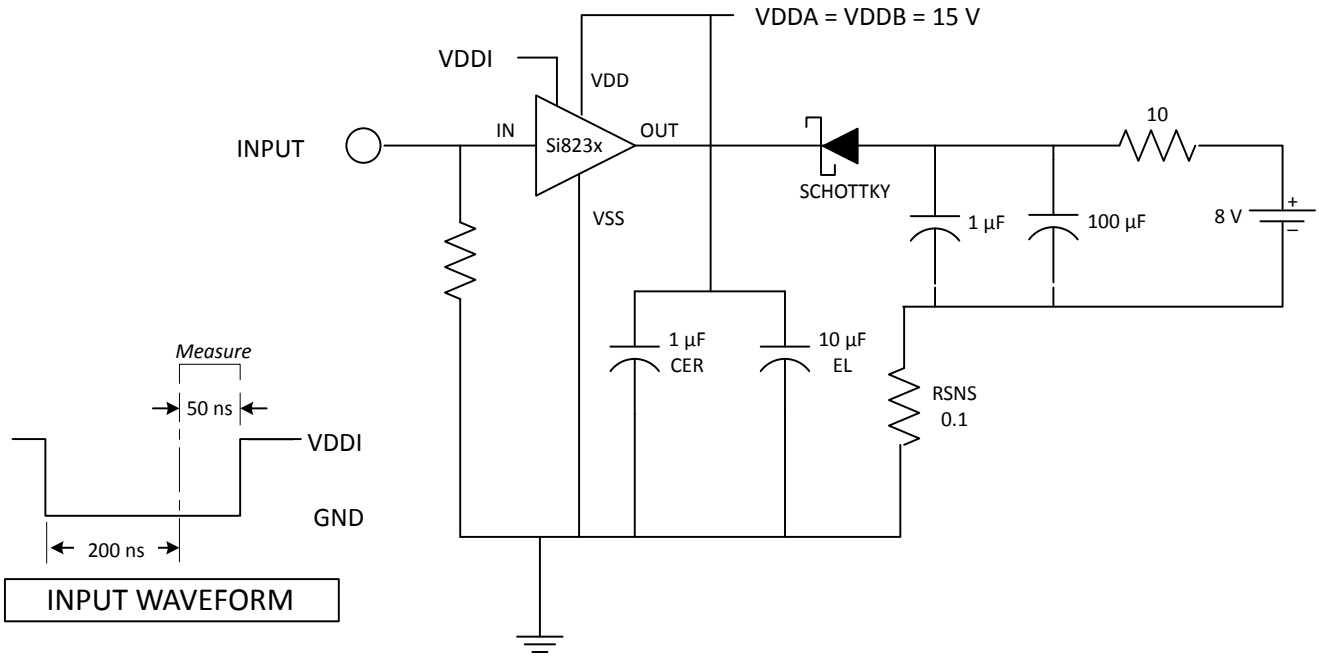


Figure 4.1. IOL Sink Current Test Circuit

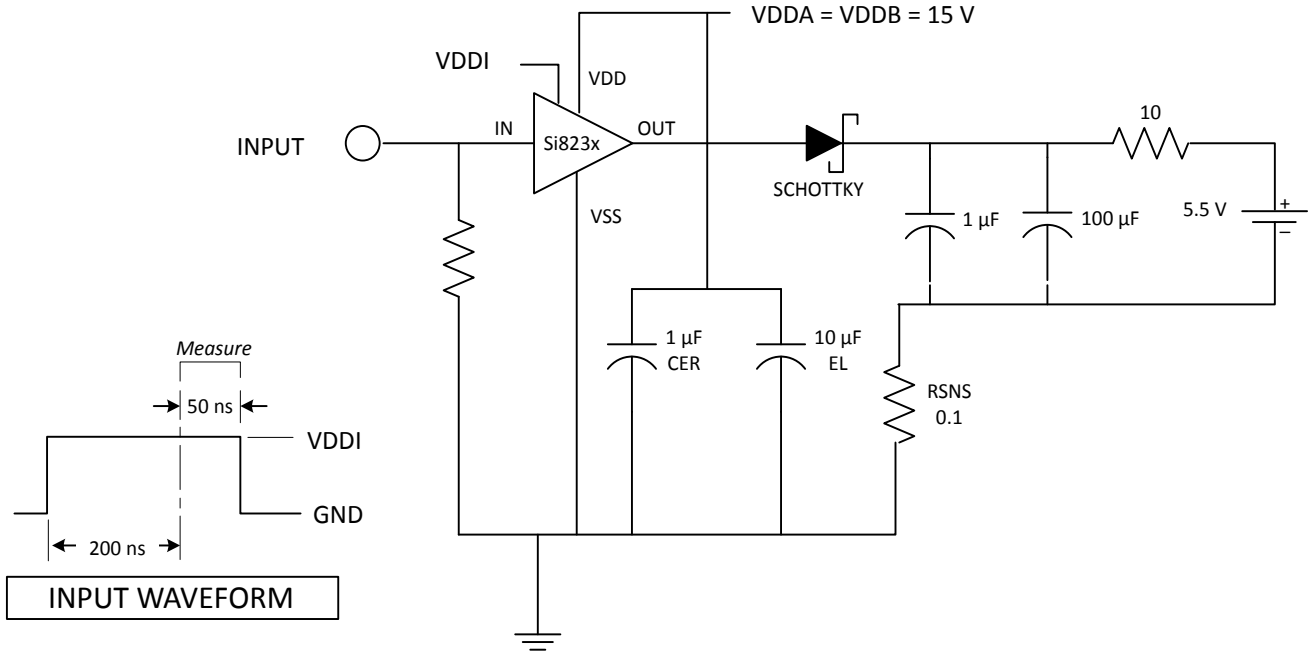


Figure 4.2. IOH Source Current Test Circuit