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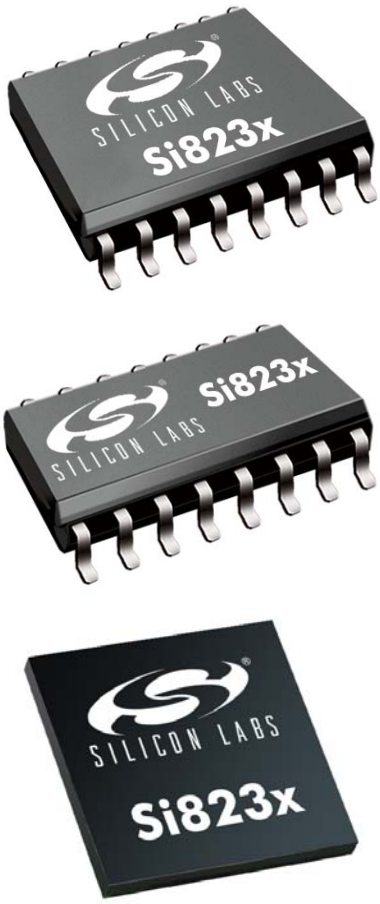
0.5 AND 4.0 AMP ISODRIVERS (2.5 AND 5 kV_{RMS})

Features

- Two completely isolated drivers in one package
  - Up to 5 kV_{RMS} input-to-output isolation
  - Up to 1500 V_{DC} peak driver-to-driver differential voltage
- HS/LS and dual driver versions
- Up to 8 MHz switching frequency
- 0.5 A peak output (Si8230/1/2/7)
- 4.0 A peak output (Si8233/4/5/6/8)
- High electromagnetic immunity
- 60 ns propagation delay (max)
- Independent HS and LS inputs or PWM input versions
- Transient immunity >45 kV/µs
- Overlap protection and programmable dead time
- AEC-Q100 qualification
- Wide operating range
  - –40 to +125 °C
- RoHS-compliant packages
  - SOIC-16 wide body
  - SOIC-16 narrow body
  - LGA-14



Ordering Information:

See page 39.

Applications

- Power delivery systems
- Motor control systems
- Isolated dc-dc power supplies
- Lighting control systems
- Plasma displays
- Solar and industrial inverters

Safety Approval

- UL 1577 recognized
  - Up to 5000 Vrms for 1 minute
- CSA component notice 5A approval
  - IEC 60950-1, 61010-1, 60601-1 (reinforced insulation)
- VDE certification conformity
  - IEC 60747-5-5 (VDE 0884 Part 5)
  - EN 60950-1 (reinforced insulation)
- CQC certification approval
  - GB4943.1

Description

The Si823x isolated driver family combines two independent, isolated drivers into a single package. The Si8230/1/3/4 are high-side/low-side drivers, and the Si8232/5/6/7/8 are dual drivers. Versions with peak output currents of 0.5 A (Si8230/1/2/7) and 4.0 A (Si8233/4/5/6/8) are available. All drivers operate with a maximum supply voltage of 24 V.

The Si823x drivers utilize Silicon Labs' proprietary silicon isolation technology, which provides up to 5 kV_{RMS} withstand voltage per UL1577 and fast 60 ns propagation times. Driver outputs can be grounded to the same or separate grounds or connected to a positive or negative voltage. The TTL level compatible inputs with >400 mV hysteresis are available in individual control input (Si8230/2/3/5/6/7/8) or PWM input (Si8231/4) configurations. High integration, low propagation delay, small installed size, flexibility, and cost-effectiveness make the Si823x family ideal for a wide range of isolated MOSFET/IGBT gate drive applications.

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Section **Page**

1. Top-Level Block Diagrams

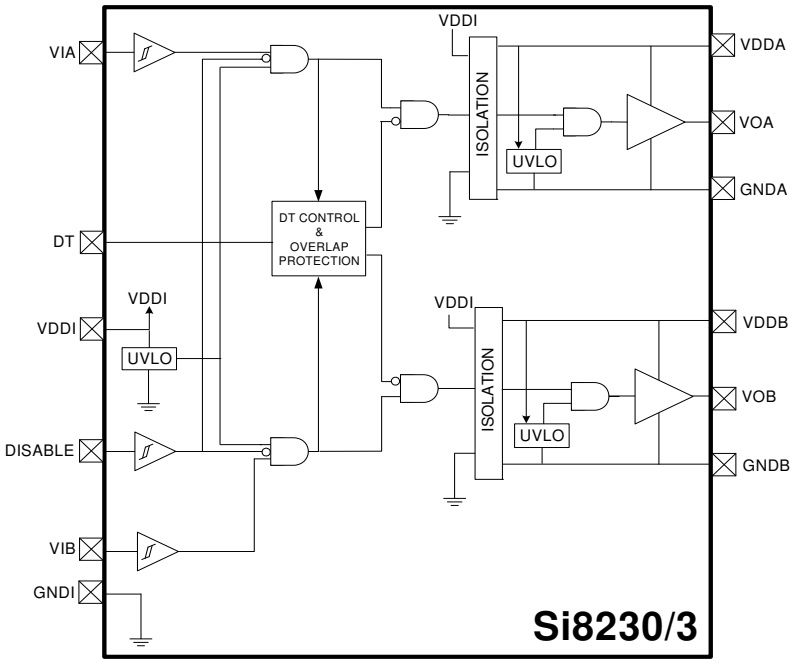

Figure 1. Si8230/3 Two-Input High-Side/Low-Side Isolated Drivers

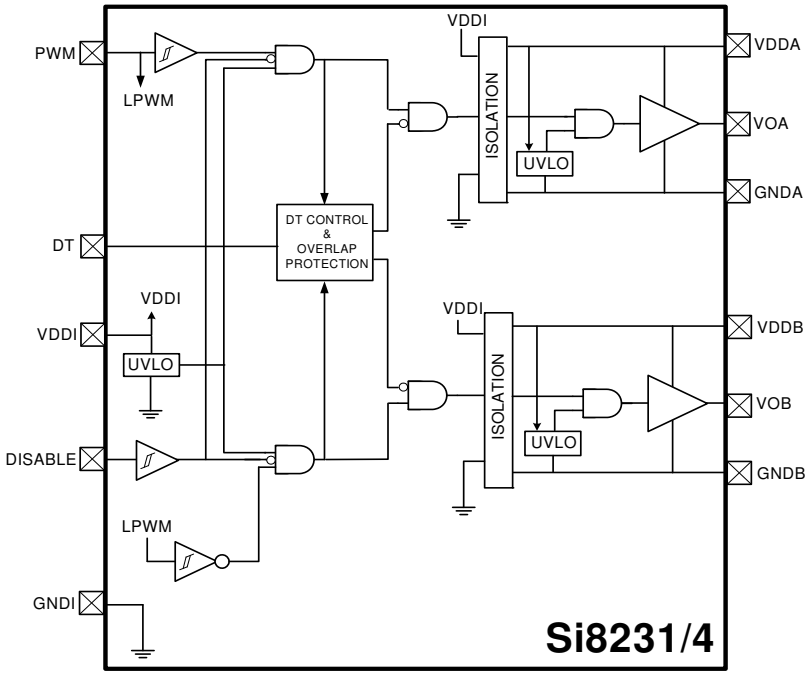

Figure 2. Si8231/4 Single-Input High-Side/Low-Side Isolated Drivers

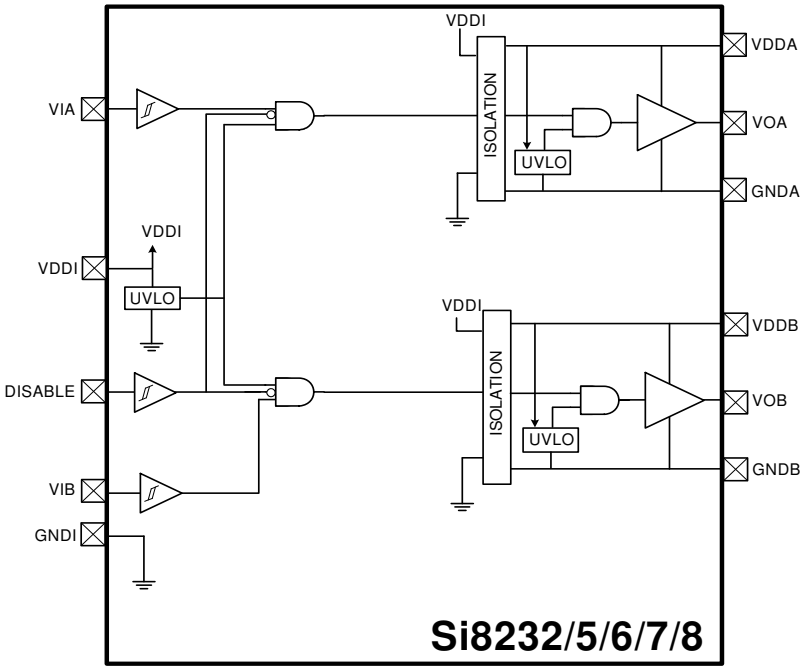

Figure 3. Si8232/5/6/7/8 Dual Isolated Drivers

2. Electrical Specifications

Table 1. Electrical Characteristics[1]

2.7 V < VDDI < 5.5 V, VDDA = VDDB = 12 V or 15 V. TA = –40 to +125 °C. Typical specs at 25 °C

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
DC Specifications						
Input-side Power Supply Voltage	VDDI	Si8230/1/2/3/4/5/6 Si8237/8	4.5 2.7	— —	5.5 5.5	V
Driver Supply Voltage	VDDA, VDDB	Voltage between VDDA and GNDA, and VDDB and GNDB (See “6. Ordering Guide”)	6.5	—	24	V
Input Supply Quiescent Current	IDDI(Q)	Si8230/2/3/5/6/7/8	—	2	3	mA
		Si8231/4	—	3.5	5	mA
Output Supply Quiescent Current	IDDA(Q), IDDB(Q)	Current per channel	—	—	3.0	mA
Input Supply Active Current	IDDI	Input freq = 500 kHz, no load	—	3.5	—	mA
Output Supply Active Current	IDDA IDDB	Current per channel with Input freq = 500 kHz, no load	—	6	—	mA
Input Pin Leakage Current	IVIA, IVIB, IPWM		–10	—	+10	µA dc
Input Pin Leakage Current	IDISABLE		–10	—	+10	µA dc
Logic High Input Threshold	VIH		2.0	—	—	V
Logic Low Input Threshold	VIL		—	—	0.8	V
Input Hysteresis	VI_{HYST}	Si8230/1/2/3/4/5/6/7/8	400	450	—	mV
Logic High Output Voltage	VOAH, VOBH	IOA, IOB = –1 mA	(VDDA /VDDB) — 0.04	—	—	V
Logic Low Output Voltage	VOAL, VOBL	IOA, IOB = 1 mA	—	—	0.04	V
Output Short-Circuit Pulsed Sink Current	IOA(SCL), IOB(SCL)	Si8230/1/2/7, Figure 4	—	0.5	—	A
		Si8233/4/5/6/8, Figure 4	—	4.0	—	A
Output Short-Circuit Pulsed Source Current	IOA(SCH), IOB(SCH)	Si8230/1/2/7, Figure 5	—	0.25	—	A
		Si8233/4/5/6/8, Figure 5	—	2.0	—	A
Output Sink Resistance	$R_{ON(SINK)}$	Si8230/1/2/7	—	5.0	—	Ω
		Si8233/4/5/6/8	—	1.0	—	Ω

Notes:

1. VDDA = VDDB = 12 V for 5, 8, and 10 V UVLO devices; VDDA = VDDB = 15 V for 12.5 V UVLO devices.
2. TDD is the minimum overlap time without triggering overlap protection (Si8230/1/3/4 only).
3. The largest RDT resistor that can be used is 220 kΩ..

Table 1. Electrical Characteristics[1] (Continued)

2.7 V < VDDI < 5.5 V, VDDA = VDDB = 12 V or 15 V. TA = –40 to +125 °C. Typical specs at 25 °C

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Output Source Resistance	$R_{ON(SOURCE)}$	Si8230/1/2/7	—	15	—	Ω
		Si8233/4/5/6/8	—	2.7	—	Ω
VDDI Undervoltage Threshold	$VDDI_{UV+}$	VDDI rising (Si8230/1/2/3/4/5/6)	3.60	4.0	4.45	V
VDDI Undervoltage Threshold	$VDDI_{UV-}$	VDDI falling (Si8230/1/2/3/4/5/6)	3.30	3.70	4.15	V
VDDI Lockout Hysteresis	$VDDI_{HYS}$	(Si8230/1/2/3/4/5/6)	—	250	—	mV
VDDI Undervoltage Threshold	$VDDI_{UV+}$	VDDI rising (Si8237/8)	2.15	2.3	2.5	V
VDDI Undervoltage Threshold	$VDDI_{UV-}$	VDDI falling (Si8237/8)	2.10	2.22	2.40	V
VDDI Lockout Hysteresis	$VDDI_{HYS}$	(Si8237/8)	—	75	—	mV
VDDA, VDDB Undervoltage Threshold	$VDDA_{UV+}$, $VDDB_{UV+}$	VDDA, VDDB rising				
5 V Threshold		See Figure 37 on page 27.	5.20	5.80	6.30	V
8 V Threshold		See Figure 38 on page 27.	7.50	8.60	9.40	V
10 V Threshold		See Figure 39 on page 27.	9.60	11.1	12.2	V
12.5 V Threshold		See Figure 40 on page 27.	12.4	13.8	14.8	V
VDDA, VDDB Undervoltage Threshold	$VDDA_{UV-}$, $VDDB_{UV-}$	VDDA, VDDB falling				
5 V Threshold		See Figure 37 on page 27.	4.90	5.52	6.0	V
8 V Threshold		See Figure 38 on page 27.	7.20	8.10	8.70	V
10 V Threshold		See Figure 39 on page 27.	9.40	10.1	10.9	V
12.5 V Threshold		See Figure 40 on page 27.	11.6	12.8	13.8	V
VDDA, VDDB Lockout Hysteresis	$VDDA_{HYS}$, $VDDB_{HYS}$	UVLO voltage = 5 V	—	280	—	mV
VDDA, VDDB Lockout Hysteresis	$VDDA_{HYS}$, $VDDB_{HYS}$	UVLO voltage = 8 V	—	600	—	mV
VDDA, VDDB Lockout Hysteresis	$VDDA_{HYS}$, $VDDB_{HYS}$	UVLO voltage = 10 V or 12.5 V	—	1000	—	mV

Notes:

1. VDDA = VDDB = 12 V for 5, 8, and 10 V UVLO devices; VDDA = VDDB = 15 V for 12.5 V UVLO devices.
2. TDD is the minimum overlap time without triggering overlap protection (Si8230/1/3/4 only).
3. The largest RDT resistor that can be used is 220 kΩ..

Table 1. Electrical Characteristics[1] (Continued)

2.7 V < VDDI < 5.5 V, VDDA = VDDB = 12 V or 15 V. TA = –40 to +125 °C. Typical specs at 25 °C

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
AC Specifications						
Minimum Pulse Width			—	10	—	ns
Propagation Delay	t_{PHL}, t_{PLH}	CL = 200 pF	—	30	60	ns
Pulse Width Distortion $\lvert t_{PLH} - t_{PHL} \rvert$	PWD		—	—	5.60	ns
Minimum Overlap Time[2]	TDD	DT = VDDI, No-Connect	—	0.4	—	ns
Programmed Dead Time[3]	DT	Figure 42, RDT = 100 k	—	900	—	ns
		Figure 42, RDT = 6 k	—	70	—	ns
Output Rise and Fall Time	t_R,t_F	C_L = 200 pF (Si8230/1/2/7)	—	—	20	ns
		C_L = 200 pF (Si8233/4/5/6/8)	—	—	12	ns
Shutdown Time from Disable True	t_{SD}		—	—	60	ns
Restart Time from Disable False	$t_{RESTART}$		—	—	60	ns
Device Start-up Time	t_{START}	Time from VDD_ = VDD_UV+ to VOA, VOB = VIA, VIB	—	—	40	µs
Common Mode Transient Immunity	CMTI	VIA, VIB, PWM = VDDI or 0 V V_{CM} = 1500 V (see Figure 6)	20	45	—	kV/µs

Notes:

1. VDDA = VDDB = 12 V for 5, 8, and 10 V UVLO devices; VDDA = VDDB = 15 V for 12.5 V UVLO devices.
2. TDD is the minimum overlap time without triggering overlap protection (Si8230/1/3/4 only).
3. The largest RDT resistor that can be used is 220 kΩ..

2.1. Test Circuits

Figures 4, 5, and 6 depict sink current, source current, and common-mode transient immunity test circuits, respectively.

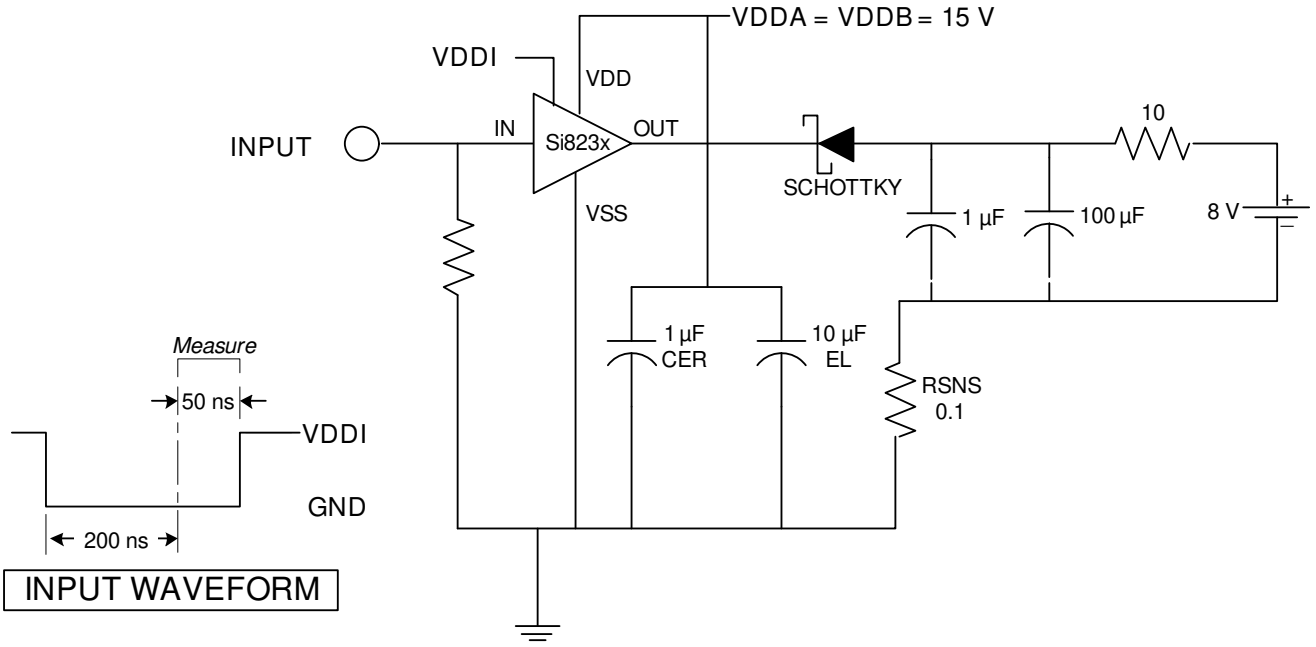

Figure 4. IOL Sink Current Test Circuit

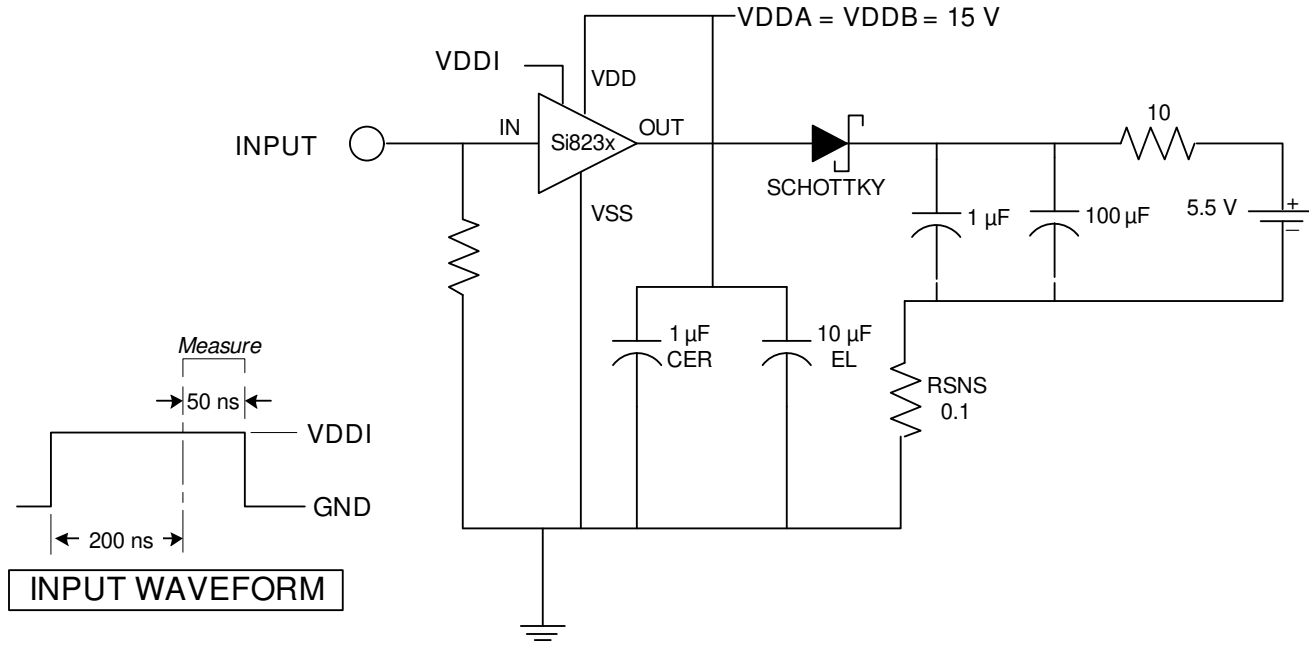

Figure 5. IOH Source Current Test Circuit

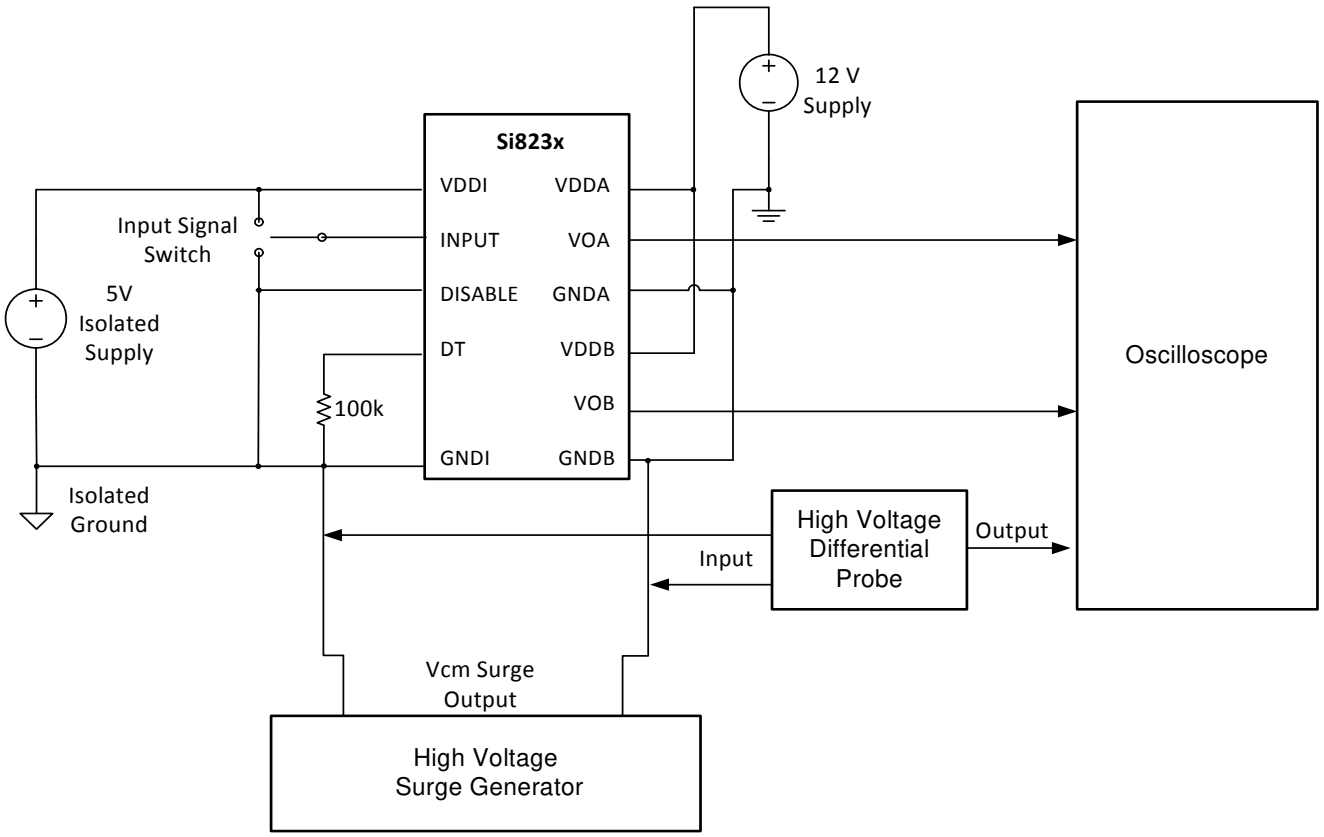

Figure 6. Common Mode Transient Immunity Test Circuit

Table 2. Regulatory Information[1,2,3,4]

CSA
The Si823x is certified under CSA Component Acceptance Notice 5A. For more details, see File 232873.
61010-1: Up to 600 V_{RMS} reinforced insulation working voltage; up to 600 V_{RMS} basic insulation working voltage.
60950-1: Up to 600 V_{RMS} reinforced insulation working voltage; up to 1000 V_{RMS} basic insulation working voltage.
60601-1: Up to 125 V_{RMS} reinforced insulation working voltage; up to 380 V_{RMS} basic insulation working voltage.
VDE
The Si823x is certified according to IEC 60747-5-5. For more details, see File 5006301-4880-0001.
60747-5-5: Up to 891 V_{peak} for basic insulation working voltage.
60950-1: Up to 600 V_{RMS} reinforced insulation working voltage; up to 1000 V_{RMS} basic insulation working voltage.
UL
The Si823x is certified under UL1577 component recognition program. For more details, see File E257455.
Rated up to 5000 V_{RMS} isolation voltage for basic protection.
CQC
The Si823x is certified under GB4943.1-2011. For more details, see File V2012CQC001041.
Rated up to 600 V_{RMS} reinforced insulation working voltage; up to 1000 V_{RMS} basic insulation working voltage.
Notes: **1.** Regulatory Certifications apply to 2.5 kV_{RMS} rated devices which are production tested to 3.0 kV_{RMS} for 1 sec. **2.** Regulatory Certifications apply to 3.75 kV_{RMS} rated devices which are production tested to 4.5 kV_{RMS} for 1 sec. **3.** Regulatory Certifications apply to 5.0 kV_{RMS} rated devices which are production tested to 6.0 kV_{RMS} for 1 sec. **4.** For more information, see "6. Ordering Guide" on page 39.

Table 3. Insulation and Safety-Related Specifications

Parameter	Symbol	Test Condition	Value				Unit
			WBSOIC-16 5 kV_{RMS}	WBSOIC-16 NBSOIC-16 2.5 kV_{RMS}	14 LD LGA 2.5 kV_{RMS}	14 LD LGA with Pad 1.0 kV_{RMS}	
Nominal Air Gap (Clearance)[1]	L(1O1)		8.0	8.0/4.01	3.5	1.75	mm
Nominal External Tracking (Creepage)[1]	L(1O2)		8.0	8.0/4.01	3.5	1.75	mm
Minimum Internal Gap (Internal Clearance)			0.014	0.014	0.014	0.014	mm
Tracking Resistance (Proof Tracking Index)	PTI	IEC60112	600	600	600	600	V
Erosion Depth	ED		0.040	0.019	0.021	0.021	mm
Resistance (Input-Output)[2]	R_{IO}		10^{12}	10^{12}	10^{12}	10^{12}	Ω
Capacitance (Input-Output)[2]	C_{IO}	f = 1 MHz	1.4	1.4	1.4	1.4	pF
Input Capacitance[3]	C_I		4.0	4.0	4.0	4.0	pF

Notes:

1. The values in this table correspond to the nominal creepage and clearance values as detailed in "7. Package Outline: 16-Pin Wide Body SOIC" , "9. Package Outline: 16-Pin Narrow Body SOIC" , "11. Package Outline: 14 LD LGA (5 x 5 mm)" , and "13. Package Outline: 14 LD LGA with Thermal Pad (5 x 5 mm)" . VDE certifies the clearance and creepage limits as 4.7 mm minimum for the NB SOIC-16 and 8.5 mm minimum for the WB SOIC-16 package. UL does not impose a clearance and creepage minimum for component level certifications. CSA certifies the clearance and creepage limits as 3.9 mm minimum for the NB SOIC 16 and 7.6 mm minimum for the WB SOIC-16 package.
2. To determine resistance and capacitance, the Si823x is converted into a 2-terminal device. Pins 1–8 (1-7, 14 LD LGA) are shorted together to form the first terminal and pins 9–16 (8-14, 14 LD LGA) are shorted together to form the second terminal. The parameters are then measured between these two terminals.
3. Measured from input pin to ground.

Table 4. IEC 60664-1 (VDE 0884 Part 5) Ratings

Parameter	Test Condition	Specification			
		WB SOIC-16	NB SOIC-16	14 LD LGA	14 LD LGA with Pad
Basic Isolation Group	Material Group	I	I	I	I
Installation Classification	Rated Mains Voltages ≤ 150 V_{RMS}	I-IV	I-IV	I-IV	I-IV
	Rated Mains Voltages ≤ 300 V_{RMS}	I-IV	I-III	I-III	I-III
	Rated Mains Voltages ≤ 400 V_{RMS}	I-III	I-II	I-II	I-II
	Rated Mains Voltages ≤ 600 V_{RMS}	I-III	I-II	I-II	I-I

Table 5. IEC 60747-5-5 Insulation Characteristics*

Parameter	Symbol	Test Condition	Characteristic			Unit
			WB SOIC-16	NB SOIC-16 14 LD LGA	14 LD LGA with Pad	
Maximum Working Insulation Voltage	V_{IORM}		891	560	373	V peak
Input to Output Test Voltage	V_{PR}	Method b1 (V_{IORM} x 1.875 = V_{PR}, 100% Production Test, t_m = 1 sec, Partial Discharge < 5 pC)	1375	1050	700	V peak
Transient Overvoltage	V_{IOTM}	t = 60 sec	6000	4000	2650	V peak
Pollution Degree (DIN VDE 0110, Table 1)			2	2	2	
Insulation Resistance at T_S, V_{IO} = 500 V	R_S		$>10^9$	$>10^9$	$>10^9$	Ω

***Note:** Maintenance of the safety data is ensured by protective circuits. The Si823x provides a climate classification of 40/125/21.

Table 6. IEC Safety Limiting Values[1]

Parameter	Symbol	Test Condition	WB SOIC-16	NB SOIC-16	14 LD LGA	14 LD LGA with Pad	Unit
Case Temperature	T_S		150	150	150	150	°C
Safety Input Current	I_S	θ_{JA} = 100 °C/W (WB SOIC-16), 105 °C/W (NB SOIC-16, 14 LD LGA), 50 °C/W (14 LD LGA with Pad) V_{DDI} = 5.5 V, V_{DDA} = V_{DDB} = 24 V, T_J = 150 °C, T_A = 25 °C	50	50	50	100	mA
Device Power Dissipation[2]	P_D		1.2	1.2	1.2	1.2	W

Notes:
1. Maximum value allowed in the event of a failure. Refer to the thermal derating curve in Figures 7 and 8.
2. The Si82xx is tested with V_{DDI} = 5.5 V, V_{DDA} = V_{DDB} = 24 V, T_J = 150 ºC, C_L = 100 pF, input 2 MHz 50% duty cycle square wave.

Table 7. Thermal Characteristics

Parameter	Symbol	WB SOIC-16	NB SOIC-16	14 LD LGA	14 LD LGA with Pad	Unit
IC Junction-to-Air Thermal Resistance	θ_{JA}	100	105	105	50	°C/W

Table 8. Absolute Maximum Ratings[1]

Parameter	Symbol	Min	Typ	Max	Unit
Storage Temperature[2]	T_{STG}	–65	—	+150	°C
Ambient Temperature under Bias	T_A	–40	—	+125	°C
Junction Temperature	T_J	—	—	+150	°C
Input-side Supply Voltage	VDDI	–0.6	—	6.0	V
Driver-side Supply Voltage	VDDA, VDDB	–0.6	—	30	V
Voltage on any Pin with respect to Ground	VIN	–0.5	—	VDD + 0.5	V
Output Drive Current per Channel	I_O	—	—	10	mA
Lead Solder Temperature (10 sec.)		—	—	260	°C
Maximum Isolation (Input to Output) (1 sec) WB SOIC-16		—	—	6500	V_{RMS}
Maximum Isolation (Output to Output) (1 sec) WB SOIC-16		—	—	2500	V_{RMS}
Maximum Isolation (Input to Output) (1 sec) NB SOIC-16		—	—	4250	V_{RMS}
Maximum Isolation (Output to Output) (1 sec) NB SOIC-16		—	—	2500	V_{RMS}
Maximum Isolation (Input to Output) (1 sec) 14 LD LGA without Thermal Pad		—	—	3850	V_{RMS}
Maximum Isolation (Output to Output) (1 sec) 14 LD LGA without Thermal Pad		—	—	650	V_{RMS}
Maximum Isolation (Input to Output) (1 sec) 14 LD LGA with Thermal Pad		—	—	1850	V_{RMS}
Maximum Isolation (Output to Output) (1 sec) 14 LD LGA with Thermal Pad		—	—	0	V_{RMS}

Notes:
1. Permanent device damage may occur if the absolute maximum ratings are exceeded. Functional operation should be restricted to the conditions as specified in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
2. VDE certifies storage temperature from –40 to 150 °C.

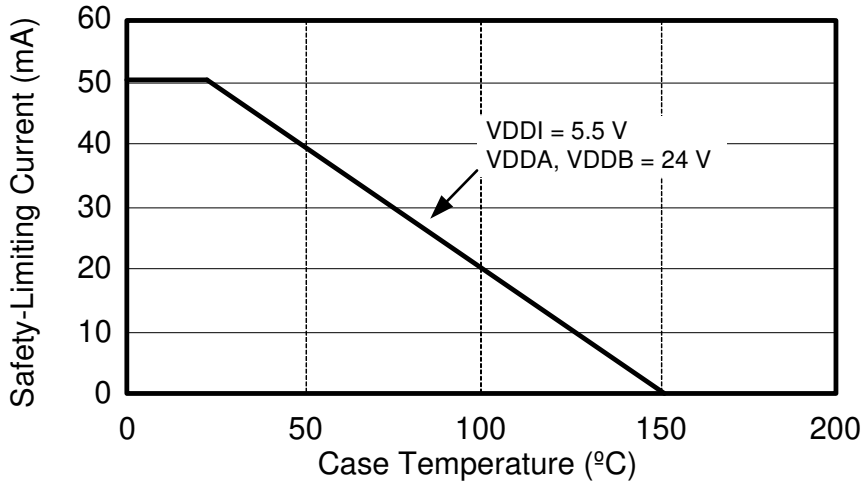

Figure 7. WB SOIC-16, NB SOIC-16, 14 LD LGA Thermal Derating Curve, Dependence of Safety Limiting Values with Case Temperature per DIN EN 60747-5-5

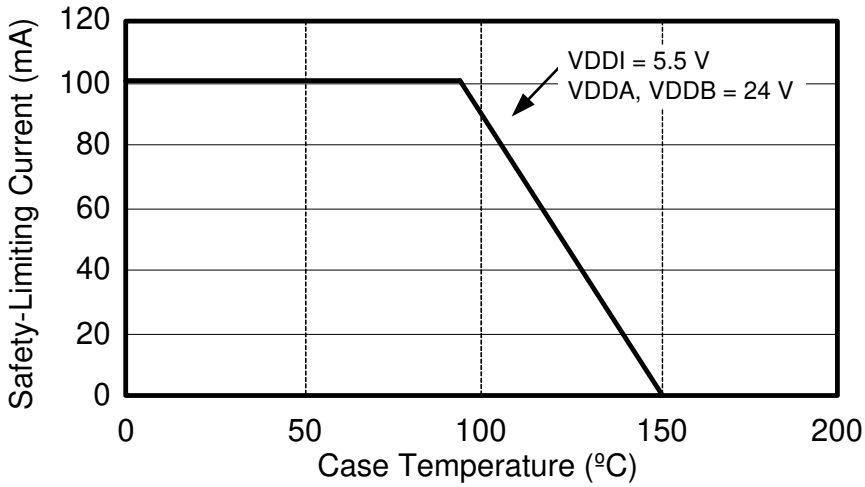

Figure 8. 14 LD LGA with Pad Thermal Derating Curve, Dependence of Safety Limiting Values with Case Temperature per DIN EN 60747-5-5

3. Functional Description

The operation of an Si823x channel is analogous to that of an optocoupler and gate driver, except an RF carrier is modulated instead of light. This simple architecture provides a robust isolated data path and requires no special considerations or initialization at start-up. A simplified block diagram for a single Si823x channel is shown in Figure 9.

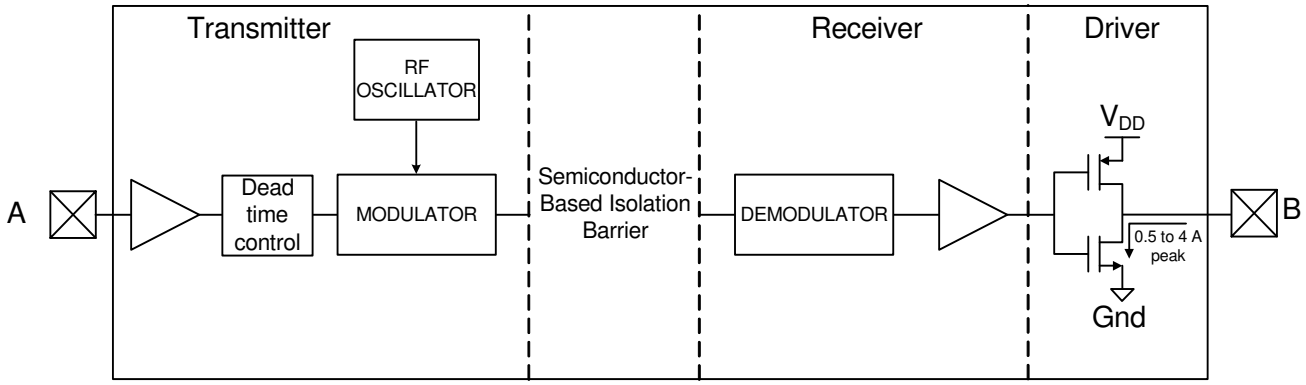

Figure 9. Simplified Channel Diagram

A channel consists of an RF Transmitter and RF Receiver separated by a semiconductor-based isolation barrier. Referring to the Transmitter, input A modulates the carrier provided by an RF oscillator using on/off keying. The Receiver contains a demodulator that decodes the input state according to its RF energy content and applies the result to output B via the output driver. This RF on/off keying scheme is superior to pulse code schemes as it provides best-in-class noise immunity, low power consumption, and better immunity to magnetic fields. See Figure 10 for more details.

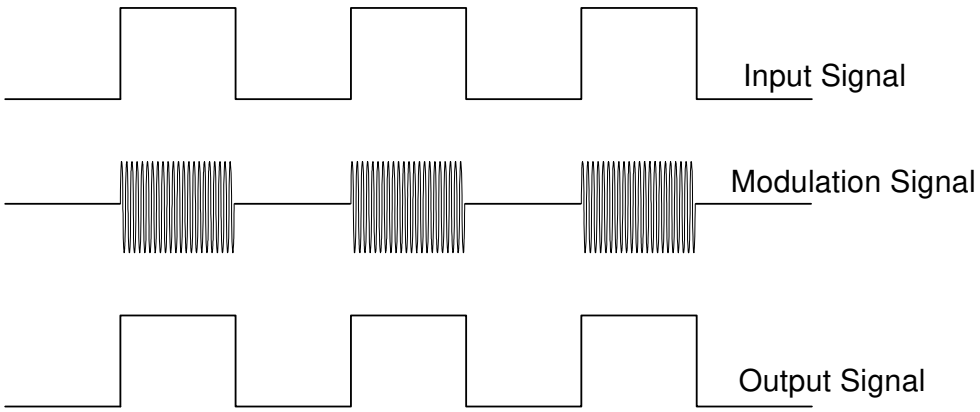

Figure 10. Modulation Scheme

3.1. Typical Operating Characteristics (0.5 Amp)

The typical performance characteristics depicted in Figures 11 through 22 are for information purposes only. Refer to Table 1 on page 6 for actual specification limits.

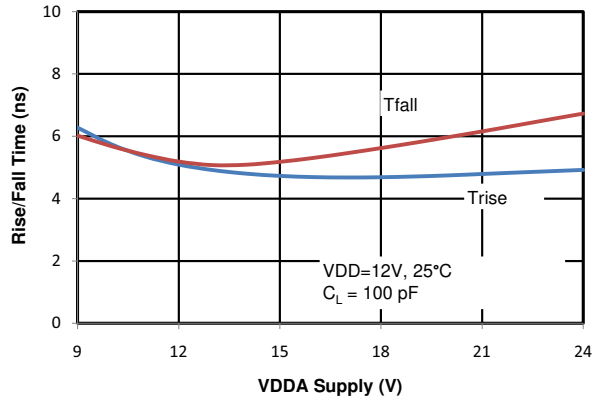

Figure 11. Rise/Fall Time vs. Supply Voltage

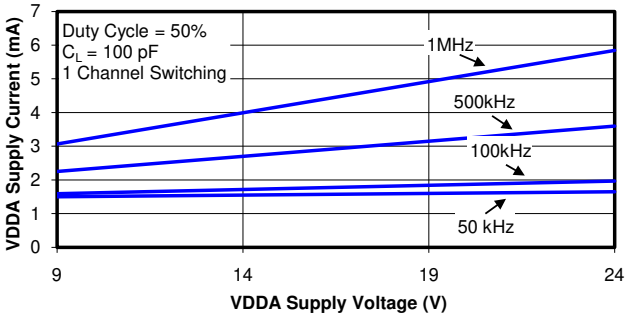

Figure 14. Supply Current vs. Supply Voltage

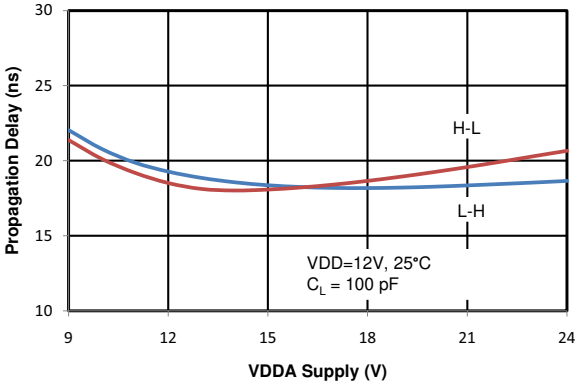

Figure 12. Propagation Delay vs. Supply Voltage

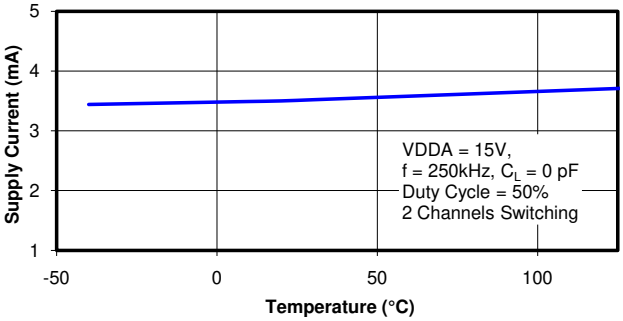

Figure 15. Supply Current vs. Temperature

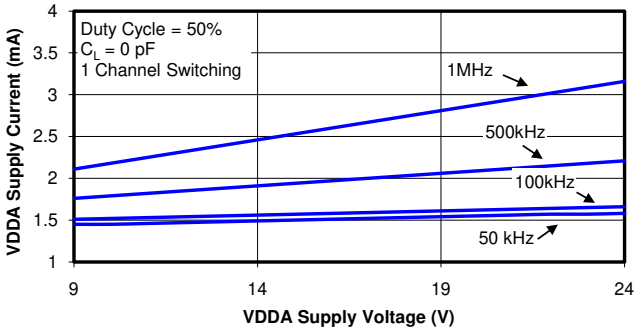

Figure 13. Supply Current vs. Supply Voltage

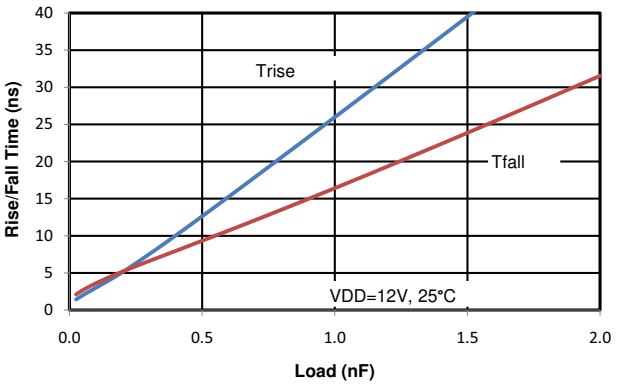

Figure 16. Rise/Fall Time vs. Load

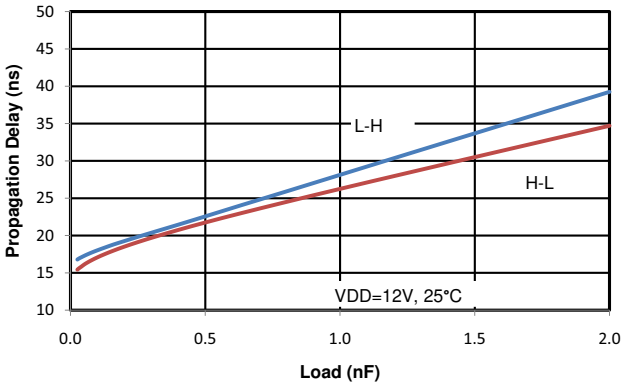

Figure 17. Propagation Delay vs. Load

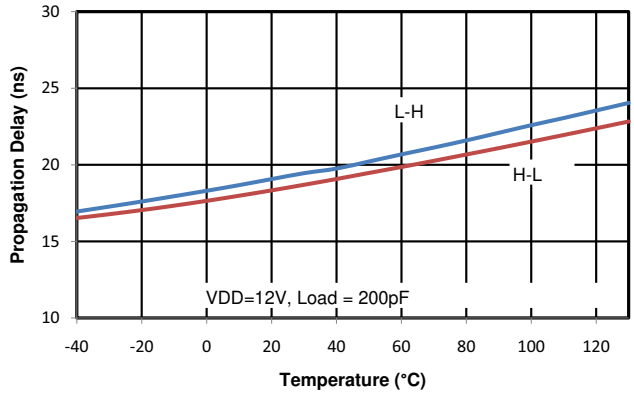

Figure 18. Propagation Delay vs. Temperature

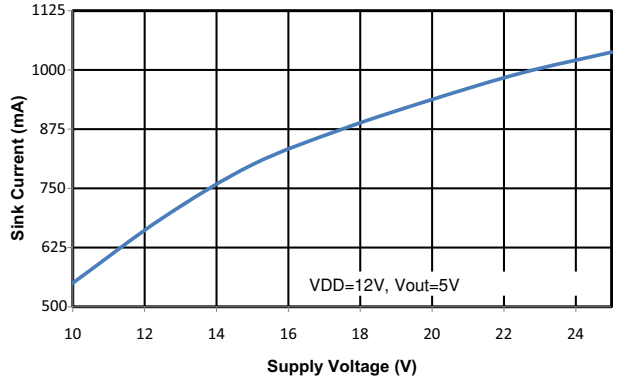

Figure 19. Output Sink Current vs. Supply Voltage

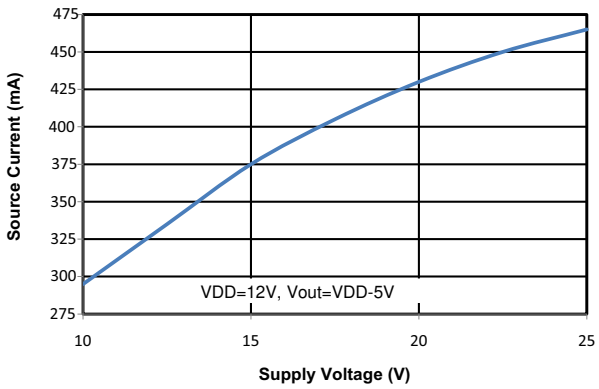

Figure 20. Output Source Current vs. Supply Voltage

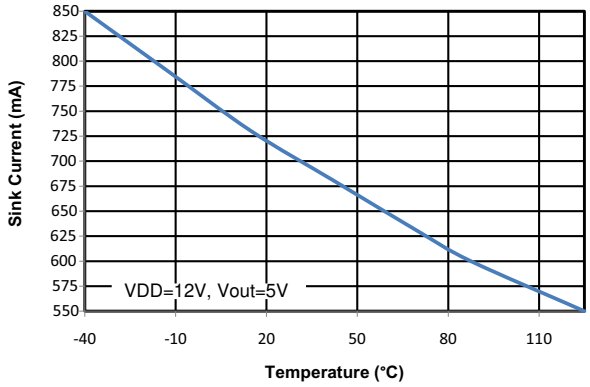

Figure 21. Output Sink Current vs. Temperature

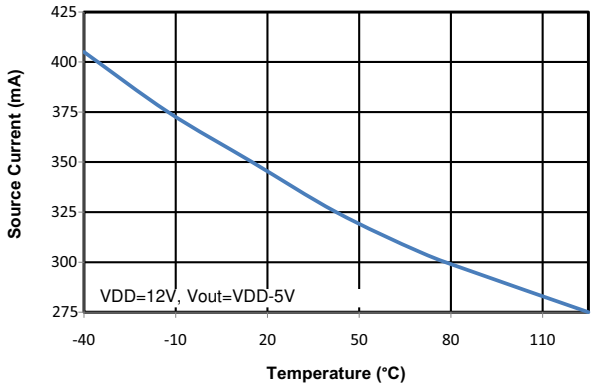

Figure 22. Output Source Current vs. Temperature

3.2. Typical Operating Characteristics (4.0 Amp)

The typical performance characteristics depicted in Figures 23 through 34 are for information purposes only. Refer to Table 1 on page 6 for actual specification limits.

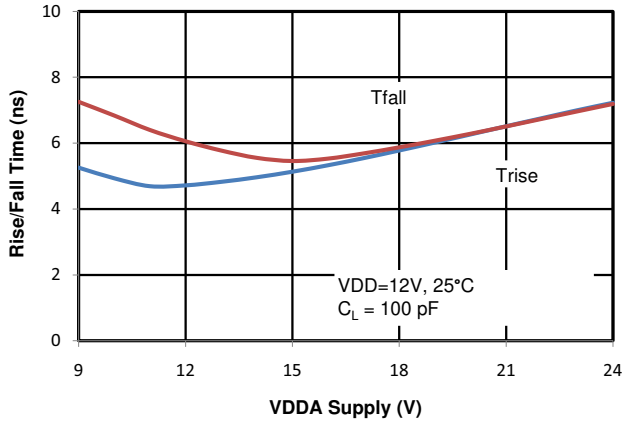

Figure 23. Rise/Fall Time vs. Supply Voltage

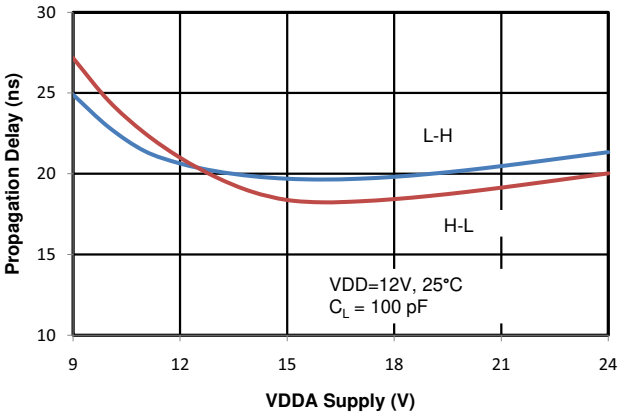

Figure 24. Propagation Delay vs. Supply Voltage

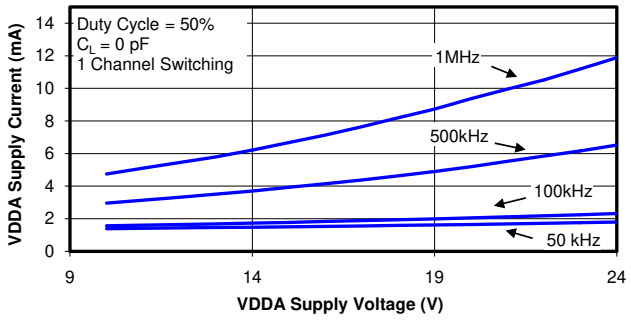

Figure 25. Supply Current vs. Supply Voltage

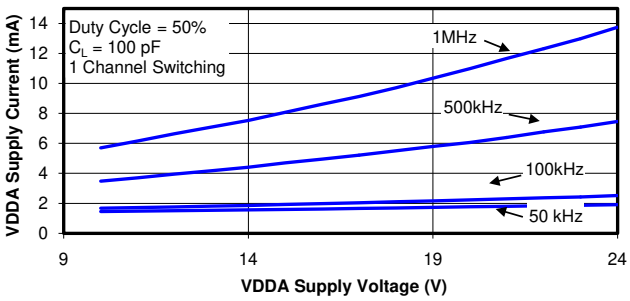

Figure 26. Supply Current vs. Supply Voltage

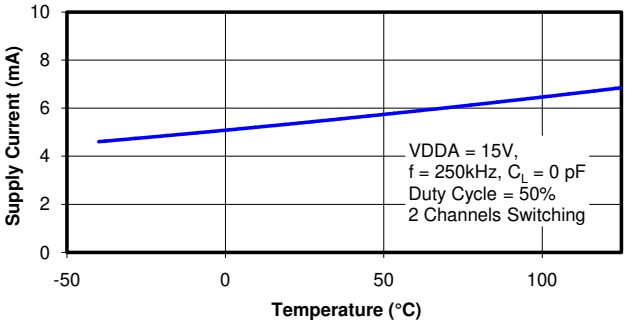

Figure 27. Supply Current vs. Temperature

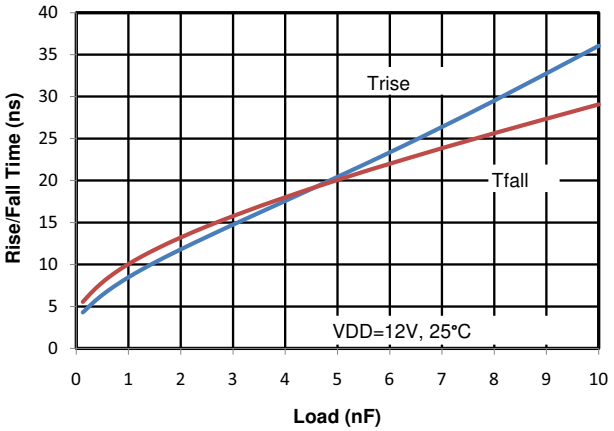

Figure 28. Rise/Fall Time vs. Load

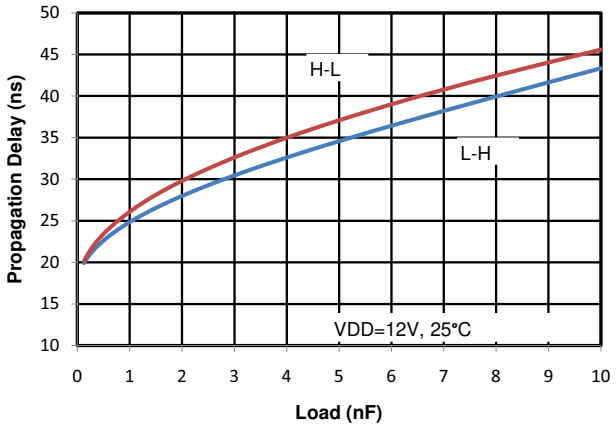

Figure 29. Propagation Delay vs. Load

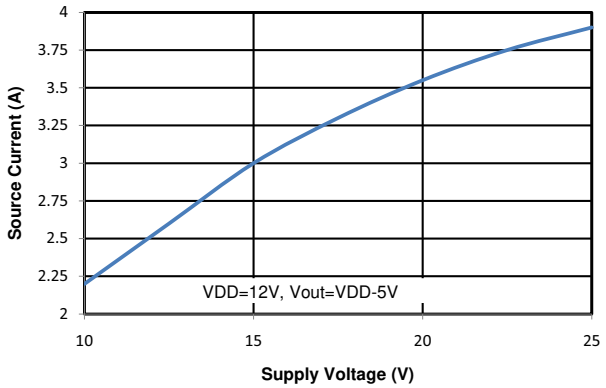

Figure 32. Output Source Current vs. Supply Voltage

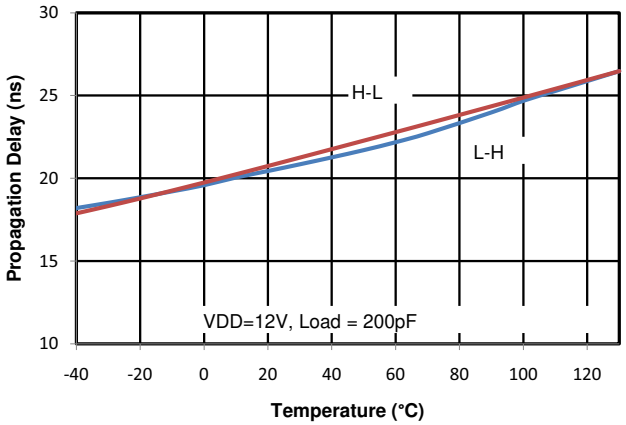

Figure 30. Propagation Delay vs. Temperature

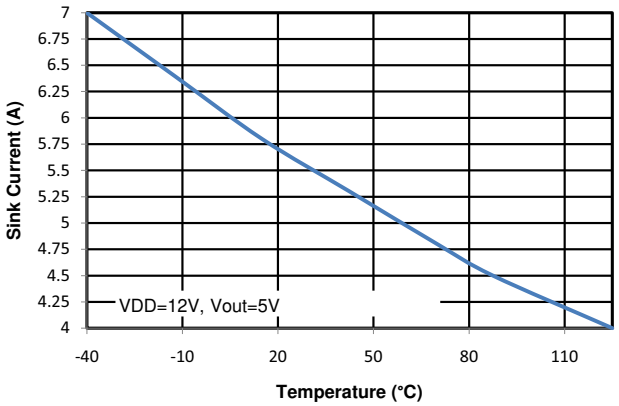

Figure 33. Output Sink Current vs. Temperature

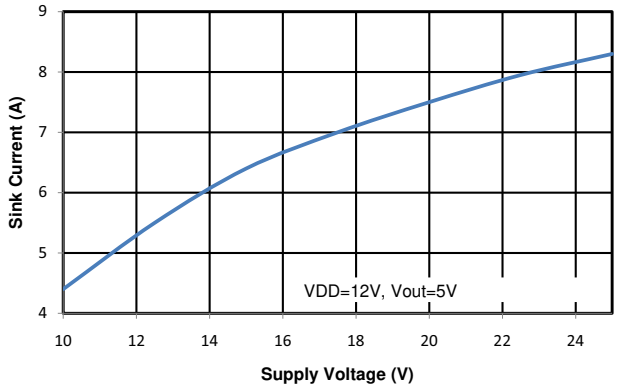

Figure 31. Output Sink Current vs. Supply Voltage

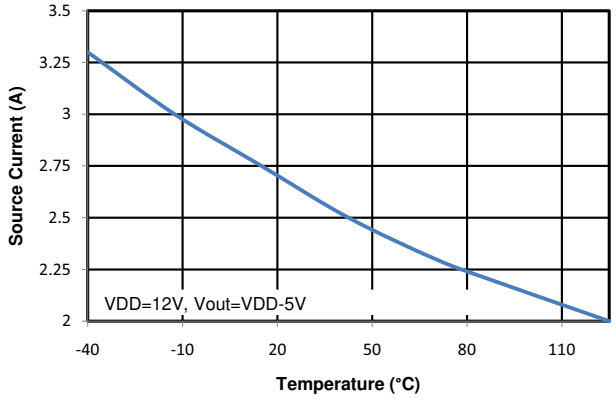

Figure 34. Output Source Current vs. Temperature

3.3. Family Overview and Logic Operation During Startup

The Si823x family of isolated drivers consists of high-side, low-side, and dual driver configurations.

3.3.1. Products

Table 9 shows the configuration and functional overview for each product in this family.

Table 9. Si823x Family Overview

Part Number	Configuration	Overlap Protection	Programmable Dead Time	Inputs	Peak Output Current (A)
Si8230	High-Side/Low-Side	✓	✓	VIA, VIB	0.5
Si8231	High-Side/Low-Side	✓	✓	PWM	0.5
Si8232/7	Dual Driver	—	—	VIA, VIB	0.5
Si8233	High-Side/Low-Side	✓	✓	VIA, VIB	4.0
Si8234	High-Side/Low-Side	✓	✓	PWM	4.0
Si8235/6/8	Dual Driver	—	—	VIA, VIB	4.0

3.3.2. Device Behavior

Table 10 consists of truth tables for the Si8230/3, Si8231/4, and Si8232/5/6 families.

Table 10. Si823x Family Truth Table[1]

Si8230/3 (High-Side/Low-Side) Truth Table						
Inputs		VDDI State	Disable	Output		Notes
VIA	VIB			VOA	VOB	
L	L	Powered	L	L	L	Output transition occurs after internal dead time expires.
L	H	Powered	L	L	H	Output transition occurs after internal dead time expires.
H	L	Powered	L	H	L	Output transition occurs after internal dead time expires.
H	H	Powered	L	L	L	Invalid state. Output transition occurs after internal dead time expires.
X[2]	X[2]	Unpowered	X	L	L	Output returns to input state within 7 µs of VDDI power restoration.
X	X	Powered	H	L	L	Device is disabled.
Si8231/4 (PWM Input High-Side/Low-Side) Truth Table						
PWM Input		VDDI State	Disable	Output		Notes
				VOA	VOB	
H		Powered	L	H	L	Output transition occurs after internal dead time expires.
L		Powered	L	L	H	Output transition occurs after internal dead time expires.
X[2]		Unpowered	X	L	L	Output returns to input state within 7 µs of VDDI power restoration.
X		Powered	H	L	L	Device is disabled.

Notes:

1. This truth table assumes VDDA and VDDB are powered. If VDDA and VDDB are below UVLO, see "3.7.2. Undervoltage Lockout" on page 26 for more information.
2. Note that an input can power the input die through an internal diode if its source has adequate current.

Table 10. Si823x Family Truth Table[1] (Continued)

Si8232/5/6/7/8 (Dual Driver) Truth Table						
Inputs		**VDDI State**	**Disable**	**Output**		**Notes**
VIA	**VIB**			**VOA**	**VOB**	
L	L	Powered	L	L	L	Output transition occurs immediately (no internal dead time).
L	H	Powered	L	L	H	Output transition occurs immediately (no internal dead time).
H	L	Powered	L	H	L	Output transition occurs immediately (no internal dead time).
H	H	Powered	L	H	H	Output transition occurs immediately (no internal dead time).
X[2]	X[2]	Unpowered	X	L	L	Output returns to input state within 7 µs of VDDI power restoration.
X	X	Powered	H	L	L	Device is disabled.

Notes:
1. This truth table assumes VDDA and VDDB are powered. If VDDA and VDDB are below UVLO, see "3.7.2. Undervoltage Lockout" on page 26 for more information.
2. Note that an input can power the input die through an internal diode if its source has adequate current.

3.4. Power Supply Connections

Isolation requirements mandate individual supplies for VDDI, VDDA, and VDDB. The decoupling caps for these supplies must be placed as close to the VDD and GND pins of the Si823x as possible. The optimum values for these capacitors depend on load current and the distance between the chip and the regulator that powers it. Low effective series resistance (ESR) capacitors, such as Tantalum, are recommended.

3.5. Power Dissipation Considerations

Proper system design must assure that the Si823x operates within safe thermal limits across the entire load range.The Si823x total power dissipation is the sum of the power dissipated by bias supply current, internal parasitic switching losses, and power dissipated by the series gate resistor and load. Equation 1 shows total Si823x power dissipation.

$$P_D = (V_{DDI})(I_{DDI}) + 2(I_{DD2})(V_{DD2}) + (f)(Q_{TL})(V_{DD2})\left[\frac{R_p}{R_p + R_g}\right] + (f)(Q_{TL})(V_{DD2})\left[\frac{R_n}{R_n + R_g}\right] + 2fCintV_{DD2}^2$$

where:

P_D is the total Si823x device power dissipation (W)

I_{DDI} is the input-side maximum bias current (3 mA)

I_{DD2} is the driver die maximum bias current (2.5 mA)

C_{int} is the internal parasitic capacitance (75 pF for the 0.5 A driver and 370 pF for the 4.0 A driver)

V_{DDI} is the input-side VDD supply voltage (2.7 to 5.5 V)

V_{DD2} is the driver-side supply voltage (10 to 24 V)

f is the switching frequency (Hz)

Q_{TL} is the total highside bootstrap charge (see Section 2.2 of AN486)

R_G is the external gate resistor

R_P is the $R_{DS(ON)}$ of the driver pull-up switch: (Rp=15Ω for the 0.5A driver; Rp=2.7Ω for the 4.0A driver)

R_n is the $R_{DS(ON)}$ of the driver pull-down switch: (Rn=5Ω for the 0.5A driver and 1Ω for the 4.0A driver)

Equation 1.

Power dissipation example for 0.5 A driver using Equation 1 with the following givens:

V_{DDI} = 5.0 V

V_{DD2} = 12 V

f = 350 kHz

R_G = 22 Ω

Q_G = 25 nC

$$Pd = 0.015 + 0.060 + (350 \times 10^3)(25 \times 10^{-9})(12)\left[\frac{15}{15 + 22}\right] + (f)(Q_{TL})(V_{DD2})\left[\frac{5}{5 + 22}\right] + 2[(350 \times 10^3)(75 \times 10^{-12})(144)]$$

= 140 mW

From which the driver junction temperature is calculated using Equation 2, where:

Pd is the total Si823x device power dissipation (W)

θ_{ja} is the thermal resistance from junction to air (105 °C/W in this example)

T_A is the ambient temperature

$$T_j = P_d \times \theta_{ja} + T_A$$
$$= (0.145)(105) + 20$$
$$= 35.2\ °C$$

The maximum power dissipation allowable for the Si823x is a function of the package thermal resistance, ambient temperature, and maximum allowable junction temperature, as shown in Equation 2:

$$P_{Dmax} \leq \frac{T_{jmax} - T_A}{\theta ja}$$

where:

P_{Dmax} = Maximum Si823x power dissipation (W)

T_{jmax} = Si823x maximum junction temperature (150 °C)

T_A = Ambient temperature (°C)

θja = Si823x junction-to-air thermal resistance (105 °C/W)

f = Si823x switching frequency (Hz)

Equation 2.

Substituting values for P_{Dmax} T_{jmax}, T_A, and θ_{ja} into Equation 2 results in a maximum allowable total power dissipation of 1.19 W. Maximum allowable load is found by substituting this limit and the appropriate data sheet values from Table 1 on page 6 into Equation 1 and simplifying. The result is Equation 3 (0.5 A driver) and Equation 4 (4.0 A driver), both of which assume VDDI = 5 V and VDDA = VDDB = 18 V.

$$C_{L(MAX)} = \frac{1.4 \times 10^{-3}}{f} - 7.5 \times 10^{-11}$$

Equation 3.

$$C_{L(MAX)} = \frac{1.4 \times 10^{-3}}{f} - 3.7 \times 10^{-10}$$

Equation 4.

Equation 1 and Equation 2 are graphed in Figure 35 where the points along the load line represent the package dissipation-limited value of CL for the corresponding switching frequency.

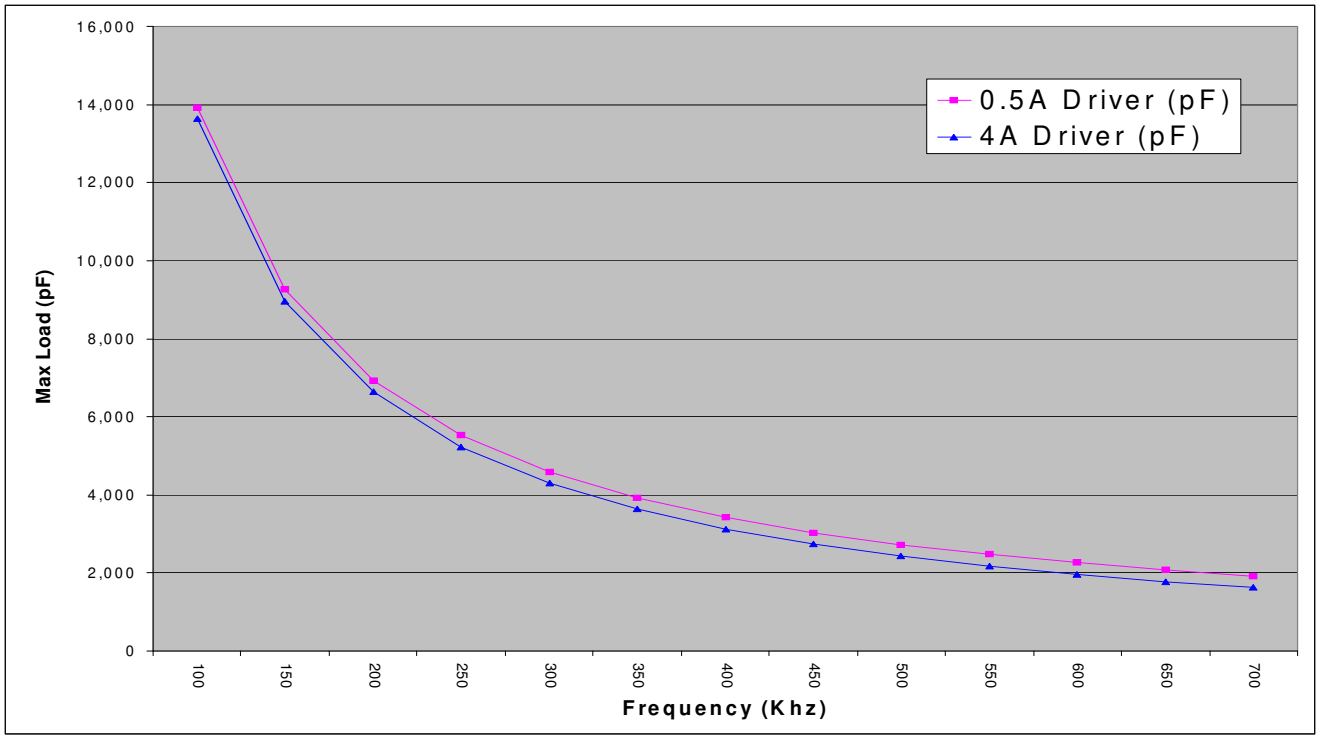

Figure 35. Max Load vs. Switching Frequency