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Si8281/82/83/84 Data Sheet

4.0 Amp ISODrivers with Integrated DC-DC Converters

The Si828x family (Si8281/82/83/84) is made up of isolated, high-current gate drivers with integrated system safety and feedback functions. These devices are ideal for driving power MOSFETs and IGBTs used in a wide variety of inverter and motor control applications. The Si828x isolated gate drivers utilize Silicon Labs' proprietary silicon isolation technology, supporting up to 5.0 kVrms withstand voltage per UL1577. This technology enables higher-performance, reduced variation with temperature and age, tighter part-to-part matching, and superior common-mode rejection compared to other isolated gate driver technologies.

In addition to the gate driver, the Si828x family integrates a dc-dc controller for simple implementation of an isolated supply for the driver side. The Si828x dc-dc controller can be ordered in two different configurations depending on what system voltage rails are available and the amount of power needed. The Si8281 and Si8283 have integrated power switch but are limited in dc-dc voltage input to the device bias. The Si8282 and Si8284 utilize and external power switch and are able to accept much higher voltage input power rail. User-adjustable frequency for minimizing emissions, a soft-start function for safety, and a shut-down option are available options. The device requires only minimal passive components and a miniature transformer.

The input to the device is a complementary digital input that can be utilized in several configurations. The input side of the isolation also has several control and feedback digital signals. The controller to the device receives information about the driver side power state and fault state of the device and recovers the device from fault through an active-low reset pin.

On the output side, Si828x devices provide separate pull-up and pull-down pins for the gate. A dedicated DSAT pin detects the desaturation condition and immediately shuts down the driver in a controlled manner. The Si828x devices also integrate a Miller clamp to facilitate a strong turn-off of the power switch.

Applications

- IGBT/ MOSFET gate drives
- Industrial, HEV, and renewable energy inverters
- AC, Brushless, and DC motor controls and drives
- Variable-speed motor controllers
- Isolated switch mode and UPS power supplies

Safety Regulatory Approvals (Pending)

- UL 1577 recognized
  - Up to 5000 V_{RMS} for 1 minute
- CSA component notice 5A approval
  - IEC 60950-1, 61010-1, 60601-1 (reinforced insulation)
- VDE certification conformity
  - IEC 60747-5-5/VDE0884 Part 10
- CQC certification approval
  - GB4943.1

KEY FEATURES

- 4 A IGBT driver
- System Safety Features
  - DESAT detection
  - FAULT feedback
  - Undervoltage Lock Out (UVLO)
  - Soft shutdown on fault condition
- Silicon Labs' high-performance isolation technology
  - Industry leading noise immunity
  - High speed, low latency and skew
  - Best reliability available
- 30 V driver-side supply voltage
- Integrated Miller clamp
- Power ready pin
- Complementary driver control input
- Compact packages: 20 and 24-pin wide-body SOIC
- Integrated DC-DC converter
  - Feedback-controlled converter with dithering for low EMI
  - DC-DC converter efficiency of 83%
  - Shutdown, frequency, and soft-start controls
- Industrial temp range: –40 to 125 °C

1. Ordering Guide

Ordering Part Number (OPN)	UVLO Voltage	DC/DC Features				Package
		Shutdown	Soft Start	Frequency Control	External Switch	
Si8281BD-IS	9 V	No	No	No	No	WB SOIC-20
Si8281CD-IS	12 V	No	No	No	No	WB SOIC-20
Si8282BD-IS	9 V	No	No	No	Yes	WB SOIC-20
Si8282CD-IS	12 V	No	No	No	Yes	WB SOIC-20
Si8283BD-IS (Sampling)	9 V	Yes	Yes	Yes	No	WB SOIC-24
Si8283CD-IS (Sampling)	12 V	Yes	Yes	Yes	No	WB SOIC-24
Si8284BD-IS (Sampling)	9 V	Yes	Yes	Yes	Yes	WB SOIC-24
Si8284CD-IS (Sampling)	12 V	Yes	Yes	Yes	Yes	WB SOIC-24

Note: Add an "R" at the end of the Part Number to denote Tape and Reel option.

2. System Overview

2.1 Isolation Channel Description

The operation of an Si828x channel is analogous to that of an optocoupler and gate driver, except an RF carrier is modulated instead of light. This simple architecture provides a robust isolated data path and requires no special considerations or initialization at start-up. A simplified block diagram for a single Si828x channel is shown in the figure below.

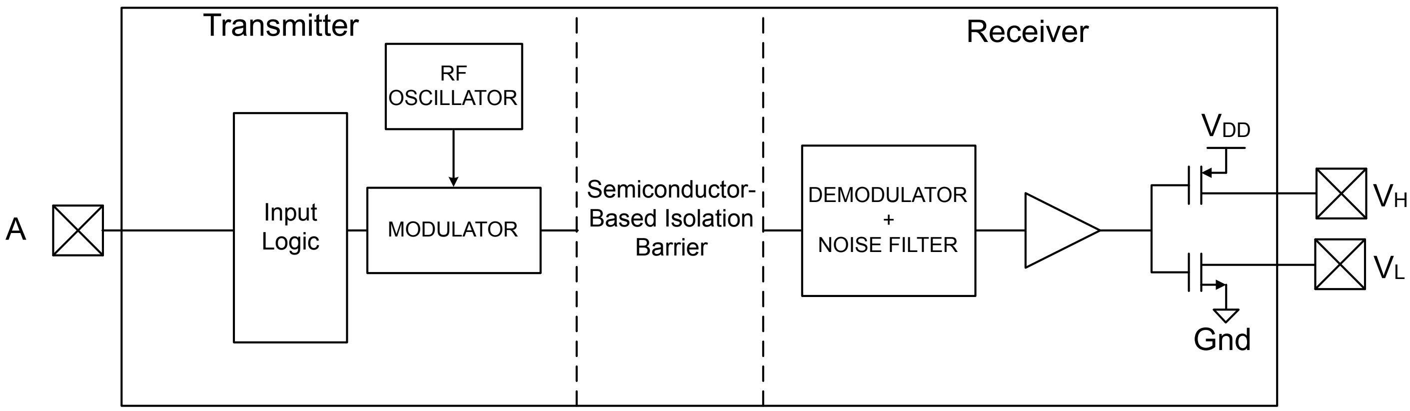

Figure 2.1. Simplified Channel Diagram

A channel consists of an RF Transmitter and RF Receiver separated by a semiconductor-based isolation barrier. Referring to the Transmitter, input A modulates the carrier provided by an RF oscillator using on/off keying. The Receiver contains a demodulator that decodes the input state according to its RF energy content and applies the result to output B via the output driver. This RF on/off keying scheme is superior to pulse code schemes as it provides best-in-class noise immunity, low power consumption, and better immunity to magnetic fields.

2.2 Device Behavior

The following table shows state relationships for the Si828x inputs and outputs.

Table 2.1. Si8281/82/83/84 Truth Table

IN+	IN–	VDDA State	VDDB–VMID State	Desaturation State	VH	VL	RDY	FLTb
H	H	Powered	Powered	Undetected	Hi-Z	Pull-down	H	H
H	L	Powered	Powered	Undetected	Pull-up	Hi-Z	H	H
L	X	Powered	Powered	Undetected	Hi-Z	Pull-down	H	H
X	X	Powered	Unpowered	—	—	—	L	H
X	X	Powered	Powered	Detected	Hi-Z	Pull-down[1]	H	L

Note:

1. Driver state after soft shutdown.

2.3 Input

The IN+ and IN– inputs to the Si828x devices act as a complementary pair. If the IN– is held low, the IN+ will act as a active-high input for the driver control. Alternatively, if IN+ is held high, then the IN– can be used as an active-low input for driver control. When the IN– is used as the control signal, taking the IN+ low will hold the output driver low.

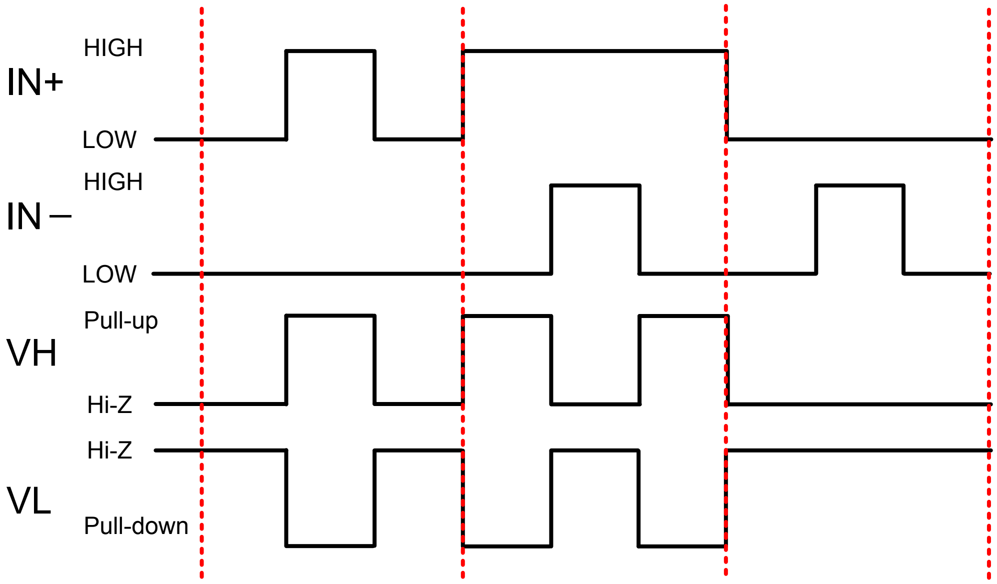

Figure 2.2. Si828x Complementary Input Diagram

2.4 Driver Side Output

The Si828x has separate pins for gate drive high (VH) and gate drive low (VL). This makes it simple for the user to use different gate resistors to control IGBT V_{CE} rise and fall time.

2.5 Fault (FLTb) Pin

FLTb is an open-drain type output. Once the UVLO condition is cleared on the driver side of the device, the FLTb pin is released. A pull-up resistor takes the pin high. When the desaturation condition is detected, the Si828x indicates the fault by bringing the FLTb pin low. FLTb stays low until the controller brings the RSTb pin low.

FLTb is also taken low if the UVLO condition is met during device operation. FLTb is released in that case as soon as the UVLO condition is cleared.

2.6 Reset (RSTb) Pin

The RSTb pin is used to clear the desaturation condition and bring the Si828x driver back to an operational state. Even though the input may be toggling, the driver will not change state until the fault condition has been reset.

2.7 Ready (RDY) Pin

The ready pin indicates to the controller that power is available on both sides of the isolation, i.e., at VDDA and VDDB. RDY goes high when both the primary side and secondary side UVLO circuits are disengaged. If the UVLO conditions are met on either side of the isolation barrier, the ready pin will return low. RDY is a push-pull output pin and can be floated if not used.

2.8 Undervoltage Lockout (UVLO)

The UVLO circuit unconditionally drives VL low when VDDB is below the lockout threshold. The Si828x is maintained in UVLO until VDDB rises above $VDDB_{UV+}$. During power down, the Si828x enters UVLO when VDDB falls below the UVLO threshold plus hysteresis (i.e., $VDDB \leq VDDB_{UV+} - VDDB_{HYS}$).

2.9 Desaturation Detection

The Si828x provides sufficient voltage and current to drive and keep the IGBT in saturation during on time to minimize power dissipation and maintain high efficiency operation. However, abnormal load conditions can force the IGBT out of saturation and cause permanent damage to the IGBT.

To protect the IGBT during abnormal load conditions, the Si828x detects an IGBT desaturation condition, shuts down the driver upon detecting a fault, and provides a fault indication to the controller. These integrated features provide desaturation protection with minimum external BOM cost. The figure below illustrates the Si828x desaturation circuit. When the Si828x driver output is high, the internal current source is on, and this current flows from the DSAT pin to charge the C_{BL} capacitor. The voltage on the DSAT pin is monitored by an internal comparator. Since the DSAT pin is connected to the IGBT collector through the D_{DSAT} and a small R_{DSAT}, its voltage is almost the same as the V_{CE} of the IGBT. If the V_{CE} of the IGBT does not drop below the Si828x desaturation threshold voltage within a certain time after turning on the IGBT (blanking period) the block will generate a fault signal. The Si828x desaturation hysteresis is fixed at 220 mV and threshold is nominally 7 V.

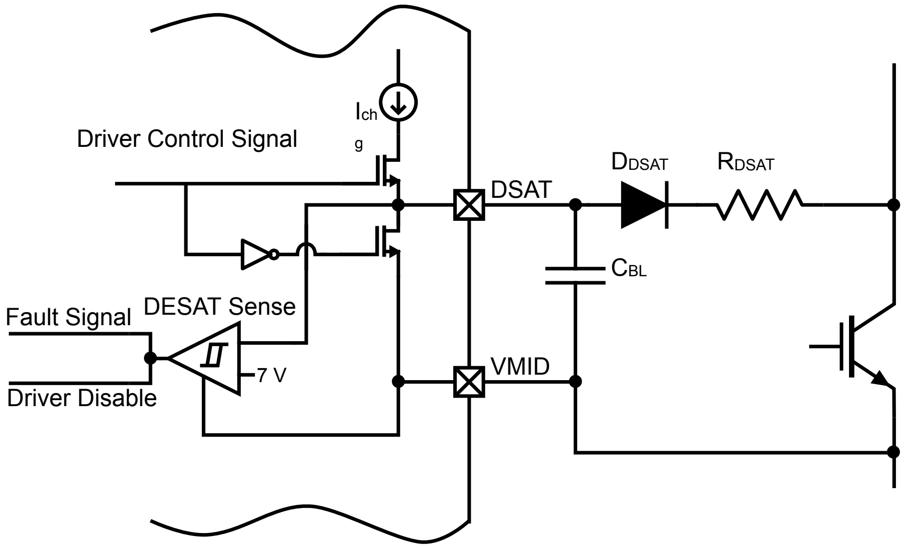

Figure 2.3. Desaturation Circuit

As an additional feature, the block supports a blanking timer function to mask the turn-on transient of the external switching device and avoid unexpected fault signal generation. This function requires an external blanking capacitor, C_{BL}, of typically 390 pF between DSAT and VMID pins. The block includes a 1 mA current source (I_{Chg}) to charge the C_{BL}. This current source, the value of the external C_{BL}, and the programmed fault threshold, determine the blanking time ($t_{Blanking}$).

$$t_{Blanking} = C_{BL} \times \frac{V_{DESAT}}{I_{chg}}$$

An internal nmos switch is implemented between DSAT and VMID to discharge the external blanking capacitor, C_{BL}, and reset the blanking timer. The current limiting R_{DSAT} resistor protects the DSAT pin from large current flow toward the IGBT collector during the IGBT's body diode freewheeling period (with possible large collector's negative voltage, relative to IGBT's emitter).

2.10 Soft Shutdown

To avoid excessive dV/dt on the IGBT's collector during fault shut down, the Si828x implements a soft shut down feature to discharge the IGBT's gate slowly. When soft shut down is activated, the high power driver goes inactive, and a weak pull down via VH and external RH discharges the gate until the gate voltage level is reduced to the VSSB + 2 V level. The high power driver is then turned on to clamp the IGBT gate voltage to VMID.

After the soft shut down, the Si828x driver output voltage is clamped low to keep the IGBT in the off state.

2.11 Miller Clamp

IGBT power circuits are commonly connected in a half bridge configuration with the collector of the bottom IGBT tied to the emitter of the top IGBT.

When the upper IGBT turns on (while the bottom IGBT is in the off state), the voltage on the collector of the bottom IGBT flies up several hundred volts quickly (fast dV/dt). This fast dV/dt induces a current across the IGBT collector-to-gate capacitor (C_{CG} that constitutes a positive gate voltage spike and can turn on the bottom IGBT. This behavior is called Miller parasitic turn on and can be destructive to the switch since it causes shoot through current from the rail right across the two IGBTs to ground. The Si828x Miller clamp's purpose is to clamp the gate of the IGBT device being driven by the Si828x to prevent IGBT turn on due to the collector C_{CG} coupling.

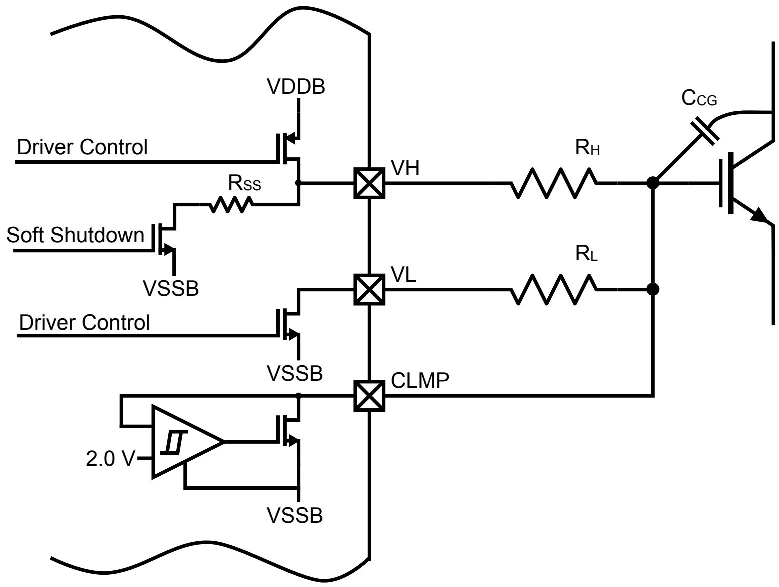

Figure 2.4. Miller Clamp Device

The Miller clamp device (Clamp) is engaged after the main driver had been on (VL) and pulled IGBT gate voltage close to VSSB, such that one can consider the IGBT being already off. This timing prevents the Miller clamp from interfering with the driver's operation. The engaging of the Miller Clamp is done by comparing the IGBT gate voltage with a 2.0 V reference (relative to VSSB) before turning on the Miller clamp NMOS.

2.12 DC-DC Converter Application Information

The Si828x isolated dc-dc converter is based on a modified fly-back topology and uses an external transformer and rectifying diodes for low cost and high operating efficiency. The PWM controller operates in closed-loop, current mode control and generates isolated output voltages with up to 2 W average output power at VDDP = 5.0 V. Voltage feedback is referenced between VDDB-VSSB. Although there is only one voltage feedback path, two output voltages are realized by the tight coupling of the two secondary transformer windings. Options are available for 24 Vdc input operation and externally configured switching frequency.

The dc-dc controller modulates a pair of internal, primary-side power switches (see Figure 2.5 Si8281/83 Block Diagram: 3 V–5 V Input to Split Voltage Output on page 8) to generate an isolated voltage at external diode D1 and D2. Divider resistors, R1 and R2, generate proper 1.05 V for the VSNS pin. Closed-loop feedback is provided by an internal compensated error amplifier, which compares the voltage at the VSNS pin to an internal voltage reference. The resulting error voltage is fed back across the isolation barrier via an internal feedback path to the controller, thus completing the control loop.

For input supply voltages higher than 5 V, an external FET Q2 is modulated by a driver pin ESW as shown in Figure 2.6 Si8282/84 Block Diagram: >5.5 V Input to Split Voltage Output on page 9. A shunt resistor based voltage sense pin, RSN, provides current sensing capability to the controller.

The Vin must be able to support the Si828x VDDB-VSSD static load current (approximately 9 mA), the output drive load requirement, and the dc-dc power dissipation (loss). The driver power requirement is dependent on the IGBT gate charge and the driver switching frequency. Below are the equations to calculate the Vin power requirement.

$$Pvin = \frac{\left(9 \times 10^{-3} \times (VDDB + VSSB) + Qg \times Fsw\right)}{\eta}$$

where:

Qg = IGBT total gate charge

Fsw = driver switching frequency

η = dc-dc efficiency (approximately 78%)

Additional part number features include an externally-triggered shutdown of the converter functionality using the SH pin and a programmable soft start configured by a capacitor connected to the SS pin. The resistor value on pin SH/FC and the capacitor value on pin SS are used during power-up to set the dc-dc switching frequency. Note that pin SH/FC and SS pins are available on the Si8283 and Si8284 only. The Si828x can be used with a low-voltage power rail or a high-voltage power rail. These features and configurations are explained in more detail in other sections.

2.12.1 External Transformer Driver

The dc-dc controller has internal switches (VSW) for driving the transformer with up to a 5.5 V voltage supply. For higher voltages on the primary side, a driver output (ESW) is provided on the Si8282 and Si8284 that can switch an external NMOS power transistor for driving the transformer. When this configuration is used, a shunt resistor based voltage sense pin (RSN) provides current sensing to the controller.

2.12.2 Output Voltage Control

The isolated output voltage, VOUT (VDDB–VSSB), is sensed by a resistor divider that provides feedback to the controller through the VSNS pin. The voltage error is encoded and transmitted back to the primary side controller across the isolation barrier, which in turn changes the duty cycle of the transformer driver. The equation for VOUT is as follows:

$$VOUT = VSNS \times \left(1 + \frac{R1}{R2}\right)$$

The VDDB-VSSB voltage split is depended on the ratio of the two secondary windings and can be calculated as follows:

$$VDDB - VMID = VOUT \times \left(\frac{S1}{S1 \times S2}\right)$$

$$VSSB - VMID = VOUT \times \left(\frac{S2}{S1 + S2}\right)$$

2.12.3 Compensation

The dc-dc converter operates in current mode control. The loop is compensated by connecting an external resistor in series with a capacitor from the COMP pin to VSSB. The compensation network, RCOMP, and CCOMP are set to 200 kΩ and 1 nF for most Si828x applications.

2.12.4 Thermal Protection

A thermal shutdown circuit is implemented to protect the system from over-temperature events. The thermal shutdown is activated at a junction temperature that prevents permanent damage from occurring.

2.12.5 Cycle Skipping

Cycle skipping is included to reduce switching power losses at light loads. This feature is transparent to the user and is activated automatically at light loads. The product options with integrated power switches (Si8281/83) may never experience cycle skipping during operation, even at light loads, while the external power switch options (Si8282/84) are likely to have cycle skipping start at light loads.

2.12.6 Shutdown (Si8283 and Si8284 Only)

This feature allows the operation of the dc-dc converter to be shut down when SH/FC is asserted high. This pin normally has a resistor to ground, the value of which is used in conjunction with the value of the capacitor on the SS pin during startup to determine the dc-dc switching frequency. Therefore, a GPIO pin connected to SH/FC pin to control the shutdown function should be in a high-impedance state during startup to avoid interfering with the internal frequency calculation circuit. During normal operation, this pin should be held low and only taken high to assert dc-dc shutdown.

2.12.7 Soft Start (Si8283 and Si8284 Only)

The dc-dc controller has an internal timer that controls the power conversion start-up to limit inrush current. There is also a Soft Start option where users can program the soft start up by an external capacitor connected to the SS pin.

The soft start period is the maximum duration of time that the Si8283/84 will try to ramp up the output voltage. If the output voltage fails to reach the targeted voltage level within this soft start period, the Si8283/84 will terminate the dc-dc startup cycle and wait for 40 seconds before initiating a new (startup) cycle.

The equations for setting the soft start period are as follows:

$$t_{SS} = 200000 \times C_{SS}$$

or

$$C_{SS} = \frac{t_{SS}}{200000}$$

2.12.8 Programmable Frequency (Si8283 and Si8284 Only)

The frequency of the PWM modulator is set to a default of 250 kHz for Si828x. Users can program their desired frequency within a given band of 200 kHz to 800 kHz by controlling the time constant of an external RC connected to the SH_FC and SS pins.

The equations for setting f_{SW} or R_{SW} are as follows:

$$f_{SW} = \frac{1025.5}{(R_{SW} \times C_{SS})}$$

or

$$R_{SW} = \frac{1025.5}{(f_{SW} \times C_{SS})}$$

The following are the recommended steps for calculating C_{SS} and R_{SW}:

1. Select the maximum soft start duration (typically 40 ms).
2. Calculate Css using Equation A.
3. Select the dc-dc switching frequency.
4. Calculate R_{SW} using the above equation.

2.12.9 Low Supply Voltage Configuration

The low supply voltage configuration is used when 3.0 V to 5.5 V supply rails are available. All product options of the Si8281 and Si8283 are intended for this configuration.

An advantage of Si828x devices over other converters that use this same topology is that the output voltage is sensed on the secondary side without requiring additional optocouplers and support circuitry to bias those optocouplers. This allows the dc-dc to operate with superior line and load regulation while reducing external components and increasing lifetime reliability.

In a typical isolated gate driver application, the dc-dc powers the Si8281 and Si8283 VDDB and VSSB as shown in the figure below. The Si8281 and Si8283 dc-dc circuit in the figure below can deliver up to 2 W of output power for V_{in} = 5 V and 1 W for V_{in} = 3.3 V. The dc-dc requires an input capacitor, C_2, blocking capacitor, C_1, transformer, T_1, rectifying diodes, D_1 and D_2, and output capacitors, C_{26}, and C_{27}. Resistors R_1 and R_2 divide the output voltage to match the internal reerence of the error amplifier. The ratio of the two secondary windings, S1 and S2, splits the output voltage into two portions. The positive VDDB and the negative VSSB with common reference to VMID (IGBT Emitter).

$$VDDB = VOUT \times \left(\frac{S1}{S1 + S2}\right)$$

$$VSSB = -VOUT \times \left(\frac{S2}{S1 + S2}\right)$$

Type 1 loop compensation made by RCOMP and CCOMP are required at the COMP pin. The combination of RCOMP = 200 kΩ and CCOMP = 1 nF satisfies most Si8281 and Si8283 dc-dc applications. Though it is not necessary for normal operation, we recommend that an RC snubber (not shown) be placed in parallel with the secondary winding to minimize radiated emissions.

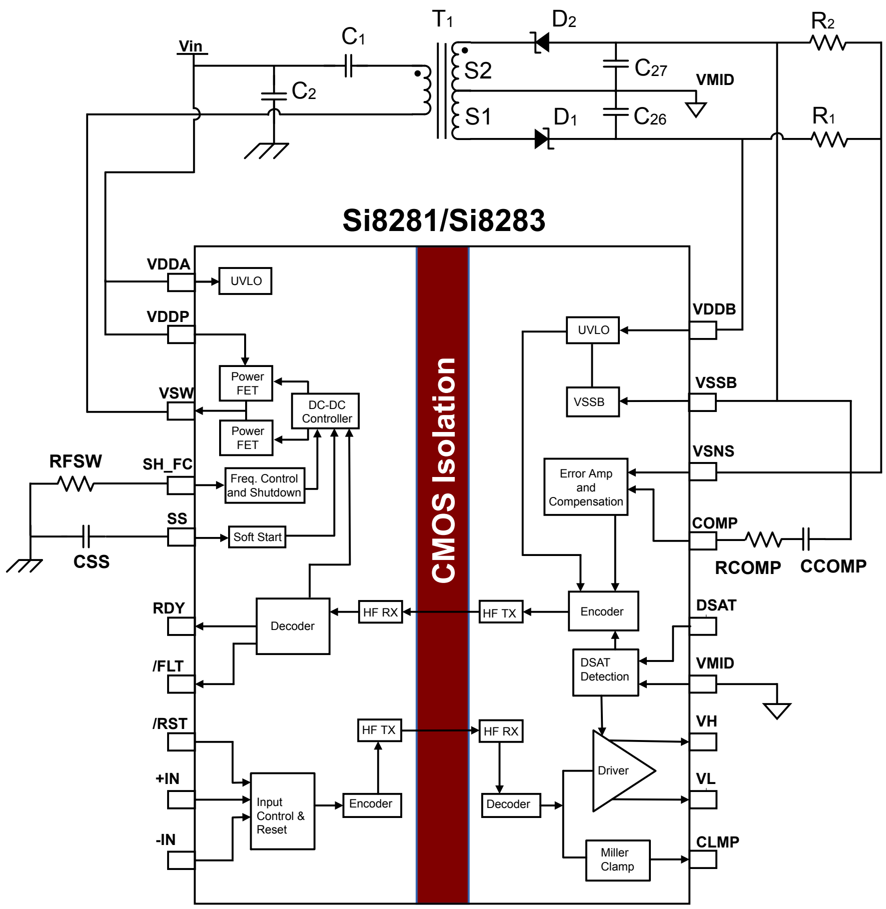

Figure 2.5. Si8281/83 Block Diagram: 3 V–5 V Input to Split Voltage Output

2.12.10 High Supply Voltage Configuration

2h

=.w..]6+*28x9q\\-

The high supply voltage configuration is used when a higher voltage power supply rail (up to 24 V) is available. All product options of the Si8282 and Si8284 are intended for this configuration. The dc-dc converter uses the isolated flyback topology. With this topology, the switch and sense resistor are external, allowing higher switching voltages.

The output voltage is sensed on the secondary side without requiring additional optocouplers and support circuitry to bias those opto-couplers. This allows the dc-dc to operate with superior line and load regulation.

The figure below shows the block diagram of an Si828x with external components. The Si8284 product option has externally controlled switching frequency and soft start. The dc-dc requires input capacitor C_{28}, transformer T_1, switch Q_4, sense resistor R_{sense}, rectifying diodes D_1 and D_2, and output capacitors C_{26} and C_{27}. To supply VDDA, Q_3 transistor is biased by R_{23}, 5.6 V Zener diode D_5 and filtered by C_{30} and C_{11}. External frequency and soft start behavior is set by CSS and RFSW. Resistors R_1 and R_2 divide the output voltage to match the internal reference of the error amplifier. The ratio of the two secondary windings splits the output voltage into two portions. The positive VDDB and the negative VSSB with common reference to VMID (IGBT Emitter).

$$VDDB = VOUT \times \left(\frac{S1}{S1 + S2}\right)$$

$$VSSB = -VOUT \times \left(\frac{S2}{S1 + S2}\right)$$

Type 1 loop compensation made by RCOMP and CCOMP are required at the COMP pin. The combination of RCOMP = 49.9 kΩ and CCOMP = 1.5 nF satisfies most Si8282 and Si8284 dc-dc applications. Though it is not necessary for normal operation, we recommend to use RC snubbers (not shown) on both primary and secondary windings to minimize high-frequency emissions.

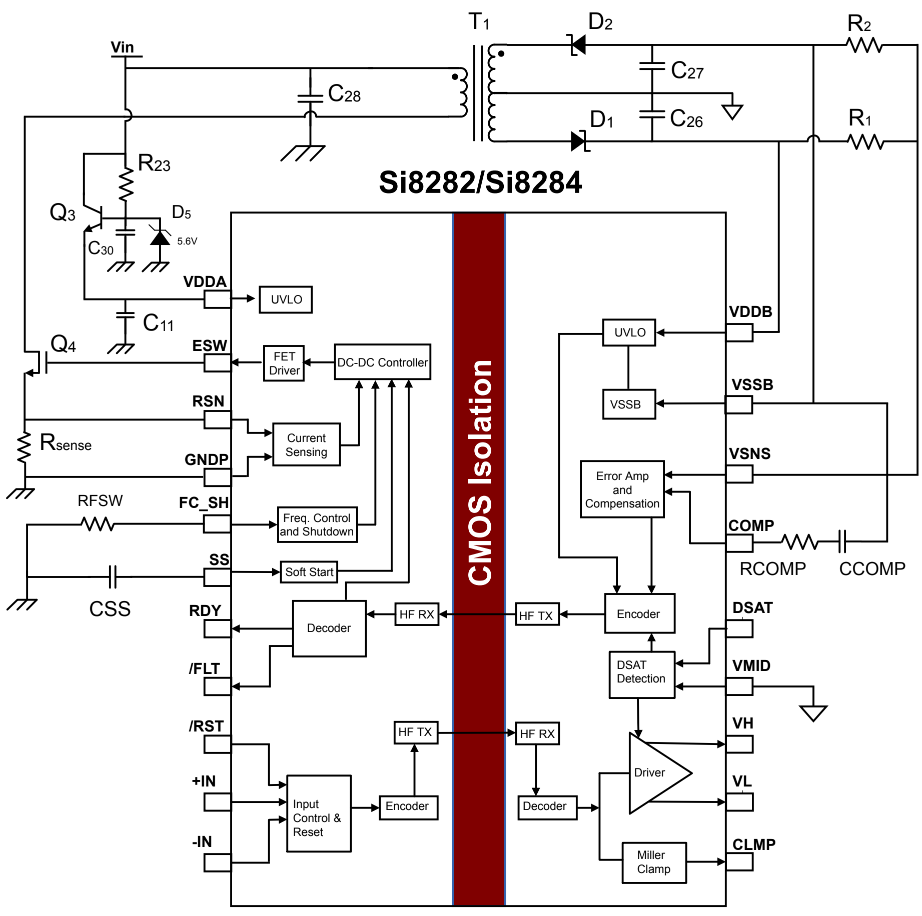

Figure 2.6. Si8282/84 Block Diagram: >5.5 V Input to Split Voltage Output

2.13 Transformer Design

The internal switch dc-dc (Si8281, Si8283) and external switch dc-dc (Si8282, Si8284) operate in different topologies and, thus, require different transformer designs. The table below provides a list of transformers and their parametric characteristics that have been validated to work with Si828x products. It is recommended that users order the transformers from the vendors per the part numbers given below.

To manufacture transformers from your preferred suppliers that may not be listed below, please specify to supplier the parametric characteristics as specified in the table below for a given input voltage and isolation rating.

Table 2.2. Si828x Recommended Transformers

Transformer Supplier	Ordering Part #	Input Voltage	Turns Ratio	Leakage Inductance	Primary Inductance	Primary Resistance	Isolation Rating
UMEC www.umec-usa.com	UTB02257s	3.0–5.5 V	1:15:5	125 nH max	1.5 µH ± 5%	0.05 Ω max	5 kV
	UTB02241s	4.5–5.5 V	1:9:33.667	100 nH max	2 µH ± 5%	0.05 Ω max	5 kV
	UTB02253s	7–24 V	1.2:1.21	200 nH max	25 µH ± 5%	0.225 Ω max	5 kV
Coilcraft www.coilcraft.com	TA7788-AL	7–24 V	1:1.25:0.75	550 nH max	25 µH ± 5%	0.460 Ω max	5 kV

3. Applications Information

The following sections detail the input and output circuits necessary for proper operation.

3.1 Recommended Application Circuits

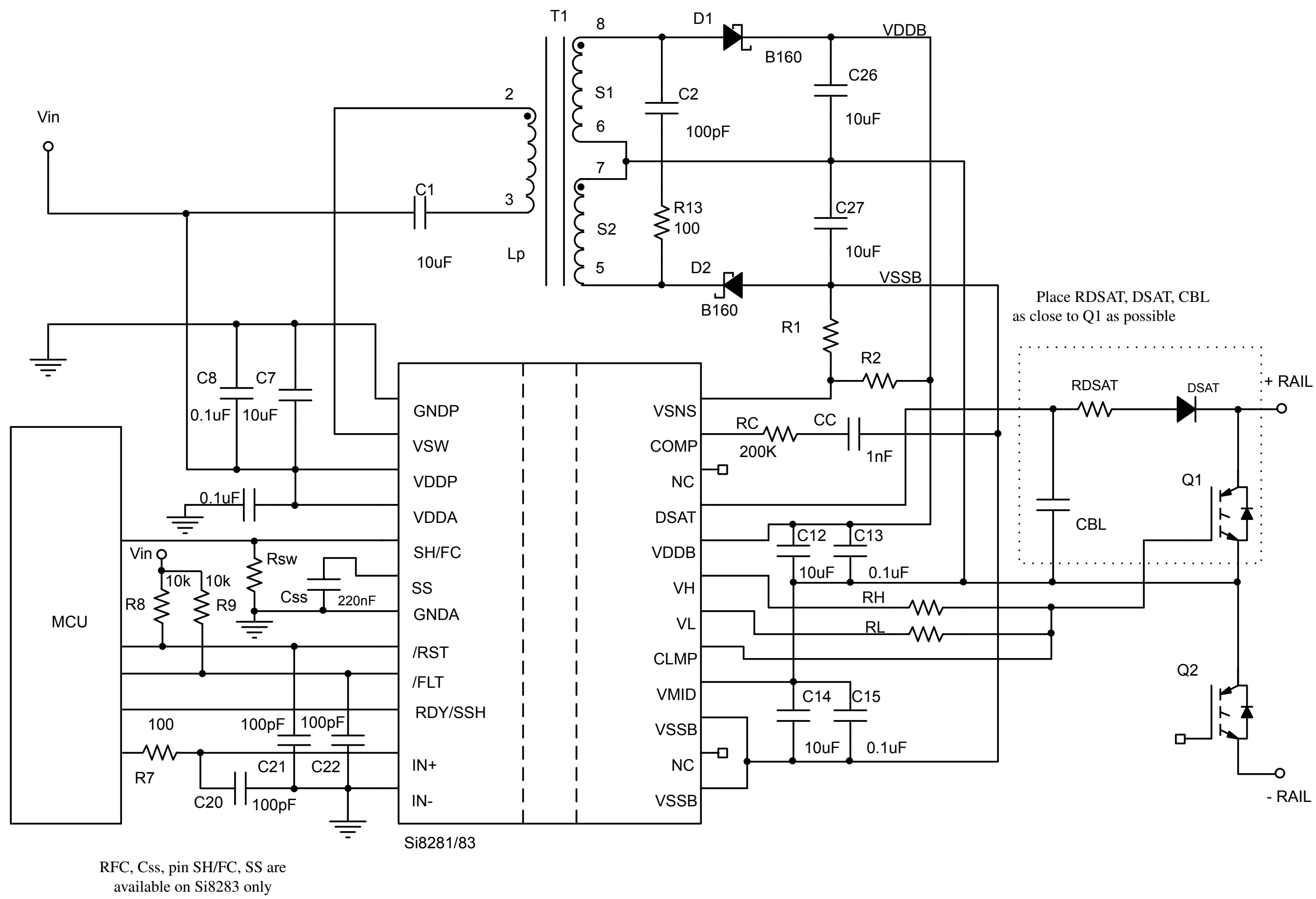

Figure 3.1. Recommended Si8281/83 Application Circuit

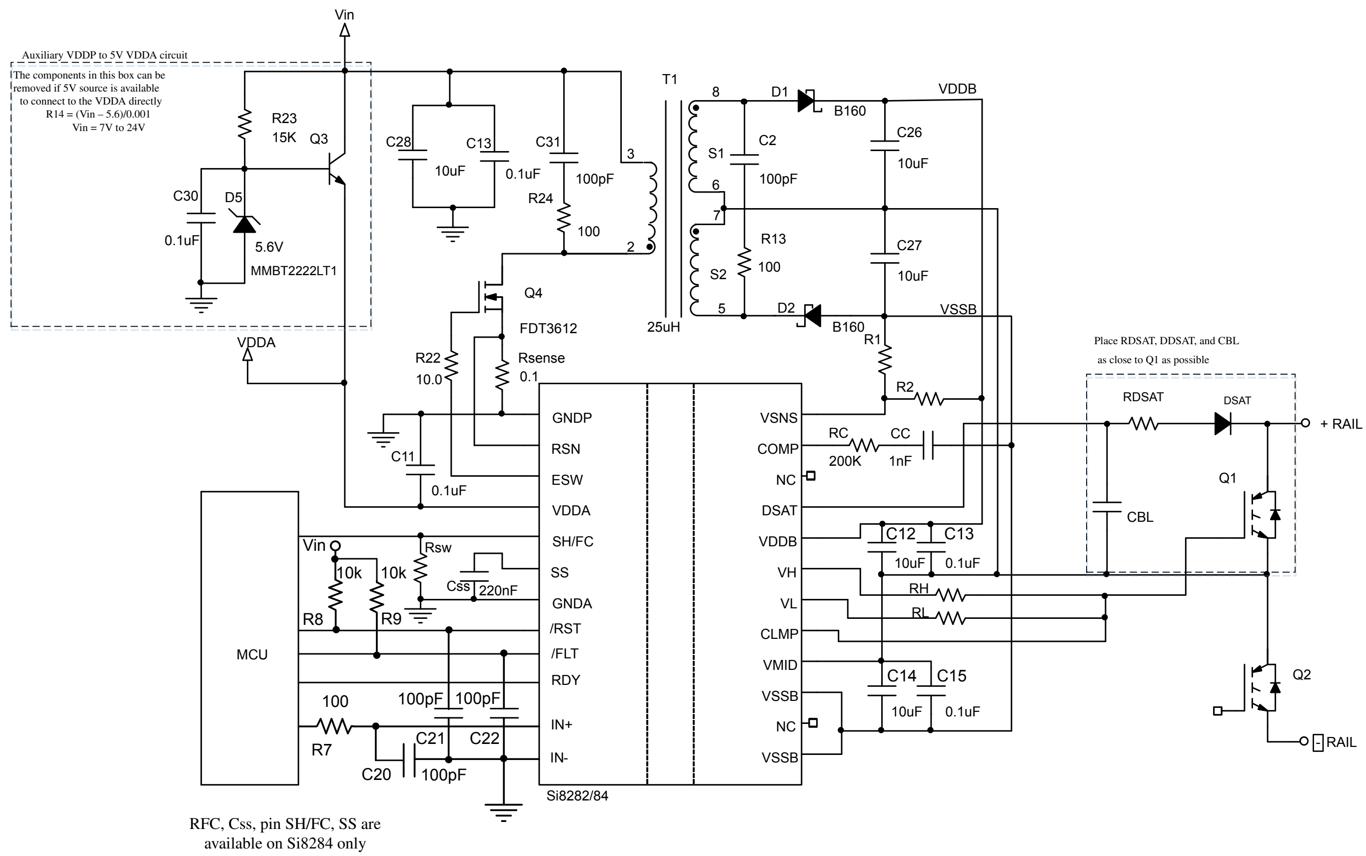

Figure 3.2. Recommended Si8282/84 Application Circuit

The Si828x has both inverting and non-inverting gate control inputs (IN– and IN+). In normal operation, one of the inputs is not used, and should be connected to GNDA (IN–) or VDDA (IN+) for proper logic termination. The Si828x has an active low reset input (RSTb), an active high ready (RDY) push pull output, and an open drain fault (FLTb) output that requires a weak 10 kΩ pull-up resistor. The Si828x gate driver will shut down when a fault is detected. It then provides FLTb indication to the MCU, and remains in the shutdown state until the MCU applies a reset signal.

The desaturation sensing circuit consisted of the 380 pF blanking capacitor, 100 Ω current limiting resistor, and DSAT diode. These components provide current and voltage protection for the Si828x desaturation DSAT pin and it is critical to place these components as close to the IGBT as possible. Also, on the layout, make sure that the loop area forming between these components and the IGBT be minimized for optimum desaturation detection. The Si828x has VH and VL gate drive outputs with external RH and RL resistors to limit output gate current. The value of these resistors can be adjusted to independently control IGBT collector voltage rise and fall time. The CLMP output should be connected to the gate of the IGBT directly to provide clamping action between the gate and VSSB. This clamping action dissipates IGBT Miller current from collector to the gate to secure the IGBT in the off-state.

3.1.1 Inputs

Inputs should be driven by CMOS level push-pull output. If input is driven by the MCU GPIO, it is recommended that the MCU be located as closed to the Si828x as possible to minimize PCB trace parasitic and noise coupling to the input circuit. In noisy environments, it is customary to add a small series resistor, and a decoupling cap to the IN traces (R7, C20 in Figure 3.1 Recommended Si8281/83 Application Circuit on page 11 and Figure 3.2 Recommended Si8282/84 Application Circuit on page 12). These RC filters attenuate glitches from electrical noise and improve input-to-output signal integrity.

3.1.2 Reset, RDY, and Fault

The Si828x has an active high ready (RDY) push pull output, an open drain fault (FLTb) output, and an active low reset input (RSTb) that require pull-up resistors (R8 and R9). Fast common-mode transients in high-power circuits can inject noise and glitches into these pins due to parasitic coupling. Depending on the IGBT power circuit layout, additional capacitance (use 100 pF to 470 pF for C21 and C22) can be included on these pins to prevent faulty RDY and FLTb indications as well as unintended reset to the device.

The FLTb outputs from multiple Si828x devices can be connected in an OR wiring configuration to provide a single FLTb signal to the MCU.

3.1.3 Desaturation

The desaturation sensing circuit consists of the blanking capacitor (390 pF recommended), 100 Ω current limiting resistor, and DSAT diode. These components provide current and voltage protection for the Si828x desaturation DSAT pin, and it is critical to place these components as close to the IGBT as possible. Also, in the layout, the loop area forming between these components and the IGBT should be minimized for optimum desaturation detection.

3.1.4 Driver Outputs

The Si828x has VH and VL gate drive outputs (see Figure 3.1 Recommended Si8281/83 Application Circuit on page 11). They work with external RH and RL resistors to limit output gate current. The value of these resistors can be adjusted to independently control IGBT collector voltage rise and fall time.

The CLMP output should be connected to the gate of the IGBT directly to provide clamping action between the gate and VSSB pin. This clamping action dissipates IGBT Miller current from the collector to the gate to secure the IGBT in the off-state. Negative VSSB provides further help to ensure the gate voltage stays below the IGBT's Vth during the off state.

3.2 Layout Considerations

It is most important to minimize ringing in the drive path and noise on the supply lines. Care must be taken to minimize parasitic inductance in these paths by locating the Si828x as close as possible to the device it is driving. In addition, the supply and ground trace paths must be kept short. For this reason, the use of power and ground planes is highly recommended. A split ground plane system having separate ground and power planes for power devices and small signal components provides the best overall noise performance.

3.3 Power Dissipation Considerations

Proper system design must assure that the Si828x operates within safe thermal limits across the entire load range. The Si828x total power dissipation is the sum of the power dissipated by bias supply current, internal parasitic switching losses, and power dissipated by the series gate resistor and load. Equation 1 shows total Si828x power dissipation.

$$PD = (VDDA)(IDDA) + 1.05(VDDB)(IDDB) + 1.05 \times f \times Q_{\text{int}} \times VDDB + \frac{1.05}{2}(f)(Q_{IGBT})(VDDB)\left[\frac{Rp}{Rp + RH} + \frac{Rn}{Rn + RL}\right]$$

where:

PD is the total Si828x device power dissipation (W).

IDDA is the input-side maximum bias current (7.5 mA).

IDDB is the driver die maximum bias current (10.8 mA).

Q_{int} is the internal parasitic charge (3 nC).

VDDA is the input-side VDD supply voltage (2.7 to 5.5 V).

VDDB is the total driver-side supply voltage (VDDB + VSSB: 12.5 to 30 V).

f is the IGBT switching frequency (Hz).

RH is the VH external gate resistor, RL is the VL external gate resistor.

Rp is the $RDS_{(ON)}$ of the driver pull-up switch: (2.6 Ω).

Rn is the $RDS_{(ON)}$ of the driver pull-down switch: (0.8 Ω).

Equation 1.

To account for the Si828x dc-dc loss, an additional 5% of power is added to the driver-side circuit (VDDB). The maximum power dissipation allowable for the Si828x is a function of the package thermal resistance, ambient temperature, and maximum allowable junction temperature, as shown in Equation 2:

$$PD\text{max} \le \frac{Tj\text{max} - TA}{\theta ja}$$

where:

PDmax = Maximum Si828x power dissipation (W).

Tjmax = Si828x maximum junction temperature (150 °C).

TA = Ambient temperature (°C)

θja = Si828x junction-to-air thermal resistance (60 °C/W for four-layer PCB)

f = Si828x switching frequency (Hz)

Equation 2.

Substituting values for PDmax Tjmax (150 °C), TA (125 °C), and θja (60 °C/W) into Equation 2 results in a maximum allowable total power dissipation of 0.42 W.

$$PD\text{max} \le \frac{150 - 125}{60} = 0.42W$$

Maximum allowable load is found by substituting this limit and the appropriate data sheet values from Table 4.1 into Equation 1 and simplifying. The result is Equation 3.

$$PD = (VDDA)(IDDA) + 1.05(VDDB)(IDDB) + 1.05 \times f \times \text{Qint} \times VDDB + \frac{1.05}{2}(f)(Q_L)(VDDB)\left[\frac{Rp}{Rp + RH} + \frac{Rn}{Rn + RL}\right]$$

$$PD = (VDDA)(IDDA) + 1.05(VDDB)(IDDB) + 1.05 \times f \times \text{Qint} \times VDDB + \frac{1.05}{2}(f)(C_L)(VDDB^2)\left[\frac{Rp}{Rp + RH} + \frac{Rn}{Rn + RL}\right]$$

$$0.42 = (VDDA)(0.0075) + 1.05(VDDB)(0.0108) + 1.05 \times f \times 3 \times 10^{-9} \times VDDB + \frac{1.05}{2}(f)(C_L)(VDDB^2)\left[\frac{2.6}{2.6 + 15} + \frac{0.8}{0.8 + 10}\right]$$

$$0.42 - (VDDA)(0.0075) - 1.05(VDDB)(0.0108) - 1.05 \times f \times 3 \times 10^{-9} \times VDDB = 0.117 VDDB^2 f(C_L)$$

$$C_L = \frac{0.42 - (VDDA \times 7.5 \times 10^{-3}) - (VDDB \times 10.8 \times 10^{-3})}{0.117 \times VDDB^2(f)} - \frac{2.692 \times 10^{-8}}{VDDB}$$

Equation 3.

Below is an example power dissipation calculation for the Si828x driver using Equation 1 with the following givens:

$V_{DDA} = 5.0$ V

$V_{DDB} = 18$ V

f = 30 kHz

$R_H = 10\ \Omega$

$R_L = 15\ \Omega$

$Q_G = 85$ nC

$$PD = (5)(0.0075) + 1.05(18)(0.0108) + 1.05(2 \times 10^4)(3 \times 10^{-9})(18) + \frac{1.05}{2}(3 \times 10^4)(85 \times 10^{-9})(18)\left[\frac{2.6}{2.6 + 10} + \frac{0.8}{0.8 + 15}\right] = 242mW$$

The driver junction temperature is calculated using Equation 2, where:

Pd is the total Si828x device power dissipation (W)

θja is the thermal resistance from junction to air (60 °C/W in this example)

TA is the maximum ambient temperature (125 °C)

$$Tj = Pd \times \theta ja + TA$$

$$Tj = (0.242) \times (60) + 125 = 139.5°C$$

Calculate maximum loading capacitance from equation 3:

1. VDDA = 5 V and (VDDB–VSSB) = 12.5 V.

$$C_L = \frac{1.51 \times 10^{-2}}{f} - 2.15 \times 10^{-9}$$

2. VDDA = 5 V and (VDDB–VSSB) = 18 V.

$$C_L = \frac{5.91 \times 10^{-3}}{f} - 1.5 \times 10^{-9}$$

3. VDDA = 5 V and (VDDB–VSSB) = 30 V.

$$C_L = \frac{1.04 \times 10^{-3}}{f} - 8.97 \times 10^{-10}$$

Graphs are shown in the following figure. All points along the load lines in these graphs represent the package dissipation-limited value of C_L for the corresponding switching frequency.

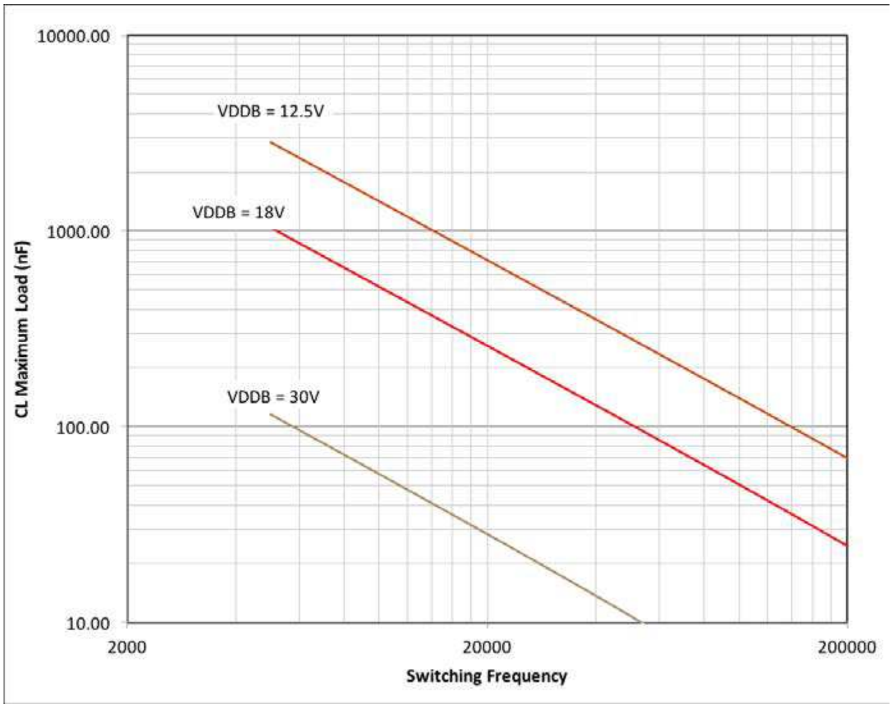

Figure 3.3. Maximum Load vs. Switching Frequency (25 °C)

4. Electrical Specifications

Table 4.1. Electrical Specifications

V_{IN} = 24 V; V_{DDA} = 4.3 V (See Figure 3) for all Si8282/84; V_{DDA} = V_{DDP} = 3.0 to 5.0 V (See Figure 2) for all Si8281/83; T_A = –40 to +125 °C unless otherwise noted.

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
DC Parameters						
Input Supply Voltage	VDDA		2.8	—	5.5	V
Power Input Voltage	VDDP		3.0	—	5.5	V
Driver Supply Voltage	(VDDB – VSSB)		9.5	—	30	V
	(VMID – VSSB)		0	—	15	V
Input Supply Quiescent Current	IDDA(Q)		—	6.8	7.5	mA
Input Supply Active Current	IDDA	f = 10 kHz	—	10.5	—	mA
Output Supply Quiescent Current	IDDB(Q)		—	8.7	10.8	mA
DC-DC Converter						
Switching Frequency Si8281, Si8282	FSW		—	250	—	kHz
Switching Frequency Si8283, Si8284	FSW	RFSW = 23.3 kΩ FSW = 1025.5/(RFSW x CSS) CSS = 220 nF (1% tolerance on BOM)	180	200	220	kHz
		RFSW = 9.3 kΩ FSW = 1025.5/(RFSW x CSS) CSS = 220 nF (1% tolerance on BOM)	450	500	550	kHz
		RFSW = 5.18 kΩ CSS = 220 nF	810	900	990	kHz
VSNS Voltage	VSNS	ILOAD = 0 A	1.002	1.05	1.097	V
VSNS Current Offset	I_{offset}		–500	—	500	nA
Output Voltage Accuracy		ILOAD = 0 mA	–5	—	+5	%
Line Regulation	ΔVOUT(line)/ ΔVDDP	ILOAD = 50 mA VDDP varies from 4.5 to 5.5 V	—	1	—	mV/V
Load Regulation	ΔVOUT(load)/ VOUT	ILOAD = 50 to 400 mA	—	0.1	—	%
Output Voltage Ripple Si8281, Si8283 Si8282, Si8284		ILOAD = 100 mA	—	100	—	mV p-p
Turn-on overshoot	ΔVOUT(start)	CIN = COUT = 0.1 µF in parallel with 10 µF ILOAD = 0 A	—	2	—	%

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Continuous Output Current **Si8281, Si8283** 5.0 V to 5.0 V 3.3 V to 3.3 V 3.3 V to 5.0 V **Si8282, Si8284** 24 V to 5.0 V 24 V to 3.0 V	ILOAD(max)			200 400 250 1000 1500		mA
Cycle-by-Cycle Average Current Limit Si8281, Si8283	ILIM	Output short circuited	—	3	—	A
No-Load Supply Current IDDP Si8281, Si8283	IDDPQ_DCDC	VDDP = VDDA = 5 V	—	30	—	mA
No-Load Supply Current IDDA Si8281, Si8283	IDDAQ_DCDC	VDDP = VDDA = 5 V	—	5.7	—	mA
No-Load Supply Current IDDP Si8282, Si8284	IDDPQ_DCDC	VIN = 24 V	—	0.8	—	mA
No-Load Supply Current IDDA Si8282, Si8284	IDDAQ_DCDC	VIN = 24 V	—	5.8	—	mA
Peak Efficiency Si8281, Si8283 Si8282, Si8284	η		—	78 83	—	%
Soft Start Time, Full Load Si8281, Si8282 Si8283, Si8284	t_{SST}		—	25 50	—	ms
Restart Delay from Fault Event	t_{OTP}		—	21	—	s
Drive Parameters						
High Drive Transistor RDS(ON)	R_{OH}		—	2.48	—	Ω
Low Drive Transistor RDS(ON)	R_{OL}		—	0.86	—	Ω
High Drive Peak Output Current	I_{OH}	VH = VDDB – 15 V $T_{PW\_IOH} \leq 250$ ns	2.5	2.8	—	A
Low Drive Peak Output Current	I_{OL}	VL = VSSB + 6.0 V $T_{PW\_IOL} \leq 250$ ns	3.0	3.4	—	A
UVLO Parameters						
UVLO Threshold +	$VDDA_{UV+}$		2.4	2.7	3.0	
UVLO Threshold –	$VDDA_{UV-}$		2.3	2.6	2.9	
UVLO Lockout Hysteresis– (Input Side)	$VDDA_{HYS}$		—	100	—	mV

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
UVLO Threshold + (Driver Side) 9 V Threshold (Si828xBD) 12 V Threshold (Si828xCD)	$VDDB_{UV+}$		8.0 10.8	9.0 12.0	10.0 13.2	V V
UVLO Threshold – (Driver Side) 9 V Threshold (Si828xBD) 12 V Threshold (Si828xCD)	$VDDB_{UV-}$		7.0 9.8	8.0 11.0	9.0 12.2	V V
UVLO lockout hysteresis (Driver Side)	$VDDB_{HYS}$		—	1	—	V
UVLO+ to RDY High Delay	$t_{UVLO+ \text{ to } RDY}$		—		100	µs
ULVO– to RDY Low Delay	$t_{UVLO- \text{ to } RDY}$		—		0.79	µs
Desaturation Detector Parameters						
DESAT Threshold	VDESAT	VDDB – VSSB > VDDBUV+	6.5	6.9	7.3	V
C_{BI} charging current	I_{Chg}		—	1	—	mA
DESAT Sense to 90% VOUT Delay	$t_{DESAT(90\%)}$		—	220	300	ns
DESAT Sense to 10% VOUT Delay	$t_{DESAT(10\%)}$		0.77	2.5	2.7	µs
DESAT Sense to FLT Low Delay	$t_{DESAT \text{ to } FLT}$		—	220	300	ns
Reset to FLT High Delay	$t_{RST \text{ to } FLT}$		—	37	45	ns
Miller Clamp Parameters (Si8285 Only)						
Clamp Pin Threshold Voltage	V_t Clamp		—	2.0	—	V
Miller Clamp Transistor RDS (ON)	R_{MC}		—	1.07	—	Ω
Clamp Low Level Sinking Current	I_{CL}	VCLMP = VSSB + 6.0	3.0	3.4	—	A
Digital Parameters						
Logic High Input Threshold	VIH		2.0	—	—	V
Logic Low Input Threshold	VIL		—	—	0.8	V
Input Hysteresis	VIHYST		—	440	—	mV
High Level Output Voltage (RDY pin only)	VOH	IO = –4 mA	VDDA – 0.4	—	—	V
Low Level Output Voltage (RDY pin only)	VOL	IO = 4 mA	—	—	0.4	V
Open-Drain Low Level Output Voltage (FLT pin only)		VDDA = 5 V, 5 kΩ pull-up resistor	—	—	200	mV
AC Switching Parameters						
Propagation Delay (Low-to-High)	t_{PLH}	CL = 200 pF	30	40	50	ns
Propagation Delay (High-to-Low)	t_{PHL}	CL = 200 pF	30	40	50	ns
Pulse Width Distortion	PWD	$\|t_{PLH} - t_{PHL}\|$	—	1	5	ns
Propagation Delay Difference[4]	PDD	$t_{PHLMAX} - t_{PLHMIN}$	–1	—	25	ns
Rise Time	t_R	CL = 200 pF	—	5.5	15	ns

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Fall Time	t_F	CL = 200 pF	—	8.5	20	ns
Common Mode Transient Immunity		Output = low or high (VCM = 1500 V)	35	50	—	kV/µs

1. See Ordering Guide for more information.
2. Minimum value of (VDD – GND) decoupling capacitor is 1 µF.
3. When performing this test, it is recommended that the DUT be soldered to avoid trace inductances, which may cause overstress conditions.
4. Guaranteed by characterization.

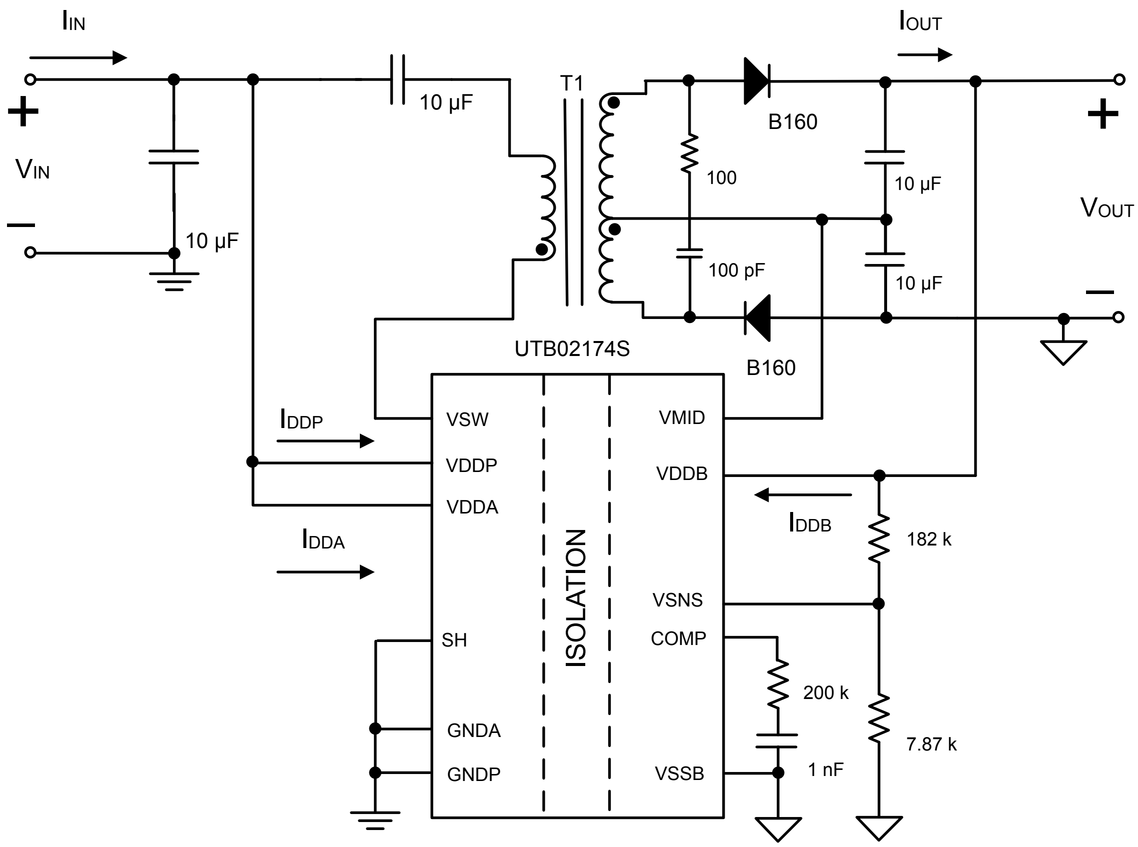

Figure 4.1. Si8281, Si8283 Measurement Circuit for Converter Efficiency and Regulation

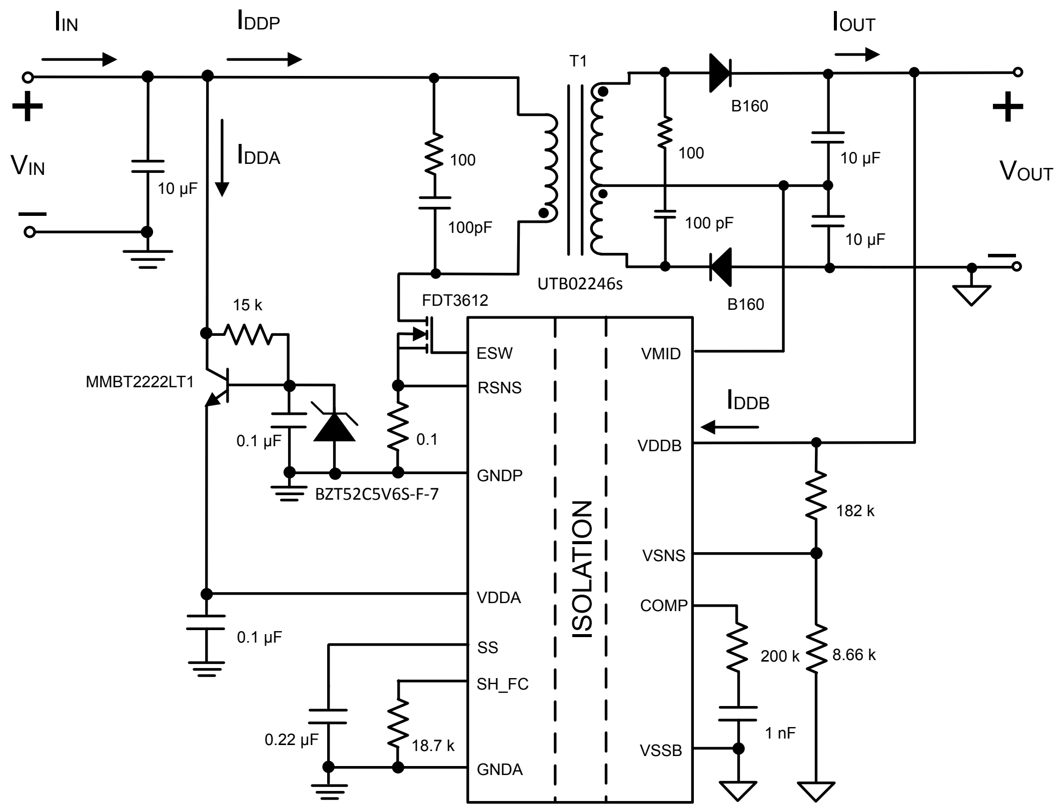

Figure 4.2. Si8282, Si8284 Measurement Circuit for Converter Efficiency and Regulation

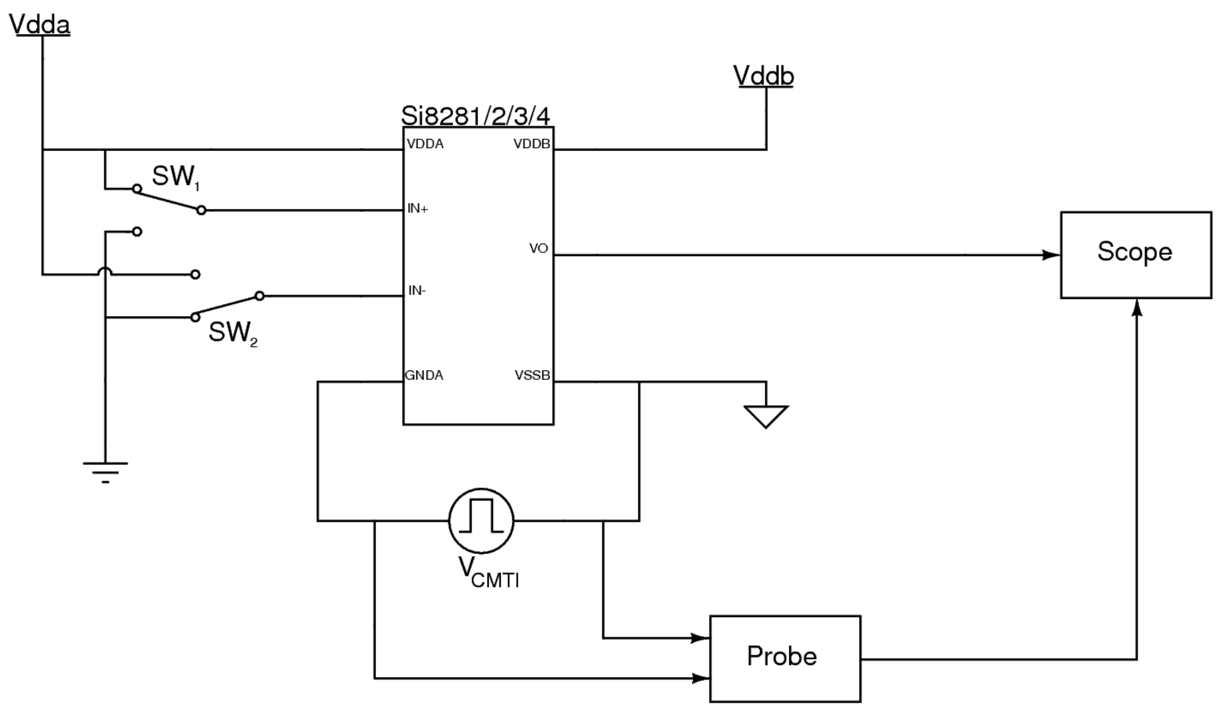

Figure 4.3. Common-Mode Transient Immunity Characterization Circuit

Table 4.2. Absolute Maximum Ratings[1]

Parameter	Symbol	Min	Max	Unit
Storage Temperature	T_{STG}	–65	+150	°C
Operating Temperature	T_A	–40	+125	°C
Junction Temperature	T_J	—	+140	°C
Peak Output Current (t_{PW} = 10 µs)	I_{OPK}	—	4.0	A
Supply Voltage	VDD	–0.5	36	V
Output Voltage	V_{OUT}	–0.5	36	V
Input Power Dissipation	P_I	—	100	mW
Output Power Dissipation	P_O	—	800	mW
Total Power Dissipation (All Packages Limited by Thermal Derating Curve)	P_T	—	900	mW
Lead Solder Temperature (10 s)		—	260	°C
HBM Rating ESD		4	—	kV
Machine Model ESD		300	—	V
CDM		2000	—	V
Maximum Isolation (Input to Output) (1 sec) WB SOIC-16		—	6500	V_{RMS}

Note:

1. Permanent device damage may occur if the absolute maximum ratings are exceeded. Functional operation should be restricted to the conditions as specified in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

4.1 Timing Diagrams

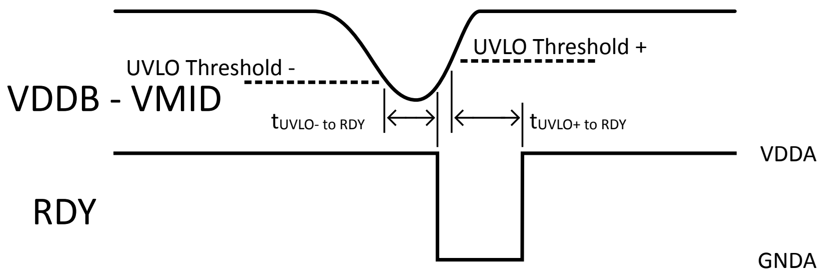

Figure 4.4. UVLO Condition to RDY Output

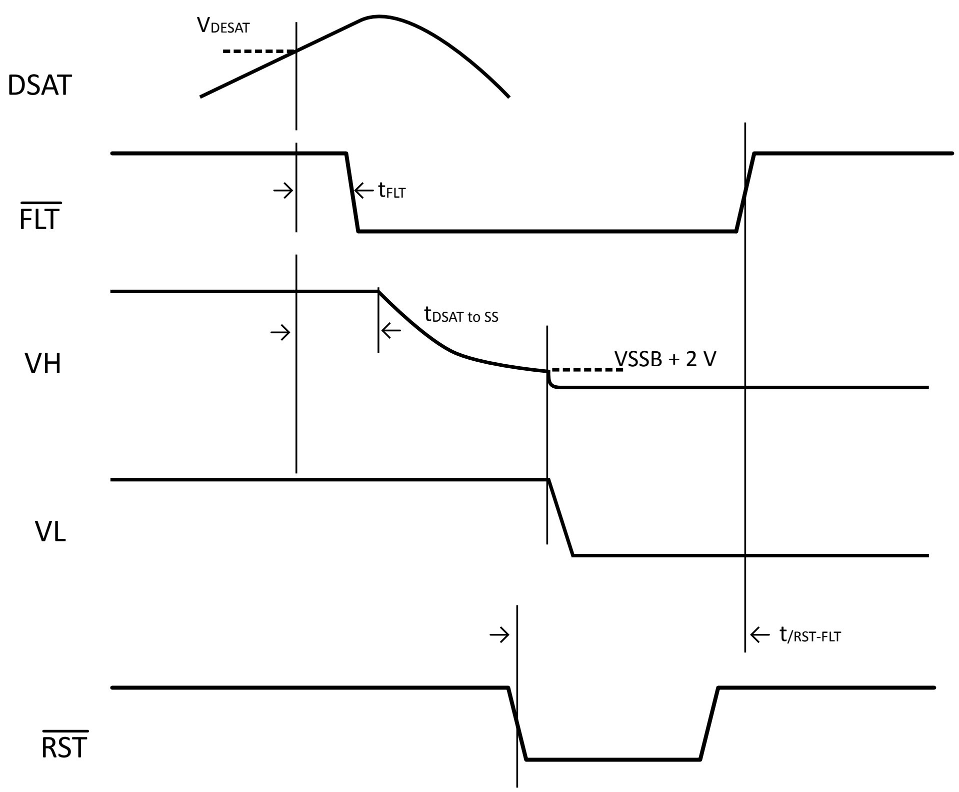

Figure 4.5. Device Reaction to Desaturation Event

4.2 Typical Operating Characteristics