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Low Power Six-Channel Digital Isolator

Features

- High-speed operation
  - DC to 150 Mbps
- No start-up initialization required
- Wide Operating Supply Voltage: 2.70–5.5 V
- Wide Operating Supply Voltage: 2.70–5.5V
- Ultra low power (typical)
  5 V Operation:
  - < 1.6 mA per channel at 1 Mbps
  - < 6 mA per channel at 100 Mbps

  2.70 V Operation:
  - < 1.4 mA per channel at 1 Mbps
  - < 4 mA per channel at 100 Mbps
- High electromagnetic immunity
- Up to 2500 V_{RMS} isolation
- 60-year life at rated working voltage
- Precise timing (typical)
  - <10 ns worst case
  - 1.5 ns pulse width distortion
  - 0.5 ns channel-channel skew
  - 2 ns propagation delay skew
  - 6 ns minimum pulse width
- Transient Immunity 25 kV/µs
- Wide temperature range
  - –40 to 125 °C at 150 Mbps
- RoHS-compliant packages
  - SOIC-16 narrow body

Ordering Information:
See page 29.

Applications

- Industrial automation systems
- Hybrid electric vehicles
- Isolated switch mode supplies
- Isolated ADC, DAC
- Motor control
- Power inverters
- Communications systems

Safety Regulatory Approvals

- UL 1577 recognized
  - Up to 2500 V_{RMS} for 1 minute
- CSA component notice 5A approval
  - IEC 60950-1, 61010-1 (reinforced insulation)
- VDE certification conformity
  - IEC 60747-5-2 (VDE0884 Part 2)

Description

Silicon Lab's family of ultra-low-power digital isolators are CMOS devices offering substantial data rate, propagation delay, power, size, reliability, and external BOM advantages when compared to legacy isolation technologies. The operating parameters of these products remain stable across wide temperature ranges throughout their service life. For ease of design, only VDD bypass capacitors are required.

Data rates up to 150 Mbps are supported, and all devices achieve worst-case propagation delays of less than 10 ns. All products are safety certified by UL, CSA, and VDE and support withstand voltages of up to 2.5 kVrms. These devices are available in a 16-pin narrow-body SOIC package.

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Section **Page**

1. Electrical Specifications

Table 1. Recommended Operating Conditions

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Ambient Operating Temperature*	T_A	150 Mbps, 15 pF, 5 V	–40	25	125	°C
Supply Voltage	V_{DD1}		2.70	—	5.5	V
	V_{DD2}		2.70	—	5.5	V

***Note:** The maximum ambient temperature is dependent on data frequency, output loading, number of operating channels, and supply voltage.

Table 2. Absolute Maximum Ratings[1]

Parameter	Symbol	Min	Typ	Max	Unit
Storage Temperature[2]	T_{STG}	–65	—	150	°C
Ambient Temperature Under Bias	T_A	–40	—	125	°C
Supply Voltage (Revision A)[3]	V_{DD1}, V_{DD2}	–0.5	—	5.75	V
Supply Voltage (Revision B)[3]	V_{DD1}, V_{DD2}	–0.5	—	6.0	V
Input Voltage	V_I	–0.5	—	V_{DD} + 0.5	V
Output Voltage	V_O	–0.5	—	V_{DD} + 0.5	V
Output Current Drive Channel	I_O	—	—	10	mA
Lead Solder Temperature (10 s)		—	—	260	°C
Maximum Isolation Voltage (1 s)		—	—	3600	V_{RMS}

Notes:
1. Permanent device damage may occur if the absolute maximum ratings are exceeded. Functional operation should be restricted to conditions as specified in the operational sections of this data sheet.
2. VDE certifies storage temperature from –40 to 150 °C.
3. See "5. Ordering Guide" on page 29 for more information.

Table 3. Electrical Characteristics

(V_{DD1} = 5 V±10%, V_{DD2} = 5 V±10%, T_A = –40 to 125 °C; applies to narrow-body SOIC package)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
High Level Input Voltage	V_{IH}		2.0	—	—	V
Low Level Input Voltage	V_{IL}		—	—	0.8	V
High Level Output Voltage	V_{OH}	Ioh = –4 mA	V_{DD1},V_{DD2} – 0.4	4.8	—	V
Low Level Output Voltage	V_{OL}	Iol = 4 mA	—	0.2	0.4	V
Input Leakage Current	I_L		—	—	±10	µA
Output Impedance[1]	Z_O		—	85	—	Ω
DC Supply Current (All inputs 0 V or at Supply)						
Si8460Ax, Bx V_{DD1} V_{DD2} V_{DD1} V_{DD2}		 All inputs 0 DC All inputs 0 DC All inputs 1 DC All inputs 1 DC	 — — — —	 1.7 3.3 7.7 3.5	 2.6 5.0 11.6 5.3	mA
Si8461Ax, Bx V_{DD1} V_{DD2} V_{DD1} V_{DD2}		 All inputs 0 DC All inputs 0 DC All inputs 1 DC All inputs 1 DC	 — — — —	 2.1 3.4 7.1 4.5	 3.2 5.1 10.7 6.8	mA
Si8462Ax, Bx V_{DD1} V_{DD2} V_{DD1} V_{DD2}		 All inputs 0 DC All inputs 0 DC All inputs 1 DC All inputs 1 DC	 — — — —	 2.5 3.0 6.5 5.0	 3.8 4.5 9.8 8.3	mA
Si8463Ax, Bx V_{DD1} V_{DD2} V_{DD1} V_{DD2}		 All inputs 0 DC All inputs 0 DC All inputs 1 DC All inputs 1 DC	 — — — —	 2.8 2.8 6.0 6.0	 4.2 4.2 9.0 9.0	mA

Notes:

1. The nominal output impedance of an isolator driver channel is approximately 85 Ω, ±40%, which is a combination of the value of the on-chip series termination resistor and channel resistance of the output driver FET. When driving loads where transmission line effects will be a factor, output pins should be appropriately terminated with controlled impedance PCB traces.
2. $t_{PSK(P-P)}$ is the magnitude of the difference in propagation delay times measured between different units operating at the same supply voltages, load, and ambient temperature.
3. Start-up time is the time period from the application of power to valid data at the output.

Table 3. Electrical Characteristics (Continued)
(V_{DD1} = 5 V±10%, V_{DD2} = 5 V±10%, T_A = –40 to 125 °C; applies to narrow-body SOIC package)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
1 Mbps Supply Current (All inputs = 500 kHz square wave, Cl = 15 pF on all outputs)						
Si8460Ax, Bx V_{DD1} V_{DD2}			— —	4.7 4.0	7.1 6.0	mA
Si8461Ax, Bx V_{DD1} V_{DD2}			— —	4.7 4.5	7.1 6.8	mA
Si8462Ax, Bx V_{DD1} V_{DD2}			— —	4.7 4.3	7.1 6.5	mA
Si8463Ax, Bx V_{DD1} V_{DD2}			— —	4.7 4.7	7.1 7.1	mA
10 Mbps Supply Current (All inputs = 5 MHz square wave, Cl = 15 pF on all outputs)						
Si8460Bx V_{DD1} V_{DD2}			— —	4.7 5.5	7.1 7.7	mA
Si8461Bx V_{DD1} V_{DD2}			— —	5.0 5.7	7.2 8	mA
Si8462Bx V_{DD1} V_{DD2}			— —	5.2 5.4	7.3 7.6	mA
Si8463Bx V_{DD1} V_{DD2}			— —	5.5 5.5	7.7 7.7	mA

Notes:
1. The nominal output impedance of an isolator driver channel is approximately 85 Ω, ±40%, which is a combination of the value of the on-chip series termination resistor and channel resistance of the output driver FET. When driving loads where transmission line effects will be a factor, output pins should be appropriately terminated with controlled impedance PCB traces.
2. $t_{PSK(P-P)}$ is the magnitude of the difference in propagation delay times measured between different units operating at the same supply voltages, load, and ambient temperature.
3. Start-up time is the time period from the application of power to valid data at the output.

Table 3. Electrical Characteristics (Continued)
(V_{DD1} = 5 V±10%, V_{DD2} = 5 V±10%, T_A = –40 to 125 °C; applies to narrow-body SOIC package)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
100 Mbps Supply Current (All inputs = 50 MHz square wave, CI = 15 pF on all outputs)						
Si8460Bx						
V_{DD1}			—	5.0	7.5	mA
V_{DD2}			—	28.8	36	
Si8461Bx						
V_{DD1}			—	9.0	11.3	mA
V_{DD2}			—	25	30	
Si8462Bx						
V_{DD1}			—	13.3	16.6	mA
V_{DD2}			—	20.8	26	
Si8463Bx						
V_{DD1}			—	17.2	21.5	mA
V_{DD2}			—	17.2	21.5	
Timing Characteristics						
Si846xAx						
Maximum Data Rate			0	—	1.0	Mbps
Minimum Pulse Width			—	—	250	ns
Propagation Delay	t_{PHL}, t_{PLH}	See Figure 1	—	—	35	ns
Pulse Width Distortion $\|t_{PLH} - t_{PHL}\|$	PWD	See Figure 1	—	—	25	ns
Propagation Delay Skew[2]	$t_{PSK(P-P)}$		—	—	40	ns
Channel-Channel Skew	t_{PSK}		—	—	35	ns
Si846xBx						
Maximum Data Rate			0	—	150	Mbps
Minimum Pulse Width			—	—	6.0	ns
Propagation Delay	t_{PHL}, t_{PLH}	See Figure 1	3.0	6.0	9.5	ns
Pulse Width Distortion $\|t_{PLH} - t_{PHL}\|$	PWD	See Figure 1	—	1.5	2.5	ns
Propagation Delay Skew[2]	$t_{PSK(P-P)}$		—	2.0	3.0	ns
Channel-Channel Skew	t_{PSK}		—	0.5	1.8	ns

Notes:
1. The nominal output impedance of an isolator driver channel is approximately 85 Ω, ±40%, which is a combination of the value of the on-chip series termination resistor and channel resistance of the output driver FET. When driving loads where transmission line effects will be a factor, output pins should be appropriately terminated with controlled impedance PCB traces.
2. $t_{PSK(P-P)}$ is the magnitude of the difference in propagation delay times measured between different units operating at the same supply voltages, load, and ambient temperature.
3. Start-up time is the time period from the application of power to valid data at the output.

Table 3. Electrical Characteristics (Continued)

(V_{DD1} = 5 V±10%, V_{DD2} = 5 V±10%, T_A = –40 to 125 °C; applies to narrow-body SOIC package)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
All Models						
Output Rise Time	t_r	C_L = 15 pF See Figure 1	—	3.8	5.0	ns
Output Fall Time	t_f	C_L = 15 pF See Figure 1	—	2.8	3.7	ns
Common Mode Transient Immunity	CMTI	$V_I = V_{DD}$ or 0 V	—	25	—	kV/µs
Start-up Time[3]	t_{SU}		—	15	40	µs

Notes:

1. The nominal output impedance of an isolator driver channel is approximately 85 Ω, ±40%, which is a combination of the value of the on-chip series termination resistor and channel resistance of the output driver FET. When driving loads where transmission line effects will be a factor, output pins should be appropriately terminated with controlled impedance PCB traces.
2. $t_{PSK(P-P)}$ is the magnitude of the difference in propagation delay times measured between different units operating at the same supply voltages, load, and ambient temperature.
3. Start-up time is the time period from the application of power to valid data at the output.

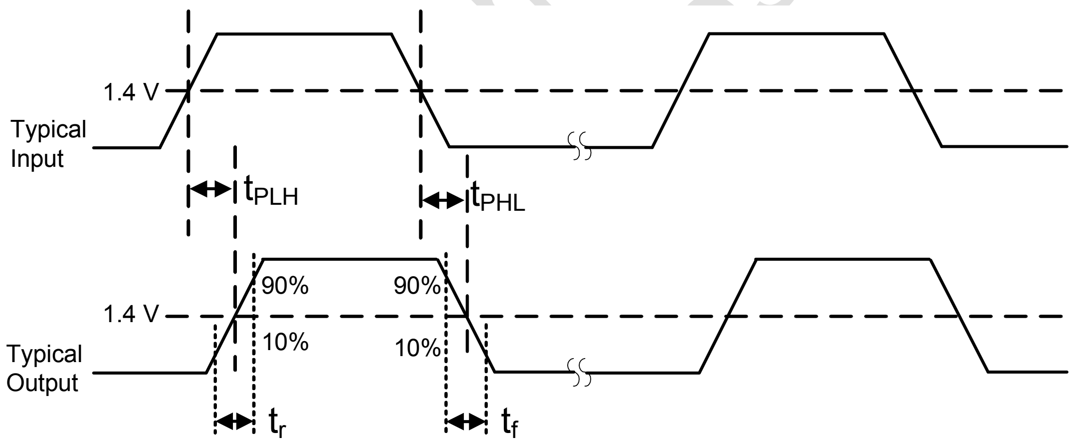

Figure 1. Propagation Delay Timing

Table 4. Electrical Characteristics
(V_{DD1} = 3.3 V±10%, V_{DD2} = 3.3 V±10%, T_A = –40 to 125 °C; applies to narrow-body SOIC package)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
High Level Input Voltage	V_{IH}		2.0	—	—	V
Low Level Input Voltage	V_{IL}		—	—	0.8	V
High Level Output Voltage	V_{OH}	Ioh = –4 mA	V_{DD1},V_{DD2} – 0.4	3.1	—	V
Low Level Output Voltage	V_{OL}	Iol = 4 mA	—	0.2	0.4	V
Input Leakage Current	I_L		—	—	±10	µA
Output Impedance[1]	Z_O		—	85	—	Ω
DC Supply Current (All inputs 0 V or at supply)						
Si8460Ax, Bx V_{DD1} V_{DD2} V_{DD1} V_{DD2}		 All inputs 0 DC All inputs 0 DC All inputs 1 DC All inputs 1 DC	 — — — —	 1.7 3.3 7.7 3.5	 2.6 5.0 11.6 5.3	mA
Si8461Ax, Bx V_{DD1} V_{DD2} V_{DD1} V_{DD2}		 All inputs 0 DC All inputs 0 DC All inputs 1 DC All inputs 1 DC	 — — — —	 2.1 3.4 7.1 4.5	 3.2 5.1 10.7 6.8	mA
Si8462Ax, Bx V_{DD1} V_{DD2} V_{DD1} V_{DD2}		 All inputs 0 DC All inputs 0 DC All inputs 1 DC All inputs 1 DC	 — — — —	 2.5 3.0 6.5 5.0	 3.8 4.5 9.8 8.3	mA
Si8463Ax, Bx V_{DD1} V_{DD2} V_{DD1} V_{DD2}		 All inputs 0 DC All inputs 0 DC All inputs 1 DC All inputs 1 DC	 — — — —	 2.8 2.8 6.0 6.0	 4.2 4.2 9.0 9.0	mA

Notes:
1. The nominal output impedance of an isolator driver channel is approximately 85 Ω, ±40%, which is a combination of the value of the on-chip series termination resistor and channel resistance of the output driver FET. When driving loads where transmission line effects will be a factor, output pins should be appropriately terminated with controlled impedance PCB traces.
2. $t_{PSK(P-P)}$ is the magnitude of the difference in propagation delay times measured between different units operating at the same supply voltages, load, and ambient temperature.
3. Start-up time is the time period from the application of power to valid data at the output.

Table 4. Electrical Characteristics (Continued)
(V_{DD1} = 3.3 V±10%, V_{DD2} = 3.3 V±10%, T_A = –40 to 125 °C; applies to narrow-body SOIC package)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
1 Mbps Supply Current (All inputs = 500 kHz square wave, Cl = 15 pF on all outputs)						
Si8460Ax, Bx V_{DD1} V_{DD2}			— —	4.7 4.0	7.1 6.0	mA
Si8461Ax, Bx V_{DD1} V_{DD2}			— —	4.7 4.5	7.1 6.8	mA
Si8462Ax, Bx V_{DD1} V_{DD2}			— —	4.7 4.3	7.1 6.5	mA
Si8463Ax, Bx V_{DD1} V_{DD2}			— —	4.7 4.7	7.1 7.1	mA
10 Mbps Supply Current (All inputs = 5 MHz square wave, Cl = 15 pF on all outputs)						
Si8460Bx V_{DD1} V_{DD2}			— —	4.7 5.5	7.1 7.7	mA
Si8461Bx V_{DD1} V_{DD2}			— —	5.0 5.7	7.2 8.0	mA
Si8462Bx V_{DD1} V_{DD2}			— —	5.2 5.4	7.3 7.6	mA
Si8463Bx V_{DD1} V_{DD2}			— —	5.5 5.5	7.7 7.7	mA

Notes:
1. The nominal output impedance of an isolator driver channel is approximately 85 Ω, ±40%, which is a combination of the value of the on-chip series termination resistor and channel resistance of the output driver FET. When driving loads where transmission line effects will be a factor, output pins should be appropriately terminated with controlled impedance PCB traces.
2. $t_{PSK(P-P)}$ is the magnitude of the difference in propagation delay times measured between different units operating at the same supply voltages, load, and ambient temperature.
3. Start-up time is the time period from the application of power to valid data at the output.

Table 4. Electrical Characteristics (Continued)
(V_{DD1} = 3.3 V±10%, V_{DD2} = 3.3 V±10%, T_A = –40 to 125 °C; applies to narrow-body SOIC package)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
100 Mbps Supply Current (All inputs = 50 MHz square wave, Cl = 15 pF on all outputs)						
Si8460Bx V_{DD1} V_{DD2}			— —	4.8 20	7.2 25	mA
Si8461Bx V_{DD1} V_{DD2}			— —	7.4 17.7	9.3 22.1	mA
Si8462Bx V_{DD1} V_{DD2}			— —	10.2 15	12.8 18.8	mA
Si8463Bx V_{DD1} V_{DD2}			— —	12.7 12.7	15.9 15.9	mA
Timing Characteristics						
Si846xAx						
Maximum Data Rate			0	—	1.0	Mbps
Minimum Pulse Width			—	—	250	ns
Propagation Delay	t_{PHL},t_{PLH}	See Figure 1	—	—	35	ns
Pulse Width Distortion $\|t_{PLH} - t_{PHL}\|$	PWD	See Figure 1	—	—	25	ns
Propagation Delay Skew[2]	$t_{PSK(P-P)}$		—	—	40	ns
Channel-Channel Skew	t_{PSK}		—	—	35	ns
Si846xBx						
Maximum Data Rate			0	—	150	Mbps
Minimum Pulse Width			—	—	6.0	ns
Propagation Delay	t_{PHL}, t_{PLH}	See Figure 1	3.0	6.0	9.5	ns
Pulse Width Distortion $\|t_{PLH} - t_{PHL}\|$	PWD	See Figure 1	—	1.5	2.5	ns
Propagation Delay Skew[2]	$t_{PSK(P-P)}$		—	2.0	3.0	ns
Channel-Channel Skew	t_{PSK}		—	0.5	1.8	ns

Notes:
1. The nominal output impedance of an isolator driver channel is approximately 85 Ω, ±40%, which is a combination of the value of the on-chip series termination resistor and channel resistance of the output driver FET. When driving loads where transmission line effects will be a factor, output pins should be appropriately terminated with controlled impedance PCB traces.
2. $t_{PSK(P-P)}$ is the magnitude of the difference in propagation delay times measured between different units operating at the same supply voltages, load, and ambient temperature.
3. Start-up time is the time period from the application of power to valid data at the output.

Table 4. Electrical Characteristics (Continued)
(V_{DD1} = 3.3 V±10%, V_{DD2} = 3.3 V±10%, T_A = –40 to 125 °C; applies to narrow-body SOIC package)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
All Models						
Output Rise Time	t_r	C_L = 15 pF See Figure 1	—	4.3	6.1	ns
Output Fall Time	t_f	C_L = 15 pF See Figure 1	—	3.0	4.3	ns
Common Mode Transient Immunity	CMTI	$V_I = V_{DD}$ or 0 V	—	25	—	kV/µs
Start-up Time[3]	t_{SU}		—	15	40	µs

Notes:

1. The nominal output impedance of an isolator driver channel is approximately 85 Ω, ±40%, which is a combination of the value of the on-chip series termination resistor and channel resistance of the output driver FET. When driving loads where transmission line effects will be a factor, output pins should be appropriately terminated with controlled impedance PCB traces.
2. $t_{PSK(P-P)}$ is the magnitude of the difference in propagation delay times measured between different units operating at the same supply voltages, load, and ambient temperature.
3. Start-up time is the time period from the application of power to valid data at the output.

Table 5. Electrical Characteristics[1]

(V_{DD1} = 2.70 V, V_{DD2} = 2.70 V, T_A = –40 to 125 °C; applies to narrow-body SOIC package)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
High Level Input Voltage	V_{IH}		2.0	—	—	V
Low Level Input Voltage	V_{IL}		—	—	0.8	V
High Level Output Voltage	V_{OH}	Ioh = –4 mA	V_{DD1},V_{DD2} – 0.4	2.3	—	V
Low Level Output Voltage	V_{OL}	Iol = 4 mA	—	0.2	0.4	V
Input Leakage Current	I_L		—	—	±10	µA
Output Impedance[2]	Z_O		—	85	—	Ω
DC Supply Current (All inputs 0 V or at supply)						
Si8460Ax, Bx						
V_{DD1}		All inputs 0 DC	—	1.7	2.6	mA
V_{DD2}		All inputs 0 DC	—	3.3	5.0	mA
V_{DD1}		All inputs 1 DC	—	7.7	11.6	mA
V_{DD2}		All inputs 1 DC	—	3.5	5.3	mA
Si8461Ax, Bx						
V_{DD1}		All inputs 0 DC	—	2.1	3.2	mA
V_{DD2}		All inputs 0 DC	—	3.4	5.1	mA
V_{DD1}		All inputs 1 DC	—	7.1	10.7	mA
V_{DD2}		All inputs 1 DC	—	4.5	6.8	mA
Si8462Ax, Bx						
V_{DD1}		All inputs 0 DC	—	2.5	3.8	mA
V_{DD2}		All inputs 0 DC	—	3.0	4.5	mA
V_{DD1}		All inputs 1 DC	—	6.5	9.8	mA
V_{DD2}		All inputs 1 DC	—	5.0	8.3	mA
Si8463Ax, Bx						
V_{DD1}		All inputs 0 DC	—	2.8	4.2	mA
V_{DD2}		All inputs 0 DC	—	2.8	4.2	mA
V_{DD1}		All inputs 1 DC	—	6.0	9.0	mA
V_{DD2}		All inputs 1 DC	—	6.0	9.0	mA

Notes:

1. Specifications in this table are also valid at VDD1 = 2.6 V and VDD2 = 2.6 V when the operating temperature range is constrained to T_A = 0 to 85 °C.
2. The nominal output impedance of an isolator driver channel is approximately 85 Ω, ±40%, which is a combination of the value of the on-chip series termination resistor and channel resistance of the output driver FET. When driving loads where transmission line effects will be a factor, output pins should be appropriately terminated with controlled impedance PCB traces.
3. $t_{PSK(P-P)}$ is the magnitude of the difference in propagation delay times measured between different units operating at the same supply voltages, load, and ambient temperature.
4. Start-up time is the time period from the application of power to valid data at the output.

Table 5. Electrical Characteristics[1] (Continued)

(V_{DD1} = 2.70 V, V_{DD2} = 2.70 V, T_A = –40 to 125 °C; applies to narrow-body SOIC package)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
1 Mbps Supply Current (All inputs = 500 kHz square wave, Cl = 15 pF on all outputs)						
Si8460Ax, Bx V_{DD1} V_{DD2}			— —	4.7 4.0	7.1 6.0	mA
Si8461Ax, Bx V_{DD1} V_{DD2}			— —	4.7 4.5	7.1 6.8	mA
Si8462Ax, Bx V_{DD1} V_{DD2}			— —	4.7 4.3	7.1 6.5	mA
Si8463Ax, Bx V_{DD1} V_{DD2}			— —	4.7 4.7	7.1 7.1	mA
10 Mbps Supply Current (All inputs = 5 MHz square wave, Cl = 15 pF on all outputs)						
Si8460Bx V_{DD1} V_{DD2}			— —	4.7 5.5	7.1 7.7	mA
Si8461Bx V_{DD1} V_{DD2}			— —	5.0 5.7	7.2 8.0	mA
Si8462Bx V_{DD1} V_{DD2}			— —	5.2 5.4	7.3 7.6	mA
Si8463Bx V_{DD1} V_{DD2}			— —	5.5 5.5	7.7 7.7	mA

Notes:

1. Specifications in this table are also valid at VDD1 = 2.6 V and VDD2 = 2.6 V when the operating temperature range is constrained to T_A = 0 to 85 °C.
2. The nominal output impedance of an isolator driver channel is approximately 85 Ω, ±40%, which is a combination of the value of the on-chip series termination resistor and channel resistance of the output driver FET. When driving loads where transmission line effects will be a factor, output pins should be appropriately terminated with controlled impedance PCB traces.
3. $t_{PSK(P-P)}$ is the magnitude of the difference in propagation delay times measured between different units operating at the same supply voltages, load, and ambient temperature.
4. Start-up time is the time period from the application of power to valid data at the output.

Table 5. Electrical Characteristics[1] (Continued)
(V_{DD1} = 2.70 V, V_{DD2} = 2.70 V, T_A = –40 to 125 °C; applies to narrow-body SOIC package)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
100 Mbps Supply Current (All inputs = 50 MHz square wave, Cl = 15 pF on all outputs)						
Si8460Bx V_{DD1} V_{DD2}			 — —	 4.8 15.8	 7.2 19.8	mA
Si8461Bx V_{DD1} V_{DD2}			 — —	 6.7 14.2	 8.4 17.8	mA
Si8462Bx V_{DD1} V_{DD2}			 — —	 8.7 12.2	 10.9 15.3	mA
Si8463Bx V_{DD1} V_{DD2}			 — —	 10.5 10.5	 13.1 13.1	mA
Timing Characteristics						
Si846xAx						
Maximum Data Rate			0	—	1.0	Mbps
Minimum Pulse Width			—	—	250	ns
Propagation Delay	t_{PHL},t_{PLH}	See Figure 1	—	—	35	ns
Pulse Width Distortion $\|t_{PLH} - t_{PHL}\|$	PWD	See Figure 1	—	—	25	ns
Propagation Delay Skew[3]	$t_{PSK(P-P)}$		—	—	40	ns
Channel-Channel Skew	t_{PSK}		—	—	35	ns
Si846xBx						
Maximum Data Rate			0	—	150	Mbps
Minimum Pulse Width			—	—	6.0	ns
Propagation Delay	t_{PHL}, t_{PLH}	See Figure 1	3.0	6.0	9.5	ns
Pulse Width Distortion $\|t_{PLH} - t_{PHL}\|$	PWD	See Figure 1	—	1.5	2.5	ns
Propagation Delay Skew[3]	$t_{PSK(P-P)}$		—	2.0	3.0	ns
Channel-Channel Skew	t_{PSK}		—	0.5	1.8	ns

Notes:
1. Specifications in this table are also valid at VDD1 = 2.6 V and VDD2 = 2.6 V when the operating temperature range is constrained to T_A = 0 to 85 °C.
2. The nominal output impedance of an isolator driver channel is approximately 85 Ω, ±40%, which is a combination of the value of the on-chip series termination resistor and channel resistance of the output driver FET. When driving loads where transmission line effects will be a factor, output pins should be appropriately terminated with controlled impedance PCB traces.
3. $t_{PSK(P-P)}$ is the magnitude of the difference in propagation delay times measured between different units operating at the same supply voltages, load, and ambient temperature.
4. Start-up time is the time period from the application of power to valid data at the output.

Table 5. Electrical Characteristics[1] (Continued)

(V_{DD1} = 2.70 V, V_{DD2} = 2.70 V, T_A = –40 to 125 °C; applies to narrow-body SOIC package)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
All Models						
Output Rise Time	t_r	C_L = 15 pF See Figure 1	—	4.8	6.5	ns
Output Fall Time	t_f	C_L = 15 pF See Figure 1	—	3.2	4.6	ns
Common Mode Transient Immunity	CMTI	$V_I = V_{DD}$ or 0 V	—	25	—	kV/µs
Start-up Time[4]	t_{SU}		—	15	40	µs

Notes:
1. Specifications in this table are also valid at VDD1 = 2.6 V and VDD2 = 2.6 V when the operating temperature range is constrained to T_A = 0 to 85 °C.
2. The nominal output impedance of an isolator driver channel is approximately 85 Ω, ±40%, which is a combination of the value of the on-chip series termination resistor and channel resistance of the output driver FET. When driving loads where transmission line effects will be a factor, output pins should be appropriately terminated with controlled impedance PCB traces.
3. $t_{PSK(P-P)}$ is the magnitude of the difference in propagation delay times measured between different units operating at the same supply voltages, load, and ambient temperature.
4. Start-up time is the time period from the application of power to valid data at the output.

Table 6. Regulatory Information*

CSA
The Si84xx is certified under CSA Component Acceptance Notice 5A. For more details, see File 232873.
61010-1: Up to 300 V_{RMS} reinforced insulation working voltage; up to 600 V_{RMS} basic insulation working voltage.
60950-1: Up to 130 V_{RMS} reinforced insulation working voltage; up to 600 V_{RMS} basic insulation working voltage.
VDE
The Si84xx is certified according to IEC 60747-5-2. For more details, see File 5006301-4880-0001.
60747-5-2: Up to 560 V_{peak} for basic insulation working voltage.
UL
The Si84xx is certified under UL1577 component recognition program. For more details, see File E257455.
Rated up to 2500 V_{RMS} isolation voltage for basic insulation.
***Note:** Regulatory Certifications apply to 2.5 kV_{RMS} rated devices which are production tested to 3.0 kV_{RMS} for 1 sec. For more information, see "5. Ordering Guide" on page 29.

Table 7. Insulation and Safety-Related Specifications

Parameter	Symbol	Test Condition	Value	Unit
			NB SOIC-16	
Nominal Air Gap (Clearance)[1]	L(IO1)		3.9 min	mm
Nominal External Tracking (Creepage)[1]	L(IO2)		3.9 min	mm
Minimum Internal Gap (Internal Clearance)			0.008	mm
Tracking Resistance (Proof Tracking Index)	PTI	IEC60112	600	V_{RMS}
Erosion Depth	ED		0.019	mm
Resistance (Input-Output)[2]	R_{IO}		10^{12}	Ω
Capacitance (Input-Output)[2]	C_{IO}	f = 1 MHz	2.0	pF
Input Capacitance[3]	C_I		4.0	pF

Notes:
1. The values in this table correspond to the nominal creepage and clearance values as detailed in "6. Package Outline: 16-Pin Narrow Body SOIC". VDE certifies the clearance and creepage limits as 4.7 mm minimum for the NB SOIC-16 package. UL does not impose a clearance and creepage minimum for component level certifications. CSA certifies the clearance and creepage limits as 3.9 mm minimum for the NB SOIC-16 package.
2. To determine resistance and capacitance, the Si84xx is converted into a 2-terminal device. Pins 1–8 are shorted together to form the first terminal and pins 9–16 are shorted together to form the second terminal. The parameters are then measured between these two terminals.
3. Measured from input pin to ground.

Table 8. IEC 60664-1 (VDE 0844 Part 2) Ratings

Parameter	Test Condition	Specification
Basic Isolation Group	Material Group	I
Installation Classification	Rated Mains Voltages ≤ 150 V_{RMS}	I-IV
	Rated Mains Voltages ≤ 300 V_{RMS}	I-III
	Rated Mains Voltages ≤ 400 V_{RMS}	I-II
	Rated Mains Voltages ≤ 600 V_{RMS}	I-II

Table 9. IEC 60747-5-2 Insulation Characteristics for Si84xxxB*

Parameter	Symbol	Test Condition	Characteristic	Unit
Maximum Working Insulation Voltage	V_{IORM}		560	V peak
Input to Output Test Voltage	V_{PR}	Method b1 (V_{IORM} x 1.875 = V_{PR}, 100% Production Test, t_m = 1 sec, Partial Discharge < 5 pC)	1050	V peak
Transient Overvoltage	V_{IOTM}	t = 60 sec	4000	V peak
Pollution Degree (DIN VDE 0110, Table 1)			2	
Insulation Resistance at T_S, V_{IO} = 500 V	R_S		$>10^9$	Ω

***Note:** Maintenance of the safety data is ensured by protective circuits. The Si84xx provides a climate classification of 40/125/21.

Table 10. IEC Safety Limiting Values[1]

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
					NB SOIC-16	
Case Temperature	T_S		—	—	150	°C
Safety input, output, or supply current	I_S	θ_{JA} = 105 °C/W (NB SOIC-16), V_I = 5.5 V, T_J = 150 °C, T_A = 25 °C	—	—	215	mA
Device Power Dissipation[2]	P_D		—	—	415	mW

Notes:
1. Maximum value allowed in the event of a failure; also see the thermal derating curve in Figure 2.
2. The Si846x is tested with VDD1 = VDD2 = 5.5 V, TJ = 150 ºC, CL = 15 pF, input a 150 Mbps 50% duty cycle square wave.

Table 11. Thermal Characteristics

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
				NB SOIC-16		
IC Junction-to-Air Thermal Resistance	θ_{JA}		—	105	—	°C/W

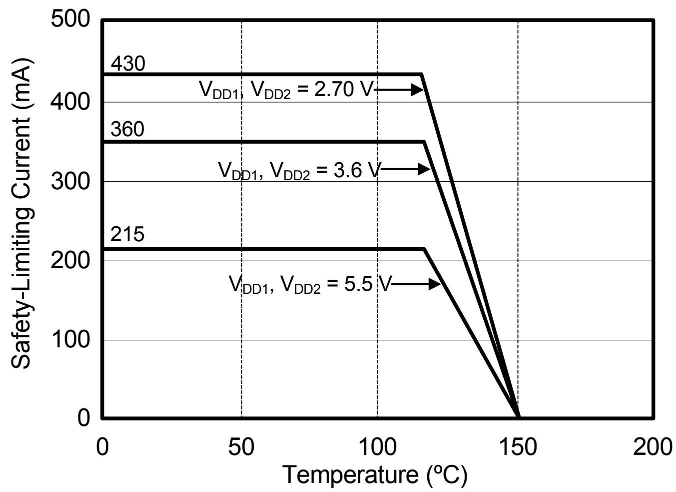

Figure 2. (NB SOIC-16) Thermal Derating Curve, Dependence of Safety Limiting Values with Case Temperature per DIN EN 60747-5-2

2. Functional Description

2.1. Theory of Operation

The operation of an Si846x channel is analogous to that of an opto coupler, except an RF carrier is modulated instead of light. This simple architecture provides a robust isolated data path and requires no special considerations or initialization at start-up. A simplified block diagram for a single Si846x channel is shown in Figure 3.

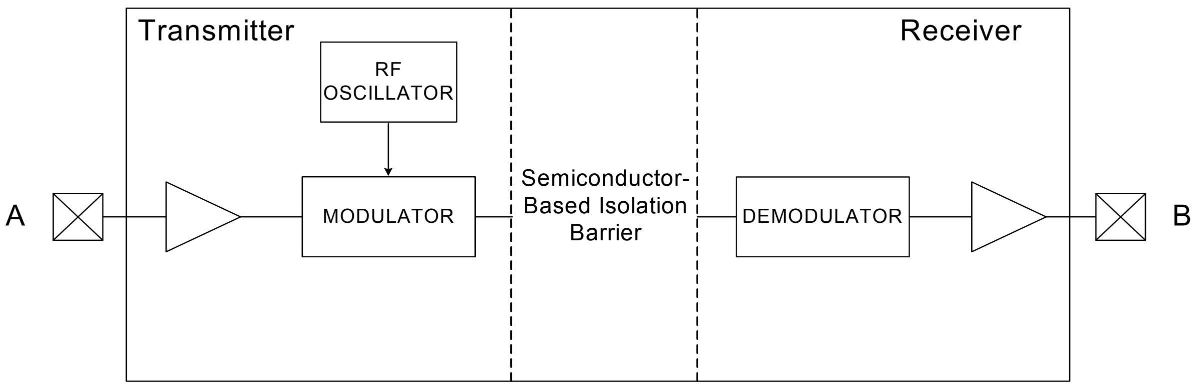

Figure 3. Simplified Channel Diagram

A channel consists of an RF Transmitter and RF Receiver separated by a semiconductor-based isolation barrier. Referring to the Transmitter, input A modulates the carrier provided by an RF oscillator using on/off keying. The Receiver contains a demodulator that decodes the input state according to its RF energy content and applies the result to output B via the output driver. This RF on/off keying scheme is superior to pulse code schemes as it provides best-in-class noise immunity, low power consumption, and better immunity to magnetic fields. See Figure 4 for more details.

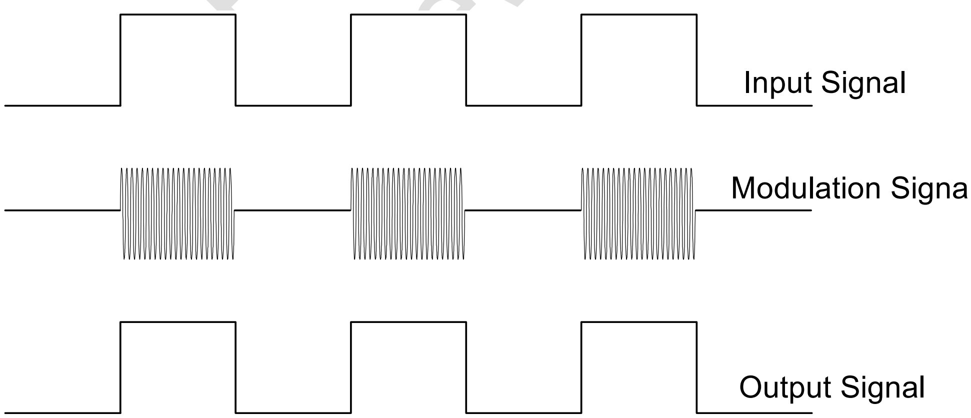

Figure 4. Modulation Scheme

2.2. Eye Diagram

Figure 5 illustrates an eye-diagram taken on an Si8460. For the data source, the test used an Anritsu (MP1763C) Pulse Pattern Generator set to 1000 ns/div. The output of the generator's clock and data from an Si8460 were captured on an oscilloscope. The results illustrate that data integrity was maintained even at the high data rate of 150 Mbps. The results also show that 2 ns pulse width distortion and 250 ps peak jitter were exhibited.

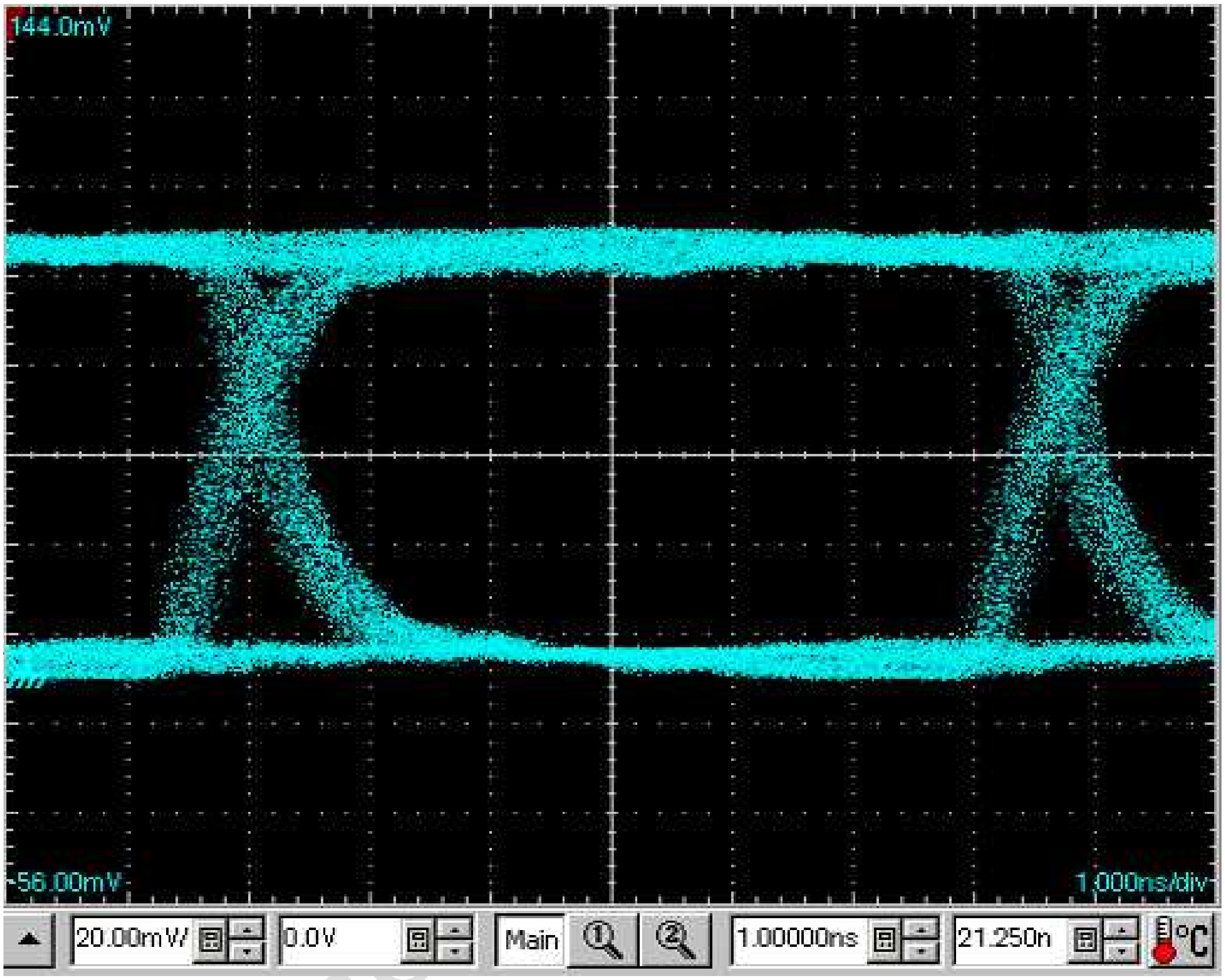

Figure 5. Eye Diagram

2.3. Device Operation

Device behavior during startup, normal operation, and shutdown is shown in Table 12.

Table 12. Si846x Logic Operation Table

V_I Input[1,2]	VDDI State[1,3,4]	VDDO State[1,3,4]	V_O Output[1,2]	Comments
H	P	P	H	Normal operation.
L	P	P	L	
X[5]	UP	P	L	Upon transition of VDDI from unpowered to powered, V_O returns to the same state as V_I in less than 1 µs.
X[5]	P	UP	Undetermined	Upon transition of VDDO from unpowered to powered, V_O returns to the same state as V_I within 1 µs.

Notes:
1. VDDI and VDDO are the input and output power supplies. V_I and V_O are the respective input and output terminals.
2. X = not applicable; H = Logic High; L = Logic Low; Hi-Z = High Impedance.
3. “Powered” state (P) is defined as 2.70 V < VDD < 5.5 V.
4. “Unpowered” state (UP) is defined as VDD = 0 V.
5. Note that an I/O can power the die for a given side through an internal diode if its source has adequate current.

2.4. Layout Recommendations

To ensure safety in the end user application, high voltage circuits (i.e., circuits with >30 V_{AC}) must be physically separated from the safety extra-low voltage circuits (SELV is a circuit with <30 V_{AC}) by a certain distance (creepage/clearance). If a component, such as a digital isolator, straddles this isolation barrier, it must meet those creepage/clearance requirements and also provide a sufficiently large high-voltage breakdown protection rating (commonly referred to as working voltage protection). Table 6 on page 16 and Table 7 on page 17 detail the working voltage and creepage/clearance capabilities of the Si84xx. These tables also detail the component standards (UL1577, IEC60747, CSA 5A), which are readily accepted by certification bodies to provide proof for end-system specifications requirements. Refer to the end-system specification (61010-1, 60950-1, etc.) requirements before starting any design that uses a digital isolator.

The following sections detail the recommended bypass and decoupling components necessary to ensure robust overall performance and reliability for systems using the Si84xx digital isolators.

2.4.1. Supply Bypass

Digital integrated circuit components typically require 0.1 µF (100 nF) bypass capacitors when used in electrically quiet environments. However, digital isolators are commonly used in hazardous environments with excessively noisy power supplies. To counteract these harsh conditions, it is recommended that an additional 1 µF bypass capacitor be added between VDD and GND on both sides of the package. The capacitors should be placed as close as possible to the package to minimize stray inductance. If the system is excessively noisy, it is recommended that the designer add 50 to 100 Ω resistors in series with the VDD supply voltage source and 50 to 300 Ω resistors in series with the digital inputs/outputs (see Figure 6). For more details, see "3. Errata and Design Migration Guidelines" on page 27.

All components upstream or downstream of the isolator should be properly decoupled as well. If these components are not properly decoupled, their supply noise can couple to the isolator inputs and outputs, potentially causing damage if spikes exceed the maximum ratings of the isolator (6 V). In this case, the 50 to 300 Ω resistors protect the isolator's inputs/outputs (note that permanent device damage may occur if the absolute maximum ratings are exceeded). Functional operation should be restricted to the conditions specified in Table 1, “Recommended Operating Conditions,” on page 4.

2.4.2. Pin Connections

No connect pins are not internally connected. They can be left floating, tied to V_{DD}, or tied to GND.

2.4.3. Output Pin Termination

The nominal output impedance of an isolator driver channel is approximately 85 Ω, ±40%, which is a combination of the value of the on-chip series termination resistor and channel resistance of the output driver FET. When driving loads where transmission line effects will be a factor, output pins should be appropriately terminated with controlled impedance PCB traces. The series termination resistor values should be scaled appropriately while keeping in mind the recommendations described in “2.4.1. Supply Bypass” above.

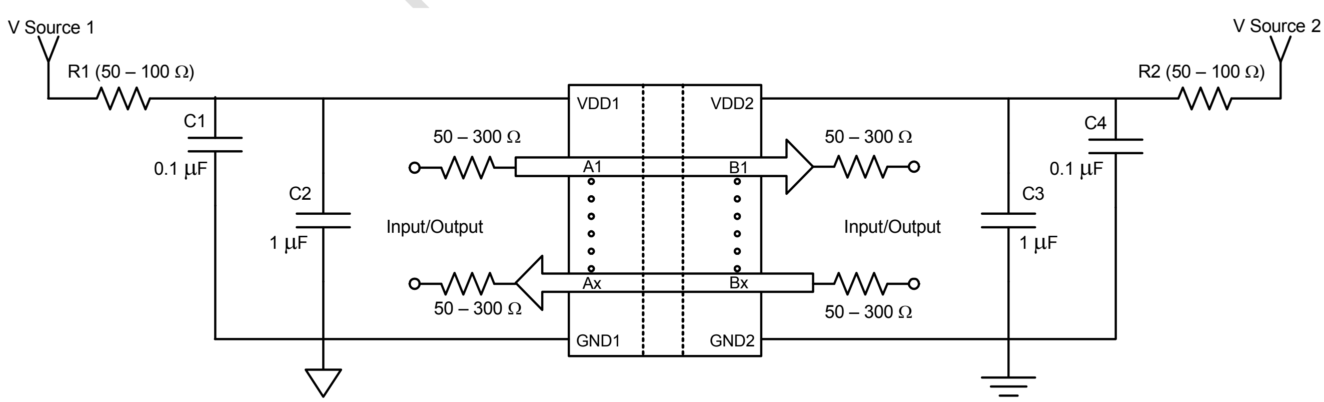

Figure 6. Recommended Bypass Components for the Si84xx Digital Isolator Family

2.5. Typical Performance Characteristics

The typical performance characteristics depicted in the following diagrams are for information purposes only. Refer to Tables 3, 4, and 5 for actual specification limits.

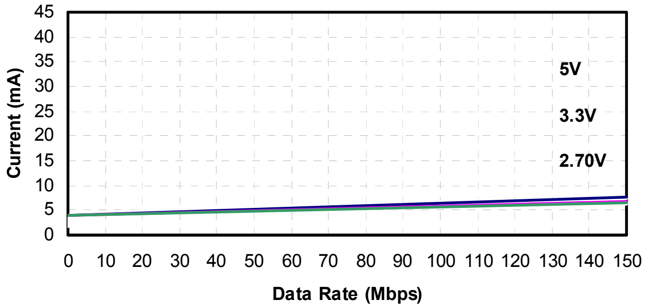

Figure 7. Si8460 Typical V_{DD1} Supply Current vs. Data Rate 5, 3.3, and 2.70 V Operation

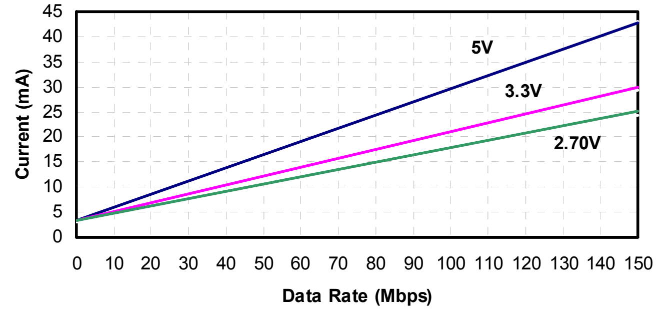

Figure 10. Si8460 Typical V_{DD2} Supply Current vs. Data Rate 5, 3.3, and 2.70 V Operation (15 pF Load)

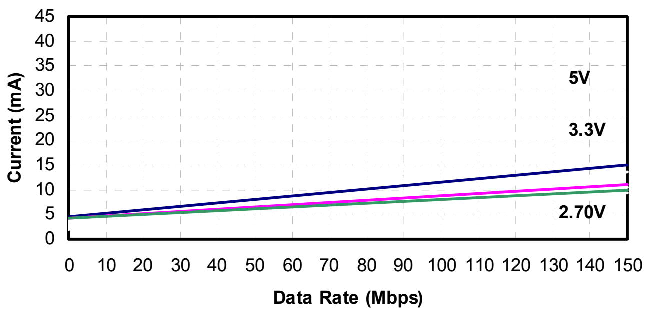

Figure 8. Si8461 Typical V_{DD1} Supply Current vs. Data Rate 5, 3.3, and 2.70 V Operation (15 pF Load)

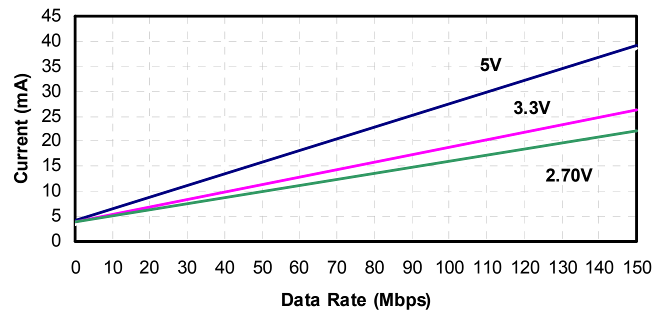

Figure 11. Si8461 Typical V_{DD2} Supply Current vs. Data Rate 5, 3.3, and 2.70 V Operation (15 pF Load)

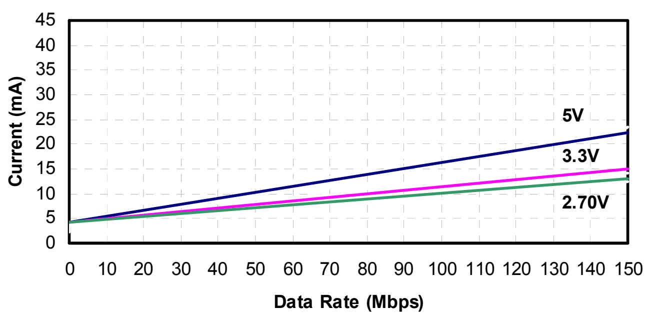

Figure 9. Si8462 Typical V_{DD1} Supply Current vs. Data Rate 5, 3.3, and 2.70 V Operation (15 pF Load)

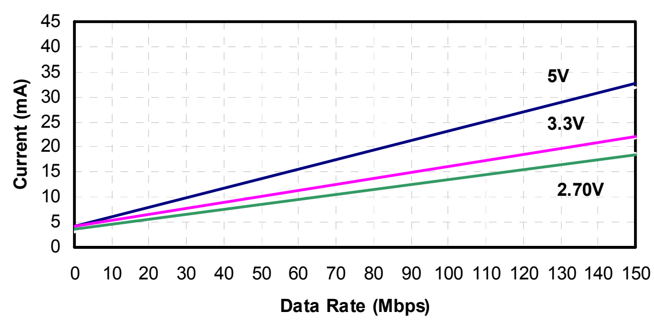

Figure 12. Si8462 Typical V_{DD2} Supply Current vs. Data Rate 5, 3.3, and 2.70 V Operation (15 pF Load)

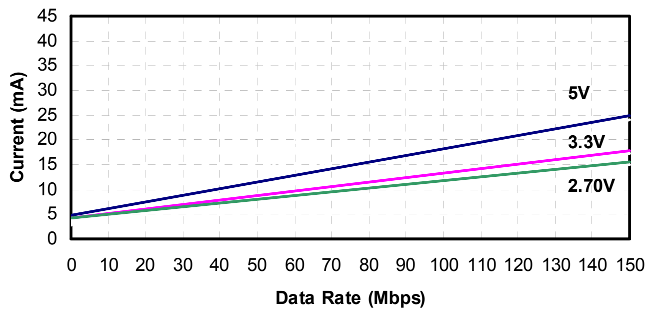

Figure 13. Si8463 Typical V_{DD1} or V_{DD2} Supply Current vs. Data Rate 5, 3.3, and 2.70 V Operation (15 pF Load)

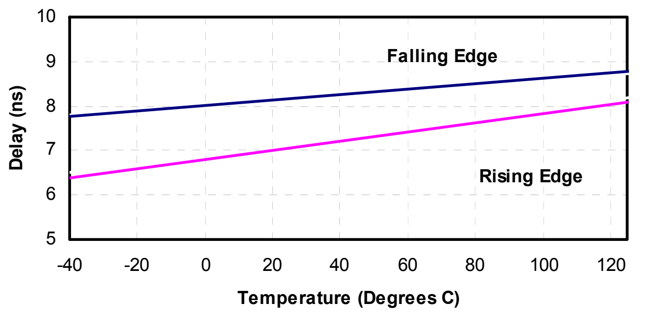

Figure 14. Propagation Delay vs. Temperature