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SILICON LABS

1MBPS, 2.5KVRMS DIGITAL ISOLATORS

Features

- High-speed operation
  - DC to 1 Mbps
- No start-up initialization required
- Wide Operating Supply Voltage
  - 2.5–5.5 V
- Up to 2500 V_{RMS} isolation
- 60-year life at rated working voltage
- High electromagnetic immunity
- Ultra low power (typical)
  5 V Operation
  - 1.6 mA per channel at 1 Mbps

  2.5 V Operation
  - 1.5 mA per channel at 1 Mbps
- Tri-state outputs with ENABLE
- Schmitt trigger inputs
- Transient Immunity 50 kV/µs
- AEC-Q100 qualification
- Wide temperature range
  - –40 to 125 °C
- RoHS-compliant packages
  - SOIC-16 wide body
  - SOIC-16 narrow body
  - SOIC-8 narrow body

Ordering Information:
See page 38.

Applications

- Industrial automation systems
- Medical electronics
- Hybrid electric vehicles
- Isolated switch mode supplies
- Isolated ADC, DAC
- Motor control
- Power inverters
- Communication systems

Safety Regulatory Approvals

- UL 1577 recognized
  - Up to 2500 V_{RMS} for 1 minute
- CSA component notice 5A approval
  - IEC 60950-1, 61010-1
- VDE certification conformity
  - IEC 60747-5-2 (VDE0884 Part 2)
- CQC certification approval
  - GB4943.1

Description

Silicon Lab's family of ultra-low-power digital isolators are CMOS devices offering substantial data rate, propagation delay, power, size, reliability, and external BOM advantages over legacy isolation technologies. The operating parameters of these products remain stable across wide temperature ranges and throughout device service life for ease of design and highly uniform performance. All device versions have Schmitt trigger inputs for high noise immunity and only require VDD bypass capacitors.
All products support Data rates up to 1 Mbps and Enable inputs which provide a single point control for enabling and disabling output drive. All products are safety certified by UL, CSA, VDE, and CQC and support withstand ratings up to 2.5 kV_{RMS}.

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1. Electrical Specifications

Table 1. Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Ambient Operating Temperature*	T_A	–40	25	125	ºC
Supply Voltage	V_{DD1}	2.5	—	5.5	V
	V_{DD2}	2.5	—	5.5	V

***Note:** The maximum ambient temperature is dependent on data frequency, output loading, number of operating channels, and supply voltage.

Table 2. Electrical Characteristics

(V_{DD1} = 5 V±10%, V_{DD2} = 5 V±10%, T_A = –40 to 125 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
VDD Undervoltage Threshold	VDDUV+	V_{DD1}, V_{DD2} rising	1.95	2.24	2.375	V
VDD Undervoltage Threshold	VDDUV–	V_{DD1}, V_{DD2} falling	1.88	2.16	2.325	V
VDD Undervoltage Hysteresis	VDD_{HYS}		50	70	95	mV
Positive-Going Input Threshold	VT+	All inputs rising	1.4	1.67	1.9	V
Negative-Going Input Threshold	VT–	All inputs falling	1.0	1.23	1.4	V
Input Hysteresis	V_{HYS}		0.38	0.44	0.50	V
High Level Input Voltage	V_{IH}		2.0	—	—	V
Low Level input voltage	V_{IL}		—	—	0.8	V
High Level Output Voltage	V_{OH}	Ioh = –4 mA	V_{DD1},V_{DD2} – 0.4	4.8	—	V
Low Level Output Voltage	V_{OL}	Iol = 4 mA	—	0.2	0.4	V
Input Leakage Current	I_L		—	—	±10	µA
Output Impedance[1]	Z_O		—	50	—	Ω
Enable Input High Current	I_{ENH}	V_{ENx} = V_{IH}	—	2.0	—	µA
Enable Input Low Current	I_{ENL}	V_{ENx} = V_{IL}	—	2.0	—	µA

Notes:

1. The nominal output impedance of an isolator driver channel is approximately 50 Ω, ±40%, which is a combination of the value of the on-chip series termination resistor and channel resistance of the output driver FET. When driving loads where transmission line effects will be a factor, output pins should be appropriately terminated with controlled impedance PCB traces.
2. $t_{PSK(P-P)}$ is the magnitude of the difference in propagation delay times measured between different units operating at the same supply voltages, load, and ambient temperature.
3. Start-up time is the time period from the application of power to valid data at the output.

Table 2. Electrical Characteristics (Continued)
(V_{DD1} = 5 V±10%, V_{DD2} = 5 V±10%, T_A = –40 to 125 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
DC Supply Current (All inputs 0 V or at Supply)						
Si8610Ax						
V_{DD1}		V_I = 0(Ax)	—	0.6	1.2	mA
V_{DD2}		V_I = 0(Ax)	—	0.8	1.5	
V_{DD1}		V_I = 1(Ax)	—	1.8	2.9	
V_{DD2}		V_I = 1(Ax)	—	0.8	1.5	
Si8620Ax						
V_{DD1}		V_I = 0(Ax)	—	0.8	1.4	mA
V_{DD2}		V_I = 0(Ax)	—	1.4	2.2	
V_{DD1}		V_I = 1(Ax)	—	3.3	5.3	
V_{DD2}		V_I = 1(Ax)	—	1.4	2.2	
Si8621Ax						
V_{DD1}		V_I = 0(Ax)	—	1.2	1.9	mA
V_{DD2}		V_I = 0(Ax)	—	1.2	1.9	
V_{DD1}		V_I = 1(Ax)	—	2.4	3.8	
V_{DD2}		V_I = 1(Ax)	—	2.4	3.8	
Si8630Ax						
V_{DD1}		V_I = 0(Ax)	—	0.9	1.6	mA
V_{DD2}		V_I = 0(Ax)	—	1.9	3.0	
V_{DD1}		V_I = 1(Ax)	—	4.6	7.4	
V_{DD2}		V_I = 1(Ax)	—	1.9	3.0	
Si8631Ax						
V_{DD1}		V_I = 0(Ax)	—	1.3	2.1	mA
V_{DD2}		V_I = 0(Ax)	—	1.7	2.7	
V_{DD1}		V_I = 1(Ax)	—	3.9	5.9	
V_{DD2}		V_I = 1(Ax)	—	3.0	4.5	
Si8640Ax						
V_{DD1}		V_I = 0(Ax)	—	1.0	1.6	mA
V_{DD2}		V_I = 0(Ax)	—	2.4	3.8	
V_{DD1}		V_I = 1(Ax)	—	6.1	9.2	
V_{DD2}		V_I = 1(Ax)	—	2.5	4.0	
Si8641Ax						
V_{DD1}		V_I = 0(Ax)	—	1.4	2.2	mA
V_{DD2}		V_I = 0(Ax)	—	2.3	3.7	
V_{DD1}		V_I = 1(Ax)	—	5.2	7.8	
V_{DD2}		V_I = 1(Ax)	—	3.6	5.4	
Si8642Ax						
V_{DD1}		V_I = 0(Ax)	—	1.8	2.9	mA
V_{DD2}		V_I = 0(Ax)	—	1.8	2.9	
V_{DD1}		V_I = 1(Ax)	—	4.4	6.6	
V_{DD2}		V_I = 1(Ax)	—	4.4	6.6	

Notes:
1. The nominal output impedance of an isolator driver channel is approximately 50 Ω, ±40%, which is a combination of the value of the on-chip series termination resistor and channel resistance of the output driver FET. When driving loads where transmission line effects will be a factor, output pins should be appropriately terminated with controlled impedance PCB traces.
2. $t_{PSK(P-P)}$ is the magnitude of the difference in propagation delay times measured between different units operating at the same supply voltages, load, and ambient temperature.
3. Start-up time is the time period from the application of power to valid data at the output.

Table 2. Electrical Characteristics (Continued)

(V_{DD1} = 5 V±10%, V_{DD2} = 5 V±10%, T_A = –40 to 125 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Si8650Ax						
V_{DD1}		V_I = 0(Ax)	—	1.1	1.8	mA
V_{DD2}		V_I = 0(Ax)	—	3.1	4.7	
V_{DD1}		V_I = 1(Ax)	—	7.0	9.8	
V_{DD2}		V_I = 1(Ax)	—	3.3	5.0	
Si8651Ax						
V_{DD1}		V_I = 0(Ax)	—	1.5	2.4	mA
V_{DD2}		V_I = 0(Ax)	—	2.7	4.1	
V_{DD1}		V_I = 1(Ax)	—	6.6	9.2	
V_{DD2}		V_I = 1(Ax)	—	4.0	6.0	
Si8652Ax						
V_{DD1}		V_I = 0(Ax)	—	2.0	3.0	mA
V_{DD2}		V_I = 0(Ax)	—	2.4	3.6	
V_{DD1}		V_I = 1(Ax)	—	5.6	7.8	
V_{DD2}		V_I = 1(Ax)	—	5.0	7.5	
Si8660Ax						
V_{DD1}		V_I = 0(Ax)	—	1.2	1.9	mA
V_{DD2}		V_I = 0(Ax)	—	3.5	5.3	
V_{DD1}		V_I = 1(Ax)	—	8.8	12.3	
V_{DD2}		V_I = 1(Ax)	—	3.7	5.6	
Si8661Ax						
V_{DD1}		V_I = 0(Ax)	—	1.7	2.7	mA
V_{DD2}		V_I = 0(Ax)	—	3.4	5.1	
V_{DD1}		V_I = 1(Ax)	—	7.9	11.1	
V_{DD2}		V_I = 1(Ax)	—	4.8	7.2	
Si8662Ax						
V_{DD1}		V_I = 0(Ax)	—	2.2	3.3	mA
V_{DD2}		V_I = 0(Ax)	—	3.0	4.5	
V_{DD1}		V_I = 1(Ax)	—	7.5	10.5	
V_{DD2}		V_I = 1(Ax)	—	5.6	8.4	
Si8663Ax						
V_{DD1}		V_I = 0(Ax)	—	2.6	3.9	mA
V_{DD2}		V_I = 0(Ax)	—	2.6	3.9	
V_{DD1}		V_I = 1(Ax)	—	6.5	9.1	
V_{DD2}		V_I = 1(Ax)	—	6.5	9.1	

Notes:

1. The nominal output impedance of an isolator driver channel is approximately 50 Ω, ±40%, which is a combination of the value of the on-chip series termination resistor and channel resistance of the output driver FET. When driving loads where transmission line effects will be a factor, output pins should be appropriately terminated with controlled impedance PCB traces.
2. $t_{PSK(P-P)}$ is the magnitude of the difference in propagation delay times measured between different units operating at the same supply voltages, load, and ambient temperature.
3. Start-up time is the time period from the application of power to valid data at the output.

Table 2. Electrical Characteristics (Continued)
(V_{DD1} = 5 V±10%, V_{DD2} = 5 V±10%, T_A = –40 to 125 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
1 Mbps Supply Current (All inputs = 500 kHz square wave, Cl = 15 pF on all Outputs)						
Si8610Ax V_{DD1} V_{DD2}			— —	1.2 0.9	2.0 1.5	mA
Si8620Ax V_{DD1} V_{DD2}			— —	2.1 1.6	3.1 2.4	mA
Si8621Ax V_{DD1} V_{DD2}			— —	1.9 1.9	2.9 2.9	mA
Si8630Ax V_{DD1} V_{DD2}			— —	2.8 2.2	3.9 3.1	mA
Si8631Ax V_{DD1} V_{DD2}			— —	2.7 2.6	3.8 3.6	mA
Si8640Ax V_{DD1} V_{DD2}			— —	3.6 2.9	5.0 4.0	mA
Si8641Ax V_{DD1} V_{DD2}			— —	3.4 3.3	4.8 4.6	mA
Si8642Ax V_{DD1} V_{DD2}			— —	3.3 3.3	4.6 4.6	mA
Si8650Ax V_{DD1} V_{DD2}			— —	4.1 3.7	5.7 5.2	mA
Si8651Ax V_{DD1} V_{DD2}			— —	4.2 3.8	5.8 5.3	mA
Si8652Ax V_{DD1} V_{DD2}			— —	4.0 4.0	5.6 5.6	mA
Si8660Ax V_{DD1} V_{DD2}			— —	5.0 4.2	7.0 5.9	mA
Si8661Ax V_{DD1} V_{DD2}			— —	4.9 4.6	6.9 6.4	mA

Notes:

1. The nominal output impedance of an isolator driver channel is approximately 50 Ω, ±40%, which is a combination of the value of the on-chip series termination resistor and channel resistance of the output driver FET. When driving loads where transmission line effects will be a factor, output pins should be appropriately terminated with controlled impedance PCB traces.
2. $t_{PSK(P-P)}$ is the magnitude of the difference in propagation delay times measured between different units operating at the same supply voltages, load, and ambient temperature.
3. Start-up time is the time period from the application of power to valid data at the output.

Table 2. Electrical Characteristics (Continued)

(V_{DD1} = 5 V±10%, V_{DD2} = 5 V±10%, T_A = –40 to 125 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Si8662Ax V_{DD1} V_{DD2}			— —	5.1 4.7	7.1 6.6	mA
Si8663Ax V_{DD1} V_{DD2}			— —	4.9 4.9	6.8 6.8	mA
Timing Characteristics						
All Models						
Maximum Data Rate			0	—	1	Mbps
Minimum Pulse Width			—	—	250	ns
Propagation Delay	t_{PHL}, t_{PLH}	See Figure 2	—	—	35	ns
Pulse Width Distortion $\|t_{PLH} - t_{PHL}\|$	PWD	See Figure 2	—	—	25	ns
Propagation Delay Skew[2]	$t_{PSK(P-P)}$		—	—	40	ns
Channel-Channel Skew	t_{PSK}		—	—	35	ns
Output Rise Time	t_r	C_L = 15 pF See Figure 2	—	2.5	4.0	ns
Output Fall Time	t_f	C_L = 15 pF See Figure 2	—	2.5	4.0	ns
Peak eye diagram jitter	$t_{JIT(PK)}$	See Figure 8	—	350	—	ps
Common Mode Transient Immunity	CMTI	V_I = V_{DD} or 0 V V_{CM} = 1500 V (see Figure 3)	35	50	—	kV/µs
Enable to Data Valid	t_{en1}	See Figure 1	—	6.0	11	ns
Enable to Data Tri-State	t_{en2}	See Figure 1	—	8.0	12	ns
Start-up Time[3]	t_{SU}		—	15	40	µs

Notes:

1. The nominal output impedance of an isolator driver channel is approximately 50 Ω, ±40%, which is a combination of the value of the on-chip series termination resistor and channel resistance of the output driver FET. When driving loads where transmission line effects will be a factor, output pins should be appropriately terminated with controlled impedance PCB traces.
2. $t_{PSK(P-P)}$ is the magnitude of the difference in propagation delay times measured between different units operating at the same supply voltages, load, and ambient temperature.
3. Start-up time is the time period from the application of power to valid data at the output.

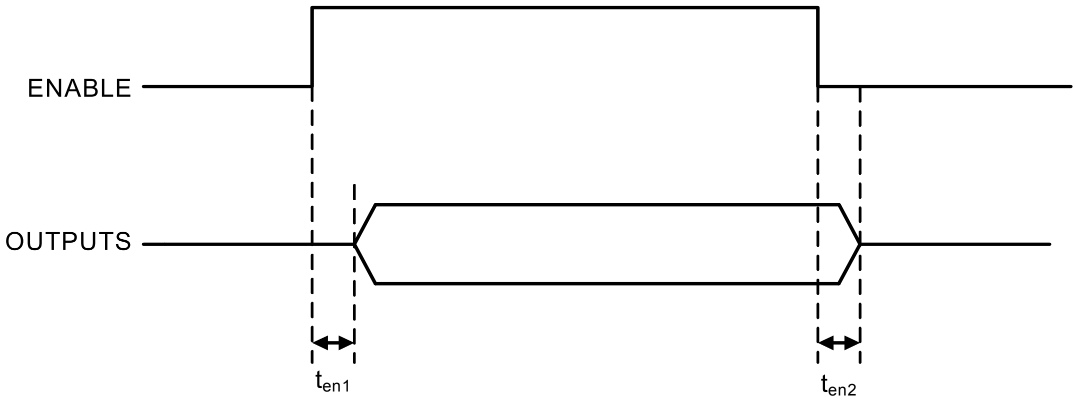

Figure 1. ENABLE Timing Diagram

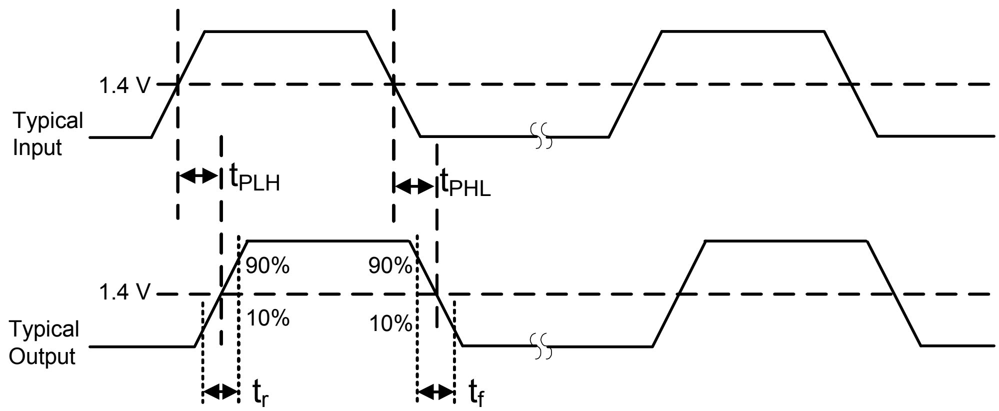

Figure 2. Propagation Delay Timing

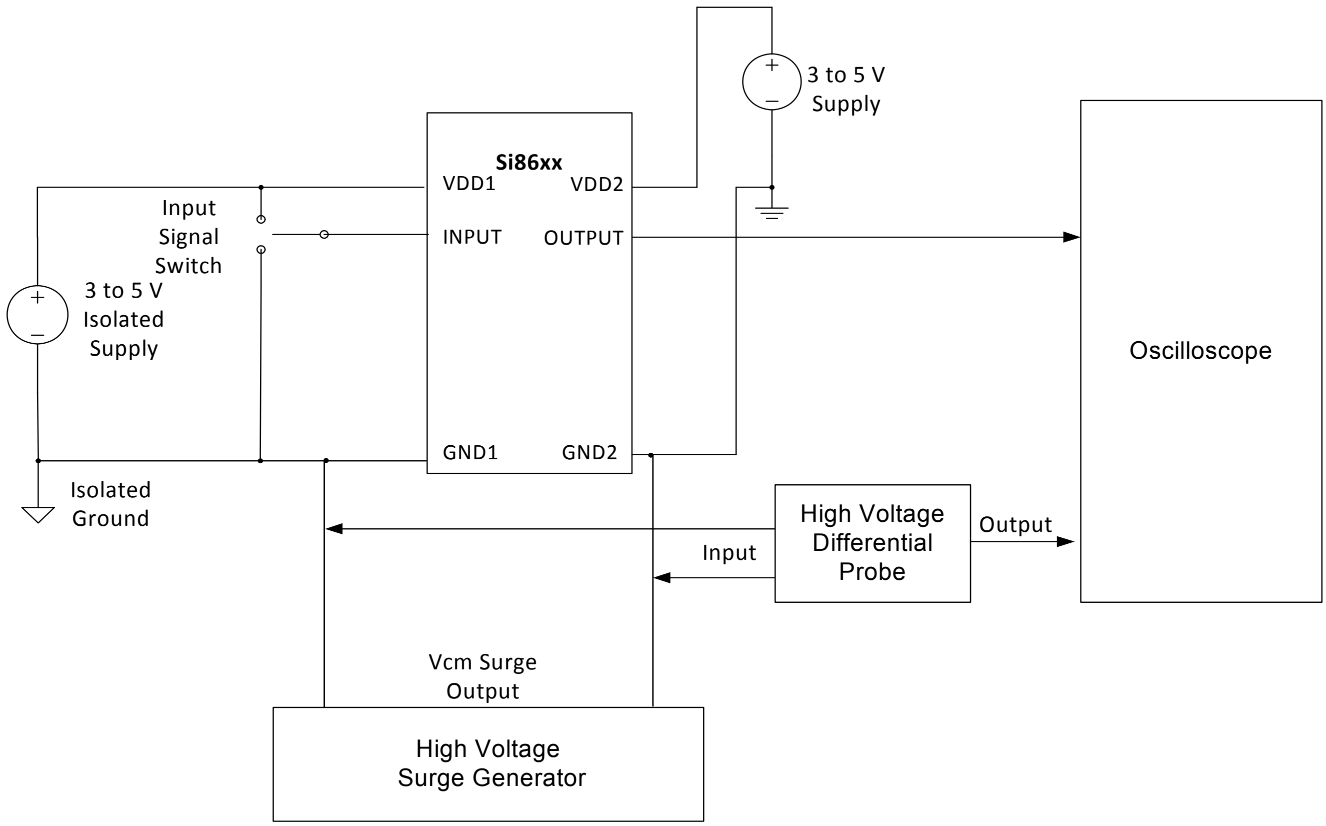

Figure 3. Common-Mode Transient Immunity Test Circuit

Table 3. Electrical Characteristics
(V_{DD1} = 3.3 V±10%, V_{DD2} = 3.3 V±10%, T_A = –40 to 125 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
VDD Undervoltage Threshold	VDDUV+	V_{DD1}, V_{DD2} rising	1.95	2.24	2.375	V
VDD Undervoltage Threshold	VDDUV–	V_{DD1}, V_{DD2} falling	1.88	2.16	2.325	V
VDD Undervoltage Hysteresis	VDD_{HYS}		50	70	95	mV
Positive-Going Input Threshold	VT+	All inputs rising	1.4	1.67	1.9	V
Negative-Going Input Threshold	VT–	All inputs falling	1.0	1.23	1.4	V
Input Hysteresis	V_{HYS}		0.38	0.44	0.50	V
High Level Input Voltage	V_{IH}		2.0	—	—	V
Low Level Input Voltage	V_{IL}		—	—	0.8	V
High Level Output Voltage	V_{OH}	Ioh = –4 mA	V_{DD1}, V_{DD2} – 0.4	3.1	—	V
Low Level Output Voltage	V_{OL}	Iol = 4 mA	—	0.2	0.4	V
Input Leakage Current	I_L		—	—	±10	µA
Output Impedance[1]	Z_O		—	50	—	Ω
Enable Input High Current	I_{ENH}	$V_{ENx} = V_{IH}$	—	2.0	—	µA
Enable Input Low Current	I_{ENL}	$V_{ENx} = V_{IL}$	—	2.0	—	µA
DC Supply Current (All inputs 0 V or at supply)						
Si8610Ax V_{DD1} V_{DD2} V_{DD1} V_{DD2}		 V_I = 0(Ax) V_I = 0(Ax) V_I = 1(Ax) V_I = 1(Ax)	 — — — —	 0.6 0.8 1.8 0.8	 1.2 1.5 2.9 1.5	mA
Si8620Ax V_{DD1} V_{DD2} V_{DD1} V_{DD2}		 V_I = 0(Ax) V_I = 0(Ax) V_I = 1(Ax) V_I = 1(Ax)	 — — — —	 0.8 1.4 3.3 1.4	 1.4 2.2 5.3 2.2	mA
Si8621Ax V_{DD1} V_{DD2} V_{DD1} V_{DD2}		 V_I = 0(Ax) V_I = 0(Ax) V_I = 1(Ax) V_I = 1(Ax)	 — — — —	 1.2 1.2 2.4 2.4	 1.9 1.9 3.8 3.8	mA
Si8630Ax V_{DD1} V_{DD2} V_{DD1} V_{DD2}		 V_I = 0(Ax) V_I = 0(Ax) V_I = 1(Ax) V_I = 1(Ax)	 — — — —	 0.9 1.9 4.6 1.9	 1.6 3.0 7.4 3.0	mA

Notes:
1. The nominal output impedance of an isolator driver channel is approximately 50 Ω, ±40%, which is a combination of the value of the on-chip series termination resistor and channel resistance of the output driver FET. When driving loads where transmission line effects will be a factor, output pins should be appropriately terminated with controlled impedance PCB traces.
2. $t_{PSK(P-P)}$ is the magnitude of the difference in propagation delay times measured between different units operating at the same supply voltages, load, and ambient temperature.
3. Start-up time is the time period from the application of power to valid data at the output.

Table 3. Electrical Characteristics (Continued)
(V_{DD1} = 3.3 V±10%, V_{DD2} = 3.3 V±10%, T_A = –40 to 125 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Si8631Ax						
V_{DD1}		V_I = 0(Ax)	—	1.3	2.1	mA
V_{DD2}		V_I = 0(Ax)	—	1.7	2.7	
V_{DD1}		V_I = 1(Ax)	—	3.9	5.9	
V_{DD2}		V_I = 1(Ax)	—	3.0	4.5	
Si8640Ax						
V_{DD1}		V_I = 0(Ax)	—	1.0	1.6	mA
V_{DD2}		V_I = 0(Ax)	—	2.4	3.8	
V_{DD1}		V_I = 1(Ax)	—	6.1	9.2	
V_{DD2}		V_I = 1(Ax)	—	2.5	4.0	
Si8641Ax						
V_{DD1}		V_I = 0(Ax)	—	1.4	2.2	mA
V_{DD2}		V_I = 0(Ax)	—	2.3	3.7	
V_{DD1}		V_I = 1(Ax)	—	5.2	7.8	
V_{DD2}		V_I = 1(Ax)	—	3.6	5.4	
Si8642Ax						
V_{DD1}		V_I = 0(Ax)	—	1.8	2.9	mA
V_{DD2}		V_I = 0(Ax)	—	1.8	2.9	
V_{DD1}		V_I = 1(Ax)	—	4.4	6.6	
V_{DD2}		V_I = 1(Ax)	—	4.4	6.6	
Si8650Ax						
V_{DD1}		V_I = 0(Ax)	—	1.1	1.8	mA
V_{DD2}		V_I = 0(Ax)	—	3.1	4.7	
V_{DD1}		V_I = 1(Ax)	—	7.0	9.8	
V_{DD2}		V_I = 1(Ax)	—	3.3	5.0	
Si8651Ax						
V_{DD1}		V_I = 0(Ax)	—	1.5	2.4	mA
V_{DD2}		V_I = 0(Ax)	—	2.7	4.1	
V_{DD1}		V_I = 1(Ax)	—	6.6	9.2	
V_{DD2}		V_I = 1(Ax)	—	4.0	6.0	
Si8652Ax						
V_{DD1}		V_I = 0(Ax)	—	2.0	3.0	mA
V_{DD2}		V_I = 0(Ax)	—	2.4	3.6	
V_{DD1}		V_I = 1(Ax)	—	5.6	7.8	
V_{DD2}		V_I = 1(Ax)	—	5.0	7.5	

Notes:
1. The nominal output impedance of an isolator driver channel is approximately 50 Ω, ±40%, which is a combination of the value of the on-chip series termination resistor and channel resistance of the output driver FET. When driving loads where transmission line effects will be a factor, output pins should be appropriately terminated with controlled impedance PCB traces.
2. $t_{PSK(P-P)}$ is the magnitude of the difference in propagation delay times measured between different units operating at the same supply voltages, load, and ambient temperature.
3. Start-up time is the time period from the application of power to valid data at the output.

Table 3. Electrical Characteristics (Continued)
(V_{DD1} = 3.3 V±10%, V_{DD2} = 3.3 V±10%, T_A = –40 to 125 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Si8660Ax						
V_{DD1}		V_I = 0(Ax)	—	1.2	1.9	mA
V_{DD2}		V_I = 0(Ax)	—	3.5	5.3	
V_{DD1}		V_I = 1(Ax)	—	8.8	12.3	
V_{DD2}		V_I = 1(Ax)	—	3.7	5.6	
Si8661Ax						
V_{DD1}		V_I = 0(Ax)	—	1.7	2.7	mA
V_{DD2}		V_I = 0(Ax)	—	3.4	5.1	
V_{DD1}		V_I = 1(Ax)	—	7.9	11.1	
V_{DD2}		V_I = 1(Ax)	—	4.8	7.2	
Si8662Ax						
V_{DD1}		V_I = 0(Ax)	—	2.2	3.3	mA
V_{DD2}		V_I = 0(Ax)	—	3.0	4.5	
V_{DD1}		V_I = 1(Ax)	—	7.5	10.5	
V_{DD2}		V_I = 1(Ax)	—	5.6	8.4	
Si8663Ax						
V_{DD1}		V_I = 0(Ax)	—	2.6	3.9	mA
V_{DD2}		V_I = 0(Ax)	—	2.6	3.9	
V_{DD1}		V_I = 1(Ax)	—	6.5	9.1	
V_{DD2}		V_I = 1(Ax)	—	6.5	9.1	

Notes:

1. The nominal output impedance of an isolator driver channel is approximately 50 Ω, ±40%, which is a combination of the value of the on-chip series termination resistor and channel resistance of the output driver FET. When driving loads where transmission line effects will be a factor, output pins should be appropriately terminated with controlled impedance PCB traces.
2. $t_{PSK(P-P)}$ is the magnitude of the difference in propagation delay times measured between different units operating at the same supply voltages, load, and ambient temperature.
3. Start-up time is the time period from the application of power to valid data at the output.

Table 3. Electrical Characteristics (Continued)
(V_{DD1} = 3.3 V±10%, V_{DD2} = 3.3 V±10%, T_A = –40 to 125 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
1 Mbps Supply Current (All inputs = 500 kHz square wave, Cl = 15 pF on all outputs)						
Si8610Ax V_{DD1} V_{DD2}			— —	1.2 0.9	2.0 1.5	mA
Si8620Ax V_{DD1} V_{DD2}			— —	2.1 1.6	3.1 2.4	mA
Si8621Ax V_{DD1} V_{DD2}			— —	1.9 1.9	2.9 2.9	mA
Si8630Ax V_{DD1} V_{DD2}			— —	2.8 2.2	3.9 3.1	mA
Si8631Ax V_{DD1} V_{DD2}			— —	2.7 2.6	3.8 3.6	mA
Si8640Ax V_{DD1} V_{DD2}			— —	3.6 2.9	5.0 4.0	mA
Si8641Ax V_{DD1} V_{DD2}			— —	3.4 3.3	4.8 4.6	mA
Si8642Ax V_{DD1} V_{DD2}			— —	3.3 3.3	4.6 4.6	mA
Si8650Ax V_{DD1} V_{DD2}			— —	4.1 3.7	5.7 5.2	mA
Si8651Ax V_{DD1} V_{DD2}			— —	4.2 3.8	5.8 5.3	mA
Si8652Ax V_{DD1} V_{DD2}			— —	4.0 4.0	5.6 5.6	mA
Si8660Ax V_{DD1} V_{DD2}			— —	5.0 4.2	7.0 5.9	mA

Notes:
1. The nominal output impedance of an isolator driver channel is approximately 50 Ω, ±40%, which is a combination of the value of the on-chip series termination resistor and channel resistance of the output driver FET. When driving loads where transmission line effects will be a factor, output pins should be appropriately terminated with controlled impedance PCB traces.
2. $t_{PSK(P-P)}$ is the magnitude of the difference in propagation delay times measured between different units operating at the same supply voltages, load, and ambient temperature.
3. Start-up time is the time period from the application of power to valid data at the output.

Table 3. Electrical Characteristics (Continued)
(V_{DD1} = 3.3 V±10%, V_{DD2} = 3.3 V±10%, T_A = –40 to 125 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Si8661Ax V_{DD1} V_{DD2}			 — —	 4.9 4.6	 6.9 6.4	 mA
Si8662Ax V_{DD1} V_{DD2}			 — —	 5.1 4.7	 7.1 6.6	 mA
Si8663Ax V_{DD1} V_{DD2}			 — —	 4.9 4.9	 6.8 6.8	 mA

Notes:
1. The nominal output impedance of an isolator driver channel is approximately 50 Ω, ±40%, which is a combination of the value of the on-chip series termination resistor and channel resistance of the output driver FET. When driving loads where transmission line effects will be a factor, output pins should be appropriately terminated with controlled impedance PCB traces.
2. $t_{PSK(P-P)}$ is the magnitude of the difference in propagation delay times measured between different units operating at the same supply voltages, load, and ambient temperature.
3. Start-up time is the time period from the application of power to valid data at the output.

Table 3. Electrical Characteristics (Continued)
(V_{DD1} = 3.3 V±10%, V_{DD2} = 3.3 V±10%, T_A = –40 to 125 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Timing Characteristics						
All Models						
Maximum Data Rate			0	—	1	Mbps
Minimum Pulse Width			—	—	250	ns
Propagation Delay	t_{PHL}, t_{PLH}	See Figure 2	—	—	35	ns
Pulse Width Distortion $\|t_{PLH} - t_{PHL}\|$	PWD	See Figure 2	—	—	25	ns
Propagation Delay Skew[2]	$t_{PSK(P-P)}$		—	—	40	ns
Channel-Channel Skew	t_{PSK}		—	—	35	ns
Output Rise Time	t_r	C_L = 15 pF See Figure 2	—	2.5	4.0	ns
Output Fall Time	t_f	C_L = 15 pF See Figure 2	—	2.5	4.0	ns
Peak eye diagram jitter	$t_{JIT(PK)}$	See Figure 8	—	350	—	ps
Common Mode Transient Immunity	CMTI	V_I = V_{DD} or 0 V V_{CM} = 1500 V (see Figure 3)	35	50	—	kV/µs
Enable to Data Valid	t_{en1}	See Figure 1	—	6.0	11	ns
Enable to Data Tri-State	t_{en2}	See Figure 1	—	8.0	12	ns
Start-Up Time[3]	t_{SU}		—	15	40	µs

Notes:
1. The nominal output impedance of an isolator driver channel is approximately 50 Ω, ±40%, which is a combination of the value of the on-chip series termination resistor and channel resistance of the output driver FET. When driving loads where transmission line effects will be a factor, output pins should be appropriately terminated with controlled impedance PCB traces.
2. $t_{PSK(P-P)}$ is the magnitude of the difference in propagation delay times measured between different units operating at the same supply voltages, load, and ambient temperature.
3. Start-up time is the time period from the application of power to valid data at the output.

Table 4. Electrical Characteristics
(V_{DD1} = 2.5 V ±5%, V_{DD2} = 2.5 V ±5%, T_A = –40 to 125 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
VDD Undervoltage Threshold	VDDUV+	V_{DD1}, V_{DD2} rising	1.95	2.24	2.375	V
VDD Undervoltage Threshold	VDDUV–	V_{DD1}, V_{DD2} falling	1.88	2.16	2.325	V
VDD Undervoltage Hysteresis	VDD_{HYS}		50	70	95	mV
Positive-Going Input Threshold	VT+	All inputs rising	1.4	1.67	1.9	V
Negative-Going Input Threshold	VT–	All inputs falling	1.0	1.23	1.4	V
Input Hysteresis	V_{HYS}		0.38	0.44	0.50	V
High Level Input Voltage	V_{IH}		2.0	—	—	V
Low Level Input Voltage	V_{IL}		—	—	0.8	V
High Level Output Voltage	V_{OH}	Ioh = –4 mA	V_{DD1},V_{DD2} – 0.4	2.3	—	V
Low Level Output Voltage	V_{OL}	Iol = 4 mA	—	0.2	0.4	V
Input Leakage Current	I_L		—	—	±10	µA
Output Impedance[1]	Z_O		—	50	—	Ω
Enable Input High Current	I_{ENH}	$V_{ENx} = V_{IH}$	—	2.0	—	µA
Enable Input Low Current	I_{ENL}	$V_{ENx} = V_{IL}$	—	2.0	—	µA
DC Supply Current (All inputs 0 V or at supply)						
Si8610Ax V_{DD1} V_{DD2} V_{DD1} V_{DD2}		 V_I = 0(Ax)) V_I = 0(Ax) V_I = 1(Ax) V_I = 1(Ax)	 — — — —	 0.6 0.8 1.8 0.8	 1.2 1.5 2.9 1.5	mA
Si8620Ax V_{DD1} V_{DD2} V_{DD1} V_{DD2}		 V_I = 0(Ax)) V_I = 0(Ax) V_I = 1(Ax) V_I = 1(Ax)	 — — — —	 0.8 1.4 3.3 1.4	 1.4 2.2 5.3 2.2	mA
Si8621Ax V_{DD1} V_{DD2} V_{DD1} V_{DD2}		 V_I = 0(Ax)) V_I = 0(Ax) V_I = 1(Ax) V_I = 1(Ax)	 — — — —	 1.2 1.2 2.4 2.4	 1.9 1.9 3.8 3.8	mA

Notes:
1. The nominal output impedance of an isolator driver channel is approximately 50 Ω, ±40%, which is a combination of the value of the on-chip series termination resistor and channel resistance of the output driver FET. When driving loads where transmission line effects will be a factor, output pins should be appropriately terminated with controlled impedance PCB traces.
2. $t_{PSK(P-P)}$ is the magnitude of the difference in propagation delay times measured between different units operating at the same supply voltages, load, and ambient temperature.
3. Start-up time is the time period from the application of power to valid data at the output.

Table 4. Electrical Characteristics (Continued)
(V_{DD1} = 2.5 V ±5%, V_{DD2} = 2.5 V ±5%, T_A = –40 to 125 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Si8630Ax						
V_{DD1}		V_I = 0(Ax)	—	0.9	1.6	mA
V_{DD2}		V_I = 0(Ax)	—	1.9	3.0	
V_{DD1}		V_I = 1(Ax)	—	4.6	7.4	
V_{DD2}		V_I = 1(Ax)	—	1.9	3.0	
Si8631Ax						
V_{DD1}		V_I = 0(Ax)	—	1.3	2.1	mA
V_{DD2}		V_I = 0(Ax)	—	1.7	2.7	
V_{DD1}		V_I = 1(Ax)	—	3.9	5.9	
V_{DD2}		V_I = 1(Ax)	—	3.0	4.5	
Si8640Ax						
V_{DD1}		V_I = 0(Ax)	—	1.0	1.6	mA
V_{DD2}		V_I = 0(Ax)	—	2.4	3.8	
V_{DD1}		V_I = 1(Ax)	—	6.1	9.2	
V_{DD2}		V_I = 1(Ax)	—	2.5	4.0	
Si8641Ax						
V_{DD1}		V_I = 0(Ax)	—	1.4	2.2	mA
V_{DD2}		V_I = 0(Ax)	—	2.3	3.7	
V_{DD1}		V_I = 1(Ax)	—	5.2	7.8	
V_{DD2}		V_I = 1(Ax)	—	3.6	5.4	
Si8642Ax						
V_{DD1}		V_I = 0(Ax)	—	1.8	2.9	mA
V_{DD2}		V_I = 0(Ax)	—	1.8	2.9	
V_{DD1}		V_I = 1(Ax)	—	4.4	6.6	
V_{DD2}		V_I = 1(Ax)	—	4.4	6.6	
Si8650Ax						
V_{DD1}		V_I = 0(Ax)	—	1.1	1.8	mA
V_{DD2}		V_I = 0(Ax)	—	3.1	4.7	
V_{DD1}		V_I = 1(Ax)	—	7.0	9.8	
V_{DD2}		V_I = 1(Ax)	—	3.3	5.0	
Si8651Ax						
V_{DD1}		V_I = 0(Ax)	—	1.5	2.4	mA
V_{DD2}		V_I = 0(Ax)	—	2.7	4.1	
V_{DD1}		V_I = 1(Ax)	—	6.6	9.2	
V_{DD2}		V_I = 1(Ax)	—	4.0	6.0	

Notes:
1. The nominal output impedance of an isolator driver channel is approximately 50 Ω, ±40%, which is a combination of the value of the on-chip series termination resistor and channel resistance of the output driver FET. When driving loads where transmission line effects will be a factor, output pins should be appropriately terminated with controlled impedance PCB traces.
2. $t_{PSK(P-P)}$ is the magnitude of the difference in propagation delay times measured between different units operating at the same supply voltages, load, and ambient temperature.
3. Start-up time is the time period from the application of power to valid data at the output.

Table 4. Electrical Characteristics (Continued)

(V_{DD1} = 2.5 V ±5%, V_{DD2} = 2.5 V ±5%, T_A = –40 to 125 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Si8652Ax						
V_{DD1}		V_I = 0(Ax)	—	2.0	3.0	mA
V_{DD2}		V_I = 0(Ax)	—	2.4	3.6	
V_{DD1}		V_I = 1(Ax)	—	5.6	7.8	
V_{DD2}		V_I = 1(Ax)	—	5.0	7.5	
Si8660Ax						
V_{DD1}		V_I = 0(Ax)	—	1.2	1.9	mA
V_{DD2}		V_I = 0(Ax)	—	3.5	5.3	
V_{DD1}		V_I = 1(Ax)	—	8.8	12.3	
V_{DD2}		V_I = 1(Ax)	—	3.7	5.6	
Si8661Ax						
V_{DD1}		V_I = 0(Ax)	—	1.7	2.7	mA
V_{DD2}		V_I = 0(Ax)	—	3.4	5.1	
V_{DD1}		V_I = 1(Ax)	—	7.9	11.1	
V_{DD2}		V_I = 1(Ax)	—	4.8	7.2	
Si8662Ax						
V_{DD1}		V_I = 0(Ax)	—	2.2	3.3	mA
V_{DD2}		V_I = 0(Ax)	—	3.0	4.5	
V_{DD1}		V_I = 1(Ax)	—	7.5	10.5	
V_{DD2}		V_I = 1(Ax)	—	5.6	8.4	
Si8663Ax						
V_{DD1}		V_I = 0(Ax)	—	2.6	3.9	mA
V_{DD2}		V_I = 0(Ax)	—	2.6	3.9	
V_{DD1}		V_I = 1(Ax)	—	6.5	9.1	
V_{DD2}		V_I = 1(Ax)	—	6.5	9.1	

Notes:

1. The nominal output impedance of an isolator driver channel is approximately 50 Ω, ±40%, which is a combination of the value of the on-chip series termination resistor and channel resistance of the output driver FET. When driving loads where transmission line effects will be a factor, output pins should be appropriately terminated with controlled impedance PCB traces.
2. $t_{PSK(P-P)}$ is the magnitude of the difference in propagation delay times measured between different units operating at the same supply voltages, load, and ambient temperature.
3. Start-up time is the time period from the application of power to valid data at the output.

Table 4. Electrical Characteristics (Continued)
(V_{DD1} = 2.5 V ±5%, V_{DD2} = 2.5 V ±5%, T_A = –40 to 125 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
1 Mbps Supply Current (All inputs = 500 kHz square wave, Cl = 15 pF on all outputs)						
Si8610Ax V_{DD1} V_{DD2}			— —	1.2 0.9	2.0 1.5	mA
Si8620Ax V_{DD1} V_{DD2}			— —	2.1 1.6	3.1 2.4	mA
Si8621Ax V_{DD1} V_{DD2}			— —	1.9 1.9	2.9 2.9	mA
Si8630Ax V_{DD1} V_{DD2}			— —	2.8 2.2	3.9 3.1	mA
Si8631Ax V_{DD1} V_{DD2}			— —	2.7 2.6	3.8 3.6	mA
Si8640Ax V_{DD1} V_{DD2}			— —	3.6 2.9	5.0 4.0	mA
Si8641Ax V_{DD1} V_{DD2}			— —	3.4 3.3	4.8 4.6	mA
Si8642Ax V_{DD1} V_{DD2}			— —	3.3 3.3	4.6 4.6	mA
Si8650Ax V_{DD1} V_{DD2}			— —	4.1 3.7	5.7 5.2	mA
Si8651Ax V_{DD1} V_{DD2}			— —	4.2 3.8	5.8 5.3	mA
Si8652Ax V_{DD1} V_{DD2}			— —	4.0 4.0	5.6 5.6	mA
Si8660Ax V_{DD1} V_{DD2}			— —	5.0 4.2	7.0 5.9	mA

Notes:
1. The nominal output impedance of an isolator driver channel is approximately 50 Ω, ±40%, which is a combination of the value of the on-chip series termination resistor and channel resistance of the output driver FET. When driving loads where transmission line effects will be a factor, output pins should be appropriately terminated with controlled impedance PCB traces.
2. $t_{PSK(P-P)}$ is the magnitude of the difference in propagation delay times measured between different units operating at the same supply voltages, load, and ambient temperature.
3. Start-up time is the time period from the application of power to valid data at the output.

Table 4. Electrical Characteristics (Continued)
(V_{DD1} = 2.5 V ±5%, V_{DD2} = 2.5 V ±5%, T_A = –40 to 125 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Si8661Ax						
V_{DD1}			—	4.9	6.9	mA
V_{DD2}			—	4.6	6.4	
Si8662Ax						
V_{DD1}			—	5.1	7.1	mA
V_{DD2}			—	4.7	6.6	
Si8663Ax						
V_{DD1}			—	4.9	6.8	mA
V_{DD2}			—	4.9	6.8	

Notes:
1. The nominal output impedance of an isolator driver channel is approximately 50 Ω, ±40%, which is a combination of the value of the on-chip series termination resistor and channel resistance of the output driver FET. When driving loads where transmission line effects will be a factor, output pins should be appropriately terminated with controlled impedance PCB traces.
2. $t_{PSK(P-P)}$ is the magnitude of the difference in propagation delay times measured between different units operating at the same supply voltages, load, and ambient temperature.
3. Start-up time is the time period from the application of power to valid data at the output.

Table 4. Electrical Characteristics (Continued)
(V_{DD1} = 2.5 V ±5%, V_{DD2} = 2.5 V ±5%, T_A = –40 to 125 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Timing Characteristics						
All Models						
Maximum Data Rate			0	—	1	Mbps
Minimum Pulse Width			—	—	250	ns
Propagation Delay	t_{PHL}, t_{PLH}	See Figure 2	—	—	35	ns
Pulse Width Distortion $\lvert t_{PLH} - t_{PHL} \rvert$	PWD	See Figure 2	—	—	25	ns
Propagation Delay Skew[2]	$t_{PSK(P-P)}$		—	—	40	ns
Channel-Channel Skew	t_{PSK}		—	—	35	ns
Output Rise Time	t_r	C_L = 15 pF See Figure 2	—	2.5	4.0	ns
Output Fall Time	t_f	C_L = 15 pF See Figure 2	—	2.5	4.0	ns
Peak Eye Diagram Jitter	$t_{JIT(PK)}$	See Figure 8	—	350	—	ps
Common Mode Transient Immunity	CMTI	$V_I = V_{DD}$ or 0 V V_{CM} = 1500 V (see Figure 3)	35	50	—	kV/µs
Enable to Data Valid	t_{en1}	See Figure 1	—	6.0	11	ns
Enable to Data Tri-State	t_{en2}	See Figure 1	—	8.0	12	ns
Startup Time[3]	t_{SU}		—	15	40	µs

Notes:
1. The nominal output impedance of an isolator driver channel is approximately 50 Ω, ±40%, which is a combination of the value of the on-chip series termination resistor and channel resistance of the output driver FET. When driving loads where transmission line effects will be a factor, output pins should be appropriately terminated with controlled impedance PCB traces.
2. $t_{PSK(P-P)}$ is the magnitude of the difference in propagation delay times measured between different units operating at the same supply voltages, load, and ambient temperature.
3. Start-up time is the time period from the application of power to valid data at the output.

Table 5. Regulatory Information*

CSA
The Si86xx is certified under CSA Component Acceptance Notice 5A, IEC61010-1 and IEC60950-1. For more details, see File 232873.
VDE
The Si86xx is certified according to IEC 60747-5-2. For more details, see File 5006301-4880-0001.
UL
The Si86xx is certified under UL1577 component recognition program. For more details, see File E257455.
CQC
The Si86xx is certified under GB4943.1-2011. For more details, see certificates CQC13001096110 and CQC13001096239.
***Note:** Regulatory Certifications apply to 2.5 kV_{RMS} rated devices which are production tested to 3.0 kV_{RMS} for 1 sec. For more information, see "8. Pin Descriptions (Si866x)" on page 38.

Table 6. Insulation and Safety-Related Specifications

Parameter	Symbol	Test Condition	Value			Unit
			WB SOIC-16	NB SOIC-16	NB SOIC-8	
Nominal Air Gap (Clearance)[1]	L(IO1)		8.0	4.9	4.9	mm
Nominal External Tracking (Creepage)[1]	L(IO2)		8.0	4.01	4.01	mm
Minimum Internal Gap (Internal Clearance)			0.014	0.014	0.014	mm
Tracking Resistance (Proof Tracking Index)	PTI	IEC60112	600	600	600	V_{RMS}
Erosion Depth	ED		0.019	0.019	0.040	mm
Resistance (Input-Output)[2]	R_{IO}		10^{12}	10^{12}	10^{12}	Ω
Capacitance (Input-Output)[2]	C_{IO}	f = 1 MHz	2.0	2.0	2.0	pF
Input Capacitance[3]	C_I		4.0	4.0	4.0	pF

Notes:
1. The values in this table correspond to the nominal creepage and clearance values. VDE certifies the clearance and creepage limits as 4.7 mm minimum for the NB SOIC-16 and SOIC-8 packages and 8.5 mm minimum for the WB SOIC-16 package. UL does not impose a clearance and creepage minimum for component-level certifications. CSA certifies the clearance and creepage limits as 3.9 mm minimum for the NB SOIC-16 and SOIC-8 and 7.6 mm minimum for the WB SOIC-16 package.
2. To determine resistance and capacitance, the Si86xx is converted into a 2-terminal device. Pins 1–8 (Pins 1-4 for the NB SOIC-8) are shorted together to form the first terminal and pins 9–16 (Pins 5-8 for the NB SOIC-8) are shorted together to form the second terminal. The parameters are then measured between these two terminals.
3. Measured from input pin to ground.

Table 7. IEC 60664-1 (VDE 0844 Part 2) Ratings

Parameter	Test Conditions	Specification	
		NB SOIC-16 NB SOIC-8	WB SOIC-16
Basic Isolation Group	Material Group	I	I
Installation Classification	Rated Mains Voltages ≤ 150 V_{RMS}	I-IV	I-IV
	Rated Mains Voltages ≤ 300 V_{RMS}	I-III	I-IV
	Rated Mains Voltages ≤ 400 V_{RMS}	I-II	I-III
	Rated Mains Voltages ≤ 600 V_{RMS}	I-II	I-III

Table 8. IEC 60747-5-2 Insulation Characteristics for Si86xxxx*

Parameter	Symbol	Test Condition	Characteristic		Unit
			WB SOIC-16	NB SOIC-16 SOIC-8	
Maximum Working Insulation Voltage	V_{IORM}		1200	630	Vpeak
Input to Output Test Voltage	V_{PR}	Method b1 (V_{IORM} x 1.875 = V_{PR}, 100% Production Test, t_m = 1 sec, Partial Discharge < 5 pC)	2250	1182	
Transient Overvoltage	V_{IOTM}	t = 60 sec	6000	6000	Vpeak
Pollution Degree (DIN VDE 0110, Table 1)			2	2	
Insulation Resistance at T_S, V_{IO} = 500 V	R_S		$>10^9$	$>10^9$	Ω

***Note:** Maintenance of the safety data is ensured by protective circuits. The Si86xxxx provides a climate classification of 40/125/21.

Table 9. IEC Safety Limiting Values[1]

Parameter	Symbol	Test Condition	Max			Unit
			WB SOIC-16	NB SOIC-16	NB SOIC-8	
Case Temperature	T_S		150	150	150	°C
Safety Input, Output, or Supply Current	I_S	θ_{JA} = 100 °C/W (WB SOIC-16), 105 °C/W (NB SOIC-16), 140 °C/W (NB SOIC-8), V_I = 5.5 V, T_J = 150 °C, T_A = 25 °C	220	215	160	mA
Device Power Dissipation[2]	P_D		415	415	150	mW

Notes:
1. Maximum value allowed in the event of a failure; also see the thermal derating curve in Figures 4, 5 and 6.
2. The Si86xx is tested with VDD1 = VDD2 = 5.5 V, T_J = 150 ºC, C_L = 15 pF, input a 150 Mbps 50% duty cycle square wave.