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SiI9127A/SiI1127A HDMI Receiver with Deep Color Output

Data Sheet

SiI-DS-1059-D

May 2017

Contents

Figures

Tables

Acronyms in This Document

A list of acronyms used in this document.

Acronym	Definition
ACR	Audio Clock Regeneration
AVI	Auxiliary Video Information
CBUS	Control Bus
CEC	Consumer Electronics Control
CPI	CEC Programming Interface
CPU	Central Processing Unit
CSC	Color Space Converter
DDC	Display Data Channel
DSC	Display Stream Compression
DSD	Direct-Stream Digital
DTV	Digital Television
EDDC	Enhanced Display Data Channel
EDID	Extended Display Identification Data
ESD	Electrostatic Discharge
GPIO	General Purpose Input/Output
HDCP	High-bandwidth Digital Content Protection
HDMI	High-Definition Multimedia Interface
HPD	Hot Plug Detect
I^2C	Inter-Integrated Circuit
I^2S	Inter-IC Sound, Integrated Interchip Sound
KSV	Key Selection Vector
NVM	Non Volatile Memory
PCM	Pulse Code Modulation
S/PDIF	Sony/Philips Digital Interface Format
TMDS	Transition Minimized Differential Signaling
TQFP	Thin Quad Flat Pack

1. General Description

The SiI9127A/SiI1127A HDMI® Receiver with Deep Color Outputs from Lattice Semiconductor Corporation is a 2-port receiver that allows DTVs that can display 10/12-bit color depth to provide the highest quality protected digital audio and video over a single cable. The SiI9127A/SiI1127A receiver can receive Deep Color video up to 12-bit, 1080p at 60 Hz. Efficient color space conversion receives RGB or YCbCr video data and sends either standard-definition or high-definition RGB or YCbCr formats.

The SiI9127A/SiI1127A receiver supports the extended gamut YCC or xvYCC color space described in the IEC 61966-2-4 Specification, which supports approximately 1.8 times the number of colors as the RGB color space. The xvYCC color space also makes full use of the range provided by the standard 8-bit resolution per pixel format.

The SiI9127A receiver is preprogrammed with High-bandwidth Digital Content Protection (HDCP) keys and contains an integrated HDCP decryption engine for receiving protected audio and video content. This set of keys helps reduce programming overhead, lowers manufacturing costs, and provides the highest level of security.

The SiI1127A receiver is functionally equivalent to the SiI9127A receiver except that the HDCP keys are not preprogrammed, therefore SiI1127A does not support HDCP decryption.

An integrated Extended Display Identification Data (EDID) block stored in non-volatile memory (NVM) can be programmed at the time of manufacture using the local I^2C bus. On-board RAM can also be loaded through the I^2C bus with EDID data from the system microcontroller during initialization if the EDID content of the NVM is not used.

The EDID is reflected on the two HDMI ports through the DDC bus. The device allows different EDID formats to be mixed in an application. Having the flexibility to provide EDID content from the sources described above or from external ROM can eliminate up to two EDID ROMs and save board space.

Flexible power management provides extremely low standby power consumption. Standby power can be supplied from an HDMI 5 V signal or from a separate standby power pin. If the NVM stores the EDID, only the 5 V power from the source device is needed to read the EDID.

1.1. Inputs

- Two HDMI/DVI-compatible ports
- The TMDS™ core runs at 25 MHz–225 MHz
- Dynamic cable equalization automatically detects the equalization required for the incoming signal

1.2. Digital Video Output

- xvYCC to extended RGB
- 36-bit RGB/YCbCr 4:4:4
- 16/20/24-bit YCbCr 4:2:2
- 8/10/12-bit YCbCr 4:2:2 (ITU BT.656)
- True 12-bit accurate output data using an internal 14-bit wide processing path
- Drive strength is programmable from 2 mA to 14 mA

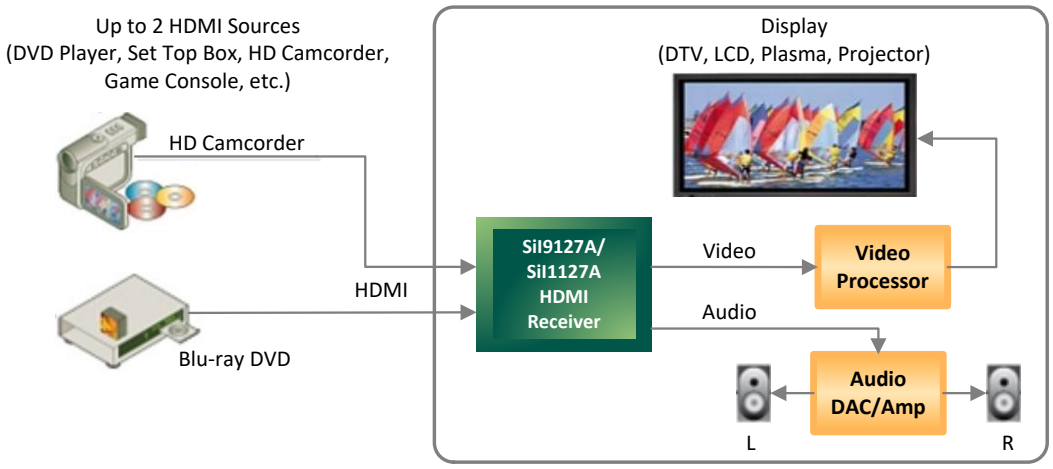


Figure 1.1. Digital Television System Diagram

1.3. Digital Audio Interface

- Sends and receives up to two channels of uncompressed digital audio at the rate of 192 kHz.
- I^2S output with one data signal for stereo formats
- S/PDIF output supports PCM, Dolby Digital, DTS digital audio transmission with a 32 kHz–192 kHz Fs sample rate
- Intelligent audio mute capability avoids pops and noise with automatic soft mute and unmute
- IEC60958 or IEC61937 compatible

1.4. Consumer Electronic Control

- Consumer Electronics Control (CEC) interface incorporates an HDMI CEC I/O
- An integrated CEC Programming Interface (CPI) relieves the burden of the microcontroller having to write low-level commands
- Automatic Feature Abort response for unsupported commands
- Automatic Message Retry on transmit

1.5. System Applications

The SiI9127A/SiI1127A receiver is designed for digital televisions that require support for HDMI Deep Color. The device allows receipt of 10/12-bit color depth up to 1080p resolutions. A single receiver chip provides two HDMI input ports. The video output interfaces to a video processor and the audio output can interface directly to an audio DAC or an audio DSP for further processing as shown in Figure 3.1.

1.6. Package

14 mm × 14 mm 128-pin TQFP package with an exposed pad (ePad).

2. Product Family

Table 2.1 summarizes the functional differences among the SiI9127A/SiI1127A, SiI9125, SiI9135A, SiI9223A and the SiI9233A receivers.

Table 2.1. Summary of New Features

Feature	SiI9125	SiI9127A/SiI1127A	SiI9135A	SiI9223A	SiI9233A
HDMI Input Connections					
TMDS Input Ports	2	2	2	4	4
Color Depth	8/10/12-bit	8/10/12-bit	8/10/12-bit	8/10/12-bit	8/10/12-bit
DDC Input Ports	2	2	2	4	4
Maximum TMDS Input Clock	225 MHz	225 MHz	225 MHz	225 MHz	225 MHz
Video Output					
Digital Video Output Ports	1	1	1	1	1
Maximum Output Pixel Clock	165 MHz	165 MHz	165 MHz	165 MHz	165 MHz
Maximum Output Bus Width	36	36	36	36	36
Audio Formats					
S/PDIF Output Ports	1	1	1	1	1
I²S Output	2 channel	2 channel	8 channel	2 channel	8 channel
DSD Output	2 channel	NA	6 channel	NA	8 channel
High Bit Rate Audio Support Compressed DTS-HD and Dolby True-HD	No	No	Yes	No	Yes
Maximum Audio Sample Rate (Fs)	192 kHz	192 kHz	192 kHz	192 kHz	192 kHz
Video Processing					
Color Space Converter	RGB to/from YCbCr	RGB to/from YCbCr xvYCC to RGB	RGB to/from YCbCr	RGB to/from YCbCr xvYCC to RGB	RGB to/from YCbCr xvYCC to RGB
Pixel Clock Divider	÷ 4, ÷ 2	÷ 4, ÷ 2	÷ 4, ÷ 2	÷ 4, ÷ 2	÷ 4, ÷ 2
Digital Video Bus Mapping	swap Cb, Cr pins	swap Cb, Cr pins	swap Cb, Cr pins	swap Cb, Cr pins	swap Cb, Cr pins
Other Features					
Local fixed I²C Device Address[1]	0x60/0x68 or 0x62/0x6A	0x60/0x68 or 0x62/0x6A	0x60/0x68 or 0x62/0x6A	0x60/0x68 or 0x62/0x6A	0x60/0x68 or 0x62/0x6A
Programmable I²C Device Address[1]	NA	0x64, 0xC0, 0xE0	NA	0x64, 0xC0, 0xE0	0x64, 0xC0, 0xE0
Reserved I²C Device Address[2]	NA	0x90, 0xD0, 0xE6	NA	0x90, 0xD0, 0xE6	0x90, 0xD0, 0xE6
3D Support	No	Yes	No	Yes	Yes
CEC	No	Yes	No	Yes	Yes
EDID	No	NVRAM	No	NVRAM	NVRAM
HDCP Repeater Support	No	No	Yes	No	Yes
Interlaced Format Detection Pin	Yes	Yes	Yes	Yes	Yes
Package	144-pin TQFP ePad	128-pin TQFP ePad	144-pin TQFP ePad	144-pin TQFP ePad	144-pin TQFP ePad

Notes:

1. Refer to the SiI9223A/SiI9233A/SiI9127A/SiI1127A HDMI Receivers Programmer Reference for a description of these I²C register addresses.
2. These are reserved I²C register addresses which are within the I²C register address map of the chip. Do not access these registers on the chip and do not use these addresses for other devices, in the system which use the same I²C bus.

3. Functional Description

The SiI9127A/SiI1127A receiver provides a complete solution for receiving HDMI-compliant digital audio and video. Specialized audio and video processing is available within the receiver to add HDMI capability to consumer electronics such as DTVs. Figure 3.1 shows the SiI9127A/SiI1127A receiver incorporated into a digital television reciever. Figure 3.2 on the next page shows the functional blocks of the chip. The receiver supports two HDMI input ports. Only one port can be active at any time.

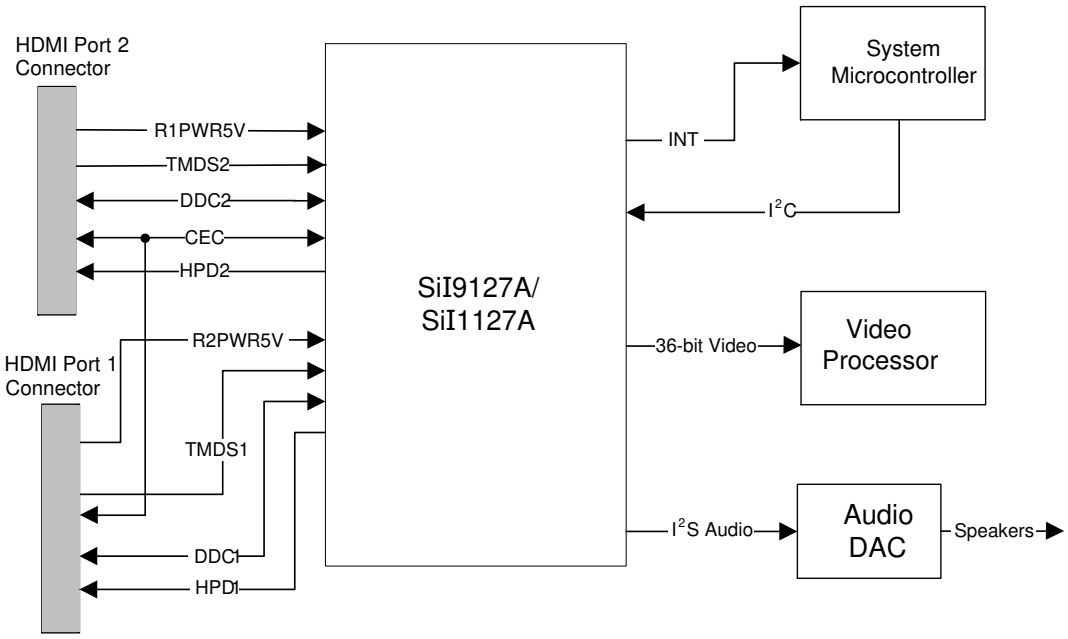


Figure 3.1. Digital Television Receiver Block Diagram

3.1. TMDS Digital Cores

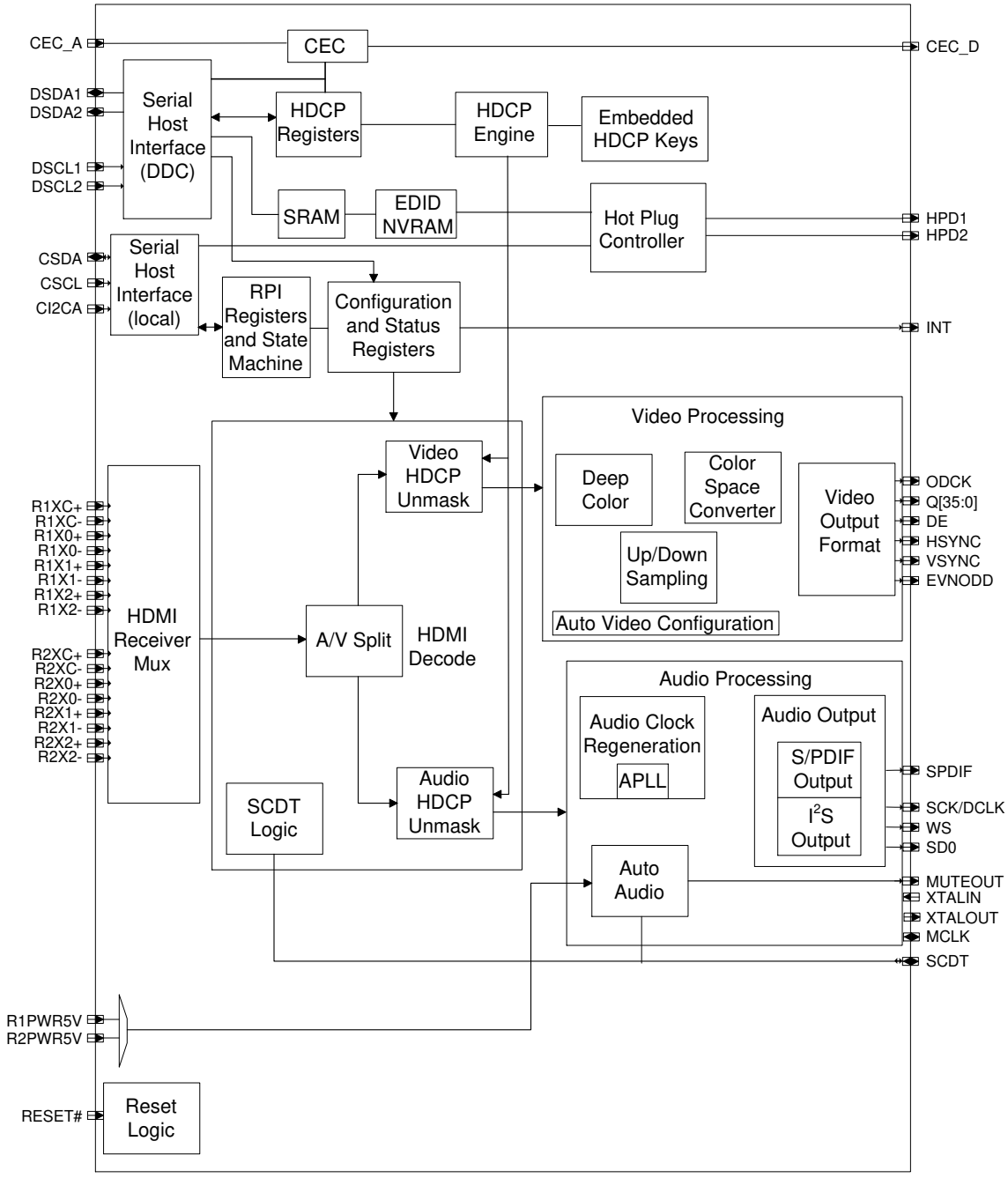
The TMDS digital core is the latest generation core that supports HDMI and the ability to carry 10/12-bit color depth. The core can receive TMDS data at up to 225 MHz. Each core performs 10-to-8 bit TMDS decoding on the video data and 10-to-4 bit TMDS decoding on the audio data received from the three TMDS differential data lines along with a TMDS differential clock. The TMDS core can sense a stopped clock or stopped video and software can put the receiver into power-down mode.

3.1.1. Active Port Detection and Selection

Only one port can be active at a time, under control of the receiver firmware. Active TMDS signaling can arrive at both ports, but only one has internal circuitry enabled. The firmware in the display controls these states using register settings.

Other control signals are associated with the TMDS signals on each HDMI port. The receiver can monitor the +5 V supply from each attached host. The firmware can poll registers to check which ports are connected. The firmware also controls functional connection to one of the two E-DDC buses, enabling one while disabling the other. An attached host determines the active status of an attached HDMI device by polling the E-DDC bus to the device.

Refer to the SiI-PR-1033 Programmer Reference (see Lattice Semiconductor Documents on page 74) for a complete description of port detection and selection. *The Programmer's Reference requires an NDA with Lattice Semiconductor.*



Note: HDCP blocks do not apply to the SiI1127A receiver.

Figure 3.2. Functional Block Diagram

3.2. HDCP Decryption Engine/XOR Mask

The HDCP decryption engine contains all the necessary logic to decrypt the incoming audio and video data. The decryption process is entirely controlled by the host-side microcontroller/microprocessor through a set sequence of register reads and writes through the DDC channel. Preprogrammed HDCP keys and Key Selection Vector (KSV) stored in the on-chip non-volatile memory are used in the decryption process. A resulting calculated value is applied to an XOR mask during each clock cycle to decrypt the audio and video data.

3.2.1. HDCP Embedded Keys

The SiI9127A receiver comes preprogrammed with a set of production HDCP keys stored on-chip in non-volatile memory. System manufacturers do not need to purchase key sets from the Digital Content Protection LLC. All purchasing, programming, and security for the HDCP keys is handled by Lattice Semiconductor. The preprogrammed HDCP keys provide the highest level of security, as keys cannot be read out of the device after they are programmed. Before receiving samples of the receiver, customers must sign the HDCP license agreement available from Digital Content Protection, LLC, or have a special NDA with Lattice Semiconductor.

The SiI1127A receiver does not come preprogrammed with a set of production HDCP keys stored on-chip in non-volatile memory.

3.3. Data Input and Conversion

3.3.1. Mode Control Logic

The mode control logic determines if the decrypted data is video, audio, or auxiliary information, and directs it to the appropriate logic block.

3.3.2. Video Data Conversion and Video Output

The SiI9127A/SiI1127A receiver can output video in many different formats (see the examples in Table 3.1) and can process the video data before it is sent, as shown in Figure 3.3. It is possible to bypass each of the processing blocks by setting the appropriate register bits.

Table 3.1. Digital Video Output Formats

Color Space	Video Format	Bus Width	HSYNC/ VSYNC	Output Clock (MHz)								Notes
				480i/576i[2, 3]	480p	XGA	720p	1080i	SXGA	1080p	UXGA	
RGB	4:4:4	36	Separate	27	27	65	74.25	74.25	108	148.5	162	—
		30	Separate	27	27	65	74.25	74.25	108	148.5	162	—
		24	Separate	27	27	65	74.25	74.25	108	148.5	162	—
		12/15/18	Separate	27	27	65	74.25	74.25	—	—	—	4
YCbCr	4:4:4	36	Separate	27	27	65	74.25	74.25	108	148.5	162	—
		30	Separate	27	27	65	74.25	74.25	108	148.5	162	—
		24	Separate	27	27	65	74.25	74.25	108	148.5	162	—
		12/15/18	Separate	27	27	65	74.25	74.25	—	—	—	4
	4:2:2	16/20/24	Separate	27	27	—	74.25	74.25	—	148.5	162	—
		16/20/24	Embedded	27	27	—	74.25	74.25	—	148.5	162	1
		8/10/12	Separate	27	54	—	148.5	148.5	—	—	—	—
		8/10/12	Embedded	27	54	—	148.5	148.5	—	—	—	1

Notes:

1. Embedded syncs use SAV/EAV coding.
2. 480i and 576i modes can output a 13.25 MHz clock using the internal clock divider.
3. Output clock frequency depends on programming of internal registers. Differential TMDS clock is always 25 MHz or faster.
4. Output clock supports 12/15/18-bit mode by using both edges.

Color Range Scaling

The color range depends on the video format, according to the CEA-861D specification. In some applications the 8-bit input range uses the entire span of 0x00 (0) to 0xFF (255) values. In other applications the range is scaled narrower. The receiver cannot detect the incoming video data range and there is no required range specification in the HDMI AVI packet. The device chooses scaling depending on the detected video format. 10 and 12-bit color range scaling are both handled the same way. Refer to the SiI-PR-1033 Programmer Reference for more details.

When the receiver outputs embedded syncs (SAV/EAV codes), it also limits the YCbCr data output values to 1 to 254.

Up Sample/Down Sample

Additional logic can convert from 4:2:2 to 4:4:4 (8/10/12-bit) or from 4:4:4 (8/10/12-bit) to 4:2:2 YCbCr format. All processing is done with 14 bits of accuracy for true 12-bit data.

3.3.3. Deep Color Support

The HDMI 1.3 Specification introduces Color Depth modes greater than 24 bits, known as Deep Color modes, to the HDMI system architecture. The Deep Color modes employ a new pixel packing scheme to enable the extra bits of higher color depth data to be carried over the existing TMDS data encoding scheme. Currently, three Deep Color modes are defined: 30-bit, 36-bit, and 48-bit. The SiI9127A/SiI1127A receiver supports two of these three Deep Color modes; 30-bit, and 36-bit modes. In addition, each Deep Color mode is supported up to 1080p HD format.

For Deep Color modes, the TMDS clock is run faster than the pixel clock in order to create extra bandwidth for the additional bits of the higher color depth data. The increase in the TMDS clock is by the ratio of the pixel size to 24 bits, as follows:

- 30-bit mode: TMDS clock = 1.25x pixel clock (5:4)
- 36-bit mode: TMDS clock = 1.5x pixel clock (3:2)

Because the receiver supports 36-bit mode at 1080p, the highest TMDS clock rate it supports is therefore 225 MHz. When in Deep Color mode, the transmitter periodically sends a General Control Packet with the current color depth and pixel packing phase information to the receiver. The receiver captures the color depth information in a register, which the firmware can then use to set the appropriate clock divider to recover the pixel clock and data.

3.3.4. xvYCC

The SiI9127A/SiI1127A receiver adds support for the extended gamut xvYCC color space; this extended format has roughly 1.8 times more colors than the RGB color space. The use of the xvYCC color space is made possible because of the availability of LED and laser based light sources for the next generation displays. This format also makes use of the full range of values 1 to 254 in an 8-bit space instead of 16 to 235 in the RGB format. The use of xvYCC along with Deep Color helps in reducing color banding and allows display of a larger range of colors than is currently possible.

3.3.4.1. Color Space Conversion

Color space converter (CSC) blocks are provided to convert RGB data to Standard-Definition (ITU.601) or High-Definition (ITU.709) YCbCr formats, and vice-versa. To support the latest extended-gamut xvYCC displays, the SiI9127A/SiI1127A receiver implements color space converter blocks to convert RGB data to extended-gamut Standard-Definition (ITU.601) or High-Definition (ITU.709) xvYCC formats, and vice-versa.

RGB to YCbCr

The RGB→YCbCr color space converter (CSC) can convert from video data RGB to standard definition (ITU.601) or to high definition (ITU.709) YCbCr formats. The HDMI AVI packet defines the color space of the incoming video.

YCbCr to RGB

The YCbCr→RGB color space converter is available to interface to MPEG decoders with RGB-only inputs. The CSC can convert from YCbCr in standard-definition (ITU.601) or high-definition (ITU.709) to RGB.

3.4. 3D Video Formats

The SiI9127A/SiI1127A receiver has support for the 3D video modes described in the HDMI 1.4 Specification. All modes support RGB 4:4:4, YCbCr 4:4:4, and YCbCr 4:2:2 color formats and 8-, 10-, and 12-bit data width per color component. Table 3.2 on the next page shows only the maximum possible resolution with a given frame rate; for example, Side-by-Side (Half) mode is defined for 1080p60, which implies that 720p60 and 480p60 are also supported. Furthermore, a frame rate of 24 Hz also means that a frame rate of 23.98 Hz is supported and a frame rate of 60 Hz also means a frame rate of 59.94 Hz is supported. The input pixel clock changes accordingly.

When using Side-by-Side formats the use of 4:2:2 to 4:4:4 up-sampling and 4:4:4 to 4:2:2 down-sampling should not be enabled as it may result in visible artifacts.

Video processing should be bypassed in the case of L + depth format.

Table 3.2. Supported 3D Video Formats

3D Format	Extended Definition	Resolution	Frame Rate (Hz)	Input Pixel Clock (MHz)
Frame Packing	—	1080p	24	148.5
		720p	50 / 60	
	interlaced	1080i	50 / 60	
L + depth	—	1080p	24	
		720p	50 / 60	
Side-by-Side	full	1080p	24	
		720p	50 / 60	
	half	1080p	50 / 60	
		1080i	50 / 60	74.25

Default Video Configuration

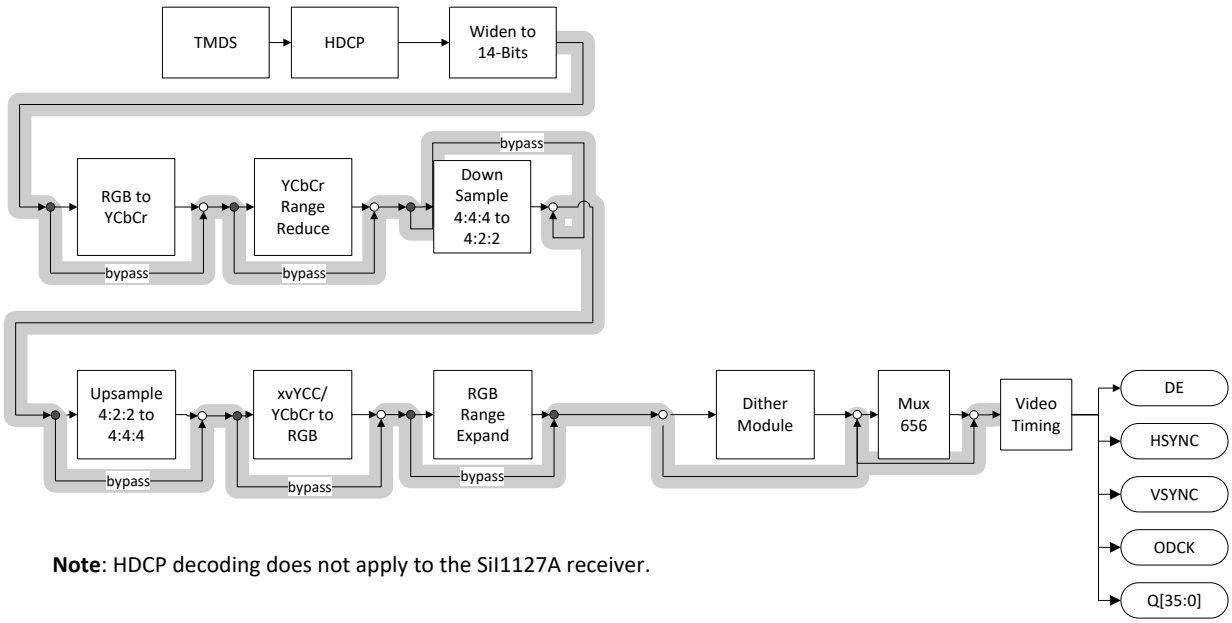
After hardware reset, the SiI9127A/SiI1127A chip is configured in its default mode. This mode is summarized in Table 3.3. For more details and for a complete register listing, refer to the SiI-PR-1033 Programmer Reference.

Table 3.3. Default Video Processing

Video Control	Default after Hardware Reset
HDCP Decryption	HDCP decryption is OFF
Color Space Conversion	No color space conversion
Color Space Selection	BT.601 selected
Color Range Scaling	No range scaling
Upsampling/Downsampling	No upsampling or downsampling
HSYNC & VSYNC Timing	No inversions of HSYNC or VSYNC
Data Bit Width	Uses 8-bit data
Pixel Clock Replication	No pixel clock replication
Power Down	Everything is powered down

Notes:

1. The receiver assumes DVI mode after reset, which is RGB 24-bit 4:4:4 video with a range of 0–255.
2. HDCP decryption is not supported on the SiI1127A receiver.



Note: HDCP decoding does not apply to the SiI1127A receiver.

Figure 3.3. Default Video Processing Path

3.4.1. Automatic Video Configuration

The SiI9127A/SiI1127A receiver adds automatic video configuration to simplify the firmware task of updating the video path whenever the incoming video changes format. Bits in the HDMI Auxiliary Video Information (AVI) InfoFrame are used to reprogram the registers in the video path.

Table 3.4. AVI InfoFrame Video Path Details

AVI Byte 1 Bits [6:5]		AVI Byte 2 Bits [7:6]		AVI Byte 5 Bits [3:0]	
Y[1:0]	Color Space	C[1:0]	Colorimetric	PR[3:0]	Pixel Repetition
00	RGB 4:4:4	00	No Data	0000	No repetition
01	YCbCr 4:2:2	01	ITU 601	0001	Pixel sent 2 times
10	YCbCr 4:4:4	10	ITU 709	0010	Pixel sent 3 times
11	Future	11	Extended Colorimetry Information Valid	0011	Pixel sent 4 times
				0100	Pixel sent 5 times
				0101	Pixel sent 6 times
				0110	Pixel sent 7 times
				0111	Pixel sent 8 times
				1000	Pixel sent 9 times
				1001	Pixel sent 10 times

Notes:

1. The Auto Video Configuration assumes that the AVI information is accurate. If information is not available, then the receiver must choose the video path based on measurement of the incoming resolution.
2. Refer to EIA/CEA-861D Specification for details.
3. The SiI9127A/SiI1127A device can support only pixel replication modes 0b0000, 0b0001, and 0b0011. Other modes are unsupported and can result in an unpredictable behavior.

The format of the digital video output bus can be automatically configured to many different formats by programming the Auto Output Format Register. The available formats are listed in Table 3.5. For detailed definitions of how to set this register, refer to the SiI-PR-1033 Programmer Reference.

Table 3.5. Digital Output Formats Configurable through Auto Output Format Register

Digital Output Formats			
Color	Width	MUX	Sync
RGB	4:4:4	N	Separate
YCbCr	4:4:4	N	Separate
YCbCr	4:2:2	N	Separate
YCbCr	4:2:2	Y	Separate
YCbCr	4:2:2	Y	Embedded

3.5. Audio Data Output Logic

The SiI9127A/SiI1127A receiver can send digital audio over S/PDIF and two-channel I^2S outputs.

3.5.1. S/PDIF

The S/PDIF stream can carry 2-channel uncompressed PCM data (IEC 60958). The audio data output logic forms the audio data output stream from the decoded HDMI audio packets. The S/PDIF output supports audio sampling rates from 32 kHz to 192 kHz. A separate master clock output (MCLK), coherent with the S/PDIF output, is provided for time-stamping purposes. *Coherent* means that the MCLK and S/PDIF are created from the same clock source.

3.5.2. I^2S

The I^2S bus format is programmable through registers, to allow interfacing with I^2S audio DACs or audio DSPs with I^2S inputs. Refer to the SiI-PR-1033 Programmer Reference for the different options on the I^2S bus. Additionally, the MCLK (audio master clock) frequency is selectable to be an integer multiple of the audio sample rate F_s.

MCLK frequencies support various audio sample rates as shown in Table 3.6 on the next page.

Table 3.6. Supported MCLK Frequencies

Multiple of Fs	Audio Sample Rate, Fs: I²S and S/PDIF Supported Rates						
	32 kHz	44.1 kHz	48 kHz	88.2 kHz	96 kHz	176.4 kHz	192 kHz
128	4.096 MHz	5.645 MHz	6.144 MHz	11.290 MHz	12.288 MHz	22.579 MHz	24.576 MHz
192	6.144 MHz	8.467 MHz	9.216 MHz	16.934 MHz	18.432 MHz	33.868 MHz	36.864 MHz
256	8.192 MHz	11.290 MHz	12.288 MHz	22.579 MHz	24.576 MHz	45.158 MHz	49.152 MHz
384	12.288 MHz	16.934 MHz	18.432 MHz	33.864 MHz	36.864 MHz		
512	16.384 MHz	22.579 MHz	24.576 MHz	45.158 MHz	49.152 MHz		

3.6. Control and Configuration

3.6.1. Register/Configuration Logic

The Register/Configuration Logic block incorporates all the registers required for configuring and managing the features of the SiI9127A/SiI1127A receiver. These registers are used to perform HDCP authentication; audio, video, or auxiliary format processing; CEA-861B InfoFrame Packet format; and power-down control.

The registers are accessible from one of the two serial ports. The first port is the DDC port, which is connected through the HDMI cable to the HDMI host. It is used to control the receiver from the host system for HDCP operation. The second port is the local I²C port, which is used to control the receiver from the display system. This is shown in Figure 3.4. The Local Bus accesses the General Registers and the Common Registers. The DDC Bus accesses the HDCP Operation registers and the Common Registers. The HDCP Operation registers are not applicable to the SiI1127A receiver.

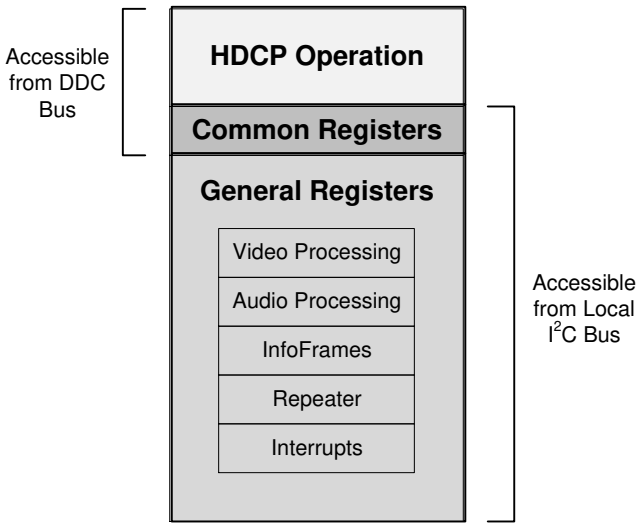


Figure 3.4. I²C Register Domains

3.6.2. I²C Serial Ports

The SiI9127A/SiI1127A receiver provides three I²C serial interfaces: two DDC ports to communicate back to the HDMI or DVI hosts, along with one I²C port for initialization and control by a local microcontroller in the display. Each interface is 5 V tolerant.

E-DDC Bus Interface to HDMI Host

The two DDC interfaces, DSDA1-2 and DSCL1-2, on the receiver are slave interfaces that can run up to 100 kHz. Each interface is connected to one E-DDC bus and is used for reading the integrated EDID in addition to HDCP authentication.

The SiI9127A/SiI1127A receiver is accessible on the E-DDC bus at device addresses 0xA0 for the EDID, and 0x74 for HDCP control. This feature complies with the HDCP Specification.

3.6.3. EDID FLASH and RAM Block

The EDID block consists of 512 bytes of RAM. Each port has a block of 256 bytes of RAM for EDID data. This feature allows simultaneous reads of both ports from two different source devices that are connected to the SiI9127A/SiI1127A device.

In addition to the RAM, the EDID block contains 256 bytes of FLASH that is shared by both ports. As a result, the timing information must be identical between both ports if the internal EDID is used. An additional area of FLASH contains unique CEC physical address and checksum values for each of the ports. This feature allows simultaneous reads of both ports from two different source devices if they are connected and attempt an EDID read at the same time. If independent EDIDs are required on any of the ports, a CPU can externally load the 256 bytes of RAM for that port, by using the local I^2C bus.

The internal EDID can be selected on a per-port basis using registers on the local I^2C bus. For example, Port 1 can use the internal EDID, and Port 2 can use a discrete EEPROM for the EDID.

3.6.4. CEC Interface

The Consumer Electronics Control (CEC) Interface block provides CEC electrically compliant signals between CEC devices and a CEC master. It allows products to meet the electrical specifications of CEC signaling by translating the LVTTL signals of an external microcontroller (CEC host-side or transmit-side) to CEC signaling levels for CEC devices at the receive side, and vice versa.

Additionally, a CEC controller compatible with the Lattice Semiconductor CEC Programming Interface (CPI) is included on-chip. This CEC controller has a high-level register interface accessible through the I^2C interface which can be used to send and receive CEC commands. This controller makes CEC control very easy and straightforward, and removes the burden of having a host CPU perform these low-level transactions on the CEC bus. As a result, CEC pass-through mode is neither required nor supported.

I^2C Interface to Display Controller

The Controller I^2C interface (CSDA, CSCL) on the SiI9127A/SiI1127A receiver is a slave interface capable of running up to 400 kHz. This bus is used to configure the chip by reading or writing to the appropriate registers. It is accessible on the local I^2C bus at two device addresses. Refer to the SiI-PR-1033 Programmer Reference for more information.

3.6.5. Standby and HDMI Port Power Supplies

The receiver incorporates a power island that continues to supply power to the EDID memory, the DDC ports, and the CEC bus when power is removed from the VCC pins, as long as power continues to be provided through at least one connected HDMI cable or by system standby power. Refer to Figure 3.5 on the next page. The internal power multiplexer selects power from either SBVCC5, if it is available, or from one of the R*n*PWR5V pins.

The power island results in an extremely low power standby mode, but allows the EDID to be readable and the CEC controller to be functional. No damage will occur to the device when in this mode.

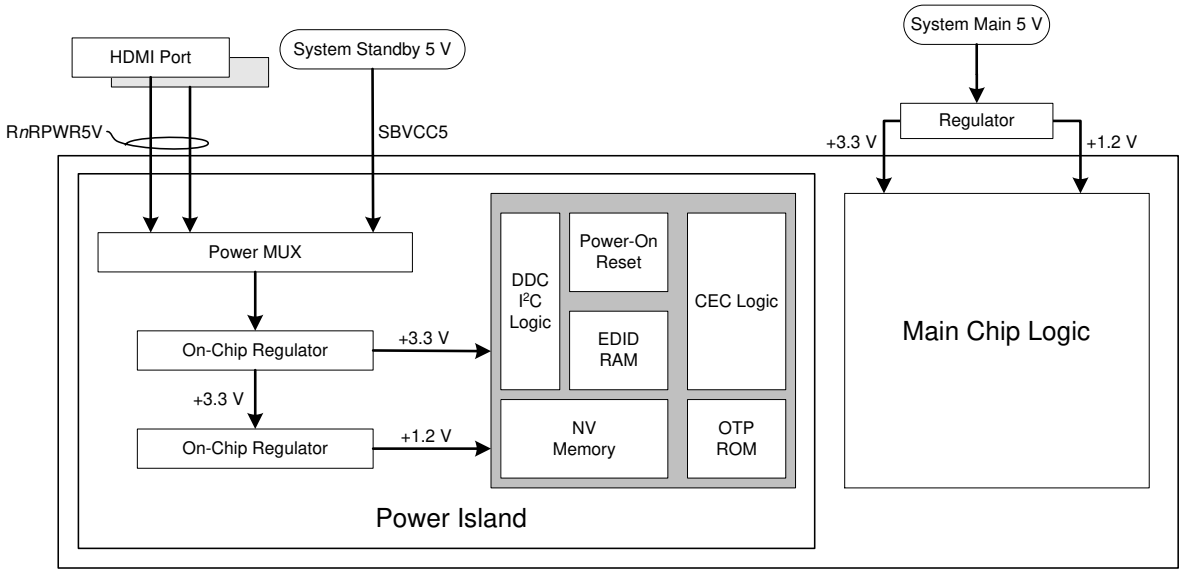


Figure 3.5. Power Island

4. Electrical Specifications

4.1. Absolute Maximum Conditions

Symbol	Parameter	Min	Typ	Max	Units	Note
IOVCC33	I/O Pin Supply Voltage	–0.3	—	4.0	V	1, 2, 3
AVCC12	TMDS Analog Supply Voltage	–0.3	—	1.9	V	1, 2
AVCC33	TMDS Analog Supply Voltage	–0.3	—	4.0	V	1, 2
APVCC12	Audio PLL Supply Voltage	–0.3	—	1.9	V	1, 2
CVCC12	Digital Core Supply Voltage	–0.3	—	1.9	V	1, 2
XTALVCC33	ACR PLL Crystal Oscillator Supply Voltage	–0.3	—	4.0	V	1, 2
SBVCC5	Standby Supply Voltage	–0.3	—	5.7	V	1,2
V_I	Input Voltage	–0.3	—	IOVCC33 + 0.3	V	1, 2
$V_{5V\text{-}Tolerant}$	Input Voltage on 5 V tolerant Pins	–0.3	—	5.5	V	5
T_J	Junction Temperature	—	—	125	°C	—
T_{STG}	Storage Temperature	–65	—	150	°C	—

Notes:

1. Permanent device damage can occur if absolute maximum conditions are exceeded.
2. Functional operation should be restricted to the conditions described in the Normal Operating Conditions section on page 20.
3. Voltage undershoot or overshoot cannot exceed absolute maximum conditions.
4. Refer to the SiI9127A/SiI1127A receiver Qualification Report for information on ESD performance.
5. All VCC supplies must be available to the device. If the device is not powered and 5 V is applied to these inputs, damage can occur.

4.2. Normal Operating Conditions

Symbol	Parameter	Min	Typ	Max	Units	Note
IOVCC33	I/O Pin Supply Voltage	3.13	3.3	3.47	V	1, 4
AVCC12	TMDS Analog Supply Voltage	1.14	1.2	1.26	V	3
AVCC33	TMDS Analog Supply Voltage	3.13	3.3	3.47	V	1, 6
APVCC12	Audio PLL Supply Voltage	1.14	1.2	1.26	V	—
CVCC12	Digital Core Supply Voltage	1.14	1.2	1.26	V	2
XTALVCC33	ACR PLL Crystal Oscillator Supply Voltage	3.13	3.3	3.47	V	4
SBVCC5	Standby Supply Voltage	4.75	5.0	5.25	V	10
R*n*PWR5V	DDC I^2C I/O Reference Voltage	4.7	5.00	5.3	V	11
DIFF33	Difference between two 3.3-V Power Pins	—	—	1.0	V	4
DIFF12	Difference between two 1.2-V Power Pins	—	—	1.0	V	4
DIFF3312	Difference between any 3.3-V and 1.2-V Pin	–1.0	—	2.6	V	4, 5
V_{CCN}	Supply Voltage Noise	—	—	100	mV_{P-P}	7
T_A	Ambient Temperature (with power applied)	0	25	70	°C	—
Θ_{ja}	Ambient Thermal Resistance (Theta JA)	—	—	27	°C/W	—

Notes:

1. IOVCC33 and AVCC33 pins should be controlled from one power source.
2. CVCC12 should be controlled from one power source.
3. AVCC12 pin should be regulated.
4. Power supply sequencing must guarantee that power pins stay within these limits of each other. See Figure 5.2.
5. No 1.2 V pin can be more than DIFF3312[min] higher than any 3.3 V pin. No 3.3 V pin can be more than DIFF3312[max] higher than any 1.2 V pin.
6. The HDMI Specification requires termination voltage (AVCC33) to be controlled to 3.3 V±5%. The SiI9127A/SiI1127A receiver tolerates a wider range of ±300 mV.
7. The supply voltage noise is measured at test point VCCTP in Figure 4.1. The ferrite bead provides filtering of power supply noise. The figure is representative and applies to other VCC pins as well.
8. Airflow at 0 m/s.
9. The schematics on page 65 show decoupling and power supply regulation.
10. SBVCC5V should provide a stable 5 V before any other VCC is applied to the device; see the Power Supply Sequencing section on page 28.
11. Maximum current draw from this source is 50 mA. There is no power-on sequence requirement for this source.

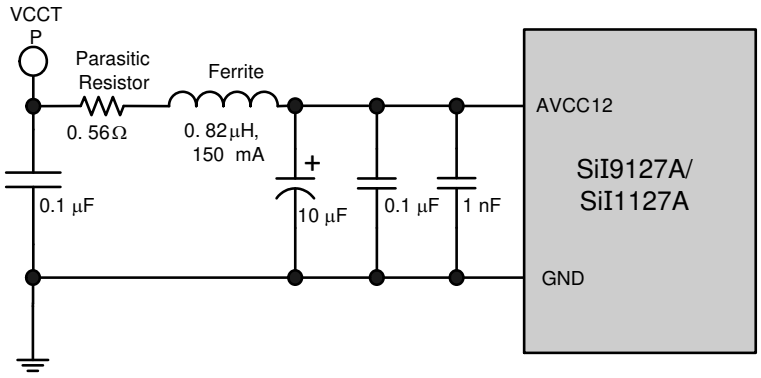


Figure 4.1. Test Point VCCTP for VCC Noise Tolerance Specification

Notes:

1. The Ferrite (0.82 µH, 150 mA) attenuates the PLL power supply noise at 10 kHz and above.
2. The optional parasitic resistor minimizes the peaking. The typical value used here is 0.56 Ω. 1 Ω is the maximum.

4.3. DC Specifications

4.3.1. Digital I/O Specifications

Symbol	Parameter	Pin Type[3]	Conditions[2]	Min	Typ	Max	Units	Note
V_{IH}	HIGH-level Input Voltage	LVTTL	—	2.0	—	—	V	—
V_{IL}	LOW-level Input Voltage	LVTTL	—	—	—	0.8	V	—
V_{TH+}	LOW to HIGH Threshold RESET # Pin	Schmitt	—	1.46	—	—	V	5
V_{TH-}	HIGH to LOW Threshold RESET# Pin	Schmitt	—	—	—	0.96	V	5
DDC V_{TH+}	LOW to HIGH Threshold DSDA0, DSDA1, DSCL0, and DSCL1 pins.	Schmitt	—	3.0	—	—	V	—
DDC V_{TH-}	HIGH to LOW Threshold DSDA0, DSDA1, DSCL0, and DSCL1 pins.	Schmitt	—	—	—	1.5	V	—
Local I^2C V_{TH+}	LOW to HIGH Threshold CSCL and CSDA pins	Schmitt	—	2.1	—	—	V	11, 13
Local I^2C V_{TH-}	HIGH to LOW Threshold CSCL and CSDA pins	Schmitt	—	—	—	0.86	V	11, 13
V_{OH}	HIGH-level Output Voltage	LVTTL	—	2.4	—	—	V	10
V_{OL}	LOW-level Output Voltage	LVTTL	—	—	—	0.4	V	10
I_{OL}	Output Leakage Current	—	High Impedance	–10	—	10	µA	—
V_{ID}	Differential Input Voltage	—	—	75	250	780	mV	4
I_{OD4}	4 mA Digital Output Drive	Output	V_{OUT} = 2.4 V	4	—	—	mA	1, 6, 7
			V_{OUT} = 0.4 V	4	—	—	mA	1, 6, 7
I_{OD8}	8 mA Digital Output Drive	Output	V_{OUT} = 2.4 V	8	—	—	mA	1, 6, 8
			V_{OUT} = 0.4 V	8	—	—	mA	1, 6, 8
I_{OD12}	12 mA Digital Output Drive	Output	V_{OUT} = 2.4 V	12	—	—	mA	1, 6, 9
			V_{OUT} = 0.4 V	12	—	—	mA	1, 6, 9
R_{PD}	Internal Pull Down Resistor	Outputs	IOVCC33 = 3.3 V	25	50	110	kΩ	1, 12
I_{OPD}	Output Pull Down Current	Outputs	IOVCC33 = 3.6 V	—	60	90	µA	1, 12
I_{IPD}	Input Pull Down Current	Input	IOVCC33 = 3.6 V	—	60	90	µA	1

Notes:

1. These limits are guaranteed by design.
2. Under normal operating conditions unless otherwise specified, including output pin loading C_L = 10 pF.
3. See the Pin Descriptions section on page 36 for pin type designations for all package pins.
4. Differential input voltage is a single-ended measurement, according to DVI Specification.
5. Schmitt trigger input pin thresholds V_{TH+} and V_{TH-} correspond to V_{IH} and V_{IL}, respectively.
6. Minimum output drive specified at ambient = 70 °C and IOVCC33 = 3.0 V. Typical output drive specified at ambient = 25 °C and IOVCC33 = 3.3 V. Maximum output drive specified at ambient = 0 °C and IOVCC33 = 3.6 V.
7. I_{OD4} Output applies to pins SPDIF, SCK, WS, SD[3:0], DCLK, INT, and CSDA.
8. I_{OD8} Output applies to pins DE, HSYNC, VSYNC, Q[35:0].and MCLK.
9. I_{OD12} Output applies to pin ODCK.
10. Note that the S/PDIF output drives LVTTL levels, not the low-swing levels defined by IEC958.
11. The SCL and SDA pins are not true open-drain buffers. When no VCC is applied to the chip, these pins can continue to draw a small current, and prevent the master IC from communicating with other devices on the I^2C bus. Therefore, do not power-down the SiI9127A/SiI1127A receiver (remove VCC) unless the attached I^2C bus is completely idle.
12. The chip includes an internal pull-down resistor on many of the output pins. When in the high-impedance state, these pins draw a pull- down current according to this specification when the signal is driven HIGH by another source device.
13. With –10% IOVCC33 supply, the HIGH-to-LOW threshold on DDC and I^2C bus is marginal. A –5% tolerance on the IOVCC33 power supply is recommended.

4.3.2. DC Power Supply Pin Specifications

Total Power versus Power-Down Modes

Symbol	Parameter	Mode	Frequency	Typ[3]			Max[4]			Units	Notes
				3.3 V	1.2 V	SBVCC5	3.3 V	1.2 V	SBVCC5		
I_{PDQ3}	Complete Power-Down Current	A	—				65	3	8	mA	1, 6
I_{PDS}	Sleep Power-down Current	B	27 MHz				68	15	8	mA	2, 7
			74.25 MHz				85	19	8	mA	
			150 MHz				74	19	8	mA	
			225 MHz				74	19	8	mA	
I_{STBY}	Standby Current	C	27 MHz				0	0	8	mA	2, 8
			74.25 MHz				0	0	8	mA	
			150 MHz				0	0	8	mA	
			225 MHz				0	0	8	mA	
I_{UNS}	Unselected Current	D	27 MHz	67	111	8	68	119	8	mA	2, 9
			74.25 MHz	70	173	8	72	180	8	mA	
			150 MHz	75	291	8	79	299	8	mA	
			225 MHz	78	313	8	79	315	8	mA	
I_{CCTD}	Full Power Digital Out Current	E	27 MHz	97	112	8	102	121	8	mA	2, 10
			74.25 MHz	158	175	8	167	177	8	mA	
			150 MHz	259	295	8	280	302	8	mA	
			225 MHz	335	321	8	366	326	8	mA	

Notes:

1. Power is not related to input TMDS clock (RxC) frequency because the selected TMDS port is powered down.
2. Power is related to input TMDS clock (RxC) frequency at the selected TMDS port. Only one port can be selected.
3. Typical power specifications measured with supplies at typical normal operating conditions, and a video pattern that combines gray scale, checkerboard and text.
4. Maximum power limits measured with supplies at maximum normal operating conditions, minimum normal operating ambient temperature, and a video pattern with single-pixel vertical lines.
5. Registers are always accessible on local I2C (CSDA/CSCL) without active link clock.
6. Power Down Mode A: Minimum power. Everything is powered off. Host sees no termination of TMDS signals on either TMDS port. I2C access is still available.
7. Power Down Mode B: Powers down TMDS core. CKDT remains enabled and state can be polled in register. Host device can sense TMDS termination.
8. Power Down Mode C: Power off to 3.3 V and 1.2 V supplies. Power on to SBVCC5 standby supply.
9. Power Down Mode D: Monitor SCDT on selected TMDS port with outputs in the high-impedance state. HDCP continues in the selected port, but the output of the receiver can be connected to a shared bus.
10. Digital Functional Mode E: Full operation on one port with digital outputs.

Power Down Mode Definitions

Mode		3.3 V Supply	1.2 V Supply	SBVCC5	Register Bit States				Description
					PDTOT#	PD_TMDS#	PD_AO#	PD_VO#	
A	Power Down	ON	ON	ON	0	1	1	1	Minimum power. Everything is powered off. Host sees no termination of TMDS signals on either TMDS port. I^2C access is still available.
B	Sleep Mode Power	ON	ON	ON	1	0	1	1	Powers down TMDS core. CKDT remains enabled and state can be polled in register. Host device can sense TMDS termination.
C	Standby Power	OFF	OFF	ON	1	1	1	1	Power off to 3.3 V and 1.2 V supplies. Power on to SBVCC5 standby supply.
D	Unselected Power	ON	ON	ON	1	1	0	0	Monitor SCDT on selected TMDS port with outputs in the high-impedance state. HDCP continues in the selected port, but the output of the receiver can be connected to a shared bus.
E	Digital	ON	ON	ON	1	1	1	1	Full operation on one port with digital outputs.

Notes:

1. PD Clks include PD_MCLK#, PD_XTAL#, PD_APLL#, and PD_PCLK# all set to zero.
2. PD Outs include PD_AO#, and PD_VO# all set to zero.
3. Refer to the SiI-PR-1033 Programmer Reference for register bit descriptions. *The Programmer's Reference requires an NDA with Lattice Semiconductor.*

4.4. AC Specifications

TMDS Input Timings

Symbol	Parameter	Conditions	Min	Typ	Max	Units	Figure	Notes
T_{DPS}	Intra-Pair Differential Input Skew	—	—	—	T_{BIT}	ps	—	2, 4
T_{CCS}	Channel to Channel Differential Input Skew	—	—	—	T_{CIP}	ns	Figure 5.1	2, 3
F_{RXC}	Differential Input Clock Frequency	—	25	—	225	MHz	—	—
T_{RXC}	Differential Input Clock Period	—	4.44	—	40	ns	—	—
T_{IJIT}	Differential Input Clock Jitter tolerance (0.3 Tbit)	74.25 MHz	—	—	400	ps	—	2, 5, 6

Notes:
1. Under normal operating conditions unless otherwise specified, including output pin loading of C_L = 10 pF.
2. Guaranteed by design.
3. IDCK Period. Refer to the applicable Lattice Semiconductor HDMI Transmitter Data Sheet.
4. 1/10 of IDCK Period. Refer to the applicable Lattice Semiconductor HDMI Transmitter Data Sheet.
5. Jitter as defined by the HDMI Specification.
6. Jitter measured with Clock Recovery Unit per HDMI Specification. Actual jitter tolerance can be higher depending on the frequency of the jitter.

Refer to the SiI-PR-1033 Programmer Reference for more details on controlling timing modes.

4.4.1. Video Output Timings

12/15/18-Bit Data Output Timings

Symbol	Parameter	Conditions	Min	Typ	Max	Units	Figure	Notes
D_{LHT}	LOW-to-HIGH Rise Time Transition	C_L = 10 pF	—	—	1.5	ns	Figure 5.4	2
D_{HLT}	HIGH-to-LOW Fall Time Transition	C_L = 10 pF	—	—	1.5	ns	Figure 5.4	2
R_{CIP}	ODCK Cycle Time	C_L = 10 pF	13	—	40	ns	Figure 5.5	8
F_{CIP}	ODCK Frequency	C_L = 10 pF	25	—	82.5	MHz	—	5
T_{DUTY}	ODCK Duty Cycle	C_L = 10 pF	40%	—	60%	R_{CIP}	Figure 5.5	3
T_{CK2OUT}	ODCK-to-Output Delay	C_L = 10 pF	0.6	—	3.8	ns	Figure 5.5	—

16/20/24/30/36-Bit Data Output Timings

Symbol	Parameter	Conditions	Min	Typ	Max	Units	Figure	Notes
D_{LHT}	LOW-to-HIGH Rise Time Transition	C_L = 10 pF	—	—	1.5	ns	Figure 5.4	2
D_{HLT}	HIGH-to-LOW Fall Time Transition	C_L = 10 pF	—	—	1.5	ns	Figure 5.4	2
R_{CIP}	ODCK Cycle Time	C_L = 10 pF	—	—	40	ns	Figure 5.5	5, 8
F_{CIP}	ODCK Frequency	C_L = 10 pF	—	—	165	MHz	Figure 5.5	5
T_{DUTY}	ODCK Duty Cycle	C_L = 10 pF	40%	—	60%	R_{CIP}	Figure 5.5	3
T_{CK2OUT}	ODCK-to-Output Delay	C_L = 10 pF	0.4	—	2.5	ns	Figure 5.5	—

Notes:
1. Under normal operating conditions unless otherwise specified, including output pin loading of C_L = 10 pF.
2. Rise time and fall time specifications apply to HSYNC, VSYNC, DE, ODCK, EVNODD and Q[35:0].
3. Output clock duty cycle is independent of the differential input clock duty cycle. Duty cycle is a component of output setup and hold times.
4. See Table 5.2 on page 33 for calculation of worst case output setup and hold times.
5. All output timings are defined at the maximum operating ODCK frequency, F_{CIP}, unless otherwise specified.
6. F_{CIP} can be the same as F_{RXC} or one-half of F_{RXC}, depending on OCLKDIV setting. F_{CIP} can also be F_{RXC} /1.25 or F_{RXC} /1.5 if Deep Color mode is being transmitted.
7. R_{CIP} is the inverse of F_{CIP} and is not a controlling specification.
8. Output skew specified when ODCK is programmed to divide-by-two mode.

4.4.2. Audio Output Timings

I²S Output Port Timings

Symbol	Parameter	Conditions	Min	Typ	Max	Units	Figure	Notes
T_{tr}	SCK Clock Period (TX)	C_L = 10 pF	1.00	—	—	T_{tr}	Figure 5.6	1
T_{HC}	SCK Clock HIGH Time	C_L = 10 pF	0.35	—	—	T_{tr}		1
T_{LC}	SCK Clock LOW Time	C_L = 10 pF	0.35	—	—	T_{tr}		1
T_{SU}	Setup Time, SCK to SD/WS	C_L = 10 pF	$0.4T_{TR} - 5$	—	—	ns		1
T_{HD}	Hold Time, SCK to SD/WS	C_L = 10 pF	$0.4T_{TR} - 5$	—	—	ns		1
$T_{SCKDUTY}$	SCK Duty Cycle	C_L = 10 pF	40%	—	60%	T_{tr}		1
T_{SCK2SD}	SCK to SD or WS Delay	C_L = 10 pF	–5	—	+5	ns		2
T_{AUDDLY}	Audio Pipeline Delay	—	—	40	80	µs	—	—

Notes:
1. Refer to Figure 5.6. Meets timings in Philips I²S Specification.
2. Applies also to SDC-to-WS delay.

S/PDIF Output Port Timings

Symbol	Parameter	Conditions	Min	Typ	Max	Units	Figure	Notes
T_{SPCYC}	S/PDIF Cycle Time	C_L = 10 pF	—	1.0	—	UI	Figure 5.7	1, 2
F_{SPDIF}	S/PDIF Frequency	—	4	—	24	MHz		3
T_{SPDUTY}	S/PDIF Duty Cycle	C_L = 10 pF	90%	—	110%	UI		2, 5
$T_{MCLKCYC}$	MCLK Cycle Time	C_L = 10 pF	20	—	250	ns	Figure 5.8	1, 2, 4
F_{MCLK}	MCLK Frequency	C_L = 10 pF	4	—	50	MHz		1, 2, 4
$T_{MCLKDUTY}$	MCLK Duty Cycle	C_L = 10 pF	40%	—	60%	$T_{MCLKCYC}$		2, 4
T_{AUDDLY}	Audio Pipeline Delay	—	—	40	80	µs	—	—

Notes:
1. Guaranteed by design.
2. Proportional to unit time (UI), according to sample rate.
3. S/PDIF is not a true clock, but is generated from the internal 128Fs clock, for Fs from 128 to 512 kHz.
4. MCLK refers to MCLKOUT.
5. Intrinsic jitter on S/PDIF output can limit its use as an S/PDIF transmitter. The S/PDIF intrinsic jitter is approximately 0.1 UI.

Audio Crystal Timings

Symbol	Parameter	Conditions	Min	Typ	Max	Units	Figure
F_{XTAL}	External Crystal Freq.	—	26	27	28.5	MHz	Figure 4.2

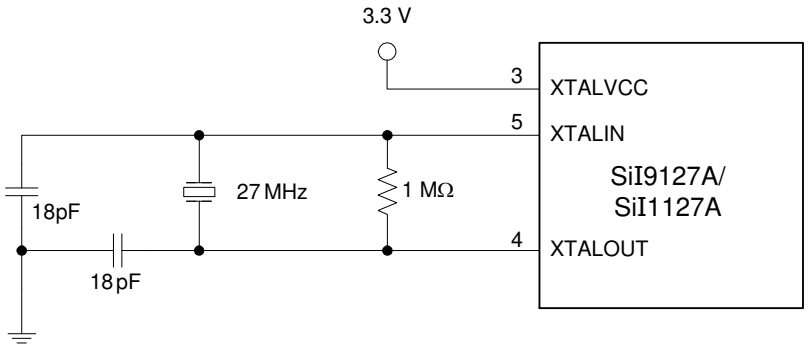


Figure 4.2. Audio Crystal Schematic