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SiI9136-3/SiI1136 HDMI Deep Color Transmitter

Data Sheet

SiI-DS-1084-D

June 2017

Contents

Figures

Tables

Acronyms in This Document

A list of acronyms used in this document.

Acronym	Definition
ACPI	Advanced Configuration and Power Interface
CBUS	Control Bus
CEC	Consumer Electronics Control
CPI	CEC Programming Interface
CSC	Color Space Converters
DDC	Display Data Channel
DSC	Display Stream Compression
DVI	Digital Visual Interface
EDDC	Enhanced Display Data Channel
EDID	Extended Display Identification Data
EMI	Electromagnetic interference
ESD	Electrostatic Discharge
GPIO	General Purpose Input/Output
HDCP	High-bandwidth Digital Content Protection
HDMI	High-Definition Multimedia Interface
HDTV	High-Definition Television
HPD	Hot Plug Detect
I^2C	Inter-Integrated Circuit
KSV	Key Selection Vector
MCLK	Master Clock
SPDIF	Sony/Philips Digital Interface Format
TMDS	Transition Minimized Differential Signaling
TPI	Transmitter Programming Interface
VSIF	Vendor Specific InfoFrame

1. General Description

The Lattice Semiconductor SiI9136-3/SiI1136 transmitter is an HDMI® Deep Color transmitter with 3D and 4K x 2K support for consumer electronics products such as set-top boxes, Blu-ray players and recorders, A/V Receivers, DVD players and recorders, personal video recorders, home theater-in-a-box systems, and home theater PCs. Figure 1.1 shows an example of system architecture using the SiI9136-3/SiI1136 device.

The SiI9136-3/SiI1136 transmitter, with the latest generation 300 MHz TMDS™ core, enables home theater devices to deliver up to 16-bit Deep Color at 1080p/30 resolutions and up to 12-bit Deep Color at 1080p/60 resolutions. On the audio side, high bitrate audio formats such as Dolby® TrueHD and DTS-HD are supported for an enhanced digital audio experience.

1.1. Video Input

- Supports most common standard and nonstandard video input formats
- Supports most common 3D formats
- Supports video resolutions up to 8-bit 4K (30 Hz), 12-bit 1080p (60 Hz), 12-bit 720p/1080i (120 Hz), and 16-bit 1080p (30 Hz)

1.2. Audio Input

- S/PDIF input supports PCM and compressed audio formats (Dolby Digital, DTS, AC-3)
- DSD input supports Super Audio CD applications (SACD)
- I²S input supports PCM, DVD-Audio input (up to 8-channel 192 kHz)
- High Bitrate audio support such as DTS HD and Dolby True HD

1.3. HDMI Output

- DVI, HDCP (on SiI9136-3 only), and HDMI transmitter with xvYCC extended color gamut, Deep Color up to 16-bit color, 3D, and high bitrate audio support
- 300 MHz HDMI transmitter
- Supports all mandatory and some optional 3D modes
- Preprogrammed HDCP key set (on SiI9136-3 only) simplifies the manufacturing process, lowers cost, and provides the highest level of HDCP key security

1.4. Control Capability

- Consumer Electronics Control (CEC) interface that incorporates an HDMI-compliant CEC I/O and the Lattice CEC Programming Interface (CPI) reduces the need for system-level control by the system microcontroller and simplifies firmware overhead
- Four General Purpose I/O (GPIO) pins
- Three dynamic power management modes as required in the Advanced Configuration and Power Interface (ACPI) Specification, according to system needs

1.5. Packaging

- 100-pin, 14 mm x 14 mm, 0.5 mm pitch TQFP package with ePad

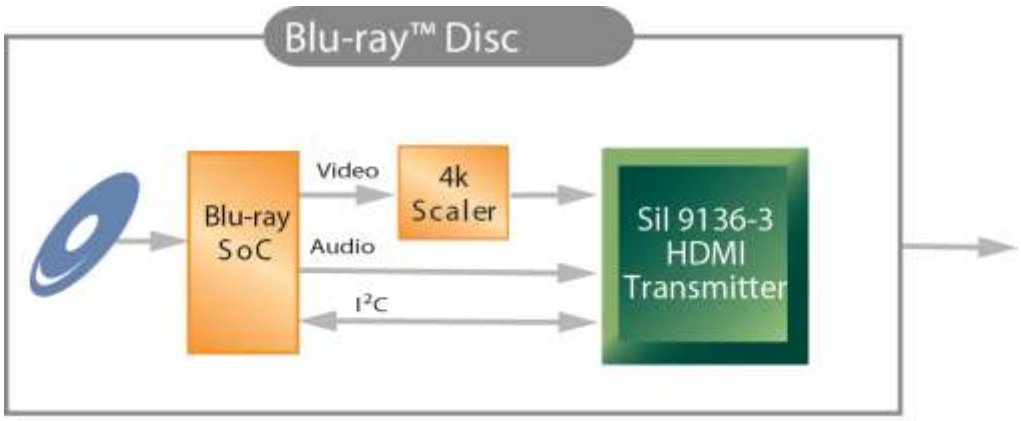


Figure 1.1. Typical Application for Streaming Sticks

2. Product Family

Table 2.1 summarizes the differences between the SiI9136-3/SiI1136 transmitter and the SiI9134 transmitter.

Table 2.1. Product Selection Guide

Transmitter	SiI9134	SiI9136	SiI9136-3/SiI1136
Video Input			
Digital Video Input Ports	1	1	1
I/O Voltage	3.3 V	3.3 V	3.3 V
Core Voltage	1.8 V	1.2 V	1.2 V
Input Pixel Clock Multiply/Divide	0.5x, 2x, 4x	0.5x, 2x, 4x	0.5x, 2x, 4x
Maximum Pixel Input Clock Rate	165 MHz	165 MHz	300 MHz
Maximum TMDS Output Clock	225 MHz	225 MHz	300 MHz
BTA-T1004 Format Support	Yes	Yes	Yes
Video Format Conversion			
36-bit and 30-bit Deep Color	Yes	Yes	Yes
48-bit Deep Color	No	Yes	Yes
xvYCC	No	Yes	Yes
YCbCr → RGB CSC	Yes	Yes	Yes
RGB → YCbCr CSC	Yes	Yes	Yes
4:2:2 → 4:4:4 Upsampling	Yes	Yes	Yes
4:4:4 → 4:2:2 Decimation	Yes	Yes	Yes
16–235 → 0–255 Expansion	Yes	Yes	Yes
0–255 → 16–235 Compression	Yes	Yes	Yes
16–235/240 Clipping	Yes	Yes	Yes
Audio Input			
S/PDIF Input Ports	1	1	1
I²S Input Bits	4 (8-channel)	4 (8-channel)	4 (8-channel)
High Bitrate Audio Support Compressed DTS-HD and Dolby True-HD	Yes	Yes	Yes
One-bit Audio (DSD/SACD)	Yes	Yes[1]	Yes[1]
2-Channel Maximum Sample Rate	192 kHz on I²S 192 kHz on S/PDIF	192 kHz on I²S 192 kHz on S/PDIF	192 kHz on I²S 192 kHz on S/PDIF
8-Channel Maximum Sample Rate	192 kHz	192 kHz	192 kHz
Down Sampling	96 kHz to 48 kHz 192 kHz to 48 kHz	96 kHz to 48 kHz 192 kHz to 48 kHz	96 kHz to 48 kHz 192 kHz to 48 kHz
Internal MCLK Generator	No	Yes[2]	Yes[2]
I²C Address Bus			
Device Address Select	CI2CA Pin	CI2CA Pin	CI2CA Pin
Master DDC Bus	Yes	Yes	Yes
Other			
CEC Interface	No	Yes	Yes
xvYCC Gamut Data	Yes	Yes	Yes
3D Support	Yes	Yes	Yes
Programming Interface	No	Yes	Yes
HDCP Reset	Software Register	Software Register	Software Register
Package	100-pin TQFP	100-pin TQFP	100-pin TQFP

Notes:

1. Shared with I²S Input Interface.
2. Internal MCLK generation is ON by default.
3. HDCP Reset does not apply to the SiI1136 transmitter.

3. Functional Description

Figure 3.1 shows the functional diagram of the SiI9136-3/SiI1136 transmitter. Pin descriptions begin on page 23. A description of each of the blocks shown in the diagram follows the figure. The power domains are described in the Power Domains section on page 29.

Note: HDCP blocks do not apply to the SiI1136 transmitter.

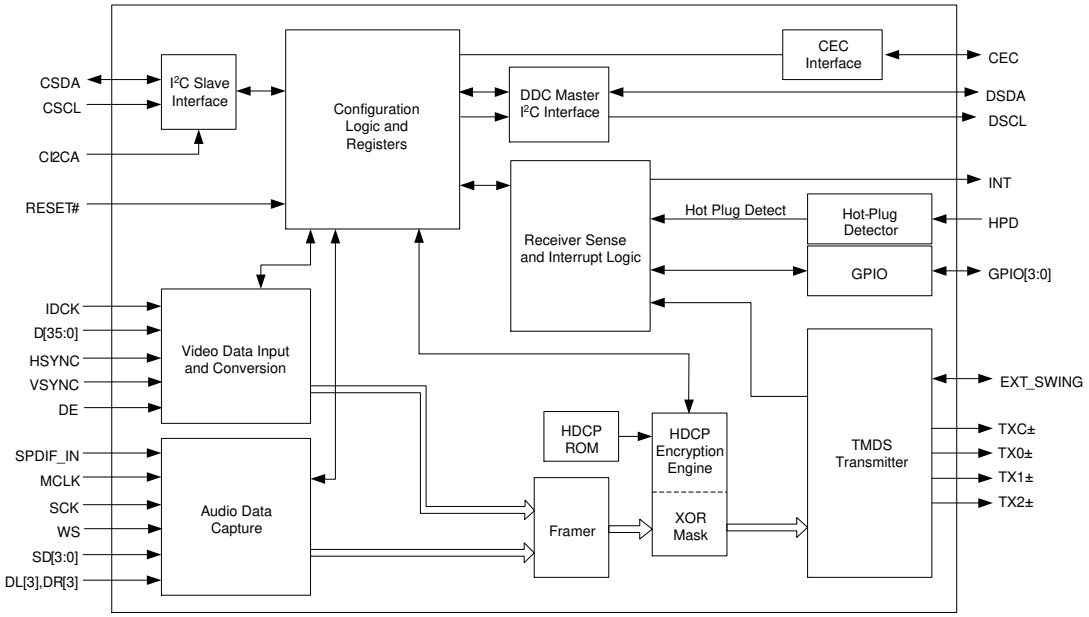


Figure 3.1. SiI9136-3/SiI1136 Functional Block Diagram

3.1. Video Data Input and Conversion

Figure 3.2 shows the video data processing stages through the transmitter. Each of the processing blocks can be bypassed by setting the appropriate register bits. The HSYNC and VSYNC input signals are required, except in embedded sync modes. The DE input signal is optional, because it can be created with the DE generator using the HSYNC and VSYNC signals.

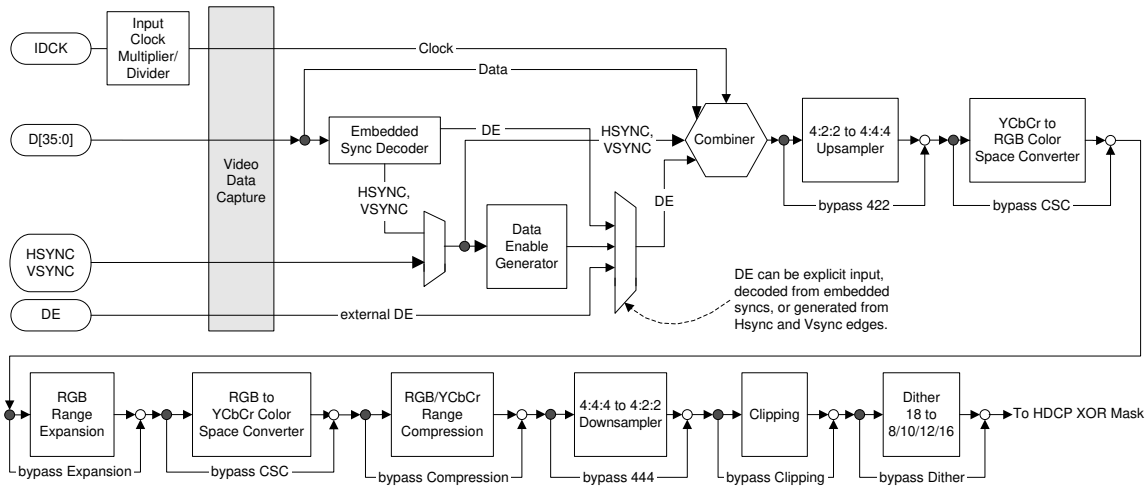


Figure 3.2. Transmitter Video Data Processing Path

3.1.1. Input Clock Multiplier/Divider

The input pixel clock can be multiplied by 0.5, 2, or 4. Video input formats that use a 2x clock, such as YC Mux mode, can be transmitted across the HDMI link with a 1x clock. Similarly, 1x-to-2x, 1x-to-4x, and 2x-to-4x conversions are possible.

3.1.2. Video Data Capture

The bus configurations support most standardized video input formats as well as other widely used non-standard formats. Each configuration has four key attributes: data width, input mode, clock mode, and synchronization.

The video input port is a 36-bit wide bus that can be configured to any of the following data widths:

- 8-, 10-, or 12-bit input in double speed clock mode
- 12-, 15-, 18-, or 24-bit input in dual edge clock mode
- 16-, 20-, 24-, 30-, or 36-input in single speed clock mode

The input mode includes color format such as RGB, YCbCr, or xvYCC, and color sampling such as 4:4:4 or 4:2:2.

Clock mode refers to the input clock rate relative to the pixel clock rate. The SiI9136-3/SiI1136 device supports 1x mode and 2x mode, or dual edge mode. 1x mode and 2x mode means that the input clock operates at one or two times the pixel clock rate. Dual edge mode means that the input clock rate equals the pixel clock rate, but a sample is captured on both the rising edge and the falling edge of the input clock. Thus, with the Video Input configured for 24 bits with a dual edge clock, 48 bits of video data are received per clock cycle. The 24 MSBs of the video data are latched on the first clock edge, and the 24 LSBs are latched on the next clock edge. The first clock edge is programmable and can be either the rising or falling edge.

Synchronization attributes refer to how the horizontal and vertical sync signals are configured. Separate synchronization involves placing the horizontal sync, vertical sync, and data enable signals on separate input pins. Embedded synchronization combines these signals with one or more of the data inputs.

3.1.3. Embedded Sync Decoder

The transmitter can create DE, HSYNC, and VSYNC signals using the Start of Active Video (SAV) and End of Active Video (EAV) codes within the ITU-R BT.656-format video stream.

3.1.4. Data Enable Generator

The transmitter includes logic to construct a Data Enable (DE) signal from the incoming HSYNC, VSYNC, and IDCK. This signal is used to correct timing from sync extraction to conform to CEA-861D timing specifications. By programming registers, the DE signal can define the size of the active display region. This feature is particularly useful when the transmitter connects to MPEG decoders that do not provide a specific DE output signal.

3.1.5. Combiner

The clock, data, and sync information is combined into a complete set of signals required for TMDS encoding. From here, the signals are manipulated by the register-selected video processing blocks.

3.1.6. 4:2:2 to 4:4:4 Upsampler

Chrominance upsampling doubles the number of chrominance samples per line, converting 4:2:2 sampled video to 4:4:4.

3.1.7. RGB Range Expansion

The SiI9136-3/SiI1136 transmitter can scale the input color range from limited-range into full-range using the range expansion block. When enabled by itself, the range expansion block expands 16–235 (64–943 to 256–3775, 4096-60415 for 30/36/48-bit color depth) limited-range data into 0–255 (0–1023, 0–4095 to 0-65535 for 30/36/48-bit color depth) full-range data for each video channel. When range expansion and the YCbCr to RGB color space converter are both enabled, the input conversion range for the Cb and Cr channels is 16–240 (64–963, 256–3855 to 4096-61695 for 30/36/48-bit color depth).

3.1.8. Color Space Converter

Two Color Space Converters (CSCs) (YCbCr to RGB and RGB to YCbCr) are available to interface to the many video formats supplied by A/V processors and to provide full DVI backward compatibility. The CSC can be adjusted to perform standard-definition conversions (ITU.601) or high-definition conversions (ITU.709) by setting the appropriate registers.

3.1.9. RGB/YCbCr Range Compression

When enabled by itself, the range compression block compresses 0–255/0–1023/0–4095/0–65535 full-range data into 16–235/64–943/256–3775/4096–60415 limited-range data for each video channel. When enabled with the RGB to YCbCr converter, this block compresses to 16–240/64–963/256–3855/4096–61695 for the Cb and Cr channels. The color range scaling is linear.

3.1.10. 4:4:4 to 4:2:2 Downsampler

Downsampling reduces the number of chrominance samples per line by half, converting 4:4:4 sampled video to 4:2:2.

3.1.11. Clipping

The clipping block, when enabled, clips the values of the output video to 16–235 for RGB video or the Y channel, and to 16–240 for the Cb and Cr channels.

3.1.12. 18-to-8/10/12/16-Dither

The 18-to-8/10/12/16-dither block dithers internally processed, 18-bit data to 8, 10, 12, or 16 bits for output on the HDMI link. It can be bypassed to output 10/12-bit modes when supplied by the A/V processor or converted in the decimator and CSC.

3.2. Audio Data Capture

The audio capture block supports I^2S, Direct Stream Digital, and S/PDIF audio input formats. The appropriate registers must be configured to describe the audio format provided to the SiI9136-3/SiI1136 transmitter. This information is passed over the HDMI link in the CEA-861D Audio Info (AI) packets.

3.3. Framer

The framer block handles the packetizing and framing of the data stream sent across the HDMI link. Audio and video data packets are inserted into the respective HDMI Video Data and Data Island periods. This block handles the correct insertion of all HDMI packet types.

3.4. HDCP Encryption Engine/XOR Mask

The HDCP encryption engine contains the logic necessary to encrypt the incoming audio and video data and includes support for HDCP authentication and repeater checks. The system microcontroller or microprocessor controls the encryption process by using a set sequence of register reads and writes. An algorithm uses HDCP keys and a Key Selection Vector (KSV) stored in the HDCP key ROM to calculate a number that is then applied to an XOR mask. This process encrypts the audio and video data on a pixel-by-pixel basis during each clock cycle. The HDCP encryption engine/XOR mask does **not** apply to the SiI1136 transmitter.

3.5. HDCP Key ROM

The SiI9136-3/SiI1136 transmitter comes preprogrammed with a set of production HDCP keys stored in an internal ROM. System manufacturers do not need to purchase key sets from the Digital-Content Protection LLC. Lattice Semiconductor handles all purchasing, programming, and security for the HDCP keys. The preprogrammed HDCP keys provide the highest level of security because there is no way to read the keys once the device is programmed. Customers must sign the HDCP license agreement (www.digital-cp.com) or be under a specific NDA with Lattice Semiconductor before receiving SiI9136-3/SiI1136 samples.

The SiI1136 transmitter is functionally equivalent to the SiI9136-3 except the HDCP keys are not preprogrammed and therefore does not support HDCP encryption.

3.6. TMDS Transmitter

The TMDS digital core performs 8-to-10-bit TMDS encoding on the data received from the HDCP XOR mask, and is then sent over three TMDS data and a TMDS clock differential lines. A resistor connected to the EXT_SWING pin controls the swing amplitude of the TMDS signal.

3.7. GPIO

The SiI9136-3/SiI1136 transmitter has four General Purpose I/O pins. Each pin supports the following functions:

- Input mode: The value can be read through local I^2C bus access; an interrupt can be generated on either the falling or the rising edge of the input signal.
- Output mode: The value can be set through the local I^2C bus access.

3.8. Hot Plug Detector

When HIGH, the Hot Plug Detection signal indicates to the transmitter that the EDID of the connected receiver is readable. A HIGH voltage is at least 2.0 V, and a LOW voltage is less than 0.8 V.

3.9. CEC Interface

The Consumer Electronics Control (CEC) Interface block provides CEC-compliant signals between CEC devices and a CEC master. A CEC controller compatible with the Lattice Semiconductor CEC API is included on-chip. The controller has a high-level register interface accessible through the I^2C interface, and can be used to send and receive CEC commands. This controller makes CEC control easy and straightforward by removing the burden of programming the host processor to perform these low-level transactions on the CEC bus. See the *CEC Programming Interface (CPI) Programmer Reference* for details on the API (see the Lattice Semiconductor Documents section on page 52). *The Programmer's Reference requires an NDA with Lattice Semiconductor.*

3.10. DDC Master I^2C Interface

The host uses the DDC master logic to read the EDID by programming the target address, offset, and number of bytes. Upon completion, or when the DDC master FIFO becomes full, an interrupt signal is sent to the host so that the host can read data out of the FIFO.

The TPI hardware uses the DDC master logic to carry out HDCP authentication tasks. The arbitration logic arbitrates the access from host and the internal TPI hardware. See the Internal DDC Master section on page 30 for more information.

3.11. Receiver Sense and Interrupt Logic

The Interrupt logic of this block buffers interrupt events from different sources. Receiver Sense and Hot Plug Interrupts are also available in power down mode. The logic for handling these interrupts when all clocks are disabled is also part of this block. The INT pin provides an interrupt signal to the system microcontroller when any of the following occur:

- Monitor Detect (either from the HPD input level or from the Receiver Sense feature) changes
- VSYNC (useful for synchronizing a microcontroller to the vertical timing interval)
- Error in the audio format
- DDC FIFO status change
- HDCP authentication error.

3.12. Configuration Logic and Registers

This block contains the configuration registers that control the operation of the transmitter. The registers are accessed via the I^2C interface. This block also contains logic for simplifying the configuration of the transmitter by automatically programming different parameters.

3.13. I^2C Slave Interface

The controller I^2C interface on the transmitter (signals CSCL and CSDA) is a slave interface with an operating frequency from 3 kHz to 400 kHz and with an input tolerance of up to 4.0 V when all device operating voltages are present. The host uses this interface to configure the transmitter by reading from and writing to appropriate registers.

4. Electrical Specifications

4.1. Absolute Maximum Conditions

Table 4.1. Absolute Maximum Conditions

Symbol	Parameter	Min	Typ	Max	Units	Note
IOVCC33	I/O Pin Supply Voltage	–0.3	—	4.0	V	2
CVCC12	Digital Core Supply Voltage	–0.5	—	1.5	V	2
AVCC	Analog Supply Voltage 1.2 V	–0.5	—	1.5	V	2
V_I	Input Voltage	–0.3	—	IOVCC + 0.3	V	—
V_O	Output Voltage	–0.3	—	IOVCC + 0.3	V	—
T_J	Junction Temperature	—	—	125	°C	—
T_{STG}	Storage Temperature	–65	—	150	°C	—

Notes:
1. Permanent device damage can occur if absolute maximum conditions are exceeded.
2. Functional operation should be restricted to the conditions described in the Normal Operating Conditions section.

4.2. Normal Operating Conditions

Table 4.2. Normal Operating Conditions

Symbol	Parameter	Min	Typ	Max	Units	Note
IOVCC33	I/O Pin Supply Voltage	3.135	3.3	3.465	V	—
CVCC12	Digital Core Supply Voltage	1.14	1.2	1.26	V	—
AVCC	Analog Supply Voltage, 1.2 V	1.14	1.2	1.26	V	—
V_{CCN}	Supply Voltage Noise Tolerance	—	—	100	mV_{P-P}	*
T_A	Ambient Temperature (with power applied)	0	25	70	°C	—
Θ_{ja}	Thermal Resistance (Theta JA)	—	—	29.3	°C/W	—
Θ_{jc}	Junction to case resistance (Theta JC)	—	—	12.8	°C/W	—

***Note:** The supply voltage noise is measured at test point VCCTP. See Figure 4.1. The ferrite bead provides filtering of power supply noise. The figure is representative and applies to the IOVCC33, CVCC12, and AVCC pins.

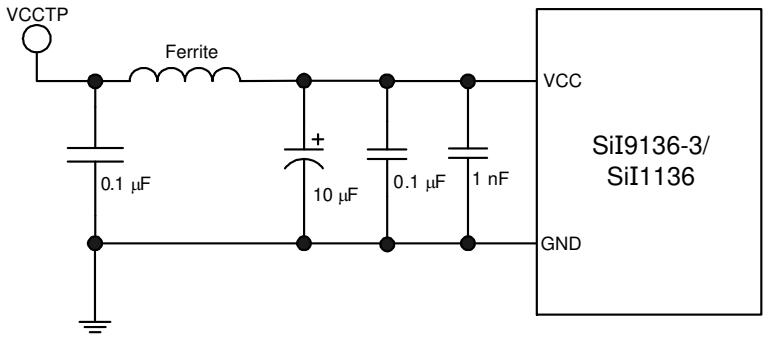


Figure 4.1. VCCTP Test Point for VCC Noise Tolerance

4.2.1. I/O Specifications

Under normal operating conditions unless otherwise specified.

Table 4.3. DC Digital I/O Specifications

Symbol	Parameter	Signal Type	Conditions	Min	Typ	Max	Units
V_{IH}	HIGH-level Input Voltage*	LVTTL	—	2.0	—	5.5	V
V_{IL}	LOW-level Input Voltage*			–0.3	—	0.8	V
VTH+	LOW to HIGH Threshold	Schmitt	RESET#, CSCL, CSDA	1.9	—	—	V
VTH-	HIGH to LOW Threshold			—	—	0.7	V
V_{TH+}	LOW to HIGH Threshold	Schmitt	DSCL, DSDA	3.0	—	—	V
V_{TH-}	HIGH to LOW Threshold			—	—	1.5	V
V_{TH+}	LOW to HIGH Threshold	Schmitt	CEC_A	2.0	—	—	V
V_{TH-}	HIGH to LOW Threshold			—	—	0.8	V
V_{OH}	HIGH-level Output Voltage	LVTTL	—	2.4	—	—	V
V_{OL}	LOW-level Output Voltage			—	—	0.4	V
I_{OZ}	High Impedance Output Leakage Current	—	@ V_O = 3.3 V or 0 V	–10	—	10	µA
I_{OH}	HIGH level Output Current	—	@ V_{OH} {Min}	—	—	8	mA
I_{OL}	LOW level Output Current	—	@ V_{OL} {Max}	—	—	8	mA

***Note:** All unused input signals should be tied LOW.

Table 4.4. TMDS I/O Specifications

Symbol	Parameter	Signal Type	Conditions	Min	Typ	Max	Units
V_{OD}	Differential outputs: single-ended swing amplitude*	TMDS	R_{LOAD} = 50 Ω R_{EXT_SWING} as defined in the Pin Descriptions section	400	500	600	mV
V_{ODD}	Differential outputs: differential swing amplitude	TMDS	—	800	1000	1200	mV
V_{DOH}	Differential HIGH level output voltage	TMDS	≤ 165 MHz TMDS clock	AVCC – 10 mV	—	AVCC + 10 mV	V
			> 165 MHz TMDS clock	AVCC – 200 mV	—	AVCC + 10 mV	V
V_{DOL}	Differential LOW level output voltage	TMDS	≤ 165 MHz TMDS clock	AVCC – 600 mV	—	AVCC – 400 mV	V
			> 165 MHz TMDS clock	AVCC – 700 mV	—	AVCC – 400 mV	V
I_{DOS}	Differential output short circuit current	TMDS	V_{OUT} = 0 V	—	—	5	µA

***Note:** Single-ended swing amplitude limits are defined by the HDMI Specification.

4.2.2. DC Power Supply Specifications

Table 4.5 shows the power consumption in the three power modes. Measurement uses Dot Moiré pattern with 8-chanel I²S audio and HDCP enabled.

Table 4.5. DC Specifications

Symbol	Parameter	Mode	Frequency[1]	IOVCC33		AVCC		CVCC12		Units
				Typ	Max	Typ	Max	Typ	Max	
I_{PON}	Power On Current	D0	74.25 MHz	1.8	1.7	10.9	12.2	36.3	40.0	mA
			148.5 MHz	3.6	3.1	18.2	20.3	68.4	75.6	mA
			225 MHz	4.7	3.8	25.4	28.3	83.9	92.9	mA
			297 MHz	3.8[2]	3.2[2]	33.1	37.3	94.9	105.2	mA
I_{PSTBY}	Power Standby Current	D2	—	4.70		0.50		9.10		mA
I_{POFF}	Power Off current	D3	—	4.70		0.50		5.10		mA

Notes:
1. TMDS clock frequency does not matter in D3 and D2 modes.
2. Current measurement for IOVCC33 is lower at 297 MHz since only 24-bits per pixel is used. At 225 MHz used for deep color, each pixel is 36-bits wide.

4.3. AC Specifications

4.3.1. Video/HDMI Timing Specifications

Under normal operating conditions unless otherwise specified.

Table 4.6. Video Input AC Specifications

Symbol	Parameter	Conditions	Min	Typ	Max	Units	Figure
T_{DDF}	VSYNC and HSYNC Delay from DE falling edge	—	1	—	—	T_{CIP}	Figure 4.6
T_{DDR}	VSYNC and HSYNC Delay to DE rising edge	—	1	—	—	T_{CIP}	Figure 4.6
T_{HDE}	DE HIGH Time	—	—	—	8191	T_{CIP}	Figure 4.7
T_{LDE}	DE LOW Time	—	138*	—	—	T_{CIP}	Figure 4.7

***Note:** T_{LDE} minimum is defined for HDMI mode carrying 480p video with 192 kHz audio, which requires at least 138 pixel clock cycles of blanking to carry the audio packets. If only HDCP is running, the minimum DE LOW time is 58 clock cycles, according to the HDCP Specification. If neither HDCP nor audio are running, the minimum DE LOW time is 12 clock cycles for TMDS. The minimum vertical blanking time is three horizontal line times.

Table 4.7. TMDS AC Output Specifications

Symbol	Parameter	Conditions	Min	Typ	Max	Units	Figure
S_{LHT}	Differential Swing LOW-to-HIGH Transition Time	REXT_SWING = 3.83 kΩ Internal Source Termination On	95.5	—	181.81	ps	Figure 4.10
S_{HLT}	Differential Swing HIGH-to-LOW Transition Time	REXT_SWING = 3.83 kΩ Internal Source Termination On	86.5	—	172.3	ps	Figure 4.10

Notes:
1. These limits are defined by the HDMI Specification.
2. Refer to the Source Termination section on page 31 for information about internal source termination.

4.3.2. Audio AC Timing Specifications

Table 4.8. S/PDIF Input Port Timings

Symbol	Parameter	Conditions	Min	Typ	Max	Units	Figure	Notes
F_{S_SPDIF}	Sample Rate	2 Channel	32	—	192	kHz	—	—
T_{SPCYC}	S/PDIF Cycle Time	C_L = 10 pF	—	—	1.0	UI	Figure 4.12	1
T_{SPDUTY}	S/PDIF Duty Cycle	C_L = 10 pF	90%	—	110%	UI	Figure 4.12	1
$T_{MCLKCYC}$	MCLK Cycle Time	C_L = 10 pF	13.3	—	—	ns	Figure 4.13	3
F_{MCLK}	MCLK Frequency	C_L = 10 pF	—	—	75	MHz	—	3
$T_{MCLKDUTY}$	MCLK Duty Cycle	C_L = 10 pF	40%	—	60%	$T_{MCLKCYC}$	Figure 4.13	3
T_{AUDDLY}	Audio Pipeline Delay	—	—	30	70	µs	—	4

Note: Refer to the notes for Table 4.10.

Table 4.9. I²S Input Port Timings

Symbol	Parameter	Conditions	Min	Typ	Max	Units	Figure	Notes
F_{S_I2S}	Sample Rate	—	32	—	192	kHz	—	—
T_{SCKCYC}	I²S Cycle Time	C_L = 10 pF	—	—	1.0	UI	Figure 4.11	1
$T_{SCKDUTY}$	I²S Duty Cycle	C_L = 10 pF	90%	—	110%	UI	Figure 4.11	—
T_{I2SSU}	I²S Setup Time	C_L = 10 pF	15	—	—	ns	Figure 4.11	2
T_{I2SHD}	I²S Hold Time	C_L = 10 pF	0	—	—	ns	Figure 4.11	2

Note: Refer to the notes for Table 4.10.

Table 4.10. DSD Input Port Timings

Symbol	Parameter	Conditions	Min	Typ	Max	Units	Figure	Notes
F_{S_DSD}	Sample Rate	—	—	44.1	88.2	kHz	—	—
T_{DCKCYC}	DSD Cycle Time	C_L = 10 pF	—	—	2.0	UI	Figure 4.14	1
$T_{DCKDUTY}$	DSD Duty Cycle	C_L = 10 pF	90%	—	110%	UI	Figure 4.14	1
T_{DSDSU}	DSD Setup Time	C_L = 10 pF	20	—	—	ns	Figure 4.14	—
T_{DSDHD}	DSD Hold Time	C_L = 10 pF	20	—	—	ns	Figure 4.14	—

Notes:

1. Proportional to unit time (UI) according to sample rate. Refer to the I²S, S/PDIF, or DSD Specifications.
2. Setup and hold minimum times are based on 13.388 MHz sampling, which is adapted from Figure 3 of the Philips I²S Specification.
3. If a separate master clock input (MCLK) is used for time-stamping purposes, it has to be coherent with the audio input. *Coherent* means that the MCLK and audio input have been created from the same clock source. This requirement usually uses the original MCLK to strobe the audio out from the sourcing chip.
4. Audio pipeline delay is measured from the transmitter input pins to the TMDS output.

4.3.3. Video AC Timing Specifications

Under normal operating conditions unless otherwise specified.

Table 4.11. Video AC Timing Specifications

Symbol	Parameter	Conditions	Min	Typ	Max	Units	Figure	Notes
T_{CIP}	IDCK period, one pixel per clock	—	3.3	—	40	ns	Figure 4.2	1
F_{CIP}	IDCK frequency, one pixel per clock	—	25	—	300	MHz	—	1
T_{CIP12}	IDCK period, dual-edge clock	—	12.3	—	40	ns	Figure 4.2	2
F_{CIP12}	IDCK frequency, dual-edge clock	—	25	—	82.5	MHz	—	2
T_{DUTY}	IDCK duty cycle	—	45%	—	55%	T_{CIP}	Figure 4.2	—
T_{IJIT}	Worst case IDCK clock jitter, DJ	—	—	—	0.20	T_{BIT}	—	3, 4
	Worst case IDCK clock jitter, RJ	—	—	—	0.25	T_{BIT}	—	
T_{SIDF}	Setup time to IDCK falling edge	EDGE = 0	1.36	—	—	ns	Figure 4.4	5
T_{HIDF}	Hold time to IDCK falling edge		0.45	—	—	ns		
T_{SIDR}	Setup time to IDCK rising edge	EDGE = 1	1.57	—	—	ns	Figure 4.3	5
T_{HIDR}	Hold time to IDCK rising edge		1.16	—	—	ns		
T_{SIDD}	Setup time to IDCK rising or falling edge	Dual-edge clocking	1.57	—	—	ns	Figure 4.5	6
T_{HIDD}	Hold time to IDCK rising or falling edge		1.16	—	—	ns		

Notes:

1. T_{CIP} and F_{CIP} apply in single-edge clocking modes. T_{CIP} is the inverse of F_{CIP} and is not a controlling specification.
2. T_{CIP12} and F_{CIP12} apply in dual-edge mode. T_{CIP12} is the inverse of F_{CIP12} and is not a controlling specification.
3. T_{BIT} is the TMDS bit time.
4. Total jitter (TJ) is calculated from DJ (deterministic jitter), RJ (random jitter, rms) and required BER (Bit Error Rate). For BER of 1E-9, TJ = DJ + 12 • RJ = 3.2 T_{BIT}.
5. Setup and hold time specifications apply to Data, DE, VSYNC, and HSYNC input pins, relative to IDCK input clock.
6. Setup and hold limits are not affected by the setting of the EDGE bit for 12/15/18/24-bit dual-edge clocking mode.

4.3.4. Control Signal Timing Specifications

Under normal operating conditions unless otherwise specified.

Table 4.12. Control Signal Timing Specifications

Symbol	Parameter	Conditions	Min	Typ	Max	Units	Figure	Note
T_{RESET}	RESET# signal LOW time required for reset	—	50	—	—	µs	Figure 4.8 Figure 4.9	1, 5
T_{I2CDVD}	SDA Data Valid Delay from SCL falling edge on READ command	CL = 400pF	—	—	700	ns	Figure 4.15	2, 6
T_{HDDAT}	I^2C data hold time	0–400 kHz	2.0	—	—	ns	—	3, 6
T_{INT}	Response time for INT output pin from change in input condition (HPD, Receiver Sense, VSYNC change, etc.).	RESET# = HIGH	—	—	100	µs	—	—
F_{SCL}	Frequency on master DDC SCL signal	—	40	70	100	kHz	—	4
F_{CSCL}	Frequency on master CSCL signal	—	40	—	400	kHz	—	—

Notes:

1. Reset on RESET# signal can be LOW as the supply becomes stable (shown in Figure 4.8), or pulled LOW for at least T_{RESET} (shown in Figure 4.9).
2. All standard-mode (100 kHz) I^2C timing requirements are guaranteed by design. These timings apply to the slave I^2C port (pins CSDA and CSCL) and to the master I^2C port (pins DSDA and DSCL).
3. This minimum hold time is required by CSCL and CSDA signals as an I^2C slave. The device does not include the 300 ns internal delay required by the I^2C Specification (Version 2.1, Table 5, note 2).
4. The master DDC block provides an SCL signal for the E-DDC bus. The HDMI Specification limits this to I^2C Standard Mode or 100 kHz. Use of the Master DDC block does not require an active IDCK.
5. Not a Schmitt trigger.
6. Operation of I^2C pins above 100 kHz is defined by LVTTL levels V_{IH}, V_{IL}, V_{OH}, and V_{OL} (see Table 4.3 on page 15). For these levels, I^2C speeds up to 400 kHz are supported.

4.3.5. CEC Timing Specifications

See the HDMI 1.4 Specification – Supplement 1 Consumer Electronics Control (CEC).

4.4. Timing Diagrams

4.4.1. Input Timing Diagrams

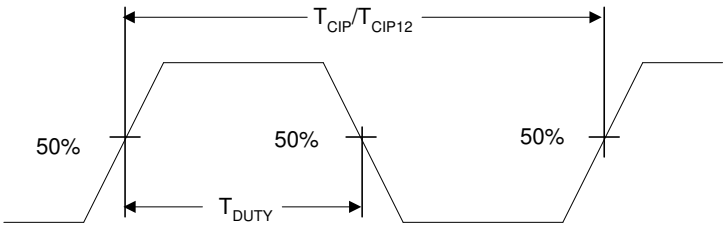
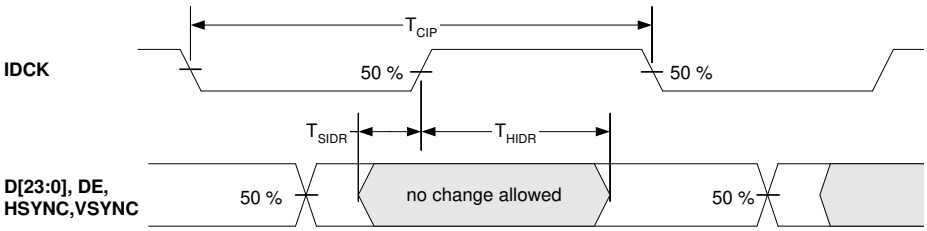
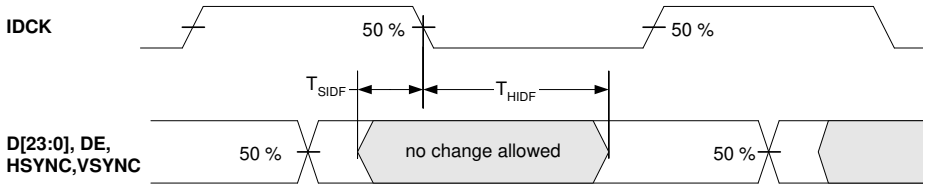


Figure 4.2. IDCK Clock Duty Cycle



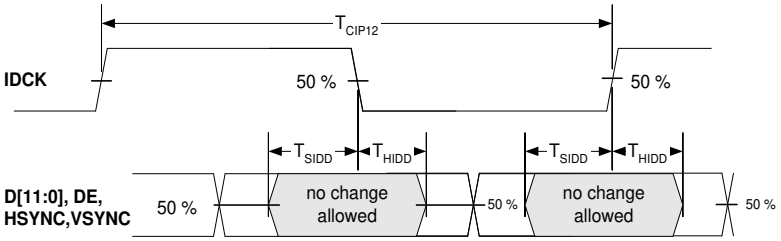
Signals may change only in the unshaded portion of the waveform, to meet both the minimum setup and minimum hold time specifications.

Figure 4.3. Control and Data Single-Edge Setup and Hold Times—EDGE = 1



Signals may change only in the unshaded portion of the waveform, to meet both the minimum setup and minimum hold time specifications.

Figure 4.4. Control and Data Single-Edge Setup and Hold Times—EDGE = 0



Signals may change only in the unshaded portion of the waveform, to meet both the minimum setup and minimum hold time specifications.

Figure 4.5. Control and Data Dual-Edge Setup and Hold Times

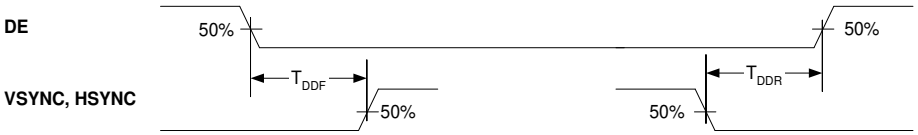


Figure 4.6. VSYNC and HSYNC Delay Times Based on DE

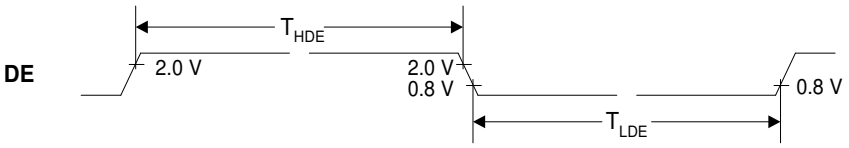


Figure 4.7. DE HIGH and LOW Times

4.4.2. Reset Timing Diagrams

VCC must be stable between its limits listed in the Normal Operating Conditions section on page 14 for T_{RESET} before RESET# goes HIGH, as shown in Figure 4.8. Before accessing registers, RESET# must be pulled LOW for T_{RESET}. This can be done by holding RESET# LOW until T_{RESET} after stable power, as described above, or by pulling RESET# LOW from a HIGH state for at least T_{RESET}, as shown in Figure 4.9.

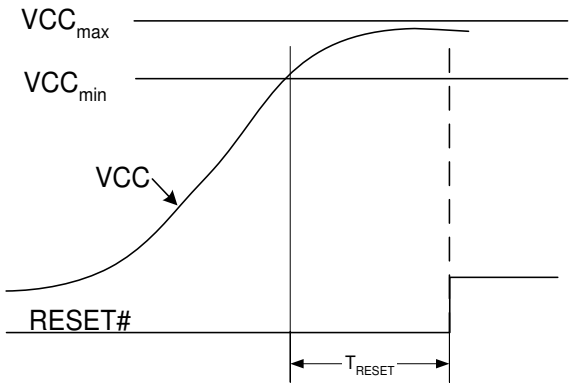


Figure 4.8. Conditions for Use of RESET#

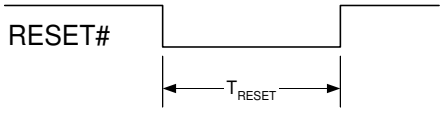


Figure 4.9. RESET# Minimum Timings

4.4.3. TMDS Timing Diagram

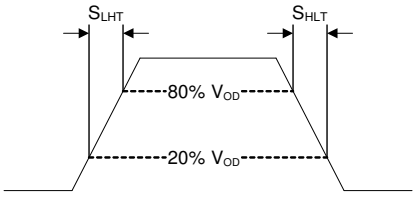


Figure 4.10. Differential Transition Times

4.4.4. Audio Timing Diagrams

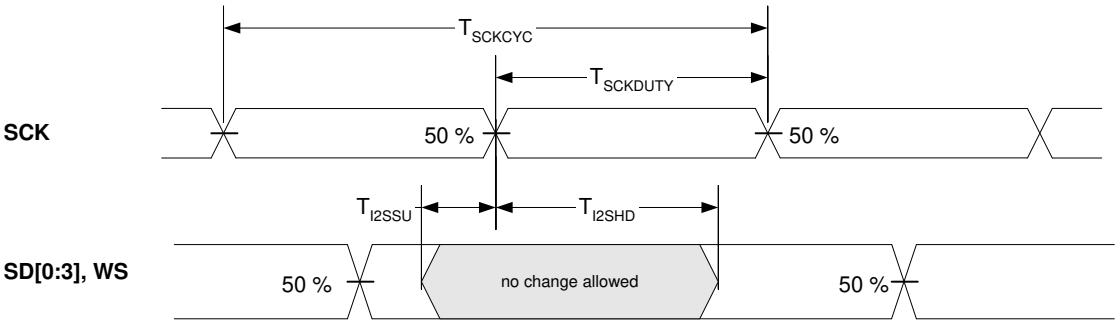


Figure 4.11. I²S Input Timings

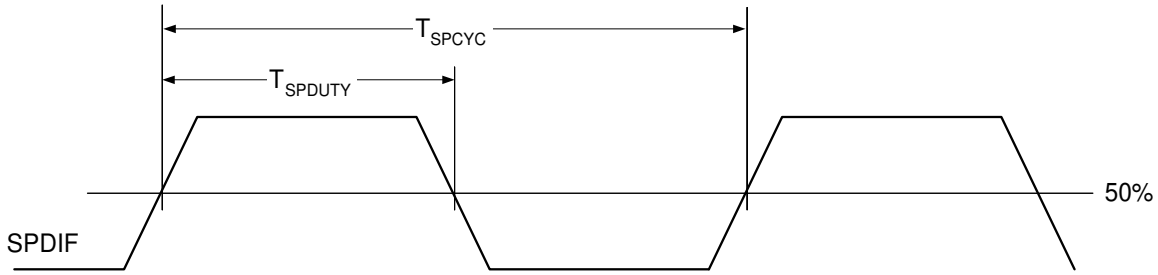


Figure 4.12. S/PDIF Input Timings

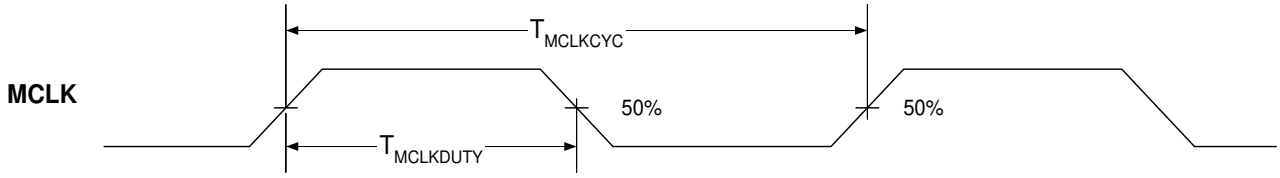


Figure 4.13. MCLK Timings

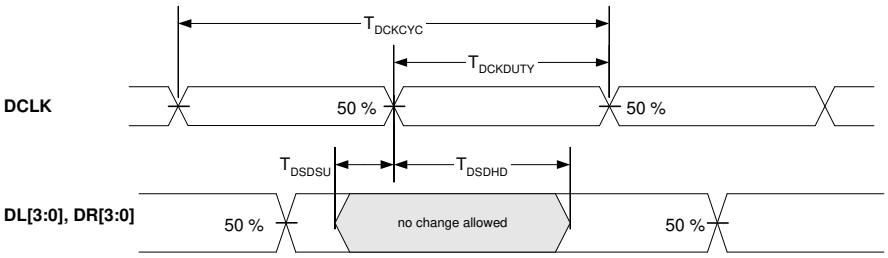


Figure 4.14. DSD Input Timings

4.4.5. I²C Timing Diagrams

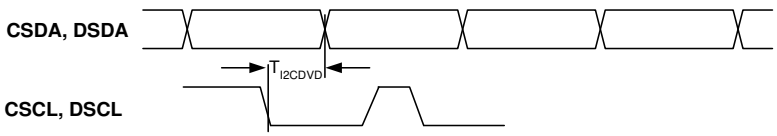


Figure 4.15. I²C Data Valid Delay (Driving Read Cycle Data)

5. Pin Diagram and Descriptions

5.1. Pin Diagram

Figure 5.1 shows the pin diagram for the SiI9136-3/SiI1136 transmitter. A description of the pin functions begins on the next page.

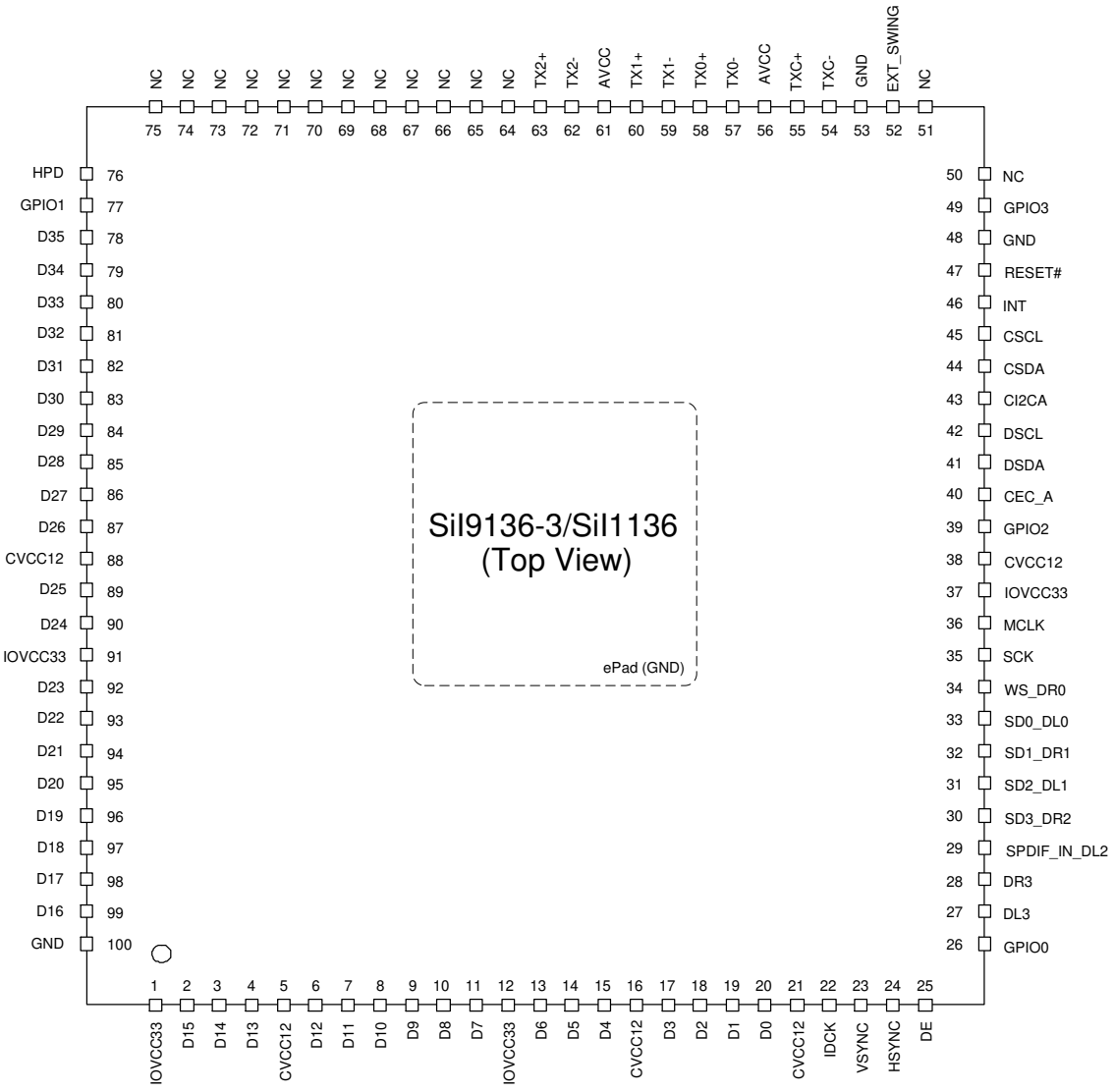


Figure 5.1. Pin Diagram

5.2. Pin Descriptions

5.2.1. Video Data Input

Name	Pin	Type	Dir	Description
D0	20	LVTTL 5 V tolerant	Input	Video Data Inputs. The video data inputs can be configured to support a wide variety of input formats, including multiple RGB and YCbCr bus formats, using the VID_CONFIG registers. See the Common Video Input Formats section on page 33 for details.
D1	19			
D2	18			
D3	17			
D4	15			
D5	14			
D6	13			
D7	11			
D8	10			
D9	9			
D10	8			
D11	7			
D12	6			
D13	4			
D14	3			
D15	2			
D16	99			
D17	98			
D18	97			
D19	96			
D20	95			
D21	94			
D22	93			
D23	92			
D24	90			
D25	89			
D26	87			
D27	86			
D28	85			
D29	84			
D30	83			
D31	82			
D32	81			
D33	80			
D34	79			
D35	78			
IDCK	22	LVTTL 5 V tolerant	Input	Input Data Clock. Input configurable using the VID_CONFIG registers.
DE	25	LVTTL 5 V tolerant	Input	Data Enable. This signal is HIGH when the transmitter input pixel data is valid and LOW otherwise. DE is optional for some input formats, such as ITU-R BT.656.
HSYNC	24	LVTTL 5 V tolerant	Input	Horizontal Sync input control signal. HSYNC is optional for some input formats, such as ITU-R BT.656.
VSYNC	23	LVTTL 5 V tolerant	Input	Vertical Sync input control signal. VSYNC is optional for some input formats, such as ITU-R BT.656.

5.2.2. TMDS Output

Name	Pin	Type	Dir	Description
TX0+	58	TMDS	Output	HDMI Transmitter Output Port Data. TMDS low voltage differential signal output data pairs.
TX0-	57			
TX1+	60			
TX1-	59			
TX2+	63			
TX2-	62			
TXC+	55	TMDS	Output	HDMI Transmitter Output Port Clock. TMDS low voltage differential signal output clock pair.
TXC-	54			
EXT_SWING	52	Analog	Input Output	External Swing Voltage Control. Recommended values (actual value depends on board design): • 5.6 kΩ resistor to ground without using internal termination. • 4.02 kΩ resistor to ground using internal termination.

5.2.3. Audio Input

Name	Pin	Type	Dir	Description	
				I²S Mode; S/PDIF Mode	DSD Mode
MCLK	36	LVTTL 5 V tolerant	Input	Audio Input Master Clock.	—
SCK	35	LVTTL 5 V tolerant	Input	I²S Serial Clock.	DSD Clock.
WS_DR0	34	LVTTL 5 V tolerant	Input	I²S Word Select.	DSD Data Right Bit 0.
SD0_DL0	33	LVTTL 5 V tolerant	Input	I²S Data 0.	DSD Data Left Bit 0.
SD1_DR1	32	LVTTL 5 V tolerant	Input	I²S Data 1.	DSD Data Right Bit 1.
SD2_DL1	31	LVTTL 5 V tolerant	Input	I²S Data 2.	DSD Data Left Bit 1.
SD3_DR2	30	LVTTL 5 V tolerant	Input	I²S Data 3.	DSD Data Right Bit 2.
SPDIF_IN_DL2	29	LVTTL 5 V tolerant	Input	S/PDIF Input.	DSD Data Left Bit 2.
DR3	28	LVTTL 5 V tolerant	Input	—	DSD Data Right Bit 3.
DL3	27	LVTTL 5 V tolerant	Input	—	DSD Data Left Bit 3.

5.2.4. DDC, CEC, Configuration, and Control

Name	Pin	Type	Dir	Description
INT	46	LVTTL	Output	Interrupt Output.
RESET#	47	Schmitt	Input	Reset signal. Active LOW asynchronous reset input for entire chip.
HPD	76	LVTTL	Input	Hot Plug Detect.
GPIO0	26	LVTTL	Input Output	General Purpose I/O Data 0.
GPIO1	77	LVTTL	Input Output	General Purpose I/O Data 1.
GPIO2	39	LVTTL	Input Output	General Purpose I/O Data 2.
GPIO3	49	LVTTL	Input Output	General Purpose I/O Data 3.
DSCL	42	Schmitt Open drain 5 V tolerant	Input Output	DDC I2C Clock. HDCP KSV, An, and Ri values are exchanged over this I2C port during authentication. True open drain, so does not pull to ground if power not applied.
DSDA	41	Schmitt Open drain 5 V tolerant	Input Output	DDC I2C Data. HDCP KSV, An, and Ri values are exchanged over this I2C port during authentication. True open drain, it does not pull to ground if power not applied.
CI2CA	43	LVTTL 5 V tolerant	Input	Selects base address group for CSCL/CSDA interface. See Table 6.3 on page 27.
CSCL	45	Schmitt 5 V tolerant	Input	Local Configuration/Status I2C Clock. Chip configuration/status registers are accessed through this I2C port.
CSDA	44	Schmitt Open drain 5 V tolerant	Input Output	Local Configuration/Status I2C Data. Chip configuration/status registers are accessed through this I2C port.
CEC_A	40	CEC Compliant 5 V tolerant	Input Output	HDMI compliant CEC I/O. As an input, this pin acts as a LVTTL Schmitt-triggered input and is 5 V tolerant. As an output, the pin acts as an NMOS driver with resistive pull-up. This pin has an internal pull-up resistor.

5.2.5. Power and Ground

Name	Pin	Type	Description	Supply
CVCC12	5, 16, 21, 38, 88	Power	Digital Core VCC.	1.2 V
IOVCC33	1, 12, 37, 91	Power	I/O VCC.	3.3 V
AVCC	56, 61	Power	Analog VCC.	1.2 V
GND	48, 53, 100	Ground	These pins must be connected to ground.	Ground

5.2.6. Not Connected and Reserved

Name	Pin	Type	Description	Supply
NC	50, 51, 64–75	Not connected	These pins should be left unconnected.	None