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Silicon Image

PanelLink®

Technology

SiI 1161
PanelLink Receiver

Data Sheet

Document # SiI-DS-0096-D

Silicon Image, Inc.

SiI-DS-0096-D
June 2005

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Revision History

Revision	Date	Comment
-SiI-DS-0096-A	08/2003	Data Sheet
SiI-DS-0096-B	11/2003	Data Sheet Rev B, page 3 - added V_{OL} / I_{OL} spec for SDA pin; page 8 – setup and hold time fixes; page 14 – hold time calculation fixes; page 36 – new signal trace routing example; page 40 – new part number added
SiI-DS-0096-C	1/2004	Part marking spec updated
SiI-DS-0096-D	6/2005	Figure 3, 15, 17, 19, 21, 22, 24, 32 add/update; Ordering Information update; I^2C Reset recommendations, T_{RESET} timing added;

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General Description

The SiI 1161 receiver uses PanelLink Digital technology to support high-resolution displays up to UXGA (25-165MHz). This receiver supports up to true color panels (24 bits per pixel, 16M colors) with both one and two pixels per clock.

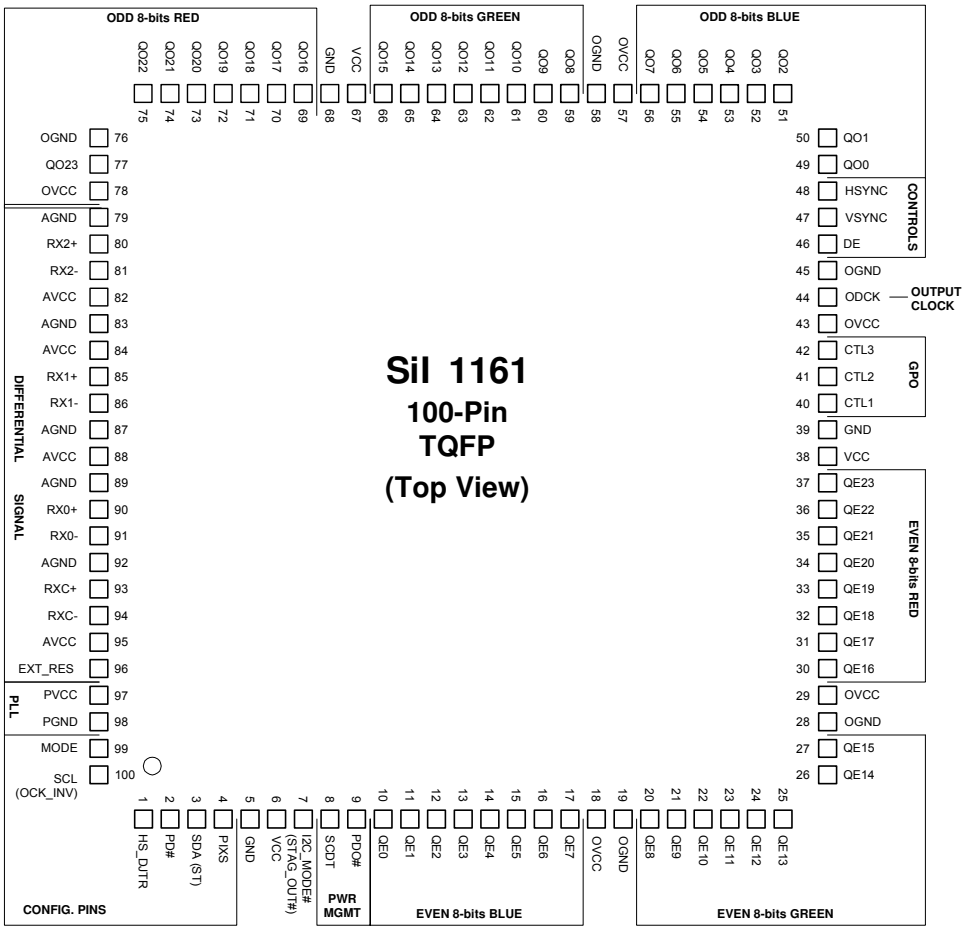
All PanelLink products are designed on a scaleable CMOS architecture, ensuring support for future performance enhancements while maintaining the same logical interface. System designers can be assured that the interface will be stable through a number of technology and performance generations.

PanelLink Digital technology simplifies PC and display interface design by resolving many of the system level issues associated with high-speed mixed signal design, providing the system designer with a digital interface solution that is quicker to market and lower in cost.

Features

- Supports 10 meter cables at UXGA speed
- I^2C port for dynamic optimization of settings to compensate for long cables and/or poor quality transmitters
- Flexible output drive controls to optimize timings for all possible configurations
- 3.3V operation
- Time staggered data output for reduced ground bounce and lower EMI
- Sync Detect feature for DVI “Hot Plugging”
- ESD tolerant to 5kV (HBM) on all pins
- Compliant with DVI 1.0
- Guaranteed interoperability with DVI-compliant transmitters
- Low power standby mode; automatic entry into standby mode with clock detect circuitry
- Pb-free packaging (see page 41).

SiI 1161 Pin Diagram



Functional Description

The SiI 1161 is a DVI 1.0 compliant PanelLink receiver in a compact package. It provides 24 or 48 bits for data output, and allows for panel support up to UXGA. Figure 1 shows the functional blocks of the chip.

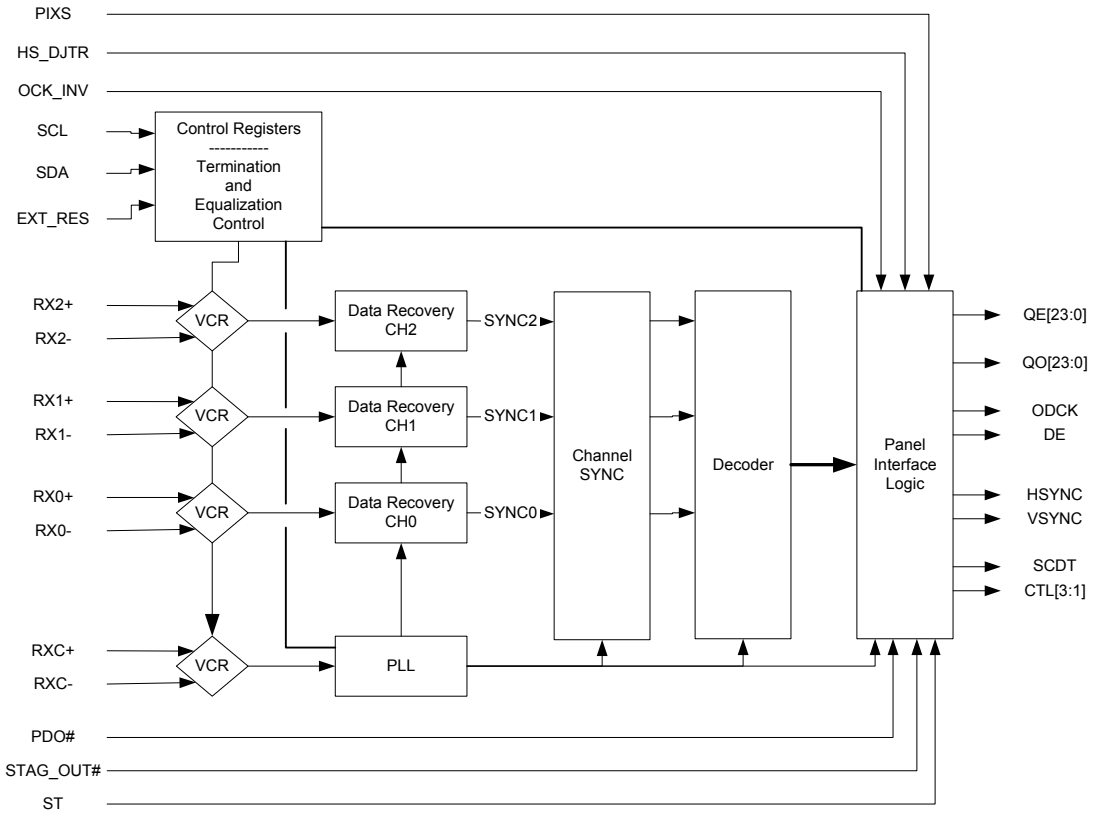


Figure 1. Functional Block Diagram

The PanelLink TMDS core accepts as inputs the three TMDS differential data lines and the differential clock. The core senses the signals on the link and properly decodes them providing accurate pixel data. The core outputs the necessary sync signals (HSYNC, VSYNC), clock (ODCK), and a DE signal that goes high when the active region of the video is present.

The SCDT signal is output when there is active video on the DVI link and the PLL in the TMDS has locked on to the video. SCDT can be used to trigger external circuitry, indicating that an active video signal is present or used to place the device in power down when no signal is present (by tying it to PDO#). The EXT_RES component is used for impedance matching.

Electrical Specifications

Absolute Maximum Conditions

Symbol	Parameter	Min	Typ	Max	Units	Notes
V_{CC}	Supply Voltage 3.3V	-0.3		4.0	V	1
V_I	Input Voltage	-0.3		V_{CC}+ 0.3	V	
V_O	Output Voltage	-0.3		V_{CC}+ 0.3	V	2
T_J	Junction Temperature			125	°C	
T_{STG}	Storage Temperature	-65		150	°C	

Notes

1. Permanent device damage may occur if absolute maximum conditions are exceeded.
2. Functional operation should be restricted to the conditions described under Normal Operating Conditions.

Normal Operating Conditions

Symbol	Parameter	Min	Typ	Max	Units	Notes
V_{CC}	Supply Voltage	3.0	3.3	3.6	V	
V_{CCN}	VCC, OVCC Supply Voltage Noise			200	mV_{P-P}	
AV_{CCN}	AVCC Supply Voltage Noise			100	mV_{P-P}	
PV_{CCN}	PVCC Supply Voltage Noise			75	mV_{P-P}	
T_A	Ambient Temperature (with power applied)	0	25	70	°C	
θ_{JCS}	Thermal Resistance (Junction to Case) soldered		13		°C/W	1
θ_{JAS}	Thermal Resistance (Junction to Ambient) soldered		26		°C/W	1
θ_{JCU}	Thermal Resistance (Junction to Case) unsoldered		19		°C/W	2
θ_{JAU}	Thermal Resistance (Junction to Ambient) unsoldered		58		°C/W	2

Notes

1. Thermal resistance specified with package ePad soldered 100% to underlying PCB pad.
2. Thermal resistance specified with package ePad unsoldered to PCB.

Digital I/O Specifications

Under normal operating conditions unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Units	Notes
V_{IH}	High-level Input Voltage		2			V	
V_{IL}	Low-level Input Voltage				0.8	V	
V_{OH}	High-level Output Voltage		2.4			V	
V_{OL}	Low-level Output Voltage				0.4	V	
V_{OL}(SDA)	Low-level Output Voltage on SDA	I_{OL}(SDA)=3mA			0.4	V	
V_{CINL}	Input Clamp Voltage	I_{CL} = -18mA			GND -0.8	V	1, 2
V_{CIPL}	Input Clamp Voltage	I_{CL} = 18mA			IVCC + 0.8	V	1, 2
V_{CONL}	Output Clamp Voltage	I_{CL} = -18mA			GND -0.8	V	1
V_{COPL}	Output Clamp Voltage	I_{CL} = 18mA			OVCC + 0.8	V	1
I_{OL}	Output Leakage Current	High Impedance	-10		10	µA	

Note

1. Guaranteed by design. Voltage undershoot or overshoot cannot exceed absolute maximum conditions for a pulse of greater than 3 ns or one third of the clock cycle.
2. Applies to toggling inputs only. Strap selected options are fixed at power-up time.

General DC Specifications

Under normal operating conditions unless otherwise specified.

Table 1. DC Parametric Specifications

Symbol	Parameter	Conditions	Min	Typ	Max	Units	Notes
V_{ID}	Differential Input Voltage Single Ended Amplitude		75		1000	mV	
I_{PD}	Power-down Current	PD#=LOW, no RXC+ input			5	mA	3
I_{PDO}	Receiver Supply Current with Outputs Powered Down	ODCK=82.5MHz, 2 pixel per clock mode PDO# = LOW			270	mA	3, 4
I_{CCR}	Receiver Supply Current for Active Device	ODCK=82.5MHz, 0°C 2 pixel per clock mode PDO#=HIGH Typ: Typical Pattern Max: Worst Case Pattern		320	400	mA	1, 2, 4
		ODCK=67.5MHz, 0°C 2 pixel per clock mode PDO#=HIGH Worst Case Pattern			330	mA	2, 4

Notes

1. The Typical Pattern contains a gray scale area, checkerboard area, and text.
2. The Worst Case Pattern consists of a black and white checkerboard pattern; each checker is two pixels wide.
3. Asserting PD# to LOW disables all internal logic and outputs, including SCDT and clock detect functions. The inactive input clock accounts for most of the power reduction.
4. Specified with capacitive load (C_{LOAD}) of 10pF on each output pin, and a worst-case TMDS signal swing of 600mV.

General AC Specifications

Table 2. General AC Specifications

Symbol	Parameter	Conditions	Min	Typ	Max	Units	Notes
T_{DPS}	Intra-Pair (+ to -) Differential Input Skew	165MHz			245	ps	1
T_{CCS}	Channel to Channel Differential Input Skew	165MHz			4	ns	1
T_{IJIT}	Worst Case Differential Input Clock Jitter tolerance	65 MHz			465	ps	2,3
		112 MHz			270	ps	
		165 MHz			182	ps	
R_{CIP}	ODCK Cycle Time (one pixel per clock)	one pixel per clock	6		40	ns	1
F_{CIP}	ODCK Frequency (one pixel per clock)		25		165	MHz	1
R_{CIP}	ODCK Cycle Time (two pixels per clock)	two pixels per clock	12		80	ns	1
F_{CIP}	ODCK Frequency (two pixels per clock)		12.5		82.5	MHz	1
T_{DUTY}	Output Clock Duty Cycle		40%		60%		7
T_{PDL}	Delay PD# / PDO# Low to high-Z outputs				10	ns	1
T_{HSC}	Link disabled (DE inactive) to SCDT low				50	ms	1
T_{FSC}	Link enabled (DE active) to SCDT high		4		10	DE edges	1
T_{CLKPD}	Delay from RXC± Inactive to high-Z outputs				10	µs	
T_{CLKPU}	Delay from RXC± active to data active				100	µs	
T_{ST}	ODCK high to even data output			0.25		R_{CIP}	1
T_{I2CDVD}	SDA Data Valid Delay from SCL high to low transition	C_L = 400pf			700	ns	5
T_{CTLW}	Control Pulse Width		2			R_{CIP}	6
T_{RESET}	PD# Signal Low Time required for a valid I^2C reset		10			µs	1

Notes

1. Guaranteed by design.
2. Jitter defined per DVI 1.0 Specification, Section 4.6 – Jitter Specification.
3. Jitter measured with Clock Recovery Unit per DVI 1.0 Specification, Section 4.7 – Electrical Measurement Procedures.
4. Measured with transmitter powered down.
5. All Standard Mode I^2C (100kHz and 400kHz) timing requirements are guaranteed by design.
6. Control pulses include HSYNC, VSYNC, CTL1, CTL2 and CTL3. Pulses narrower than this minimum width specification are filtered out in the receiver and will not be seen at the output pins.
7. ODCK duty cycle is independent of the differential input clock duty cycle and the transmitter IDCK duty cycle.

DC and AC parameters specific to the operating mode of the SiI 1161 are listed on the following pages.

The output pin timing specifications are dependent on the selection of output drive capability. Specifications are listed for two modes: SiI 161B mode, which requires no I^2C initialization; and SiI 1161 mode, which allows for optimization of input data recovery and output drive using I^2C programming. Designers should choose the mode most suited to their board-level requirements.

Compatibility Mode Selection Specifications

The 1161 design provides new features that were not available on previous TMDS receiver series. To utilize the new features and ensure backwards compatibility, two mode selections have been defined.

SiI 161B (Compatible) Mode: This mode allows drop-in replacement of SiI 161B and other pin-compatible receivers, and provides improved performance over other solutions. Strapping MODE (pin 99) = HIGH selects Compatible Mode.

SiI 1161 (Programmable) Mode. Superior link recovery performance is possible, along with additional output drive timing margin, when this mode is selected. Strapping MODE (pin 99) = LOW and I2C_MODE# (pin 7) = LOW selects Programmable Mode.

SiI 161B (Compatible) Mode DC Specifications

The output drive strength is controlled with the ST pin as indicated in Figure 2.

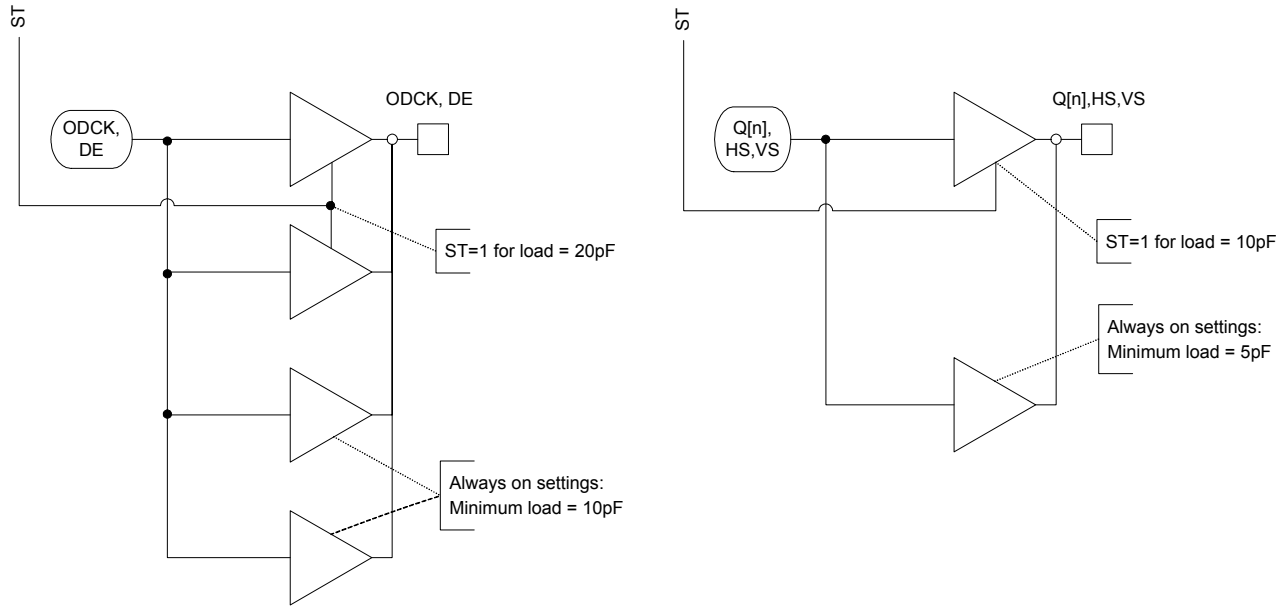


Figure 2. SiI 161B Mode Control of Output Pin Drive Strength

The output drive specifications in the Compatible mode are equivalent to the drive on the SiI 161B part.

Table 3. SiI 161B Mode DC Specifications

Strap option: ST=0 (Low Drive Strength)

Parameter		Conditions			Limits (mA)			Notes
		ST	V_{OUT}	C_L	Min	Typ	Max	
Data and Controls								
I_{OHD}	Output High Drive	0	2.4V	5pF	3.8			1
I_{OLD}	Output Low Drive	0	0.8V	5pF	5.5			2
		0	0.4V	5pF	3.2			3
ODCK and DE								
I_{OHC}	Output High Drive	0	2.4V	10pF	7.5			4
I_{OLC}	Output Low Drive	0	0.8V	10pF	11.1			
		0	0.4V	10pF	6.2			

Strap option: ST=1 (High Drive Strength)

Parameter		Conditions			Limits (mA)			Notes
		ST	V_{OUT}	C_L	Min	Typ	Max	
Data and Controls								
I_{OHD}	Output High Drive	1	2.4V	10pF	7.4			1
I_{OLD}	Output Low Drive	1	0.8V	10pF	11.1			2
		1	0.4V	10pF	6.3			3
ODCK and DE								
I_{OHC}	Output High Drive	1	2.4V	20pF	14.7			4
I_{OLC}	Output Low Drive	1	0.8V	20pF	21.2			
		1	0.4V	20pF	12.3			

Notes

1. Output loading is equivalent to one or two CMOS input loads.
2. 0.8V corresponds to LVTTL V_{IN}(max).
3. 0.4V corresponds to LVCMOS V_{IN}(max).
4. Output loading is equivalent to two or four CMOS input loads.

SiI 161B (Compatible) Mode AC Specifications

AC timings are provided here in setup/hold format at 165MHz for ease of direct comparison to the SiI 161B part. Timing specifications in Table 4 apply to worst-case one pixel per clock mode. For other modes and frequencies use the SiI 1161 Mode timings and calculation methodology, "Calculating Setup and Hold Times" on Page 12.

Table 4. SiI 161B Mode AC Specifications

Strap option: ST=0 (Low Drive Strength)

Parameter		Conditions	Limits (ns)	
Data, HSYNC, VSYNC				**Max**
D_{HLT}	1-to-0 Transition	C_L=5pF		2.5
D_{LHT}	0-to-1 Transition	C_L=5pF		2.0
ODCK, DE				**Max**
D_{HLT}	1-to-0 Transition	C_L=5pF		1.5
D_{LHT}	0-to-1 Transition	C_L=5pF		1.7
Timing @ 165MHz			**Min OCK_INV=0**	**Min OCK_INV=1**
T_{SETUP}	Data	C_L=5pF	0.9	1.2
	DE, HSYNC, VSYNC	C_L=5pF	0.2	0.4
T_{HOLD}	Data	C_L=5pF	2.8	2.4
	DE, HSYNC, VSYNC	C_L=5pF	3.6	2.6

Strap option: ST=1 (High Drive Strength)

Parameter		Conditions	Limits (ns)	
Data, HSYNC, VSYNC				**Max**
D_{HLT}	1-to-0 Transition	C_L=10pF		2.5
D_{LHT}	0-to-1 Transition	C_L=10pF		2.0
ODCK, DE				**Max**
D_{HLT}	1-to-0 Transition	C_L=10pF		1.2
D_{LHT}	0-to-1 Transition	C_L=10pF		1.4
Timing @ 165MHz			**Min OCK_INV=0**	**Min OCK_INV=1**
T_{SETUP}	Data	C_L=10pF	0.9	1.2
	DE, HSYNC, VSYNC	C_L=10pF	0.6	1.1
T_{HOLD}	Data	C_L=10pF	2.8	2.2
	DE, HSYNC, VSYNC	C_L=10pF	3.1	2.1

Notes

1. All transitions are specified at worst case of 70ºC with minimum VCC.
2. ODCK and DE output pins should be loaded with 10pF when ST=0 and 20pF when ST=1. If layout requires only a point-to-point, one load net, a discrete 10pF capacitor should be added to the net to create these loads. See Figure 3.

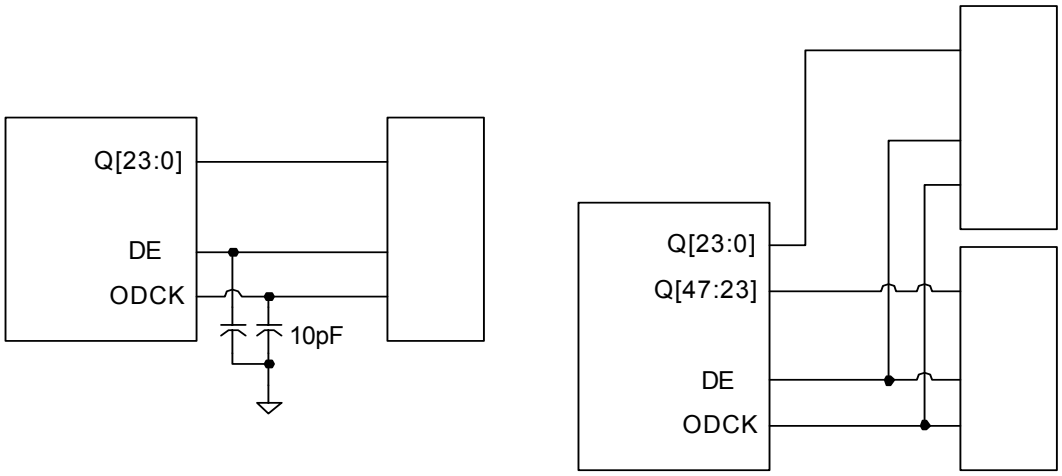


Figure 3. Output Loading in SiI 161B Mode

SiI 1161 (Programmable) Mode DC Specifications

The SiI 1161 provides an internal register, accessible via I^2C, to match the drive strengths of the output data, control and ODCK pins. This arrangement allows more flexibility in driving diverse loading configurations as shown in Figure 4.

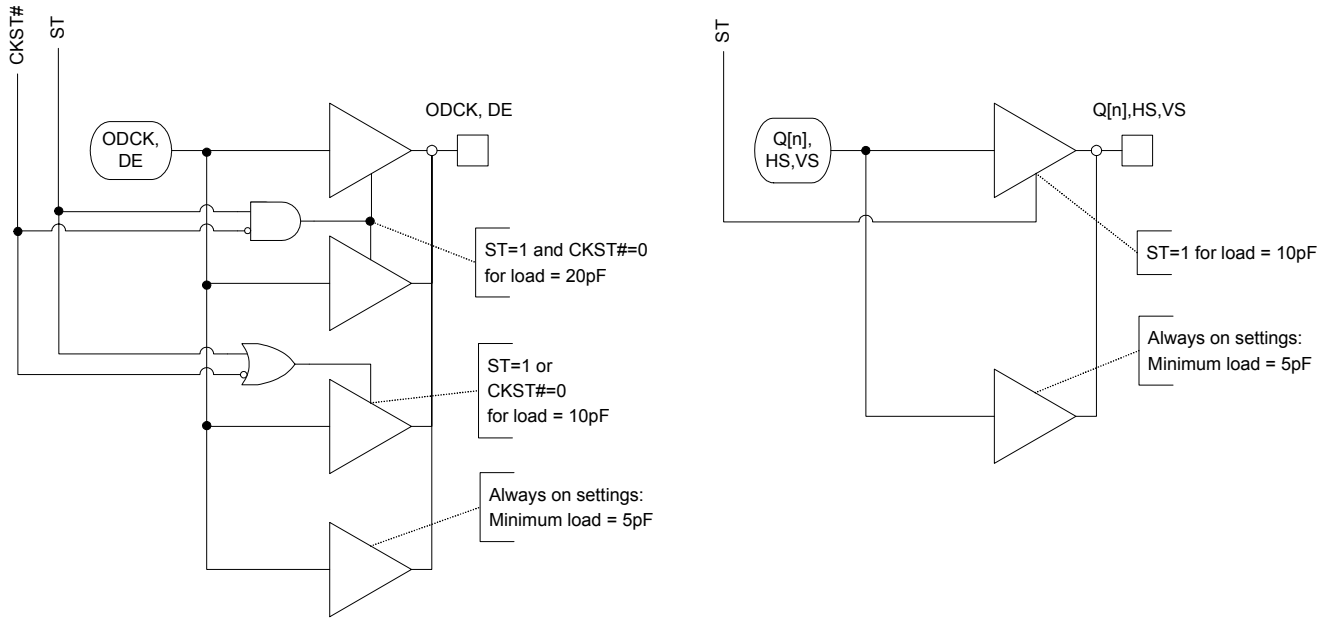


Figure 4. SiI 1161 Mode Control of Output Pin Drive Strength

Table 5. SiI 1161 Mode DC Specifications

Program Option: ST=0[1] (Low Drive Strength)

Parameter		Conditions		Limits (mA)	Notes
		CKST[1]	V_{OUT}	Min	
Data and Controls					
I_{OHD}	Output High Drive	X	2.4V	3.8	
I_{OLD}	Output Low Drive	X	0.8V	5.5	3
		X	0.4V	3.2	4
ODCK and DE					
I_{OHC}	Output High Drive	1	2.4V	3.6	
		0	2.4V	7.5	
I_{OLC}	Output Low Drive	1	0.8V	5.4	3
		0	0.8V	11.1	3
		1	0.4V	2.9	4
		0	0.4V	6.2	4

Program Option: ST=1[1] (High Drive Strength)

Parameter		Conditions		Limits (mA)	Notes
		CKST[1]	V_{OUT}	Min	
Data and Controls					
I_{OHD}	Output High Drive	X	2.4V	7.4	
I_{OLD}	Output Low Drive	X	0.8V	11.1	3
		X	0.4V	6.3	4
ODCK and DE					
I_{OHC}	Output High Drive	1	2.4V	7.2	
		0	2.4V	14.7	
I_{OLC}	Output Low Drive	1	0.8V	10.4	3
		0	0.8V	21.2	3
		1	0.4V	6.0	4
		0	0.4V	12.3	4

Notes

1. CKST and ST are controlled with bits in an I^2C register, not from pins, in Programmable Mode.
2. Output loading is equivalent to one, two or four CMOS input loads.
3. 0.8V corresponds to LVTTL V_{IN}(max).
4. 0.4V corresponds to LVCMOS V_{IN}(max).

SiI 1161 (Programmable) Mode AC Specifications

SiI 1161 Mode AC timings are based on "Clock to Output" (CK2OUT) timing measurements. This methodology provides a precise means of calculating setup and hold at any frequency and in any chip operating mode. C_L indicates the load on the ODCK line. The load on the data/control line involved depends on CKST: for CKST=1, the control/data pin load is C_L; for CKST=0, the load is 2x C_L.

Table 6. SiI 1161 Mode AC Specifications

Program Option: ST=0 (Low Drive Strength)

Parameter		Conditions			Limits (ns)			
Data, HSYNC, VSYNC		**CKST**	**ST**	**C_L**			**Max**	
D_{HLT}	1-to-0 Transition	X	0	5pF			2.5	
D_{LHT}	0-to-1 Transition	X	0	5pF			2.0	
ODCK, DE		**CKST**	**ST**	**C_L**			**Max**	
D_{HLT}	1-to-0 Transition	1	0	5pF	1X clock drive		2.5	
		0	0	10pF	2X clock drive		1.5	
D_{LHT}	0-to-1 Transition	1	0	5pF	1X clock drive		2.7	
		0	0	10pF	2X clock drive		1.7	
Clock-to-Output Timing		**CKST**	**ST**	**C_L**	**Min**		**Max**	
				OCK_INV Setting→	**0**	**1**	**0**	**1**
T_{CK2OUT}	ODCK to Data	1	0	5pF	0.4	0.0	1.5	1.2
		0	0	10pF	0.4	-0.1	1.5	1.0
T_{CK2OUT}	ODCK to DE, HSYNC, VSYNC	1	0	5pF	1.2	0.2	2.2	2.0
		0	0	10pF	0.8	0.1	2.2	1.7

Program Option: ST=1 (High Drive Strength)

Parameter		Conditions			Limits (ns)			
Data, HSYNC, VSYNC		**CKST**	**ST**	**C_L**			**Max**	
D_{HLT}	1-to-0 Transition	X	1	10pF			2.5	
D_{LHT}	0-to-1 Transition	X	1	10pF			2.0	
ODCK, DE		**CKST**	**ST**	**C_L**			**Max**	
D_{HLT}	1-to-0 Transition	1	1	10pF	2X clock drive		1.9	
		0	1	20pF	4X clock drive		1.2	
D_{LHT}	0-to-1 Transition	1	1	10pF	2X clock drive		1.7	
		0	1	20pF	4X clock drive		1.4	
Clock-to-Output Timing		**CKST**	**ST**	**C_L**	**Min**		**Max**	
				OCK_INV Setting→	**0**	**1**	**0**	**1**
T_{CK2OUT}	ODCK to Data	1	1	10pF	0.4	-0.2	1.5	1.2
		0	1	20pF	0.0	-0.8	1.4	1.0
T_{CK2OUT}	ODCK to DE, HSYNC, VSYNC	1	1	10pF	0.7	-0.3	1.8	1.3
		0	1	20pF	0.1	-0.3	1.9	1.0

Notes

1. Output loading is equivalent to one (5pF), two (10pF) or four (20pF) CMOS input loads.
2. All transition time specifications at 70°C, minimum VCC.
3. Timing specifications in Table 6 apply to both one pixel per clock and two pixel per clock modes.

Calculating Setup and Hold Times

Output setup and hold times between video output clock (ODCK) and video data (including HSYNC, VSYNC and DE) are functions of the worst case duty cycle specification for ODCK and the worst case clock to output delay. For the SiI 1161 output pins, only the minimum output setup and hold times are critical.

The SiI 1161 provides the OCK_INV feature, described on page 22, to allow external logic to decode data with either a rising or falling clock edge.

OCK_INV=0 Case

For OCK_INV=0, the worst-case setup time occurs when the clock to output delay is at a maximum (latest data) and the ODCK duty cycle is at a minimum (earliest falling edge). Conversely, the worst case hold time occurs when the clock to output delay is at a minimum (earliest next data) and the ODCK duty cycle is at a maximum (latest falling edge). This is shown in Figure 5. The falling active ODCK edge is shown with an arrowhead.

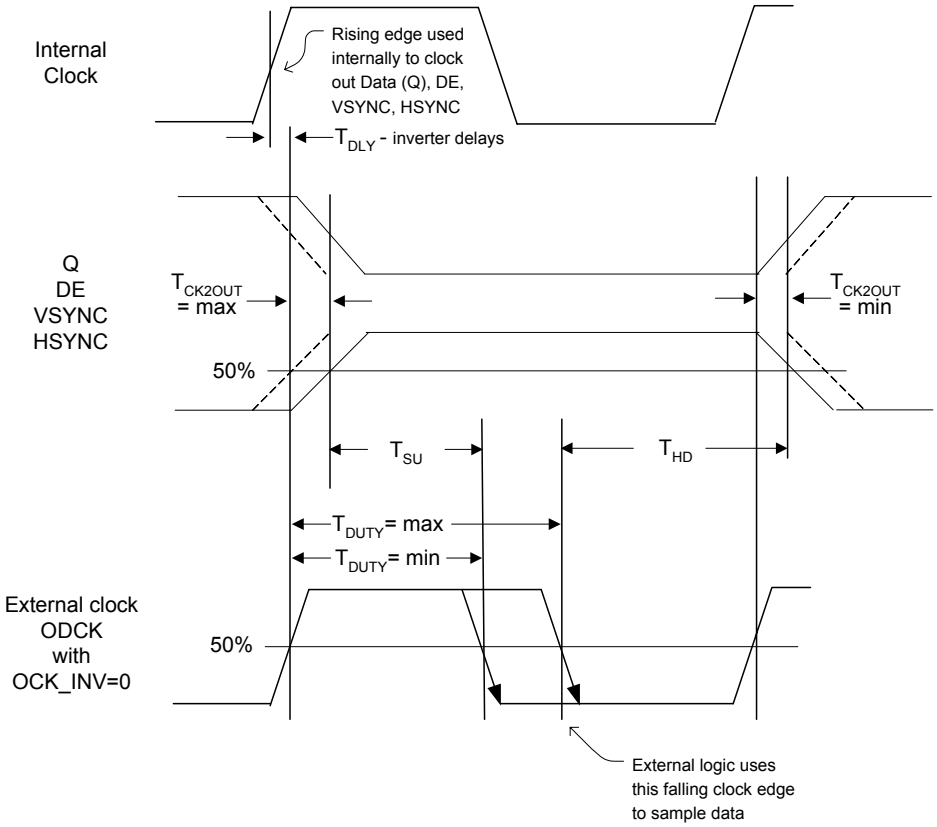


Figure 5. Receiver Output Setup and Hold Times – OCK_INV=0

Note: For Staggered Output timing in 2Pix/clk mode, refer to Figure 15.

Actual setup and hold times can be derived from the clock period at the operating frequency of interest. Clock duty cycle must also be taken into account when calculating setup and hold times.

Setup Time to ODCK: $T_{ODCK}*T_{DUTY}\{min\} - T_{CK2OUT}\{max\}$

Hold Time from ODCK: $T_{ODCK}* (1 - T_{DUTY}\{max\}) + T_{CK2OUT}\{min\}$

Table 7 shows the calculations required for determining setup and hold timings using the clock period T_{ODCK} specific to the clock frequency, also bringing in the clock duty cycle as required when OCK_INV=0. The setup and hold times apply to DE, VSYNC, HSYNC and Data output pins, as long as the appropriate T_{CK2OUT} value is used for the calculation in each case. The table also shows calculated setup and hold times for commonly used ODCK frequencies.

Table 7. Sample Calculation of Data Output Setup and Hold Times – OCK_INV=0

Symbol	Parameter	Frequency	T_{ODCK}	T_{CK2OUT} (data)	Result
T_{SU}	**Data Setup Time** to ODCK	25 MHz	40 ns	Max	=40*40% - 1.5 = 14.5ns
	=T_{ODCK}*T_{DUTY}{min}	82.5 MHz	12 ns	=1.5	=12*40% - 1.5 = 3.3ns
	-T_{CK2OUT}{max}	165 MHz	6 ns		=6*40% - 1.5 = 0.9ns
T_{HD}	**Data Hold Time** from ODCK	25 MHz	40 ns	Min	=40*40% + 0.4 = 16.4ns
	=T_{ODCK}* (1 - T_{DUTY}{max})	82.5 MHz	12 ns	=0.4	=12*40% + 0.4 = 5.2ns
	+ T_{CK2OUT}{min}	165 MHz	6 ns		=6*40% + 0.4 = 2.8ns

OCK_INV=1 Case

For OCK_INV=1, the timing is similar to that previously discussed. The worst-case setup time occurs when the clock to output delay is at a maximum (latest data) and the ODCK duty cycle is at a minimum (earliest falling edge). Conversely, the worst case hold time occurs when the clock to output delay is at a minimum (earliest next data) and the ODCK duty cycle is at a maximum (latest falling edge). This timing relationship is shown in Figure 6. The rising active ODCK edge is shown with an arrowhead.

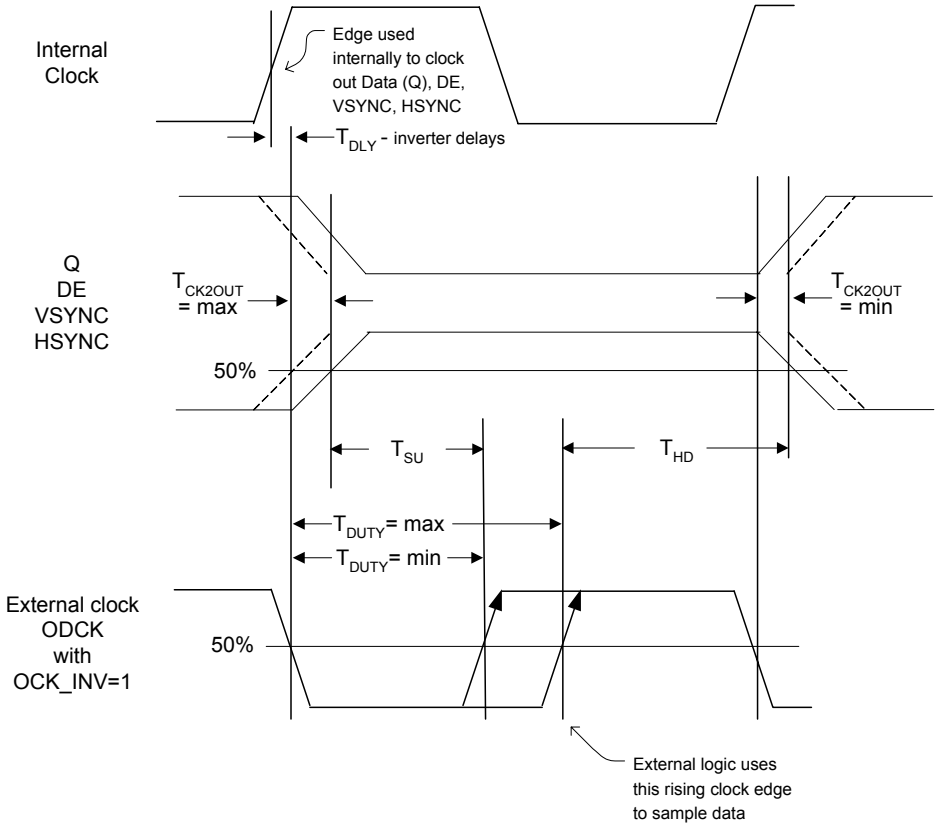


Figure 6. Receiver Output Setup and Hold Times – OCK_INV=1

Note: For Staggered Output timing in 2Pix/clk mode, refer to Figure 15.

Actual setup and hold times can be derived from the clock period at the operating frequency of interest. Clock duty cycle must also be taken into account when calculating setup and hold times.

Setup Time to ODCK: $T_{ODCK}*T_{DUTY}\{min\} - T_{CK2OUT}\{max\}$

Hold Time from ODCK: $T_{ODCK}* (1 - T_{DUTY}\{max\}) + T_{CK2OUT}\{min\}$

Table 8 shows the calculations required for determining setup and hold timings using the clock period T_{ODCK} specific to the clock frequency when OCK_INV=1. The setup and hold times apply to DE, VSYNC, HSYNC and Data output pins, as long as the appropriate T_{CK2OUT} value is used for the calculation in each case. The table also shows calculated setup and hold times for commonly used ODCK frequencies.

Table 8. Sample Calculation of Data Output Setup and Hold Times – OCK_INV=1

Symbol	Parameter	Frequency	T_{ODCK}	T_{CK2OUT} (data)	Result
T_{SU}	**Data Setup Time** to ODCK	25 MHz	40 ns	Max	=40*40% - 1.2 = 14.8ns
	$=T_{ODCK}*T_{DUTY}\{min\}$	82.5 MHz	12 ns	=1.2	=12*40% - 1.2 = 3.6ns
	$-T_{CK2OUT}\{max\}$	165 MHz	6 ns		=6*40% - 1.2 = 1.2ns
T_{HD}	**Data Hold Time** from ODCK	25 MHz	40 ns	Min	=40*40% - 0.0 = 16.0ns
	$=T_{ODCK}* (1 - T_{DUTY}\{max\})$	82.5 MHz	12 ns	=0.0	=12*40% - 0.0 = 4.8ns
	$+ T_{CK2OUT}\{min\}$	165 MHz	6 ns		=6*40% - 0.0 = 2.4ns

Timing Diagrams

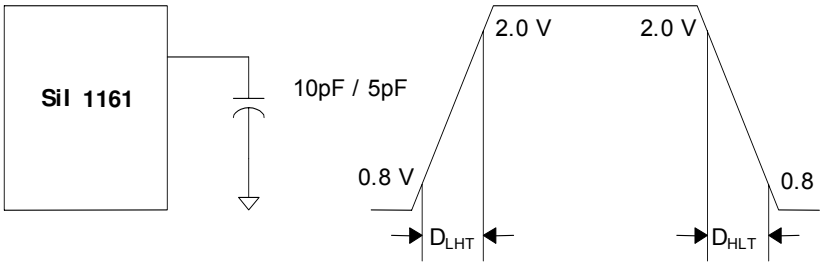


Figure 7. Digital Output Transition Times

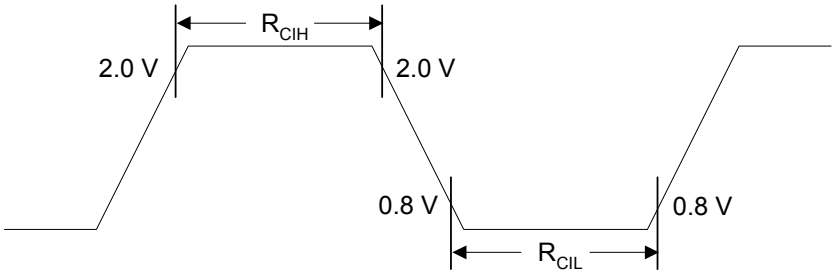


Figure 8. Receiver Clock Cycle/High/Low Times

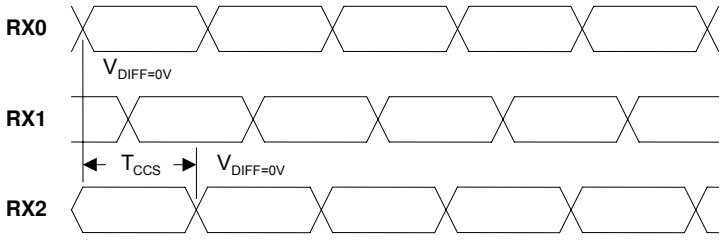


Figure 9. Channel-to-Channel Skew Timing

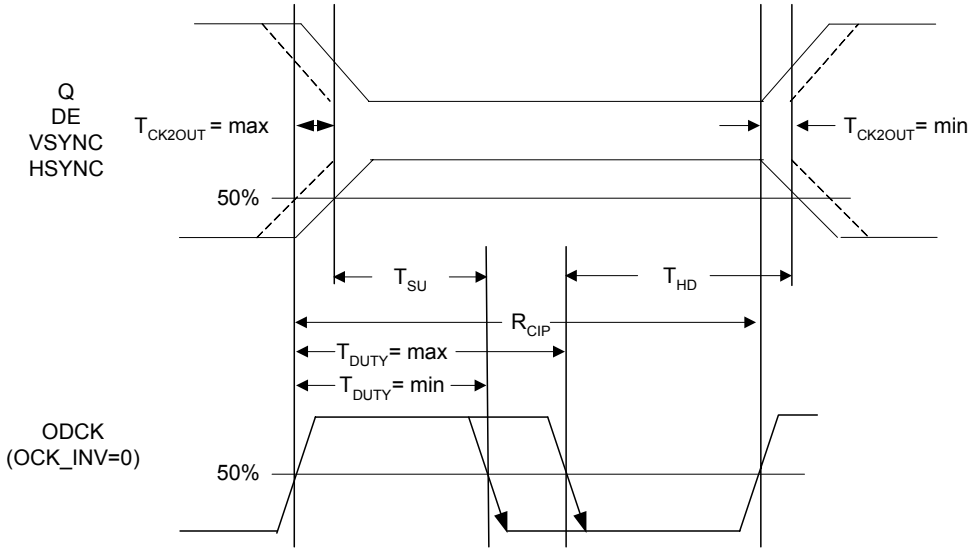


Figure 10. Receiver Clock-to-Output Delay and Duty Cycle Limits

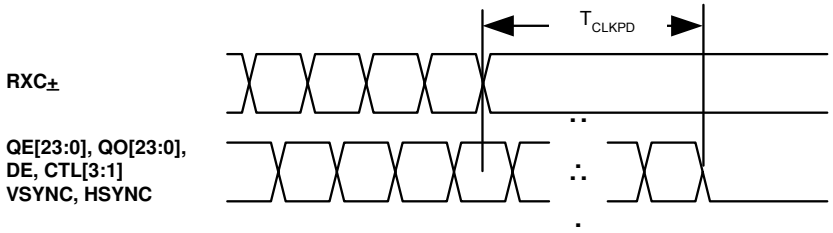


Figure 11. Output Signals Disabled Timing from Clock Inactive

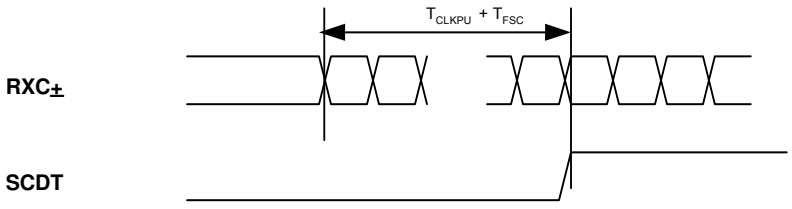


Figure 12. Wake-Up on Clock Detect

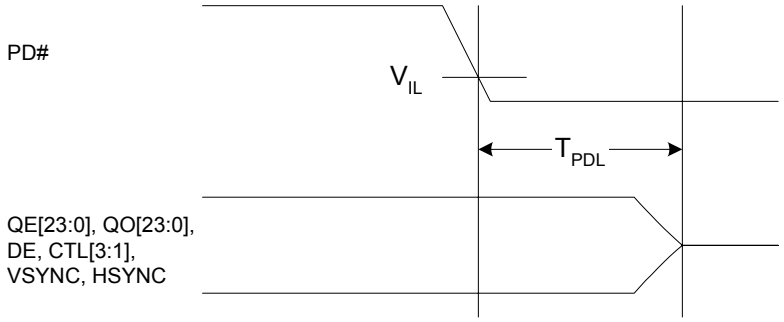


Figure 13. Output Signals Disabled Timing from PD# Active

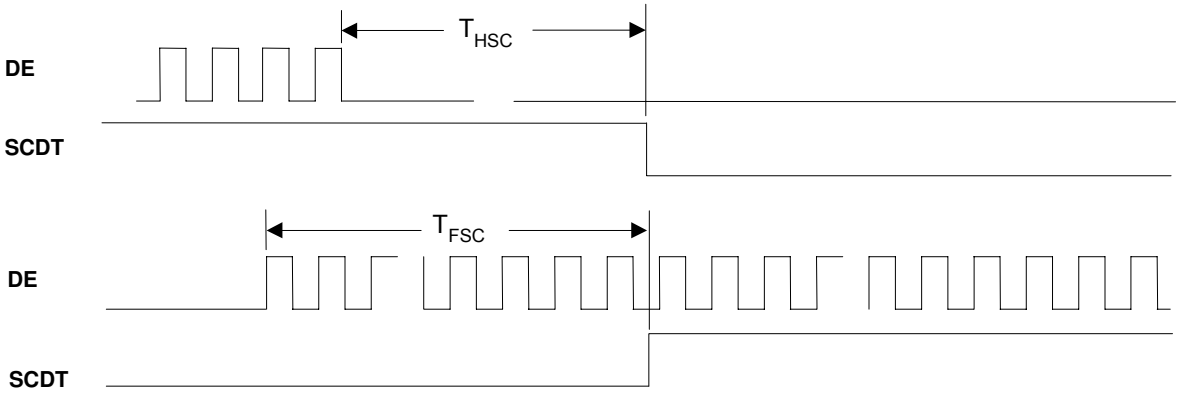


Figure 14. SCDT Timing from DE Inactive or Active

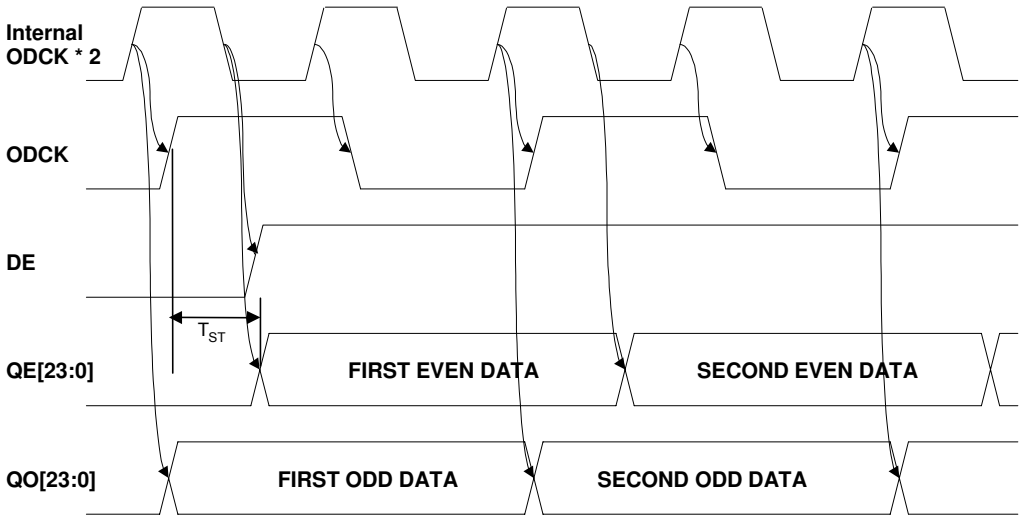


Figure 15. Two Pixels per Clock Staggered Output Timing Diagram

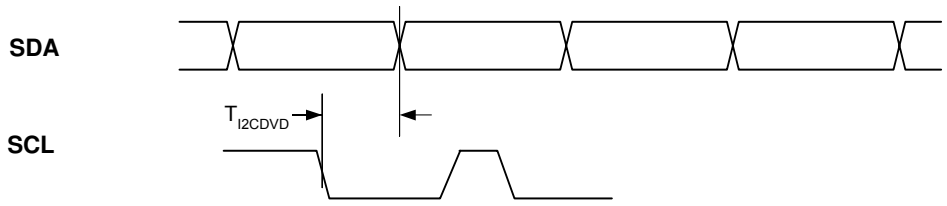


Figure 16. I²C Data Valid Delay (driving Read Cycle data)

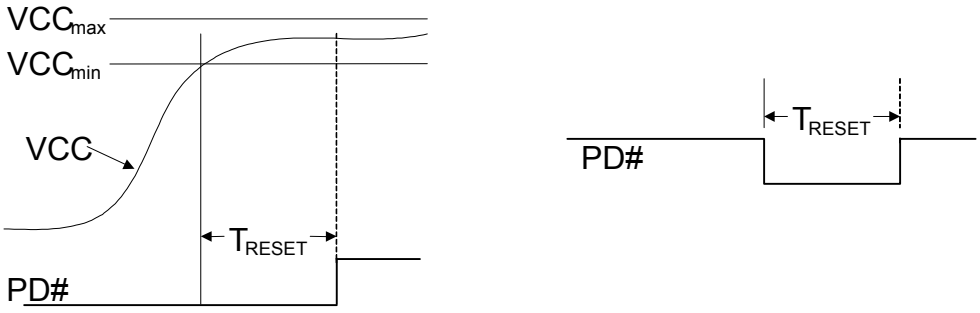


Figure 17. I²C Reset Timing at Power-Up or Prior to first I²C Acess

Pin Descriptions

Output Pins

Pin Name	Pin #	Type	Description
QE23-QE0	See SiI 1161 Pin Diagram	Out	Output Even Data[23:0] corresponds to 24-bit pixel data for one pixel per clock input mode and to the first 24-bit pixel data for two pixels per clock mode. Output data is synchronized with output data clock (ODCK). Refer to the TFT Panel Data Mapping section, which tabulates the relationship between the input data to the transmitter and output data from the receiver. A low level on PD# or PDO# will put the output drivers into a high impedance (tri-state) mode. A weak internal pull-down device brings each output to ground.
QO23-QO0	See SiI 1161 Pin Diagram	Out	Output Odd Data[23:0] corresponds to the second 24-bit pixel data for two pixels per clock mode. During one pixel per clock mode, these outputs are driven low. Output data is synchronized with output data clock (ODCK). Refer to the TFT Panel Data Mapping section, which tabulates the relationship between the input data to the transmitter and output data from the receiver. A low level on PD# or PDO# will put the output drivers into a high impedance (tri-state) mode. A weak internal pull-down device brings each output to ground.
ODCK	44	Out	Output Data Clock. This output can be inverted using the OCK_INV pin. A low level on PD# or PDO# will put the output driver into a high impedance (tri-state) mode. A weak internal pull-down device brings the output to ground.
DE	46	Out	Output Data Enable. This signal qualifies the active data area. A HIGH level signifies active display time and a LOW level signifies blanking time. This output signal is synchronized with the output data. A low level on PD# or PDO# will put the output driver into a high impedance (tri-state) mode. A weak internal pull-down device brings the output to ground.
HSYNC VSYNC CTL1 CTL2 CTL3	48 47 40 41 42	Out	Horizontal Sync output control signal. Vertical Sync output control signal. General output control signal 1. This output is **not** powered down by PDO#. General output control signal 2. General output control signal 3. A low level on PD# or PDO# will put the output drivers (except CTL1 by PDO#) into a high impedance (tri-state) mode. A weak internal pull-down device brings each output to ground.

Differential Signal Data Pins

Pin Name	Pin #	Type	Description
RX0+ RX0- RX1+ RX1- RX2+ RX2-	90 91 85 86 80 81	Analog	Receiver Differential Data Pins. TMDS Low Voltage Differential Signal input data pairs.
RXC+ RXC-	93 94	Analog	Receiver Differential Clock Pins. TMDS Low Voltage Differential Signal input clock pair.
EXT_RES	96	Analog	Impedance Matching Control. An external 390Ω resistor must be connected between AVCC and this pin.

Configuration Pins

Pin Name	Pin #	Type	Description
MODE	99	In	Mode Select Pin. Used to select between drop-in strap-selected operation, or register-programmable operation. To activate register-programmable operation, tie both pin 99 and pin 7 LOW. Refer to Selecting SiI 1161 (Programmable) Mode on page 31 for more details. HIGH=161B (Compatible) Mode – strap selections are used to set part operation. Internal registers controlling non strap-selectable functions are reset to their default values. LOW=1161 (Programmable) Mode – I^2C registers are used to program part operation.
OCK_INV	100	In	ODCK Polarity. A LOW level selects normal ODCK output. A HIGH level selects inverted ODCK output. All other output signals are unaffected by this pin. They will maintain the same timing no matter the setting of OCK_INV pin
SCL			I^2C Port Clock. When pins 99 and 7 are tied LOW, pin 100 functions as an I^2C port input clock. The slave I^2C function does not ever try to extend cycles by pulling this pin low, so the pin remains input-only at all times. Refer to Selecting SiI 1161 (Programmable) Mode on page 31 for more details. This pin accepts 3.3V signaling only; it is not 5V-tolerant.
PIXS	4	In	Pixel Select. A LOW level indicates one pixel (up to 24-bits) per clock mode using QE[23:0]. A HIGH level indicates two pixels (up to 48-bits) per clock mode using QE[23:0] for first pixel and QO[23:0] for second pixel.
STAG_OUT#	7	In	Staggered Output. A HIGH level selects normal simultaneous outputs on all odd and even data lines. A LOW level selects staggered output drive. This function is only available in two pixels per clock mode.
I2C_MODE#			This pin must be tied LOW to put the receiver into I^2C mode. Refer to Selecting SiI 1161 (Programmable) Mode on page 31 for more details.
ST	3	In/ Out	Output Drive. A HIGH level selects HIGH output drive strength. A LOW level selects LOW output drive strength.
SDA			I^2C Port Data. When pins 99 and 7 are tied LOW, pin 3 functions as an I^2C port data I/O signal. Refer to Selecting SiI 1161 (Programmable) Mode on page 31 for more details. This pin accepts 3.3V signaling only; it is not 5V-tolerant. The I^2C address of the SiI 1161 is 0x76
HS_DJTR	1	In	HSYNC De-jitter. This pin enables/disables the HSYNC de-jitter function. To enable the HSYNC de-jitter function this pin should be HIGH. To disable the HSYNC de-jitter function this pin should be LOW.

Power Management Pins

Pin Name	Pin #	Type	Description
SCDT	8	Out	Sync Detect. A HIGH level is outputted when DE is actively toggling indicating that the link is alive. A LOW level is outputted when DE is inactive, indicating the link is down. Can be connected to PDO# to power down the outputs when DE is not detected. The SCDT output itself, however, remains in the active mode at all times.
PDO#	9	In	Output Driver Power Down (active LOW). A HIGH level indicates normal operation. A LOW level puts all the output drivers only (except SCDT and CTL1) into a high impedance (tri-state) mode. A weak internal pull-down device brings each output to ground. PDO# is a sub-set of the PD# description. The chip is not in power-down mode with this pin. SCDT and CTL1 are not tri-stated by this pin. I^2C access to the registers is available when PDO#=0.
PD#	2	In	Power Down (active LOW). A HIGH level indicates normal operation. A LOW level indicates power down mode. During power down mode, all the output drivers are put into a high impedance (tri-state) mode. A weak internal pull-down device brings each output to ground. Additionally, all analog logic is powered down, and all inputs are disabled. Driving PD# LOW disables all internal logic and outputs, including SCDT and clock detect functions; it also resets all internal programmable registers to their default states. I^2C access to the registers is disabled when PD#=0.

Power and Ground Pins

Pin Name	Pin #	Type	Description
VCC	6,38,67	Power	Digital Core VCC, must be set to 3.3V.
GND	5,39,68	Ground	Digital Core GND.
OVCC	18,29,43,57,78	Power	Output VCC, must be set to 3.3V.
OGND	19,28,45,58,76	Ground	Output GND.
AVCC	82,84,88,95	Power	Analog VCC must be set to 3.3V.
AGND	79,83,87,89,92	Ground	Analog GND.
PVCC	97	Power	PLL Analog VCC must be set to 3.3V.
PGND	98	Ground	PLL Analog GND.