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SiI8788 Analog Front-end Video Processor with Parallel Video Output

Data Sheet

SiI-DS-1123-A

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1. General Description

The Lattice Semiconductor SiI8788 processor is a high quality Analog Front-end (AFE) and multistandard composite or component Video Decoder (VDC). A microcontroller is integrated to reduce the system BOM cost.

The SiI8788 processor supports worldwide PAL, NTSC and SECAM standards, YP_bP_r video signals up to 1080p @ 60 Hz resolution.

The device contains a Time Base Correction (TBC) module, a de-interlacer with a post-processor engine and a VBI decoder.

1.1. Features

1.1.1. Analog (Video) Front-end

- Four 10-bit Analog-to-Digital Converters (ADC) sampling up to 170 MHz
- Flexible input multiplexers to support four composite and two component video inputs
- Support cable plug-in detection and active video signal detection

1.1.2. Multi-format Video Decoder

- Automatic format detection
- Supports NTSC, PAL, and SECAM standards of composite input with adaptive comb filter
- Supports 240p/288p, 480i/p, 576i/p, 720p, 1080i/p component video
- Supports Macrovision Type I, II, III copy protection detection
- Supports multistandard VBI decoding: WSS, VPS, CC, CGMS, and V-CHIP

1.1.3. Video Processing

- Time Base Correction
- De-interlacer with Edge Smoothing
- Automatic Phase/Position Detection

1.1.4. 24-bit Parallel Output

- Supports 24-bit RGB/YC_bC_r 4:4:4 and 12-bit RGB/YC_bC_r 4:4:4 Double Data Rate (DDR) modes
- Supports 24-bit YC_bC_r 4:2:2 and 12-bit YC_bC_r 4:2:2 DDR modes
- Supports 8/10/12-bit YC MUX 4:2:2 modes
- Supports embedded sync for YC_bC_r 4:2:2 and YC MUX 4:2:2 modes
- Supports embedded raw VBI data (CC, WSS)

1.2. Applications

The SiI8788 device is targeted at the home theatre and profession/commercial markets, specifically in A/V Receiver and Video Switcher / Processor applications

1.3. Packaging

- 88-pin QFN with exposed pad (ePad)
- 10 mm × 10 mm × 0.9 mm

1.4. Temperature Range

- 0 °C to +70 °C

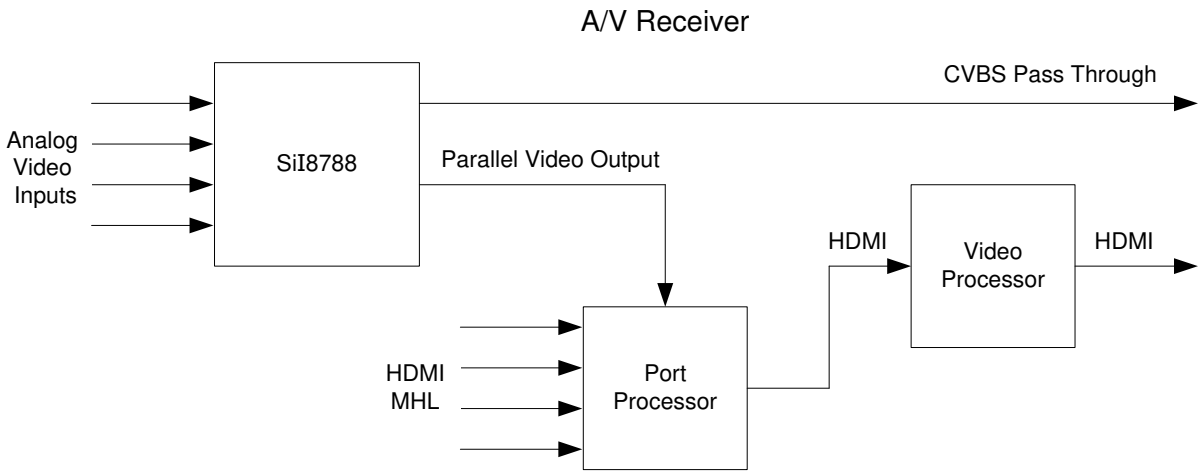

Figure 1.1. Typical Application of the SiI8788 Device

2. Product Family

A comparison of the features between the SiI8788 device and the SiI8784 device is shown in Table 2.1.

Table 2.1. Product Selection Guide

Feature	SiI8784	SiI8788
Analog Video Input		
Component Ports	YES	YES
Composite Ports (CVBS)	YES	YES
D-connector Support	YES	NO
VGA Support	YES	NO
SCART (FB/FS) Support	YES	NO
Video Output		
Parallel Digital	NO	YES
CVBS	YES	YES
HDMI	YES	NO
MHL	YES	NO
Audio Input		
SPDIF Input	YES	NO
I^2S Input	YES	NO
Package		
Package Type	QFN	QFN
Pin Count	88	88

3. Functional Description

The SiI8788 device has a multiformat AFE with 4 ADC channels to support multiple analog video inputs. The SiI8788 device offers four CVBS video inputs, two component video inputs and one parallel video output. Figure 3.1 shows the block diagram of the input processor.

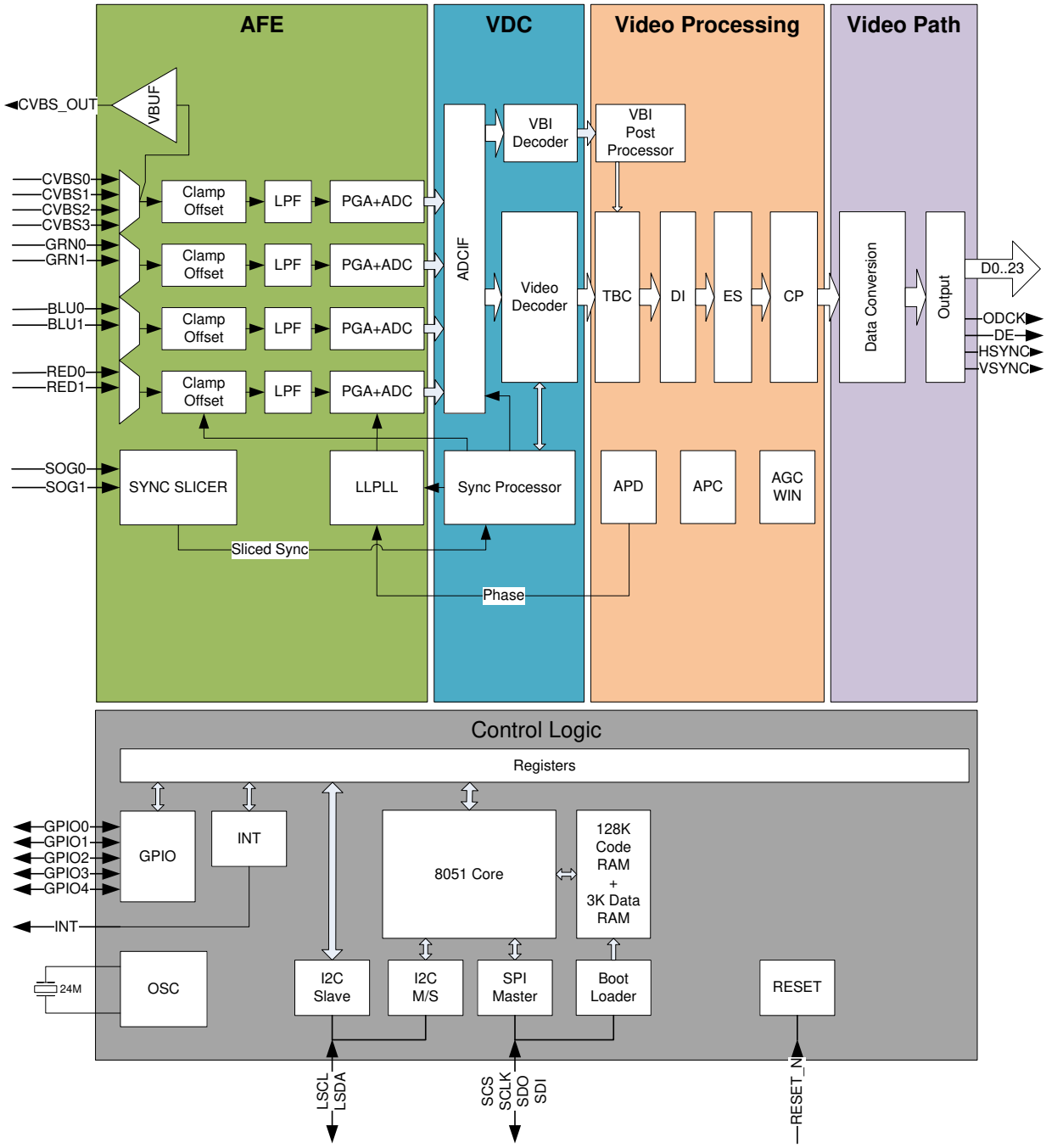

Figure 3.1. Functional Block Diagram

Each of the blocks is explained in detail in the following sections.

3.1. Analog Front-end

The Analog Front-end (AFE) provides four input channels for CVBS, R, G and B. Each channel includes an Input Multiplexer, a Clamp and Offset DAC, a Programmable Low Pass Filter, and a high quality 10-bit ADC with Programmable Gain Amplifier. In addition, there is a Line Locked PLL to generate sample clocks for ADCs and Sync Slicers to handle SOG signals.

3.1.1. Input Multiplexer

The SiI8788 device provides four CVBS inputs and two sets of components inputs.

3.1.2. Clamp and Offset

As most of the video signals, such as CVBS, are AC coupled, their DC component is lost during the transmission. A voltage type clamp circuit is positioned in front of each channel to restore the DC component.

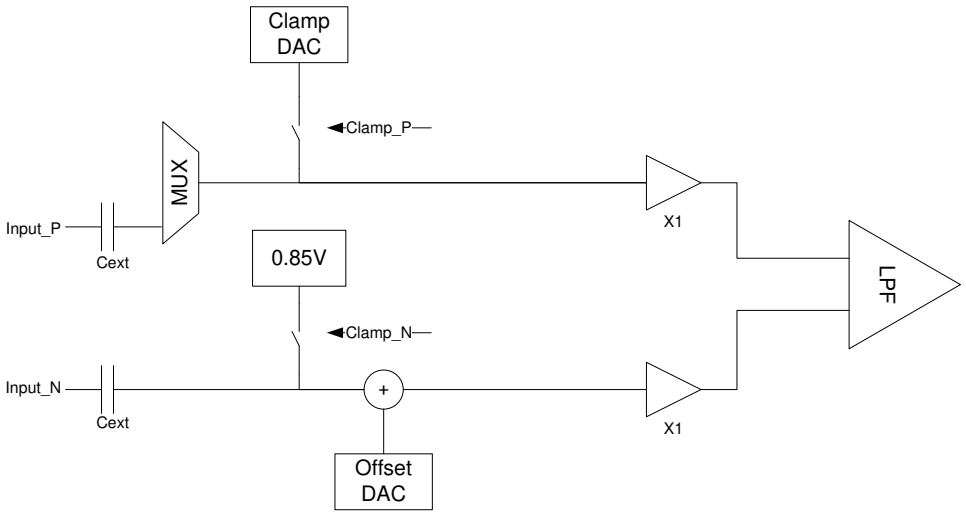

Figure 3.2. Clamp and Offset

The clamp DAC output voltage is 3-bit programmable from 0 V to 0.85 V, and the AFE provides more accurate 10-bit ±0.5 V or ±0.25 V output offset DAC to keep the input signal within the ADC input range. The offset level can be controlled automatically by ADCIF block of VDC or manually by software.

3.1.3. Low Pass Filter

The Low Pass Filter (LPF) is a first order analog filter to remove the out-of-band noise from video signal. Its –3 dB bandwidth can be set to 600 MHz (Bypass), 400 MHz, 200 MHz, 100 MHz, or 50 MHz by software. Combined together with ADC over-sampling technology and the high order digital AA (Antialias) filter inside VDC, the SiI8788 device can meet the demand of overall AA performance.

3.1.4. ADC with Programmable Gain Amplifier

The ADC samples the input video signal and converts each sample into 10 bits digital data. It supports sampling rates from 25 MSPS to 170 MSPS, and the sampling clock of CVBS channel can be independent with R, G, and B channels.

For the formats with lower pixel rate, oversampling is recommended. The SiI8788 device supports 2X, 4X and 8X oversampling.

The Programmable Gain Amplifier (PGA) in the front stage of ADC has a nominal gain range from –6 dB to +6 dB, so the SiI8788 device can adapt to a wide range of input video signal levels, especially, the CVBS signal from RF tuner. The PGA can be controlled either automatically by the gain control function of VDC or manually by software.

3.1.5. Line Locked PLL

The Line Locked PLL (LLPLL) is designed to generate the ADC sampling clock (pixel clock or oversampled pixel clock). It can be synchronized with a slower reference HSync pulses or run at a fixed frequency. The allowable input HSync range is from 15 kHz to 150 kHz, and the output pixel clock range is from 25 MHz to 170 MHz.

The LLPLL contains an high performance programmable digital PLL (DPLL) and an analog PLL (APLL) which generates the high frequency reference clock needed by DPLL from the 24 MHz crystal frequency.

The relative phase between input sync pulse and output clock of the LLPLL can be adjusted in 32 steps by setting registers or automatically by Auto Phase Detection (APD) block of the video processing module.

3.1.6. Sync Slicer

The Sync Slicer converts SOG and HSYNC signals into core domain digital signals. As shown in Figure 3.3, there are two sets of SOG slicers, each of which contains an input multiplexer, bottom level (0.5 V) clamp, low pass filter and comparator. The bandwidth of the low pass filter and the comparator threshold is programmable. There also are two sets of HS slicers for TTL level syncs. When one of the slicers is configured as an active input, the other in this pair can be used to detect the activity of other inputs. This feature is helpful to implement active channel detection and auto-switch function.

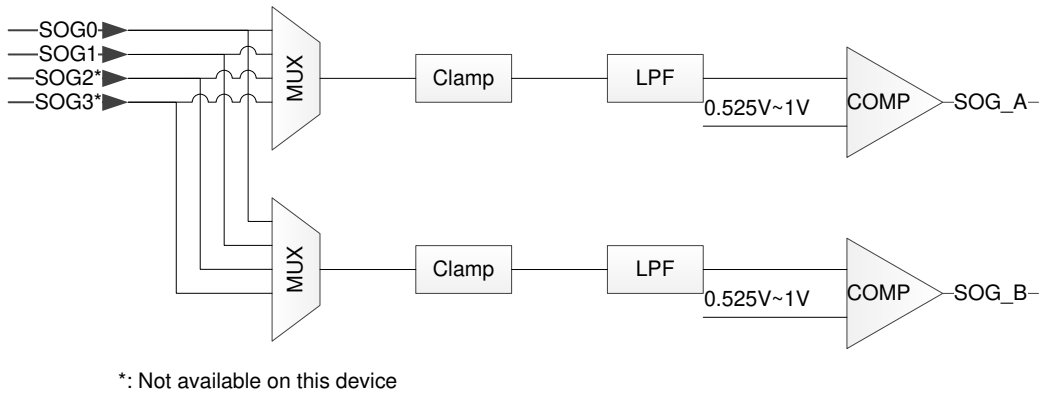

Figure 3.3. Sync Slicers

3.1.7. Video Buffer

The Video Buffer (VBUF) buffers and outputs the selected CVBS input signal. VBUF includes two major subblocks: clamp and voltage-to-current conversion. Voltage-to-current conversion subblock converts input signal to the output current which is proportional to signal voltage level. A 75 Ω source termination resistor should be connected to its output pin CVBS_OUT and signal ground.

3.2. Video Decoder

The SiI8788 device provides a multiformat video decoder. Video Decoder (VDC) includes ADCIF, Sync Processor, adaptive 2D Comb decoder, and VBI Decoder as shown in Figure 3.1 on page 7.

3.2.1. ADCIF

The ADCIF logic block contains the Automatic Gain Control and Offset Calibration, Antialias filtering and decimation subblocks. It also generates clamp pulses for clamp circuits at the proper time so that the ADC is able to digitize the input analog within the proper range. The main indicator used to determine where the clamping position should be is the horizontal synchronization pulse coming from the Sync Processor block. Since this filtered HSync pulse may not always be correct, several layers of logic have been developed to ensure the clamping is not done at an incorrect position.

3.2.2. Automatic Gain Control and Offset Calibration

Parameters such as Sync Amplitude, Back Porch Levels are measured based on the HSync position, register controls, and logic executed in the Offset Gain Calculations sub block. These measured values are then used in determining the offset and gain adjustments. To ensure the stability and accuracy of the digitized video signal, several control loops are built in the ADCIF block. These loops include Clamp, Coast, Gain, and Offset. The Clamp and Coast pulses, Gain and Offset parameters are generated by the ADCIF logic and directly connected to the AFE.

3.2.3. Antialias Filtering and Decimation

The Antialiasing (AA) filters remove high frequency noise from the raw digitized signals produced by the front-end video ADCs, and decimate the over-sampled video signal.

The AA filter has flexibility in the frequency response, sharp transition bandwidth, and good stop band attenuation. The AA filter allows the software to change the bandwidth of the filters as the signal condition changes.

3.2.4. Video Decoder

The Video Decoder detects and decodes the input video stream from ADCIF. An adaptive comb filter is included to decode CVBS signals. The Video Decoder also supports component signals.

3.2.5. CVBS Processing

CVBS Processing involves Standard Detection, 2D Video Decoder, and Sync Processor, as shown in Figure 3.4 below.

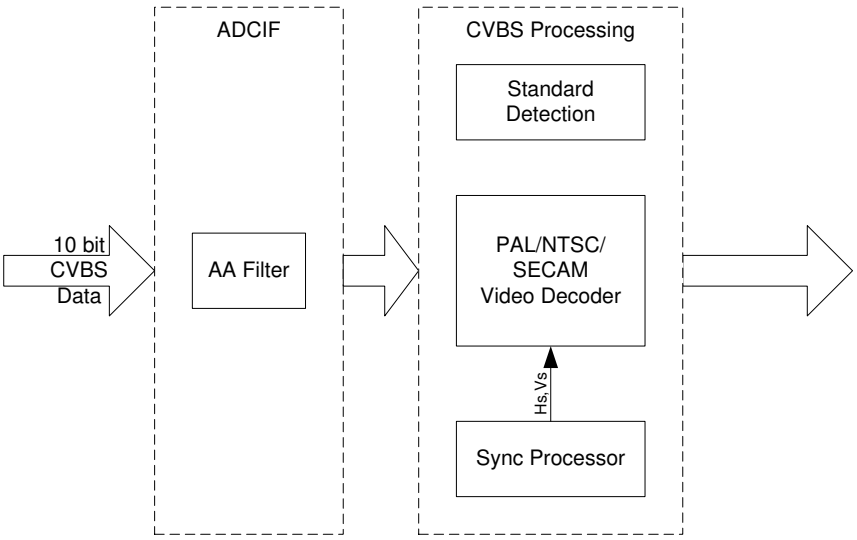

Figure 3.4. CVBS Processing Diagram

The SiI8788 device automatically detects NTSC (M/J/4.43), PAL (B/D/I/G/H/60/M/N/Nc), and SECAM (B/D/G/L/K) standards, and decodes them properly.

An adaptive 2D comb filter is used in the video decoder. The 2D comb filter has three output options, only horizontal filter, only vertical filter and blending of horizontal and vertical filter. When current sample is on a horizontal transition

edge, the vertical filter is selected. When current sample is on a vertical transition edge, the horizontal filter is selected. When it is not one of the above two phenomenon, the blending output is selected.

When the input signal is lost, the SiI8788 device supports a free-running mode to provide a stable output.

3.2.6. Component Processing

Component Processing processes Component Video inputs. The SiI8788 device supports 240p/288p, 480i/576i, 480p/576p, 720p, 1080i and 1080p for standard and high definition resolutions. Figure 3.5 shows the block diagram of the component video processing block.

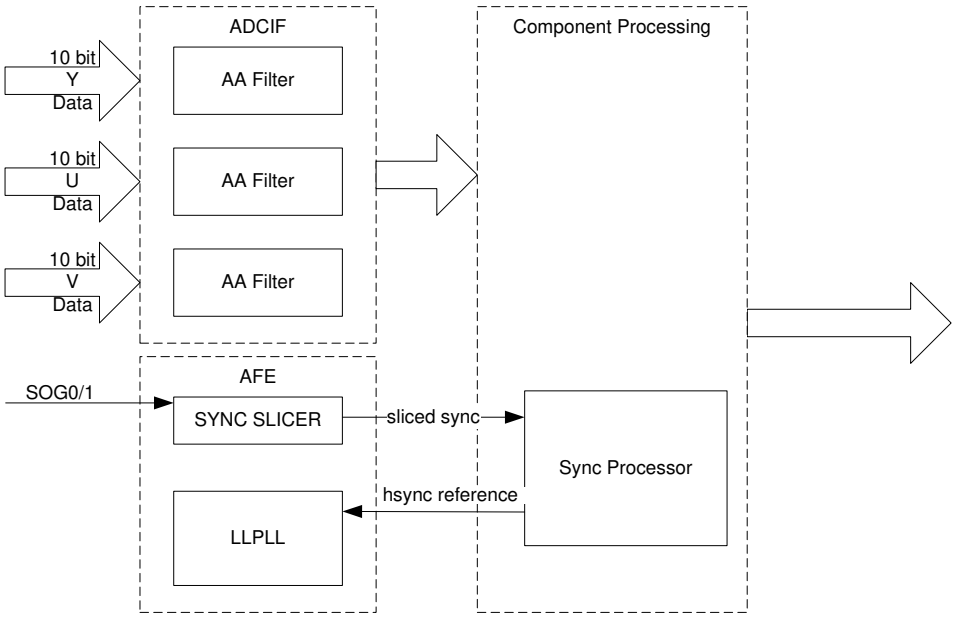

Figure 3.5. Component Processing Diagram

3.2.7. Sync Processor

The Sync Processor block contains sophisticated digital circuitry that analyzes and extracts synchronization pulses from the incoming video stream. It generates filtered vertical and horizontal sync pulses. The Sync Processor includes Sync separation, format detection and Sync stabilization.

- Sync Separation

The Sync Separation separates the HSync and VSync from the composite sync sliced from video decoder or SOG slicer.

- Format Detection

The format detection detects vertical period and horizontal period and total line number per field.

- Sync Stabilization

Sync Stabilization does de-glitch, removes serration and equalizes pulses from the sync signal. It also detects Macrovision protection status.

3.2.8. VBI Decoder

The VBI Processing block slices and processes digitized VBI data from the video. Following are some of the features of the VBI block:

- 108 MHz operating with programmable down sampling
- Supports PAL standards
- Supports NTSC standards

Table 3.1 shows the supported VBI standards.

Table 3.1. Supported Standards

VBI Standard	Video Standard	Data Rate	Scan Lines	Data per Line	Encoding	Description
WSS 625	PAL SECAM	5 MHz	23 336	14 Bits	Phase Encoding. Each bit is transmitted using 6 bits of encoded data.	Wide Screen Signaling. Used for aspect ratio settings.
VPS	PAL SECAM	5 MHz	16	13 Bytes	Biphase Encoding. Each bit is effectively represented by 2 bits.	Video Programming System. Used in Germany for program/broadcast info.
CC	NTSC	0.5030 MHz	21	2 Bytes	Parity.	Closed Captioning for the hearing impaired.
XDS VChip	NTSC	0.5035 MHz	284	2 Bytes	Parity.	Extended Data Service. Used for MISC. NTSC services
WSS 525 ID-1 CGMS	NTSC	0.4474 MHz	20	14 Bits	CRC.	Copy Guard Management System. Used for copy protection and aspect ratio.

3.3. Video Processing

The Video Processing block performs some necessary processes to the decoded video streams before they are outputted. There are also some measurement blocks inside this block to implement automatic Phase/Position/Gain adjustment functions.

3.3.1. Time Base Corrector

The Time Base Corrector (TBC) is designed to provide stable clock and video data for parallel video output. It uses a line buffer based architecture in-lieu of a frame buffer to save cost and power. To keep the video output clock jitter in a safe range, the TBC output field frequency is limited to 50 Hz ±0.5% or 59.94 Hz/60 Hz ±0.5% as default. If the field frequency of input video is beyond this range, the display will be scrolling.

Composite video formats are supported by the TBC. 480i/576i component formats can be supported by the TBC if needed.

3.3.2. VBI Post Processor

VBI Post Processor is used to transmit raw VBI data over TTL output.

3.3.3. De-interlacer and Edge Smoother

De-interlacing is designed to convert interlaced (480i/576i) video to progressive (480p/576p) video. BOB de-interlace method is adopted to reduce cost and power consumption. An edge smoother is included to reduce the saw tooth artifacts generated by de-interlacing and improve the picture quality.

3.3.4. Color Processing

Color Processing (CP) enables brightness, contrast, saturation and hue controls for end users. It supports YCbCr color space only.

3.3.5. Auto Phase Detection

Auto Phase Detection (APD) is a module used to search for the phases that can generate the best display quality. The desired phases, in general, can generate sharp and stable images, if the input image meets certain criteria during phase detection period. APD is an automatic algorithm can be enabled or disabled by software. It can be applied to Component inputs.

3.3.6. Auto Position Calibration

Auto Position Calibration (APC) detects the active picture area of input video signal and adjusts the output timing so that the final picture can fit to the display properly.

3.3.7. Auto Gain Calibration

Slight mismatch of analog input channels, including offset and gain may impact the picture quality. The SiI8788 device has been well designed to keep the mismatches in acceptable range (<0.5 dB). It is still important to calibrate these mismatches in some cases to achieve the most accurate picture. To help manufacturers complete this process in a short time, an Auto Gain Calibration (AGCWIN) mechanism is designed in SiI8788 device. This mechanism will automatically measure the digitalized signal levels through AGCWIN module, calculate the correction values. These values can be used by firmware in user mode to compensate the analog mismatches.

3.4. Video Path

3.4.1. Video Data Conversion Logic Block

The video data conversion logic block receives the output data from the video processing block. Figure 3.6 shows the video data processing stages. Each of the processing blocks can be bypassed by setting the appropriate register bits.

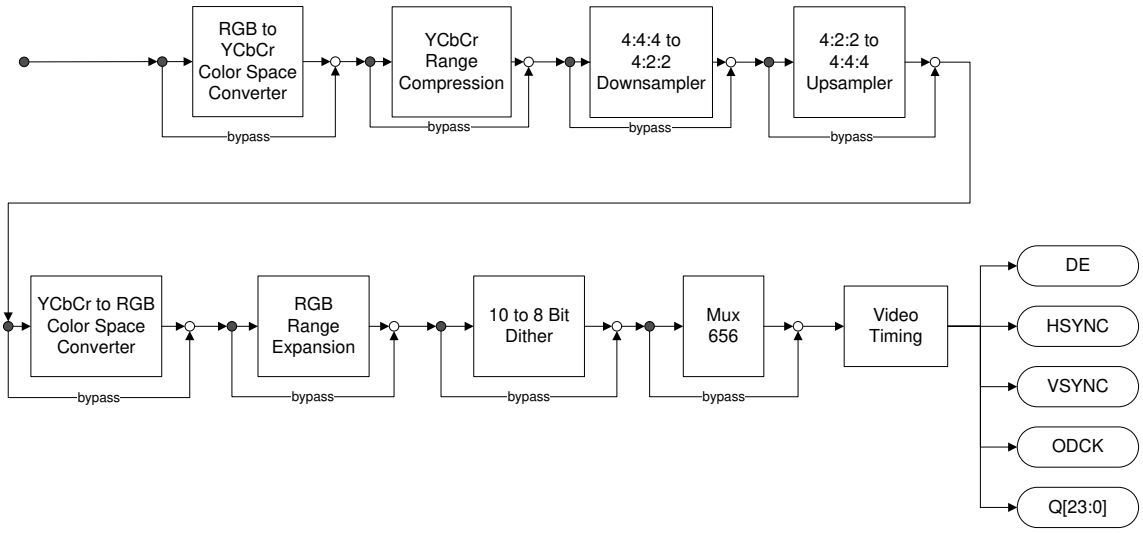

Figure 3.6. Default Video Processing Path

3.4.1.1. Color Space Converters

Color Space Converters (CSCs) are provided to convert RGB data to the Standard-definition (ITU.601) or High-definition (ITU.709) YCbCr formats, and vice-versa. The CSC can be adjusted to perform standard-definition conversions (ITU.601) or high-definition conversions (ITU.709) by setting the appropriate registers.

3.4.1.2. YCbCr Range Compression

When enabled by itself, the Range Compression Block compresses 0–255 full-range data into 16–235 limited-range data for each video channel, and compresses to 16–240 for the Cb and Cr channels. The color range scaling is linear.

3.4.1.3. 4:4:4 to 4:2:2 Downsampler

Downsampling reduces the number of chrominance samples in each line by half, converting 4:4:4 sampled video to 4:2:2 video.

3.4.1.4. 4:2:2 to 4:4:4 Up-sampler

Chrominance upsampling and downsampling increase or decrease the number of chrominance samples in each line of the video. Upsampling doubles the number of chrominance samples in each line, converting 4:2:2 sampled video to 4:4:4 sampled video.

3.4.1.5. RGB Range Expansion

The SiI8788 device can scale the input color from limited-range into full-range using the range expansion block. When enabled by itself, the range expansion block expands 16 – 235 limited-range data into 0 – 255 for each video channel. When the range expansion and the YCbCr to RGB color space converter are both enabled, the input conversion range for the Cb and Cr channels is 16 – 240.

3.4.1.6. 10 to 8 Bit Dither

The 10 to 8 Bit Dither block dithers internally processed 10-bit data to 8-bit data for output.

3.4.1.7. Mux 656

The Mux 656 block multiplexes the video data into YC Mux (ITU.656) format.

3.4.1.8. Video Timing

The video timing block is used to control the timing of the digital parallel video output automatically according to the output format setting, such as controlling the output frequency of the ODCK, and disabling the HSYNC, VSYNC and DE signals output when the output format is set as embedded syncs.

3.4.2. Digital Parallel Video Output Interface

The SiI8788 input processor outputs the uncompressed digital video with a data width of 8 to 24 bits from the digital parallel video output interface. The data path has three 8-bit data channels, which can be configured in many different video formats. The supported typical formats are listed in Table 3.2.

Table 3.2. Typical Digital Video Output Formats

Color Space	Video Format	Bus Width	HSYNC/VSYNC	Output Clock (MHz)					Notes
				480i/576i[2, 3]	480p	720p	1080i	1080p	
RGB	4:4:4	24	Separate	27	27	74.25	74.25	148.5	—
		12	Separate	27	27	74.25	74.25	—	4
YCbCr	4:4:4	24	Separate	27	27	74.25	74.25	148.5	—
		12	Separate	27	27	74.25	74.25	—	4
	4:2:2	16/20/24	Separate	27	27	74.25	74.25	148.5	—
		16/20/24	Embedded	27	27	74.25	74.25	148.5	1
		8/10/12	Separate	27	54	148.5	148.5	—	—
		8/10/12	Embedded	27	54	148.5	148.5	—	1

Notes:

1. Embedded syncs use SAV/EAV coding.
2. 480i and 576i modes can output a 13.25 MHz clock using the internal clock divider.
3. Output clock frequency depends on programming of internal registers.
4. Output clock supports 12-bit mode by using DDR mode.

3.5. Control Logic

3.5.1. Internal Microcontroller

As shown in Figure 3.1 page 7, an 8-bit 8051 compatible micro-controller is integrated in the SiI8788 device. It contains 3 KB data RAM and 128 KB code RAM. The code can be loaded into code RAM from an external SPI Flash or EEPROM memory automatically after power on. If the check sum of the code data is correct, the code will be executed. Otherwise the internal microcontroller is disabled and the chip can be controlled by an external controller through I^2C bus. The internal controller can access all the internal registers directly over the internal bus. The 8051 microcontroller runs at the crystal clock of 24 MHz.

When the booting procedure is finished, the SPI interface is handed over to the 8051 SPI module so that firmware can read/write the external memory if needed.

The internal controller can also operate other peripherals through the I^2C bus of the SiI8788 device by setting it to the master mode.

3.5.1.1. Data Structure of External SPI Memory

Figure 3.7 shows the memory structure which is required for the internal microcontroller to load the code correctly.

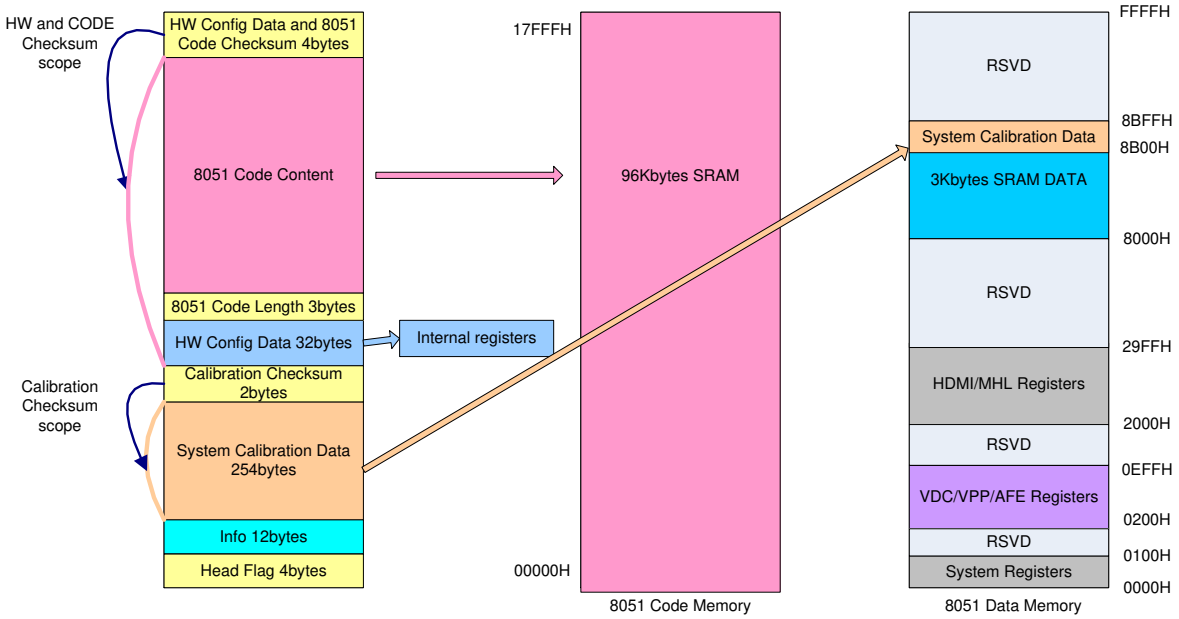

Figure 3.7. External Memory Structure

Table 3.3. Head Flags

EEPROM/Flash Address	EEPROM/Flash Content
00000H	Head0 'S'
00001H	Head1 'I'
00002H	Head2 'M'
00003H	Head3 'G'

Note: The head flag will be four bytes ASCII code of 'S', 'I', 'M', 'G'.

Table 3.4. Info Bytes

EEPROM/Flash Address	EEPROM/Flash Content
00004H	SPI PARAMETER.
00005H	Calibration Version (low byte).
00006H	Calibration Version.
00007H	Calibration Version (high byte).
00008H	Code Version (low byte).
00009H	Code Version.
0000AH	Code Version (high byte).
0000BH	Reserved.
0000CH	Reserved.
0000DH	Reserved.
0000EH	Reserved.
0000FH	Reserved.

Note: The info bytes will contain the information about the feature of Max read frequency of external EEPROM/Flash, the calibration version, and the code version. It will occupy 12 bytes.

Table 3.5. SPI Parameter

SPI Parameter	Description
0x00	2 MHz baud rate to access SPI Flash/EEPROM.
0x01	24 MHz baud rate to access SPI Flash/EEPROM.

Table 3.6. Calibration Checksum

EEPROM/Flash Address	EEPROM/Flash Content
0010EH	Calibration Checksum (low byte).
0010FH	Calibration Checksum (high byte).

Note: The calibration checksum will be two bytes which locates at the last site of 256 size calibration data.

Table 3.7. HW Configuration Data

EEPROM/Flash Address	EEPROM/Flash Content
00110H	BT_SPI_PINMUX_SEL. 00H – SPI function 01H – Reserved. Don't use 02H – Reserved. Don't use
00111H..0012FH	Reserved.

Table 3.8. 8051 Code Size

EEPROM/Flash Address	EEPROM/Flash Content
00130H	Code Size (low byte).
00131H	Code Size.
00132H	Code Size (high byte).

Table 3.9. HW Configuration Data and Code Checksum

EEPROM/Flash Address	EEPROM/Flash Content
00133H + code size	Code Checksum0 (lowest byte).
00134H + code size	Code Checksum1.
00135H + code size	Code Checksum2.
00136H + code size	Code Checksum3 (highest byte).

The boot module =tries to read data from external device and write into chip SRAM. The 8051 code content will be written into the 96 K bytes SRAM of 8051. The 256 system calibration will be written into the high 3K bytes SRAM in data memory.

For details on the selection of the SPI Flash memory, refer to the relevant Application Note (SiI-AN-1108).

3.5.2. Registers

The register block incorporates all the registers required for configuring and managing the SiI8788 device. These registers are used to perform AFE processing, VDC processing, and all other control functions. Refer to the associated Programmer Reference for the information on these registers. *The Programmer's Reference requires an NDA with Lattice Semiconductor.*

3.5.3. I^2C Bus

The local I^2C slave bus provides the host with communication to the entire system. The controller I^2C interface on the SiI8788 device (signals CSCL and CSDA) is a slave interface, which is capable of running up to 400 kHz.

All functions of the SiI8788 device are controlled and observed with I^2C registers. Device addresses can be altered with the level of the CI2CA signal. Table 3.10 shows the device addresses as altered by the level of the CI2CA signal.

Table 3.10. Control of Transmitter I^2C Address with CI2CA Signal

CI2CA = 0	CI2CA = 1	Purpose
0x8C	0x8E	System Control and Status
0x84	0x84	VD_DPGA VD_SIGNALROUTING
0x86	0x86	VD_VBI
0x8A	0x8A	VD_VDREG VD_ADCIF
0x92	0x92	VD_SYNCPROC
0x96	0x96	VD_ADCSTATUS VD_VPP Edge Smooth INT
0xDA	0xDA	FPGA APD ADC Win
0x9C	0x9C	Vidpath Calibration
0xD8	0xD8	AFE

Note: When the internal microcontroller is enabled, the I^2C bus will be taken over by the firmware and it can work as both master and slave mode, and the addresses are alterable.

3.5.4. Interrupt

The SiI8788 device contains a configurable interrupt generator with an open-drain type output pin. It can be used to notify application processor (if there is application processor) to handle some events. Refer to the associated Programmer Reference for the information on these registers.

3.5.5. GPIOs

There are five general purpose IO pins on the SiI8788 device. Generally they can be used to detect the cable plug-in status, but they can be used for other purposes as well.

Table 3.11. GPIOs

Name	Type	Pull up/down[2]	Reset Status
GPIO0[1]	IO	Pull down	I
GPIO1	IO	Pull up	I
GPIO2	IO	Pull up	I
GPIO3	IO	Pull up	I
GPIO4	IO	Pull up	I

Notes:
1. GPIO0 is also used as CI2CA pin to decide the I^2C slave address during reset.
2. The internal Pull up/down resistors are fixed and weak just to avoid floating input level when they are left unconnected. Peripheral circuits should not rely on them. 10 K or smaller resistors are recommended for external pull up/down circuit to override them if needed.

4. Electrical Specifications

4.1. Absolute Maximum Ratings

Table 4.1. Absolute Maximum Ratings

Symbol	Parameter	Min	Typ	Max	Units	Notes
VP2V5A	Analog Power for AFE	–0.3	—	3.0	V	1, 2
VP2V5D	Digital Power for AFE	–0.3	—	3.0	V	1, 2
VP2V5_SLICER	Analog Power for SOG Slicer	–0.3	—	3.0	V	1, 2
VP1V0_PLL	Power for APLL and LLPLL	–0.3	—	1.2	V	1, 2
VCC10_TPLL	TCI PLL Power	–0.3	—	1.2	V	1, 2
CVCC10	Power for Digital Core	–0.3	—	1.2	V	1, 2
VDDIO33	Power for Digital I/O	–0.3	—	4.0	V	1, 2
XTALVCC33	Power for XTAL	–0.3	—	4.0	V	1, 2
V_I	Digital Input Voltage	–0.3	—	VDDIO + 0.3	V	1, 2
V_O	Digital Output Voltage	–0.3	—	VDDIO + 0.3	V	1, 2
AV_I	Analog Input Voltage	-0.3	—	VP2V5A + 0.3	V	1, 2
$V_{5V\text{-}Tolerant}$	Input Voltage on 5 V Tolerant Pins	–0.3	—	5.5	V	—
T_J	Junction Temperature	—	—	125	°C	—
T_{STG}	Storage Temperature	–65	—	150	°C	—

Notes:

1. Permanent device damage can occur if absolute maximum conditions are exceeded.
2. Functional operation should be restricted to the conditions described under normal operating conditions.

4.2. Normal Operating Conditions

Table 4.2. Normal Operating Conditions

Symbol	Parameter	Min	Typ	Max	Units	Notes
VP2V5A	Analog Power for AFE	2.375	2.50	2.625	V	—
I_{VP2V5A}	Total Current Consumption of VP2V5A	— —	95 260	— —	mA mA	4 5
VP2V5D	Digital Power for AFE	2.375	2.50	2.625	V	—
I_{VP2V5D}	Total Current Consumption of VP2V5D	—	30	—	mA	—
VP2V5_SLICER	Analog Power for SOG slicer	2.375	2.50	2.625	V	—
I_{VP2V5_SLICER}	Current Consumption of VP2V5_SLICER	— —	0 5	— —	mA mA	4 5
VP1V0_PLL	Power for APLL and LLPLL	0.95	1.00	1.05	V	—
I_{VP1V0_PLL}	Current Consumption of VP1V0_PLL	—	20	—	mA	—
VCC10_TPLL	TCI PLL Power	0.95	1.00	1.05	V	—
I_{VCC10_TPLL}	Current Consumption of VCC10_TPLL	—	3.5	—	mA	—
CVCC10	Power for Digital Core	0.95	1.00	1.05	V	—
I_{CVCC10}	Total Current Consumption of CVCC10	— —	70 20	— —	mA mA	4 5
VDDIO33	Power for Digital I/O	3.135	3.30	3.465	V	—
$I_{VDDIO3V3}$	Current Consumption of VDDIO3V3	— —	5 20	— —	mA mA	4 5
XTALVCC33	Power for XTAL	3.135	3.30	3.465	V	—
$I_{XTALVCC33}$	Current Consumption of XTALVCC33	—	5	—	mA	—
T_A	Ambient Temperature (with power applied)	0	25	70	°C	—
Θ_{ja}	Ambient Thermal Resistance (Theta JA)	—	—	25.6	°C/W	1
Θ_{jc}	Case Thermal Resistance (Theta JC)	—	—	11.9	—	—

Notes:

1. Airflow at 0 m/s. Package ePad soldered to PCB.
2. The power ripple must be below 60mVpp to avoid video quality detrition.
3. Avoid any noise coupling to PLL power rails.
4. Measured with CVBS input.
5. Measured with YPbPr 1080p60 input.

4.3. ESD Specifications

Table 4.3. ESD Specifications

Symbol	Parameter	Min	Typ	Max	Units	Notes
Latch up	ESD Latch up	± 200	—	—	mA	1, 2
HBM	Human Body Model	2000	—	—	V	3
MM	Machine Model	200	—	—	V	4
CDM	Charged Device Model	500	—	—	V	5

Notes:

1. At 70 °C.
2. Measured as per JESD78B standard.
3. Measured as per JESD22-A114 standard.
4. Measured as per JESD22-A115 standard.
5. Measured as per JESD22-C101 standard.

4.4. DC Specifications

Table 4.4. Digital I/O Specifications

Symbol	Parameter	Conditions	Min	Typ	Max	Units	Note
Digital Inputs							
V_{IL}	Input Low Voltage	—	—	—	0.8	V	1
V_{IH}	Input High Voltage	—	2.0	—	—	V	1
V_{TH+}	Schmitt Trigger LOW to HIGH Threshold	—	1.61	1.69	1.77	V	1
V_{TH-}	Schmitt Trigger HIGH to LOW threshold	—	1.18	1.27	1.35	V	1
I_{IL}	Input Leakage Current	—	–10	—	10	µA	1
RPU	Pull-up Resistor	—	27	38	59	KΩ	1
RPD	Pull-down Resistor	—	31	46	80	KΩ	1
V_{TH+I2C}	Schmitt Trigger LOW to HIGH Threshold of LSCL, LSDA	—	2.0	—	—	V	—
V_{TH-I2C}	Schmitt Trigger HIGH to LOW Threshold of LSCL, LSDA	—	—	—	0.8	V	—
Digital Outputs							
V_{OH}	HIGH-level Output Voltage	I_{OL} = -8mA	2.4	—	—	V	1
V_{OL}	LOW-level Output Voltage	I_{OH} = 8mA	—	—	0.4	V	1
I_{OZ}	Tri-state Output Leakage Current	—	–10	—	10	µA	1

Note: Applies to general digital IOs.

4.5. AC Specifications

Table 4.5. Analog Front-end Electrical Specifications

Analog Input						
Symbol	**Parameter**	**Conditions**	**Min**	**Typ**	**Max**	**Units**
—	Input capacitance	—	—	5	—	pF
V_{FSR}	Analog Input Range	—	0.3	—	1.2	V_{pp}
—	Clamp Level	—	0.25	—	0.85	V
V_{OAR}	Offset Adjustment Range	—	–0.5	—	+ 0.5	%FS
—	Offset Adjustment Resolution	—	—	10	—	Bits
BW	Input Analog Filter Bandwidth	—	50	—	600	MHz
—	Gain Adjustment Range	—	–6	—	+ 6	dB
A/D Converters						
—	Conversion Rate	—	25	—	170	MHz
N	ADC Resolution	—	—	10	—	Bits
INL	Integral Nonlinearity	580 mVpp, 2.8 kHz Ramp Wave Sampling Rate: 55 MHz PGA Gain: 0 dB LPF Bandwidth: 50 MHz	—	4	—	LSB
DNL	Differential Nonlinearity		—	1	—	LSB
NMC	No Missing Codes	—	Guaranteed			—
ENOB	Effective Number Of Bits	300 mVpp, 1.1 MHz Sine Wave Sampling Rate: 165 MHz PGA Gain: 0 dB LPF Bandwidth: 400 MHz	—	7.5	—	Bits
PLL						
—	Clock Frequency Range	—	25	—	170	MHz
—	Period Jitter	—	—	—	450	ps
—	Phase Adjustment	—	—	11.25	—	Degrees
—	Duty Cycle	—	45	50	55	%
Video Buffer						
DP	Differential Phase	—	—	—	4	Degrees
DG	Differential Gain	—	—	—	4	%
THD	Total Harmonic Distortion	700 mVpp, 4 MHz Sine Wave Load = 37.5 Ω Internal Clamp: OFF	—	-48	—	dB

Table 4.6. Parallel Video Output Timing Specifications

Symbol	Parameter	Conditions	Min	Typ	Max	Units	Figure
DLHT_C	LOW-to-HIGH Rise Time Transition, ODCK pin	C_L = 10pF	—	—	0.74	ns	Figure 5.4
DHLT_C	HIGH-to-LOW Fall Time Transition, ODCK pin	C_L = 10pF	—	—	0.81	ns	Figure 5.4
DLHT_D	LOW-to-HIGH Rise Time Transition, data and control pins	C_L = 10pF	—	—	1.15	ns	Figure 5.4
DHLT_D	HIGH-to-LOW Fall Time Transition, data and control pins	C_L = 10pF	—	—	1.45	ns	Figure 5.4
T_{CIP}	ODCK Cycle Time	C_L = 10pF	40	—	6	ns	Figure 5.5
F_{CIP}	ODCK Frequency	C_L = 10pF	25	—	165	MHz	Figure 5.5
TDUTY	ODCK Duty Cycle	C_L = 10pF	45%	—	55%	—	Figure 5.5
T_{CK2OUT}	Clock-to-Output Delay	C_L = 10pF	0.2	—	1	ns	Figure 5.5

Notes:

1. The timings above apply to ODCK, HSYNC, VSYNC, DE, and Q[23:0].

4.6. Control Signal Timing Specifications

Table 4.7. Control Signal Timing Specifications

Symbol	Parameter	Conditions	Min	Typ	Max	Units	Figure	Notes
T_{I2CDVD}	SDA Data Valid Delay from SCL falling edge on READ command	CL = 400pF	—	—	700	ns	Figure 5.1	1, 2
T_{RESET}	RESET_N Signal LOW Time required for reset	—	5000	—	—	ns	Figure 5.2, Figure 5.3	3

Notes:

1. All standard-mode (100 kHz) I^2C timing requirements are guaranteed by design. These timings apply to the slave I^2C port (signals LSDA and LSCL).
2. Operation of I^2C signals above 100 kHz is defined by LVTTL levels V_{IH}, V_{IL}, V_{OH}, and V_{OL} (see Table 4.4 on page 21). For these levels, I^2C speeds up to 400 kHz are supported.
3. Reset on RESET_N signal can be LOW as CVCC10 and VDDIO33 become stable, or pulled LOW for at least T_{RESET}.

5. Timing Diagrams

5.1. I²C Bus Timing Diagrams

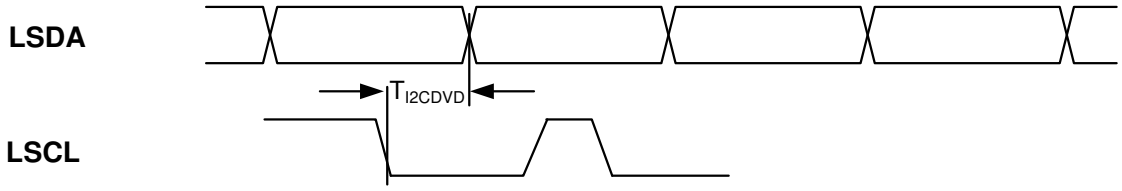

Figure 5.1. I²C Data Valid Delay (Driving Read Cycle Data)

5.2. Reset Timing Diagram

VDDIO33 must be stable between its limits for Normal Operating Conditions for T_{RESET} before RESET_N is HIGH. RESET_N must be pulled LOW for T_{RESET} before accessing registers. This can be done by holding RESET_N LOW until T_{RESET} after stable power (Figure 5.2) or by pulling RESET_N LOW from a HIGH state (Figure 5.3) for at least T_{RESET}.

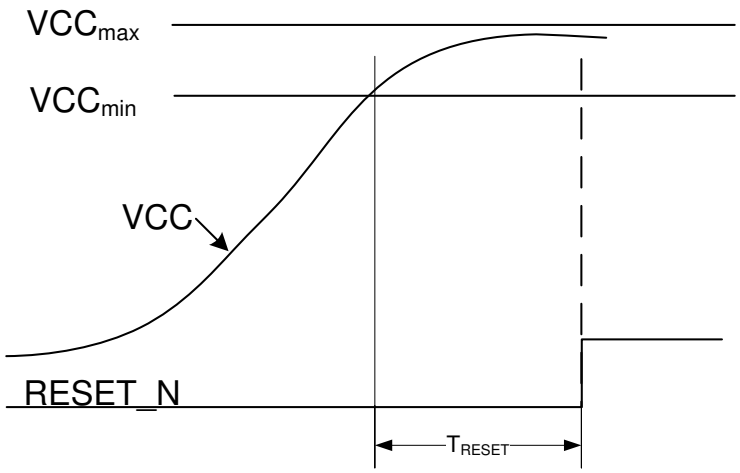

Figure 5.2. Conditions for Use of RESET_N

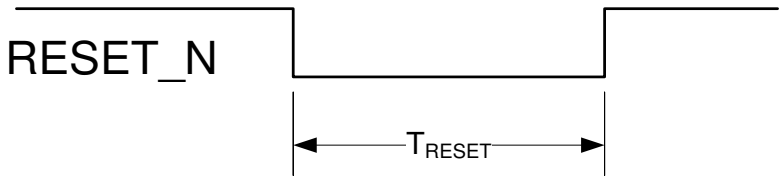

Figure 5.3. RESET_N Minimum Timings

5.3. Digital Video Output Timing Diagrams

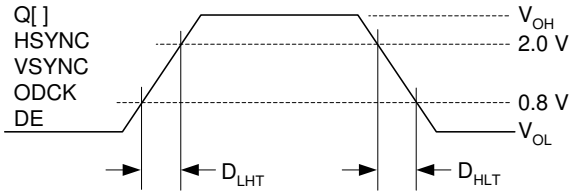

Figure 5.4. Video Digital Output Transition Times

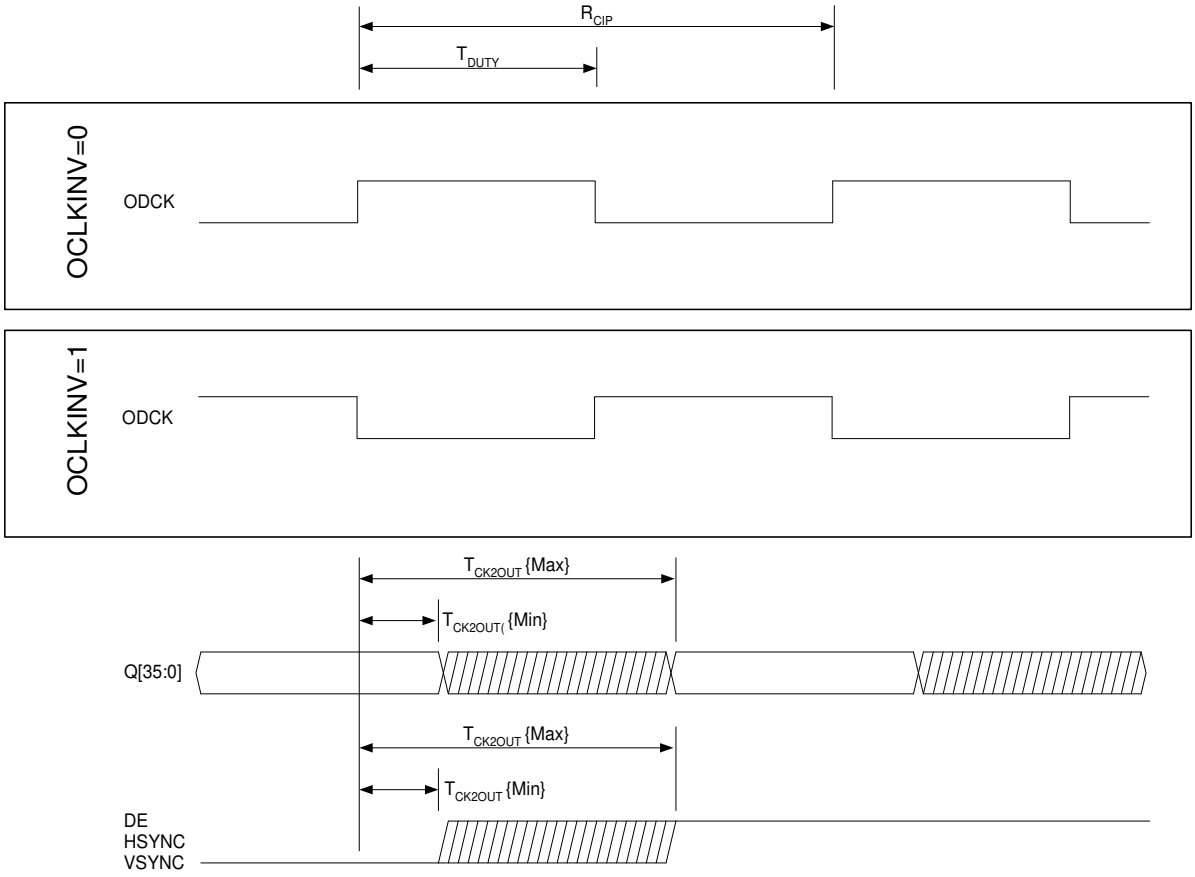

Figure 5.5. Clock-to-Output Delay and Duty Cycle Limits