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SAMSUNG

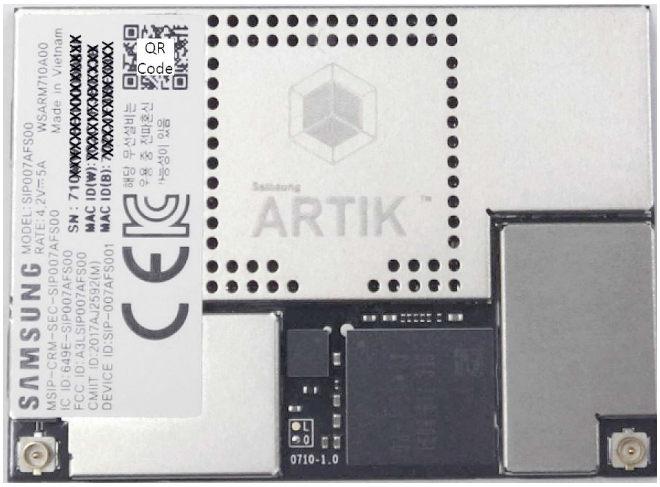
ARTIK™ Modules 7

ARTIK 710/710s Module Datasheet

1 Module Overview

Figure 1. ARTIK™ 710/710s Modules Top View

ARTIK 710



ARTIK 710s

The Samsung ARTIK™ 710/710s Module is a highly-integrated System-in-Module that combines an eight-core ARM® Cortex®-A53 processor packaged with DRAM and Flash memory, a Security Subsystem, and a wide range of wireless communication options—such as 802.11a/b/g/n/ac for Wi-Fi®, Bluetooth® 4.0 (BLE+Classic), and 802.15.4 for Zigbee—all into an extremely compact footprint. The many standard digital control interfaces support external sensors and higher performance peripherals to expand the module's capabilities. With the combination of 802.11, Bluetooth, and 802.15.4, the ARTIK 710/710s Module is the perfect choice for home automation and home hub devices, while also supporting a rich UI/UX capability for camera and display requirements. The inclusion of a hardware-based Secure Element works with the ARM® TrustZone® and Trustware's Trusted Execution Environment (TEE) to provide end-to-end security.

Processor	
CPU	Octa-core ARM® Cortex®-A53@1.4GHz
GPU	3D graphics accelerator
Media	
Camera I/F	4-lane MIPI CSI up to 5M (1920x1080@30fps)
Display	4-lane MIPI DSI and HDMI1.4a (1920x1080p@60fps) or LVDS (1280×720p@60fps)
Audio	Two I^2S audio interfaces
Memory	
DRAM	1GB DDR3 @ 800MHz
FLASH	4GB eMMC v4.5
Security	
Secure Element	Secure point-to-point authentication and data transfer
Trusted Execution Environment	Trustware
Radio	
WLAN	IEEE 802.11a/b/g/n/ac, dual-band SISO
Bluetooth	4.0 (Classic+BLE)
LR_WPAN	IEEE 802.15.4
Power Management	
PMIC	Provides all power of the ARTIK 710/710s Module using onboard bucks and LDOs
Interfaces	
Ethernet	10/100/1000Base-T MAC (External PHY required)
Analog and Digital I/O	GPIO, UART, I^2C, SPI, SDIO, USB OTG, USB Host/ HSIC, ADC, PWM, I^2S, JTAG

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2 Version History

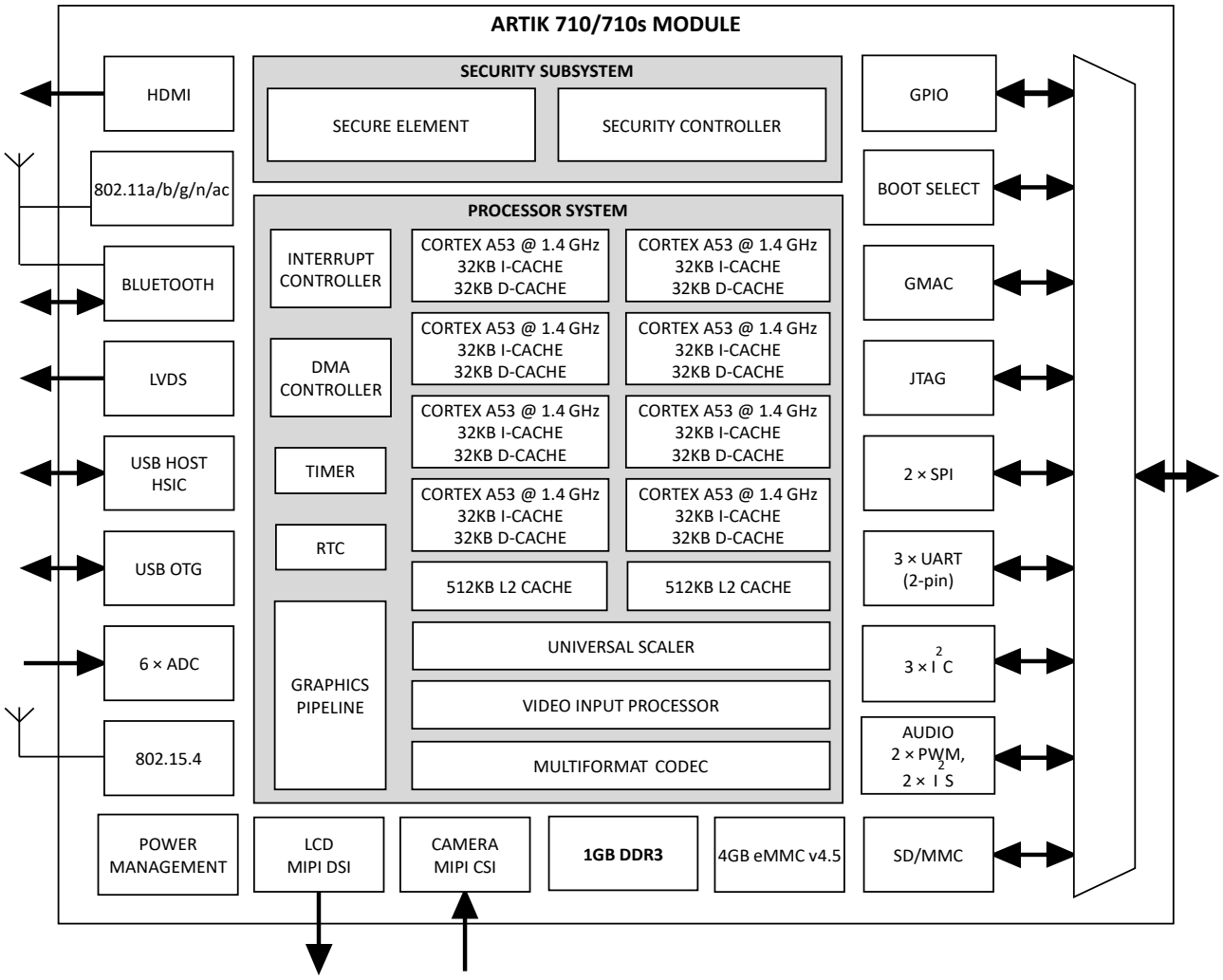
Revision	Date	Description
V1.0	October 17, 2016	Initial release.
V1.01	November 15, 2016	Updated Page 1 ARTIK 710/710s Module Picture. Updated Figure 2, Figure 3. Updated Mechanical Specification section. Updated Front Page. Updated ARTIK 710/710s Module ZigBee or Thread section. Updated ARTIK 710/710s Module Wi-Fi/ Bluetooth section.
V1.02	November 20, 2017	Updated block diagram. In *Functional Interfaces*, each subsection describing an interface that has alternate functions clarifies which are selected by hardware at power-on reset. Changed specifications in *Wi-Fi*. Cross references added to the appropriate tables in *GPIO Alternate Functions*. Secure Element and Secure IP reorganized into *Memory Controller* section. Changed format of default functions in tables of *GPIO Alternate Functions* to make it easier to see which function number is the default. Changed direction of LVDS signals in *Table 18* from IO to O. *Booting Selection* section rewritten for clarity. Power Sequence section divided into *Power Sequence* and *Power States*. Simplified power management state diagram. Section *Power/Current Consumption* added. Changed storage temperature range in *Absolute Maximum Ratings*. Updated standards compliance in *CE* and *EU Regulatory Disclosures*.
V1.03	November 30, 2017	Added ARTIK 710s features in *Module Overview*, *Block Diagram and Module Features*, and, *Security Subsystem*. Caution after block diagram in *Block Diagram and Module Features* about not applying power before connecting antennas was deemed unnecessary and removed.
V1.04	December 20, 2017	*Mechanical Specifications*: Changed pad names in *Figure 14* and *Table 66* to correlate with pad organization shown in *Figure 3*. Note that the changes address a labeling consistency issue only; no electrical or layout changes are required.
V1.05	February 2, 2018	*Module Overview*: Corrected inconsistent information about Bluetooth specification support.
V1.06	February 20, 2018	*Table 7*: Corrected note about VCC3P3_SYS pads. Deleted text indicating that the pads are switched off during sleep mode, which does not apply to this product family. The note still indicates these pads should not be used to drive external devices.
V1.07	March 22, 2018	*I^2C*: Removed support for slave mode. *Table 3*: Changed UART port from port 0 to port 5 so that the data for this pad is now consistent in the datasheet. Marked pad PAL15 for internal use only. *Table 9*: Marked pad PAL15 for internal use only. *Table 30*: Corrected GPIO functions associated with pad PAL24. Removed pad PAL15 because it is reserved for internal use only.
V1.08	April 5, 2018	Added *Temperature Thresholds for Operating Frequency Throttling* under new section *Thermal and Environmental Specifications*.

Revision	Date	Description
V1.09	April 25, 2018	*Figure 2*: Changed functional blocks for USB and HSIC. Changed *HSIC* to be a subheading to *USB HOST* to reflect hardware hierarchy. In *Functional Interfaces*, split USB OTG from USB Host and combined USB Host with HSIC. *Recommended Operating ConditionsRecommended Operating Conditions*: Added footnote about reduced retention time for Flash stored for an extended period of time at temperatures about 30°C. *Legal Information*: Clarified policy regarding third-party registered trademarks. General: Changed headings to a numbered format.
V1.10	June 22, 2018	*Table 20*: Corrected GPIO pin assignments of GPIO B11 and B18 to agree with ball tables. *Figure 3*: Missing ball column 20 inserted.
V1.11	July 19, 2018	*Figure 4*: Corrected power-up sequence time units from milliseconds to seconds.
V1.12	TBD	*Booting Selection*: Added note that USB OTG is a boot recovery option only. *Figure 3*: Removed non-existent ball (PA15).

3 Block Diagram and Module Features

Figure 2 shows the functional block diagram of the ARTIK 710/710s Module. It consists of an octa-core ARM® Cortex®-A53 application processor with 1GB of DDR3 and 4GB eMMC Flash, PMIC power management, Security Subsystem, 802.11 for Wi-Fi®, Bluetooth®, 802.15.4 for Zigbee, and RF connectors.

Figure 2. ARTIK 710/710s Module Functional Block Diagram



3.1 ARTIK 710/710s Module Features

The following subsections describe the functions of the various ARTIK 710/710s Module blocks depicted in *Figure 2*.

3.1.1 Eight-Core Processor System

The processor system architecture that resides on the ARTIK 710/710s Module is a system-on-a-chip (SoC) based on a 32/64-bit RISC architecture. Designed using the 28nm low power process, the processor system architecture provides superior performance using an eight-core CORTEX®-A53 CPU. The key features of the ARTIK 710/710s Module are

- Eight-core ARM® Cortex®-A53, RISC architecture
- Maximum core speed 1.4GHz
- 32KB I-Cache per core
- 32KB D-Cache per core
- 1024KB L2-Cache shared between eight cores
- Support for dynamic virtual-address mapping

3.1.2 Memory Controller

The ARTIK 710/710s Module has one DDR3 memory interface. The key features are

- One 32-bit DDR3 memory interface
- Two 512MB DDR3 16-bit memory chips, for a total of 1GB
- Up to 800MHz DDR3 speed with a maximum throughput of 6.4GB/s

3.1.3 Power Management

The ARTIK 710/710s Module power requirements are managed using a power management integrated circuit (PMIC). This PMIC device has five fully-integrated fixed-frequency current-mode synchronous PWM step-down converters that can achieve peak efficiencies of up to 97%.The regulators operate at a fixed high frequency, minimizing noise in sensitive applications and allowing the use of small form factor components. These five regulators fully satisfy the power and control requirements of the ARTIK 710/710s Module. Dynamic Voltage Scaling (DVS) of the various core voltages is supported using I^2C control.

In addition, the ARTIK 710/710s Module provides up to five low-noise LDOs for external use.

3.1.4 Wi-Fi

The ARTIK 710/710s Module has a fully integrated WLAN block covering IEEE 802.11 a/b/g/n/ac. The most important hardware features of the module are

- 802.11 a/b/g/n/ac dual-band SISO that is 2.4GHz/5GHz-compliant
- 1T1R 2.4GHz/5GHz band
- Support for 20MHz, 40MHz, and 80MHz bandwidth (86.7/433.3Mbps PHY rate)

- Enhanced 802.11/Bluetooth coexistence control to improve transmission quality in different profiles
- Use of an SDIO interface

3.1.5 Bluetooth®

The ARTIK 710/710s Module has a fully integrated 4.0 block (BLE+Classic). The most important hardware features of the module are

- Bluetooth 4.0 (BLE+Classic)
- Enhanced 802.11/Bluetooth Coexistence control to improve transmission quality in different profiles

3.1.6 802.15.4 for Zigbee

The ARTIK 710/710s Module carries fully-integrated 802.15.4 functionality. The most important hardware features are

- Fully integrated 2.4 GHz, IEEE 802.15.4-compliant transceiver
- Complete system-on-chip using 32-bit ARM® Cortex®-M3 processor
- Flash and RAM memory and peripherals.
- Extremely low power consumption.
- Excellent RF performance.
- Supported Protocols:
  - Zigbee
  - Thread

3.1.7 USB OTG

The ARTIK 710/710s Module provides one USB 2.0 OTG interface supporting both device and host functionality. The key features of the USB 2.0 OTG sub-system are

- Compliant with the USB 2.0 on-the-go specification revision 1.3a and 2.0
- High-speed (480Mbps) mode
- Full-speed (12Mbps) mode
- Low-speed (1.5Mbps) mode (host only)
- Support for session request protocol (SRP) and host negotiation protocol (HNP)
- One control endpoint 0 for control transfer
- Up to 15 device-programmable endpoints (excluding control endpoint 0):
  - Programmable endpoint type: Bulk, Isochronous, Interrupt
  - Programmable In/Out direction
- 16 host channels

3.1.8 USB HOST

The ARTIK 710/710s Module provides one USB 2.0 controller that is fully compliant with the USB 2.0 Host specifications, and the enhanced host controller Interface (EHCI) specification. The key features of the USB 2.0 Host sub-system are

- Detecting the attachment and removal of USB devices
- Collecting status and activity statistics
- Controlling power supply to attached USB devices
- In compliance with the UTMI+ Level 3 revision 1.0
- Controlling the association to either the open host controller interface (OHCI) or the EHCI via a port router
- Root Hub functionality to support upstream/downstream port

3.1.8.1 HSIC

The ARTIK 710/710s Module provides one high-speed inter-chip (HSIC) version 1.0 module, controlled by the USB Host Controller. The key features of the HSIC sub-system are

- Support for ping and split transactions
- Up to 30MHz operation for a 16-bit interface
- Up to 60MHz operation for a 8-bit interface
- Support for HSIC version 1.0

3.1.9 Gigabit EMAC

The ARTIK 710/710s Module provides one Gigabit EMAC interface. The most important features of the Ethernet MAC module are

- Standard compliance
  - IEEE 802.3az-2010: energy efficient Ethernet (EEE)
  - RGMII v2.6
- MAC supports the following features:
  - 10/100/1000 Mbps data transfer rates with an RGMII interface to communicate with external Gigabit PHY
  - Full duplex operation
  - Half duplex operation
  - Flexible address filtering
  - Additional frame filtering

3.1.10 SD/MMC

The ARTIK 710/710s Module provides one SD/MMC interface. The Mobile Storage Host is an interface between the system and the SD/MMC. The key features of mobile storage host sub-system are as follows:

3.1.10.1 SD

- Support for Secure Digital I/O (SDIO – version 3.0)
- Support for Secure Digital Memory (SDMEM – version 3.0)
- Consumer Electronics Advanced Transport Architecture (CE-ATA-version 1.1)
- Support 4-bit SDR mode up to 50MHz
- Support for PIO and DMA mode data transfer
- Support for 4- bit data bus width

3.1.10.2 MMC

- Support for Multimedia Cards (MMC – version 4.41)
- Support for Embedded Multimedia Cards (eMMC – version 4.5)
- Support for 4-bit SDR mode up to 50MHz
- Support for PIO and DMA mode data transfer
- Support for 4- bit data bus width

3.1.11 PCM

The ARTIK 710/710s Module provides one PCM channel. The PCM interface provides a bi-directional serial interface that can be connected to an external audio . The key features of the PCM subsystem are

- Supports both Master and Slave mode external audio codecs
- Supports both short and long frame synchronization
- Supports a variety of data formats with a default format of 13-bit 2's complement, left justified, clock MSB first

3.1.12 MIPI CSI

The ARTIK 710/710s Module provides one 4-lane mobile industry processor interface (MIPI) interface that complies with the MIPI camera serial interface (CSI) standard specification V1.01r06 and D-PHY standard specification v1.0. The key features of the MIPI CSI sub-system are

- 1, 2, 3 or 4 data lanes
- Support for the following image formats:
  - YUV420, YUV420 (Legacy), YUV420 (CSPS), 8-bit YUV422, 10-bit YUV422
  - User-defined byte-based data packet
  - Compatible to PPI (Protocol to PHY interface)

3.1.13 MIPI DSI

The ARTIK 710/710s Module provides one 4-lane MIPI interface that complies with the MIPI DSI standard specification V1.01r11. The key features of the MIPI DSI sub-system are

- Maximum resolution ranges up to 1920×1080
- Supports 1, 2, 3 or 4 data lanes
- Supports pixel format:
  - 16bpp, 18bpp packed, 18bpp loosely packed (3 byte), 24bpp
- Supported interfaces are
  - Protocol-to-PHY Interface (PPI) up to 1.5Gbps, in MIPI D-PHY
  - RGB Interface for video image input from display controller
  - PMS control interface for PLL to configure byte clock frequency
  - Prescaler to generate escape clock from byte clock

3.1.14 HDMI

The ARTIK 710/710s Module provides one HDMI v1.4a interface. The key features of the HDMI sub-system are

- Support for v1.4a spec
- Up to 1080p video resolution
- HDMI Link + HDMI PHY
- Support for the following video formats:
  - 480p@59.94/60Hz
  - 576p@50Hz
  - 720p@50/59.94/60Hz
  - 1080p@50/59.94/60Hz (No support for interlaced format)
- Support for 4:4:4 RGB
- Support for up to 8-bits per color

3.1.15 LVDS

The ARTIK 710/710s Module provides five low voltage differential signaling (LVDS) output channels with one clock channel. The key features of the LVDS channel system are

- Output clock range 30–125MHz
- Support for 630 Mbps per channel
- Up to 393.75MB/s data transport
- Support for power down mode

3.1.16 Video Input Processor

The ARTIK 710/710s Module provides one video input processor (VIP). The key features of the VIP sub-system are

- Support for external 8-bit and 16-bit MIPI
- Support for internal MIPI-CSI
- Support for images up to 8192×8192
- Support for clipping and scale-down
- Support for YUV420 memory format

3.1.17 Scaler

The ARTIK 710/710s Module provides one universal scaler. The key features of the scaler are

- Support for different input formats:
  - YUV420, YUV422, YUV444
- Flexible size, from 8×8 up to 1920×1080 with a granularity of 8
- Upscale ratio from 8×8 to 1920×1080
- Downscale ratio from 1920×1080 to 8×8
- Low pass filter available after upscale or before downscale
- Horizontal 5-tab filter with 64 sets of coefficients
- Vertical 3-tab filter with 32 sets of coefficients

3.1.18 Multiformat Codec

The ARTIK 710/710s Module provides one integrated Multiformat Codec (MFC) module. The key features of the MFC sub-system are

- Decoder:
  - H.264 : BP, MP, HP Level 4.2 up to 1920×1080, up to 50Mbps
  - MPEG4 : Advanced Simple Profile (ASP) up to 1920×1080, at up to 40Mbps
  - H.263 : Profile 3 up to 1920×1080, up to 20Mbps
  - MPEG 1,2 : Main Profile, High Level up to 1920×1080, up to 80Mbps
- Encoder:
  - H.264 : Baseline profile, Level 4.0 up to 1080p, up to 20Mbps
  - MPEG4 : Simple profile, Level 5.6 up to 1080p, up to 20Mbps
  - H.263 : Profile 3, Level 70 up to 1080p, up to 20Mbps

3.1.19 Graphics Pipeline

The ARTIK 710/710s Module provides one 2D and 3D graphics pipeline module. The key features of the graphics pipeline are

- Two pixel processors:
  - Tile oriented processing
  - Alpha blending
  - Texture support, non-power-of-2
  - Cube mapping
  - Fast dynamic branching
  - Trigonometric acceleration
  - Full floating-point arithmetic
  - Line, quad, triangle and point sprites
  - Perspective correct texturing
  - Point sampling, bilinear and trilinear filtering
  - 8-bit stencil buffering
  - 4-level hierarchical Z and stencil operation
- Geometry processor:
  - Programmable vertex shader
  - Flexible input and output formats
  - Autonomous operation tile list generation
  - Indexed and non-indexed geometry input
  - Primitive constructions with points, lines, triangles and quads
- Support for OpenGL ES 1.0 and 2.0

3.1.20 ADC

The ADC interface controls one 28nm low-power CMOS 1.8V 12-bit ADC. The key features of the ADC sub-system are

- Up to six channels of analog input can be selected
- Conversion of analog input into 12-bit binary code up to 1 Mega Sample Per Second (MSPS)
- 1.0mW power consumption when running 1MSPS
- Input frequency up to 100kHz

3.1.21 GPIO

The ARTIK 710/710s Module provides a GPIO system with up to 110 GPIOs multiplexed with other I/O interface lines, as shown in *Figure 2* to support a wide variety of use-cases. The key features of the GPIO system are as follows:

- Both edge detect and level detect functionality
- Support for programmable pull-up/pull-down resistors

- Support for fast or normal slew operation
- Drive strength can be set from a register:

Value	Drive Strength [a]
0	2.6mA approximately (default)
1	5.2mA approximately
2	10.4mA approximately
3	15.6mA approximately

a. Assumes the reference I/O voltage is 3.3V. All drive-strength values are approximate. This value represents the current drive capability of GPIO pad only. Do not use GPIO as a current source.

- Support for interrupt generation that can be triggered on one of the following:
  - Rising edge
  - Falling edge
  - High level detection
  - Low level detection
- The I/O data is clocked up to 50MHz

3.1.22 I²S

The ARTIK 710/710s Module provides two 5-line Inter-IC Sound (I^2S) channels. I^2S is one of the most popular digital audio interfaces. The I^2S bus handles audio data and other signals, such as subcoding and control. It is possible to transmit data between two I^2S buses. The key features of the I^2S sub-system are

- One-port stereo (1 channel) I^2S-bus for audio with DMA based operation
- Serial data transfer of 16/24 bits per channel in Master and Slave mode
- A variety of interface modes:
  - I^2S, Left justified, Right justified, DSP mode

3.1.23 Timer

The ARTIK 710/710s Module has four dedicated timer channels. The most important features of the Timer module are

- Timer or watchdog timer modes
- Four dedicated Timer channels with watchdog timer
- Normal interval timer mode with interrupt request
- Reset on timer countdown
- Level-triggered interrupt mechanism

3.1.24 PWM

The ARTIK 710/710s Module provides two pulse width modulation (PWM) instances with the following key features:

- Two individual PWM channels with independent duty control and polarity
- Two 32-bit PWM timers, one per channel
- Support for static as well as dynamic setup
- Support for auto-reload and one-shot pulse mode
- Dead zone generator
- Level interrupt generation
-

3.1.25 SPI

The ARTIK 710/710s Module provides two Serial Peripheral Interface (SPI) ports that transfer serial data. SPI support includes 8-bit/16-bit shift registers to transmit and receive data. During an SPI transfer, data is simultaneously transmitted (shifted out serially) and received (shifted in serially). The SPI implementation adheres to the protocols described by Texas Instruments Synchronous Serial Interface, National Semiconductor's Microwire, and Motorola's Serial Peripheral Interface. The key features of the SPI sub-system are

- Support for full-duplex
- 8-bit/16-bit shift register for Tx and Rx
- Compliant with the SPI protocol described by Texas Instruments, National Semiconductor and Motorola
- Support for independent 16-bit wide transmit and receive FIFOs 8 locations deep
- Support for master mode and slave mode
- Support for receive-without-transmit operation
- Max operating frequency :
  - Master Mode : Supports Tx up to 50MHz, Rx up to 20MHz
  - Slave Mode : Supports Tx up to 8MHz, Rx up to 8MHz

3.1.26 UART

The ARTIK 710/710s Module provides three 2-pin universal asynchronous receiver transmitters (UARTs). The key features of the UART sub-system are

- Separate 64×8 Tx and 64×8 Rx FIFO memory buffers
- Support for DMA-mode and interrupt-based mode of operation
- All independent channels support IrDA 1.0
- Each UART channel contains:
  - Programmable baud-rates
  - 1 or 2 stop bit insertion

  - 5-bit, 6-bit, 7-bit, or 8-bit data width
  - Parity checking

3.1.27 I²C

The ARTIK 710/710s Module provides three generic I²C blocks supporting both 100kb/s and 400kb/s speed modes.
The key features of the I²C sub-system are

- Support for multi-master mode
- 7-bit addressing mode only
- Serial, 8-bit oriented and bi-directional data transfer
- Up to 100 kb/s in the standard mode
- Up to 400 kb/s in the fast mode
- Support for both interrupt and polling events

3.1.28 JTAG

The JTAG core provides debug capabilities for the developer and is compliant with the IEEE 1149 standard.

3.1.29 Interrupt Controller

The ARTIK 710/710s Module has one interrupt controller module. The most important features of the interrupt module are

- Vectored interrupt controller
- Support for four interrupt types
  - Sixteen software generated interrupts
  - Six external Private Peripheral Interrupts (PPIs) per processor
  - One internal PPI for each processor
  - 128 shared peripheral interrupts
- For each interrupt source the following properties are available:
  - Fixed hardware interrupt priority level
  - Programmable interrupt priority level
  - Hardware interrupt priority level masking
  - IRQ and FIQ generation
  - Software interrupt generation
  - Test registers
  - Raw interrupt status
  - Interrupt request status

3.1.30 DMA

The ARTIK 710/710s Module has one scatter-gather DMA module. The most important features of the DMA module are

- 16 channels of dedicated DMA
- 16 DMA request lines
- Various operating modes
  - Single DMA mode
  - Burst DMA mode
  - Memory-to-memory transfer
  - Memory-to-peripheral transfer
  - Peripheral-to-memory transfer
  - Peripheral-to-peripheral transfer
- Support for 8/16/32 bit wide transactions
- Big endian and little endian (default) support

3.1.31 RTC

The ARTIK 710/710s Module has one real time clock (RTC) module. The most important features are

- Four spread-spectrum PLLs
- Two external crystals: one 24MHz crystal for the PLLs and one 32.768KHz crystal for the RTC
- One 32-bit RTC counter
- Support for alarm interrupt using RTC
- Support for various power modes:
  - Normal, Idle, and Sleep (Suspend to RAM)

3.1.32 Security Subsystem

In addition to the Secure Element, the main processor on the module provides additional security features. The key features of the Security Controller sub-system are

- Secure 128-bit die ID (available to the ARTIK 710s Module only)
- Secure JTAG featuring a secure 128-bit JTAG ID (available to the ARTIK 710s Module only)
- Secure boot featuring a 128-bit boot ID (available to the ARTIK 710s Module only)
- Security Controller (available to the ARTIK 710s Module only)
- Secure Element (all features in ARTIK 710s Module; limited features in ARTIK 710 Module)

3.1.32.1 Security Controller

The Security Controller provides ARM TrustZone features and hardware cryptographic accelerators as follows:

- ARM TrustZone
  - TZPC (TrustZone Platform Controller)
  - TZASC (TrustZone Address Space Controller)
  - TZMA (TrustZone Memory Adapter)
- Hardware cryptographic accelerators
  - DES, Triple DES
  - AES
  - SHA-1
  - MD5

3.1.32.2 Secure Element

The ARTIK 710/710s Module has a dedicated Secure Element to assure end-to-end authentication and communication between nodes in an IoT setting. The most important hardware features of the Secure Element are

- An ISO/IEC 7816 14443-compliant interface.
- Dedicated 16-bit SecuCalm CPU core
- Crypto co-processor
  - Modular exponential accelerator
  - RSA 2080 bits
  - ECC 512 bits
- Data security
  - Memory encryption for all memory
  - 256B read-only and 256B nonerasable Flash area
  - Selective reset operation if abnormal voltages/frequencies are detected
- Embedded tamper-free memory
  - 32KB ROM
  - 264KB Flash
  - 2.5KB cryptographic memory
- Serial interfaces:
  - ISO 7816-3-compliant interface
  - Asynchronous half-duplex character receive/transmit serial interface