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SAMSUNG

ARTIK™ Modules

0

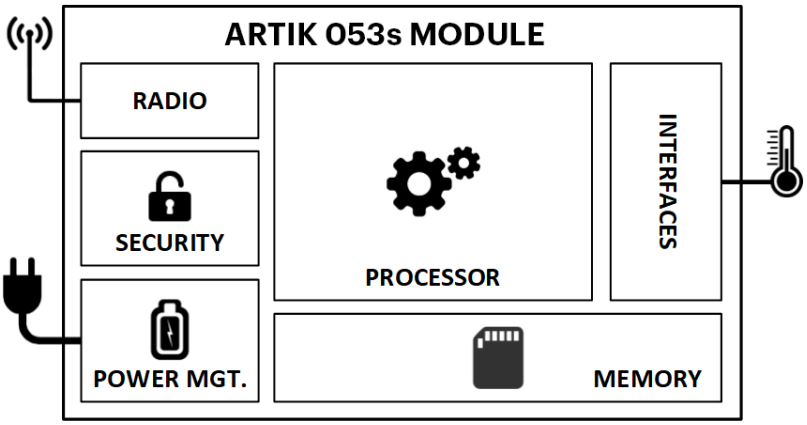
ARTIK 053/053s Module Datasheet

Module Overview

Figure 1. ARTIK 053s Module Top View

The Samsung ARTIK™ 053/053s Module is a highly integrated module for secure Internet of Things (IoT) devices that require Wi-Fi® connectivity. It is based on an ARM® Cortex® R4 core, with on-module RAM and flash memory, a complete 2.4GHz Wi-Fi subsystem with on-module antenna, an independent security subsystem, PUF-based module authentication, and a large complement of standard I/O interfaces. The Wi-Fi system supports IPv6 addressing to conform with EU standards.

The ARTIK 053/053s Module provides excellent performance in a variety of environments, with a feature set tailored specifically for IoT end nodes.



Processor	
CPU	32-bit ARM® Cortex® R4 with 32KB I-Cache and 32KB D-Cache @ 320MHz
Memory	
RAM	1280KB (General usage) 128KB (Global IPC data)
FLASH	8MB Flash
Security (ARTIK 053s only)	
Secure Subsystem	AES/DES/TDES, SHA-1/SHA-2, PKA (Public Key Accelerator), PRNG/DTRNG (Random Number Generators), Secure key storage
PUF	Physically Unclonable Function
Radio	
Wi-Fi	Certified IEEE802.11™ b/g/n Wi-Fi® 2.4GHz radio served by a dedicated 32-bit ARM Cortex R4 with 32KB I-Cache and 16KB D-Cache @ 480MHz. Supports IPv6 addressing to conform to EU standards.
Regulatory	FCC (U.S.), IC (Canada), CE (EU), KC (Korea), SRRC (China)
Power Management	
Single Supply	Wide voltage input range of 5–12V
Interfaces	
I/O	UART, I^2C, SPI, PWM, ADC, GPIO. I^2S
Form Factor	
Dimensions	15mm W x 40mm D x 3.9mm H

Operation Environment	
Temperature	–20 to 85 ^{o}C T_c

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Version History

Revision	Date	Description
V1.0	April 26, 2017	First release
V1.1	November 20, 2017	Updated *Figure 4* pinout. Updated *Table 2* to show GPP16 and GPP21. Updated *Module Antenna Placement Requirements*. Updated *Recommended Operating Conditions*. Updated other tables to show GPIO alternate functions. Changed temperature specifications in *Recommended Operating Conditions*. Added *Power and Current Consumption*.
V1.2	November 28, 2017	Modified GPIO name for XSPI1_MISO,XSPI1_MOSI, XSPI1_CLK, and XSPI1_CSN in *Table 1* and *Table 4* to be consistent with assigned GPIO name in *Table 2*. Removed GPIO names from *Table 9*. Added maximum storage temperature range, T_A, in *Absolute Maximum Rating* section.
V1.3	January 10, 2018	Updated *Mechanical Specifications*. Updated CE disclosure in *CE Statement* from R&TTE to Radio Equipment Directive. *I^2S Interface*: Changed features to indicate that the interface operates in slave mode only.
V1.4	February 23, 2018	*Module Overview*, *Wi-Fi Subsystem*: Added support for IPv6 addressing. *Table 2*: Changed hardware GPIO number to GPIO group numbers, GPPxx, GPGxx, and GPAxx. Added column for software GPIO number.
V1.5	April 9, 2018	*Table 2*: Changed hardware GPIO number to GPIO group numbers, GPPxx, GPGxx, and GPAxx. Added column for software GPIO number.

Block Diagram

Figure 2 shows a functional block diagram of the ARTIK 053/053s Module.

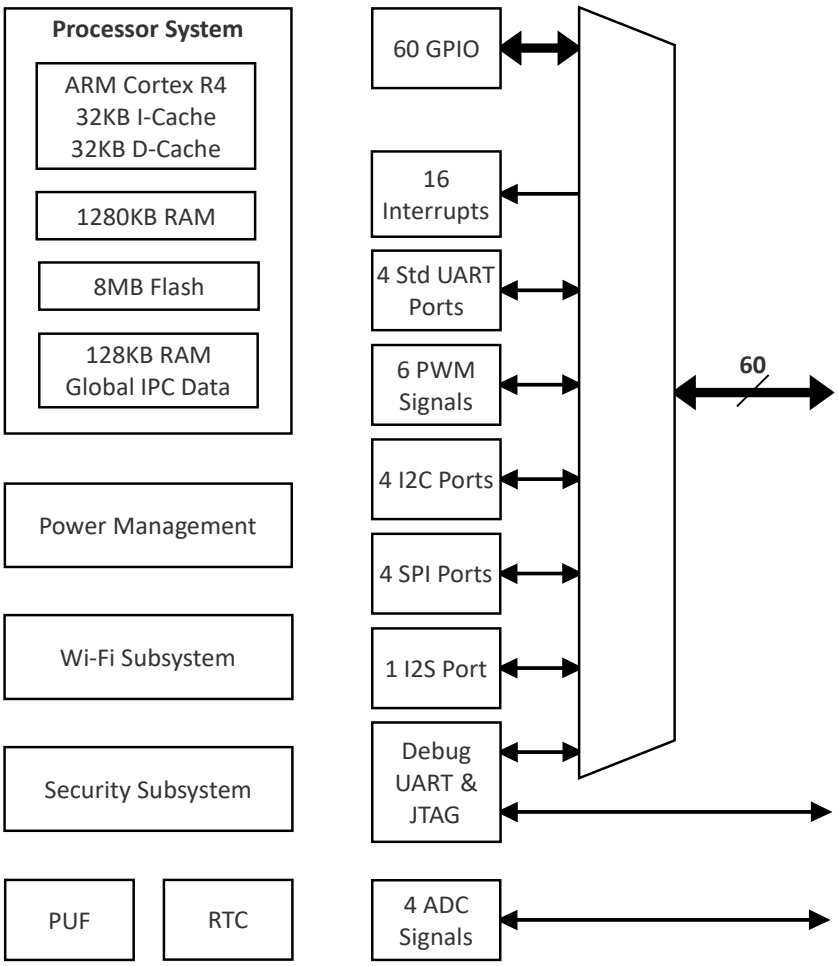

Figure 2. ARTIK 053/053s Module Block Diagram

CPU

The ARTIK 053/053s Module CPU has an ARM® Cortex® R4. It has the following features:

- 32KB of Instruction Cache (I-Cache)
- 32KB of Data Cache (D-Cache)
- 320MHz execution clock
- R4 core tuned for embedded and real-time applications

Memory

The ARTIK 053/053s Module on-module memory has the following features:

- CPU and general purpose RAM
  - 1280KB CPU RAM
  - 128KB global Inter-Process Communication (IPC) RAM
- 8MB flash

Real Time Clock

The ARTIK 053/053s Module has a Real Time Clock (RTC) for tracking date/time. The RTC has the following features:

- Binary-Coded Decimal (BCD) coded seconds, minutes, hour, day of the week, day, month, and year
- Leap year detection and compensation
- Millisecond tick time interrupt for Real-Time Operating System (RTOS) kernel time tick

PUF Unit (ARTIK 053s Module Only)

The ARTIK 053s Module has a Physically Unclonable Function (PUF) unit. The PUF unit has the following features:

- Generates unique key values, locked to an individual ARTIK 053s Module
- The algorithm construction is unique to each module
- Allows individual ARTIK 053/053s Modules to be “fingerprint-identified”

Security Subsystem (ARTIK 053s Module Only)

The ARTIK 053s Module has an independent security subsystem to ensure secure end-to-end operation in any IoT environment. The security subsystem includes the following features:

- Secure IPC Mailbox for inter-subsystem communication
- Encapsulated key support
  - Backup encryption key - 256 bits
  - Security subsystem root private key - 521 bits
  - Storage key - 256 bits
- Symmetric key engines
  - Secure AES
  - Secure DES/Triple-DES
- Stream cipher engine
  - ARC4 engine
- Various Hash engines
  - SHA-1, SHA2-256, SHA2-384, SHA2-512, MD5 HMAC
- Asymmetric key engines
  - PKA (Public Key Accelerator) engine
- PRNG (Pseudo Random Number Generator)
- DTRNG (Digital True Random Number Generator)
- Secure key storage

Wi-Fi Subsystem

The ARTIK 053/053s Module has an 802.11b/g/n Wi-Fi subsystem. The Wi-Fi subsystem has the following features:

- 802.11™ b/g/n support at 2.4GHz
- 20MHz single stream (802.11n)
- WPA/WPA2
- Dedicated Wi-Fi Processor subsystem with 480MHz 32-bit ARM Cortex R4 supported by 32KB I-Cache and 16KB D-Cache.
- Support for IPv6 addressing.

GPIO Interfaces

The ARTIK 053/053s Module has flexible General Purpose Input Output (GPIO) interfaces:

- 60 configurable GPIO ports
- Independently configurable for either general purpose input or output
- 43 configurable for alternate functionality
- Configurable internal pull-up or pull-down resistors

SPI Interfaces

The ARTIK 053/053s Module has four SPI interfaces, each with the following features:

- Full duplex communication
- 8, 16 or 32-bit shift registers and bus interface
- Motorola SPI protocol and National Semiconductor Microwire protocol
- Master and slave mode operation
- Two independent 32-bit wide transmit/receive FIFOs
- Transmit and receive speeds up to 50MHz

I^2C Interfaces

The ARTIK 053/053s Module has four high speed multi-master I^2C interfaces available, with speeds up to 3.4Mbps.

PWM Interfaces

The ARTIK 053/053s Module has six PWM timers, each with the following features:

- 32 bits of resolution for each PWM signal
- Two 8-bit prescalers (first level of division) and 5 clock dividers/multiplexers for second-level division
- Continuous run or one-shot pulse mode
- Dead zone generator to avoid simultaneous change of multiple PWM signals
- Interrupt generation

I^2S Interface

The ARTIK 053/053s Module has one I^2S interface with the following features:

- Each channel includes a 32-bit × 64 data FIFO for both transmit and receive
- Supports stereo I^2S bus channels with external DMA-based operations
- Can mix two sound sources from a primary and secondary source
- Serial data transfer formats of 8 bits, 16 bits, or 24 bits per channel
- Supports both MSB and LSB justified data formats
- Operates in I^2S slave mode only

ADC Interfaces

The ARTIK 053/053s Module has four analog-to-digital converter (ADC) channels. Each interface has the following features:

- 12-bit resolution
- ADC conversion clock at 1.08 mega-samples per second (MSPS) using a main 6.5MHz clock
- Supports sample averaging over 1, 2, 4, 8, 16, 32, or 64 samples
- Differential non-linearity error range of ±2 LSB bits (value of ±2)
- Integral non-linearity error range of ±3 LSB bits (value of ±6)
- Top and bottom offset error range of ±4 LSB bits (value of ±10)
- Voltage range up to 1.8V

Figure 3 depicts the dynamic behavior between input voltage on the ADC and resulting LSB value in the ADC register.

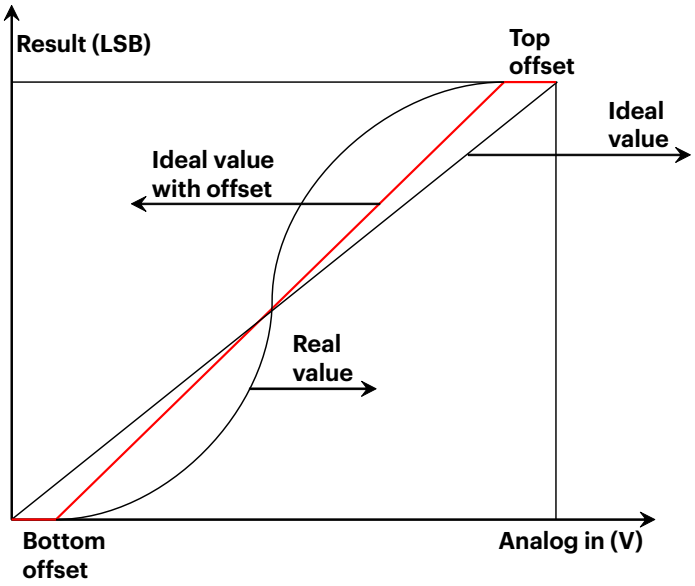

Figure 3. ADC LSB behavior

UART Interfaces

The ARTIK 053/053s Module has five 2-pin UART interfaces; UART0 (RXD/TXD has a level-shifter FET to support a 5V UART interface and is used in the debug block. Each has the following features:

- Can be operated in DMA or interrupt-based mode
- Support for 5, 6, 7, or 8-bit serial data transmit and receive
- Programmable baud rate
- One or two stop-bit insertion

Module Pad Physical Layout

The ARTIK 053/053s Module utilizes 79 signal, power, and ground pads. The figure below shows how the physical layout orients the signal pads assigned at the edge of the ARTIK 053/053s Module. *Figure 1* shows the edge pads and the signal names.

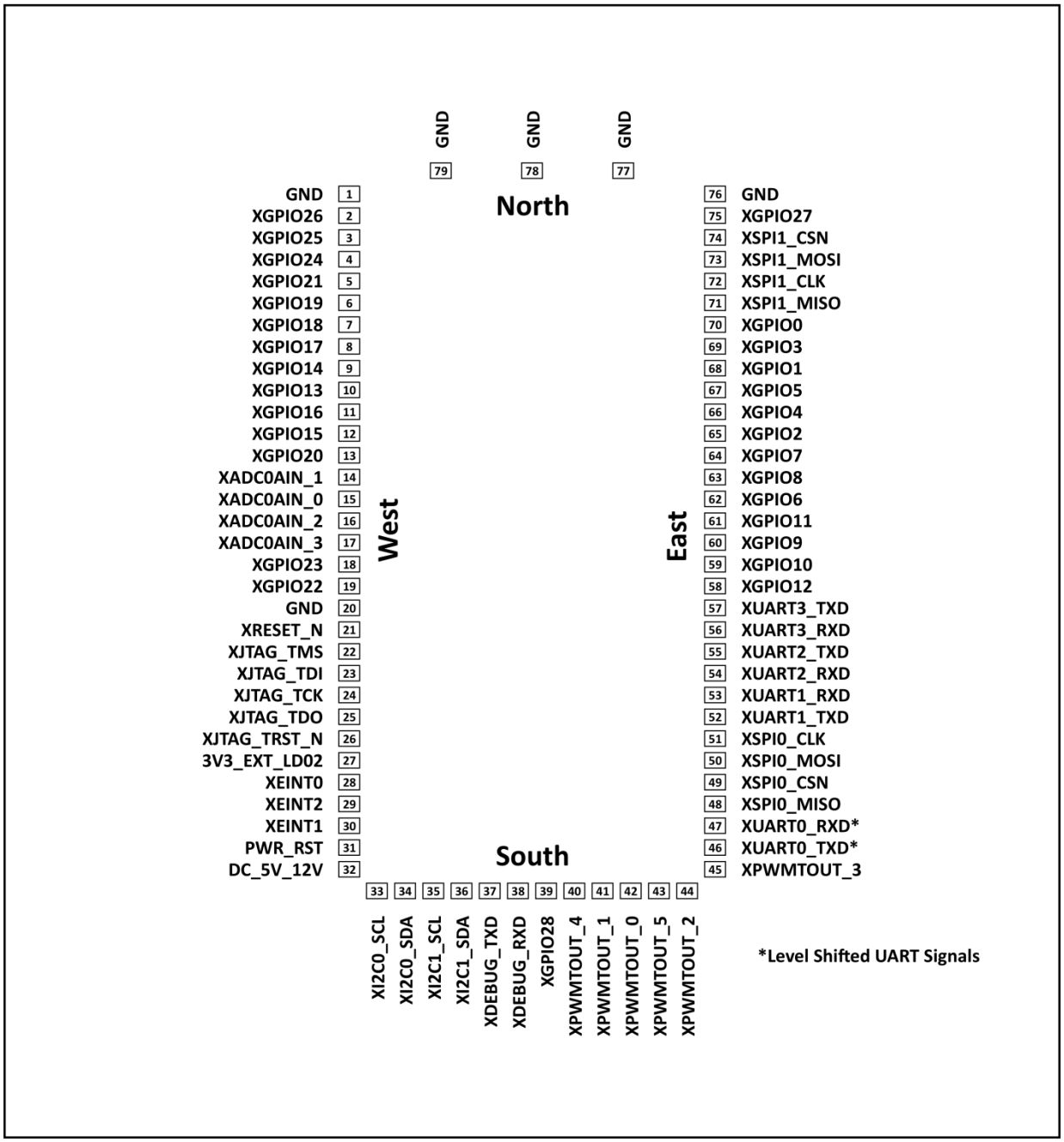

Figure 4. ARTIK 053/053s Module Edge Pinout (Top View)

Module Pad Signal Definitions

The tables below describes the characteristics of the ARTIK 053/053s Module pad signals. Some signals can be configured for alternate functionality. The remaining signals have dedicated functionality. Refer to the following column definitions.

- **Pad Number** defines the signal pad on the edge of the module. Refer to *Figure 4* for pad/signal physical layout.
- **Pad Name** defines the net list name of the signal. The pad name may reflect on one of the possible optional signal functionality, and dictates the default power-on function.
- **GPIO Name** defines a generic name for referring to GPIO signals regardless of their current configured functionality. The name order is the same order as the GPIO signals appear in the GPIO configuration registers.
- **PU/PD** defines the power-on state of the internal pull up/pull down definition. PU:pull up, PD:pull down, N:no pull up/down.
- **GPIO Drive** defines the power-on state drive strength of GPIO and other signals. Configurable to 2mA, 4mA, 8mA, or 12mA. Do not use GPIO signals to power discrete components directly (such as LEDs). Use an external driver device instead (such as a transistor).
- **Option 1 - Option 6** lists the alternative functionality some signals can be configured to. Those signals without any options are dedicated to their function. The pad name signifies the default power-on state.

Table 1. ARTIK 053/053s Module Pinout Signal Descriptions

Pad Number	Pad Name & Default Function	GPIO Name	PU/PD	GPIO Drive	Option 0	Option 1	Option 2	Option 3	Option 4	Option F
1	GND	–	–	–	–	–	–	–	–	–
2	XGPIO26	GPG32	PD	2mA	GP Input	GP Output	I2S_0_SDO	–	–	–
3	XGPIO25	GPG31	PD	2mA	GP Input	GP Output	I2S_0_LRCK	–	–	–
4	XGPIO24	GPG30	PD	2mA	GP Input	GP Output	I2S_0_BCLK	–	–	–
5	XGPIO21	GPG25	PD	2mA	GP Input	GP Output	–	–	–	NWEINT_GPG2[5]
6	XGPIO19	GPG23	PD	2mA	GP Input	GP Output	–	–	–	NWEINT_GPG2[3]
7	XGPIO18	GPG22	PD	2mA	GP Input	GP Output	–	–	–	NWEINT_GPG2[2]
8	XGPIO17	GPG21	PD	2mA	GP Input	GP Output	–	–	–	NWEINT_GPG2[1]
9	XGPIO14	GPG16	PD	2mA	GP Input	GP Output	–	–	–	NWEINT_GPG1[6]
10	XGPIO13	GPG15	PD	2mA	GP Input	GP Output	–	–	–	NWEINT_GPG1[5]
11	XGPIO16	GPG20	PD	2mA	GP Input	GP Output	–	–	–	NWEINT_GPG2[0]
12	XGPIO15	GPG17	PD	2mA	GP Input	GP Output	–	–	–	NWEINT_GPG1[7]
13	XGPIO20	GPG24	PD	2mA	GP Input	GP Output	–	–	–	NWEINT_GPG2[4]
14	XADC0AIN_1	–	–	–	–	–	–	–	–	–
15	XADC0AIN_0	–	–	–	–	–	–	–	–	–
16	XADC0AIN_2	–	–	–	–	–	–	–	–	–
17	XADC0AIN_3	–	–	–	–	–	–	–	–	–
18	XGPIO23	GPG27	PD	2mA	GP Input	GP Output	–	–	–	NWEINT_GPG2[7]
19	XGPIO22	GPG26	PD	2mA	GP Input	GP Output	–	–	–	NWEINT_GPG2[6]
20	GND	–	–	–	–	–	–	–	–	–
21	XRESET_N	–	–	–	–	–	–	–	–	–
22	XJTAG_TMS	–	PU	–	–	–	–	–	–	–
23	XJTAG_TDI	–	PU	–	–	–	–	–	–	–
24	XJTAG_TCK	–	PD	–	–	–	–	–	–	–
25	XJTAG_TDO	–	PD	2mA	–	–	–	–	–	–

Table 1. ARTIK 053/053s Module Pinout Signal Descriptions (Continued)

Pad Number	Pad Name & Default Function	GPIO Name	PU/PD	GPIO Drive	Option 0	Option 1	Option 2	Option 3	Option 4	Option F
26	XJTAG_TRST_N	–	PD	–	–	–	–	–	–	–
27	3V3_EXT_LDO2	–	–	–	–	–	–	–	–	–
28	XEINT_0	GPA00	PD	2mA	GP Input	GP Output	–	–	–	NWEINT_GPA0[0]
29	XEINT_2	GPA02	PD	2mA	GP Input	GP Output	–	–	–	NWEINT_GPA0[2]
30	XEINT_1	GPA01	PD	2mA	GP Input	GP Output	–	–	–	NWEINT_GPA0[1]
31	GND	–	–	–	–	–	–	–	–	–
32	DC_5V_12V	–	–	–	–	–	–	–	–	–
33	XI2C0_SCL	GPA10	PD	8mA	GP Input	GP Output	HSI2C_0_SCL	–	–	–
34	XI2C0_SDA	GPA11	PD	8mA	GP Input	GP Output	HSI2C_0_SDA	–	–	–
35	XI2C1_SCL	GPA12	PD	8mA	GP Input	GP Output	HSI2C_1_SCL	–	–	–
36	XI2C1_SDA	GPA13	PD	8mA	GP Input	GP Output	HSI2C_1_SDA	–	–	–
37	XDEBUG_TXD	–	–	–	–	–	–	–	–	–
38	XDEBUG_RXD	–	–	–	–	–	–	–	–	–
39	XGPIO28	GPP24	PD	8mA	GP Input	GP Output	–	–	–	–
40	XPWMTOUT_4	GPP25	PD	8mA	GP Input	GP Output	PWM_TOUT_5	–	–	–
41	XPWMTOUT_1	GPP21	PD	8mA	GP Input	GP Output	PWM_TOUT_1	COUNTER_0	UART_3_RTSn	–
42	XPWMTOUT_0	GPP20	PD	8mA	GP Input	GP Output	PWM_TOUT_0	–	UART_3_CTSn	–
43	XPWMTOUT_5	GPP26	PD	8mA	GP Input	GP Output	PWM_TOUT_6	–	–	–
44	XPWMTOUT_2	GPP22	PD	8mA	GP Input	GP Output	PWM_TOUT_2	–	–	–
45	XPWMTOUT_3	GPP23	PD	8mA	GP Input	GP Output	PWM_TOUT_3	–	–	–
46	XUART0_TXD	GPA21	PD	8mA	GP Input	GP Output	UART_0_TXD	–	–	–
47	XUART0_RXD	GPA20	PD	8mA	GP Input	GP Output	UART_0_RXD	–	–	–
48	XSPI0_MISO	GPP02	PD	8mA	GP Input	GP Output	SPI_0_MISO	–	–	–
49	XSPI0_CSN	GPP01	PD	8mA	GP Input	GP Output	SPI_0_CSn	–	–	–
50	XSPI0_MOSI	GPP03	PD	8mA	GP Input	GP Output	SPI_0_MOSI	–	–	–
51	XSPI0_CLK	GPP00	PD	8mA	GP Input	GP Output	SPI_0_CLK	–	–	–
52	XUART1_TXD	GPP05	PD	8mA	GP Input	GP Output	UART_1_TXD	UART_2_RTSn	–	–
53	XUART1_RXD	GPP04	PD	8mA	GP Input	GP Output	UART_1_RXD	UART_2_CTSn	–	–
54	XUART2_RXD	GPP06	PD	8mA	GP Input	GP Output	UART_2_RXD	–	–	–
55	XUART2_TXD	GPP07	PD	8mA	GP Input	GP Output	UART_2_TXD	–	–	–
56	XUART3_RXD	GPP16	PD	8mA	GP Input	GP Output	UART_3_RXD	–	–	–
57	XUART3_TXD	GPP17	PD	8mA	GP Input	GP Output	UART_3_TXD	–	–	–
58	XGPIO12	GPG14	PD	2mA	GP Input	GP Output	–	–	–	NWEINT_GPG1[4]
59	XGPIO10	GPG12	PD	2mA	GP Input	GP Output	SPI_3_MISO	–	–	NWEINT_GPG1[2]
60	XGPIO9	GPG11	PD	2mA	GP Input	GP Output	SPI_3_CSn	–	–	NWEINT_GPG1[1]
61	XGPIO11	GPG13	PD	2mA	GP Input	GP Output	SPI_3_MOSI	–	–	NWEINT_GPG1[3]
62	XGPIO6	GPG06	PD	2mA	GP Input	GP Output	SPI_2_MISO	–	–	–
63	XGPIO8	GPG10	PD	2mA	GP Input	GP Output	SPI_3_CLK	–	–	NWEINT_GPG1[0]
64	XGPIO7	GPG07	PD	2mA	GP Input	GP Output	SPI_2_MOSI	–	–	–
65	XGPIO2	GPG02	PD	2mA	GP Input	GP Output	HSI2C_3_SCL	–	–	–
66	XGPIO4	GPG04	PD	2mA	GP Input	GP Output	SPI_2_CLK	–	–	–
67	XGPIO5	GPG05	PD	2mA	GP Input	GP Output	SPI_2_CSn	–	–	–
68	XGPIO1	GPG01	PD	2mA	GP Input	GP Output	HSI2C_2_SDA	–	–	–
69	XGPIO3	GPG03	PD	2mA	GP Input	GP Output	HSI2C_3_SDA	–	–	–
70	XGPIO0	GPG00	PD	2mA	GP Input	GP Output	HSI2C_2_SCL	–	–	–
71	XSPI1_MISO	GPA42	PD	2mA	GP Input	GP Output	SPI_1_MISO	–	–	–
72	XSPI1_CLK	GPA40	PD	2mA	GP Input	GP Output	SPI_1_CLK	–	–	–
73	XSPI1_MOSI	GPA43	PD	2mA	GP Input	GP Output	SPI_1_MOSI	–	–	–

Table 1. ARTIK 053/053s Module Pinout Signal Descriptions (Continued)

Pad Number	Pad Name & Default Function	GPIO Name	PU/PD	GPIO Drive	Option 0	Option 1	Option 2	Option 3	Option 4	Option F
74	XSPI1_CSN	GPA41	PD	2mA	GP Input	GP Output	SPI_1_CSn	–	–	–
75	XGPIO27	GPG33	PD	2mA	GP Input	GP Output	I2S_0_SDI	–	–	–
76	GND	–	–	–	–	–	–	–	–	–
77	GND	–	–	–	–	–	–	–	–	–
78	GND	–	–	–	–	–	–	–	–	–
79	GND	–	–	–	–	–	–	–	–	–

Module Pad Signal Definitions by Function

GPIO Interface

Table 2. GPIO Interface

GPIO Name	Pad Name & Default Function	Pad Number	SW GPIO #	GPIO Drive	Option 0	Option 1	Option 2	Option 3	Option 4	Option F
GPP00	XSPI0_CLK	51	–	8mA	GP Input	GP Output	SPI_0_CLK	–	–	–
GPP01	XSPI0_CSN	49	–	8mA	GP Input	GP Output	SPI_0_CSn	–	–	–
GPP02	XSPI0_MISO	48	–	8mA	GP Input	GP Output	SPI_0_MISO	–	–	–
GPP03	XSPI0_MOSI	50	–	8mA	GP Input	GP Output	SPI_0_MOSI	–	–	–
GPP04	XUART1_RXD	53	–	8mA	GP Input	GP Output	UART_1_RXD	UART_2_CTSn	–	–
GPP05	XUART1_TXD	52	–	8mA	GP Input	GP Output	UART_1_TXD	UART_2_RTSn	–	–
GPP06	XUART2_RXD	54	–	8mA	GP Input	GP Output	UART_2_RXD	–	–	–
GPP07	XUART2_TXD	55	–	8mA	GP Input	GP Output	UART_2_TXD	–	–	–
GPP16	XUART3_RXD	56	–	8mA	GP Input	GP Output	UART_3_RXD	–	–	–
GPP17	XUART3_TXD	57	–	8mA	GP Input	GP Output	UART_3_TXD	–	–	–
GPP20	XPWMTOUT_0	42	00	8mA	GP Input	GP Output	PWM_TOUT_0	–	UART_3_CTSn	–
GPP21	XPWMTOUT_1	41	01	8mA	GP Input	GP Output	PWM_TOUT_1	COUNTER_0	UART_3_RTSn	–
GPP22	XPWMTOUT_2	44	02	8mA	GP Input	GP Output	PWM_TOUT_2	–	–	–
GPP23	XPWMTOUT_3	45	03	8mA	GP Input	GP Output	PWM_TOUT_3	–	–	–
GPP24	XGPIO28	39	20	8mA	GP Input	GP Output	–	–	–	–
GPP25	XPWMTOUT_4	40	04	8mA	GP Input	GP Output	PWM_TOUT_5	–	–	–
GPP26	XPWMTOUT_5	43	05	8mA	GP Input	GP Output	PWM_TOUT_6	–	–	–
GPG00	XGPIO0	70	29	2mA	GP Input	GP Output	HSI2C_2_SCL	–	–	–
GPG01	XGPIO1	68	30	2mA	GP Input	GP Output	HSI2C_2_SDA	–	–	–
GPG02	XGPIO2	65	31	2mA	GP Input	GP Output	HSI2C_3_SCL	–	–	–
GPG03	XGPIO3	69	32	2mA	GP Input	GP Output	HSI2C_3_SDA	–	–	–
GPG04	XGPIO4	66	33	2mA	GP Input	GP Output	SPI_2_CLK	–	–	–
GPG05	XGPIO5	67	34	2mA	GP Input	GP Output	SPI_2_CSn	–	–	–
GPG06	XGPIO6	62	35	2mA	GP Input	GP Output	SPI_2_MISO	–	–	–
GPG07	XGPIO7	64	36	2mA	GP Input	GP Output	SPI_2_MOSI	–	–	–
GPG10	XGPIO8	63	37	2mA	GP Input	GP Output	SPI_3_CLK	–	–	NWEINT_GPG1[0]
GPG11	XGPIO9	60	38	2mA	GP Input	GP Output	SPI_3_CSn	–	–	NWEINT_GPG1[1]
GPG12	XGPIO10	59	39	2mA	GP Input	GP Output	SPI_3_MISO	–	–	NWEINT_GPG1[2]
GPG13	XGPIO11	61	40	2mA	GP Input	GP Output	SPI_3_MOSI	–	–	NWEINT_GPG1[3]
GPG14	XGPIO12	58	41	2mA	GP Input	GP Output	–	–	–	NWEINT_GPG1[4]
GPG15	XGPIO13	10	42	2mA	GP Input	GP Output	–	–	–	NWEINT_GPG1[5]
GPG16	XGPIO14	9	43	2mA	GP Input	GP Output	–	–	–	NWEINT_GPG1[6]
GPG17	XGPIO15	12	44	2mA	GP Input	GP Output	–	–	–	NWEINT_GPG1[7]
GPG20	XGPIO16	11	45	2mA	GP Input	GP Output	–	–	–	NWEINT_GPG2[0]
GPG21	XGPIO17	8	46	2mA	GP Input	GP Output	–	–	–	NWEINT_GPG2[1]
GPG22	XGPIO18	7	47	2mA	GP Input	GP Output	–	–	–	NWEINT_GPG2[2]
GPG23	XGPIO19	6	48	2mA	GP Input	GP Output	–	–	–	NWEINT_GPG2[3]
GPG24	XGPIO20	13	49	2mA	GP Input	GP Output	–	–	–	NWEINT_GPG2[4]
GPG25	XGPIO21	5	50	2mA	GP Input	GP Output	–	–	–	NWEINT_GPG2[5]

Table 2. GPIO Interface (Continued)

GPIO Name	Pad Name & Default Function	Pad Number	SW GPIO #	GPIO Drive	Option 0	Option 1	Option 2	Option 3	Option 4	Option F
GPG26	XGPIO22	19	51	2mA	GP Input	GP Output	–	–	–	NWEINT_GPG2[6]
GPG27	XGPIO23	18	52	2mA	GP Input	GP Output	–	–	–	NWEINT_GPG2[7]
GPG30	XGPIO24	4	53	2mA	GP Input	GP Output	I2S_0_BCLK	–	–	–
GPG31	XGPIO25	3	54	2mA	GP Input	GP Output	I2S_0_LRCK	–	–	–
GPG32	XGPIO26	2	55	2mA	GP Input	GP Output	I2S_0_SDO	–	–	–
GPG33	XGPIO27	75	56	2mA	GP Input	GP Output	I2S_0_SDI	–	–	–
GPA00	XEINT_0	28	57	2mA	GP Input	GP Output	–	–	–	NWEINT_GPA0[0]
GPA01	XEINT_1	30	58	2mA	GP Input	GP Output	–	–	–	NWEINT_GPA0[1]
GPA02	XEINT_2	29	59	2mA	GP Input	GP Output	–	–	–	NWEINT_GPA0[2]
GPA10	XI2C0_SCL	33	–	8mA	GP Input	GP Output	HSI2C_0_SCL	–	–	–
GPA11	XI2C0_SDA	34	–	8mA	GP Input	GP Output	HSI2C_0_SDA	–	–	–
GPA12	XI2C1_SCL	35	–	8mA	GP Input	GP Output	HSI2C_1_SCL	–	–	–
GPA13	XI2C1_SDA	36	–	8mA	GP Input	GP Output	HSI2C_1_SDA	–	–	–
GPA20	XUART0_RXD	47	–	8mA	GP Input	GP Output	UART_0_RXD	–	–	–
GPA21	XUART0_TXD	46	–	8mA	GP Input	GP Output	UART_0_TXD	–	–	–
GPA40	XSPI1_CLK	72	–	2mA	GP Input	GP Output	SPI_1_CLK	–	–	–
GPA41	XSPI1_CSN	74	–	2mA	GP Input	GP Output	SPI_1_CSn	–	–	–
GPA42	XSPI1_MISO	71	–	2mA	GP Input	GP Output	SPI_1_MISO	–	–	–
GPA43	XSPI1_MOSI	73	–	2mA	GP Input	GP Output	SPI_1_MOSI	–	–	–

I^{2}C Interface

Table 3. I^{2}C Interface

Pad Name & Default Function	Pad Number	GPIO Name	PU/PD	GPIO Drive	Option 0	Option 1	Option 2	Option 3	Option 4	Option F
XI2C0_SCL	33	GPA10	PD	8mA	GP Input	GP Output	HSI2C_0_SCL	–	–	–
XI2C0_SDA	36	GPA11	PD	8mA	GP Input	GP Output	HSI2C_0_SDA	–	–	–
XI2C1_SCL	35	GPA12	PD	8mA	GP Input	GP Output	HSI2C_1_SCL	–	–	–
XI2C1_SDA	36	GPA13	PD	8mA	GP Input	GP Output	HSI2C_1_SDA	–	–	–
XGPIO0	70	GPG00	PD	2mA	GP Input	GP Output	HSI2C_2_SCL	–	–	–
XGPIO1	68	GPG01	PD	2mA	GP Input	GP Output	HSI2C_2_SDA	–	–	–
XGPIO2	65	GPG02	PD	2mA	GP Input	GP Output	HSI2C_3_SCL	–	–	–
XGPIO3	69	GPG03	PD	2mA	GP Input	GP Output	HSI2C_3_SDA	–	–	–

SPI Interface

Table 4. SPI Interface

Pad Name & Default Function	Pad Number	GPIO Name	PU/PD	GPIO Drive	Option 0	Option 1	Option 2	Option 3	Option 4	Option F
XSPI0_CLK	51	GPP00	PD	8mA	GP Input	GP Output	SPI_0_CLK	–	–	–
XSPI0_CSN	49	GPP01	PD	8mA	GP Input	GP Output	SPI_0_CSn	–	–	–
XSPI0_MISO	48	GPP02	PD	8mA	GP Input	GP Output	SPI_0_MISO	–	–	–
XSPI0_MOSI	50	GPP03	PD	8mA	GP Input	GP Output	SPI_0_MOSI	–	–	–
XSPI1_CLK	72	GPA40	PD	2mA	GP Input	GP Output	SPI_1_CLK	–	–	–
XSPI1_CSN	74	GPA41	PD	2mA	GP Input	GP Output	SPI_1_CSn	–	–	–
XSPI1_MISO	71	GPA42	PD	2mA	GP Input	GP Output	SPI_1_MISO	–	–	–
XSPI1_MOSI	73	GPA43	PD	2mA	GP Input	GP Output	SPI_1_MOSI	–	–	–
XGPIO5	67	GPG05	PD	2mA	GP Input	GP Output	SPI_2_CSn	–	–	–
XGPIO4	66	GPG04	PD	2mA	GP Input	GP Output	SPI_2_CLK	–	–	–
XGPIO6	62	GPG06	PD	2mA	GP Input	GP Output	SPI_2_MISO	–	–	–
XGPIO7	64	GPG07	PD	2mA	GP Input	GP Output	SPI_2_MOSI	–	–	–
XGPIO9	60	GPG11	PD	2mA	GP Input	GP Output	SPI_3_CSn	–	–	NWEINT_GPG1[1]
XGPIO11	61	GPG13	PD	2mA	GP Input	GP Output	SPI_3_MOSI	–	–	NWEINT_GPG1[3]
XGPIO8	63	GPG10	PD	2mA	GP Input	GP Output	SPI_3_CLK	–	–	NWEINT_GPG1[0]
XGPIO10	59	GPG12	PD	2mA	GP Input	GP Output	SPI_3_MISO	–	–	NWEINT_GPG1[2]

I^2S Interface

Table 5. I^2S Interface

Pad Name & Default Function	Pad Number	GPIO Name	PU/PD	GPIO Drive	Option 0	Option 1	Option 2	Option 3	Option 4	Option F
XGPIO24	4	GPG30	PD	2mA	GP Input	GP Output	I2S_0_BCLK	–	–	–
XGPIO25	3	GPG31	PD	2mA	GP Input	GP Output	I2S_0_LRCK	–	–	–
XGPIO26	2	GPG32	PD	2mA	GP Input	GP Output	I2S_0_SDO	–	–	–
XGPIO27	75	GPG33	PD	2mA	GP Input	GP Output	I2S_0_SDI	–	–	–

ADC Interface

Table 6. ADC Interface

Pad Name & Default Function	Pad Number	GPIO Name	PU/PD	GPIO Drive	Option 0	Option 1	Option 2	Option 3	Option 4	Option F
XADC0AIN_0	15	–	–	–	–	–	–	–	–	–
XADC0AIN_1	14	–	–	–	–	–	–	–	–	–
XADC0AIN_2	16	–	–	–	–	–	–	–	–	–
XADC0AIN_3	17	–	–	–	–	–	–	–	–	–

PWM Interface

Table 7. PWM Interface

Pad Name & Default Function	Pad Number	GPIO Name	PU/PD	GPIO Drive	Option 0	Option 1	Option 2	Option 3	Option 4	Option F
XPWMTOUT_0	42	GPP20	PD	8mA	GP Input	GP Output	PWM_TOUT_0	–	UART_3_CTSn	–
XPWMTOUT_1	41	GPP21	PD	8mA	GP Input	GP Output	PWM_TOUT_1	COUNTER_0	UART_3_RTSn	–
XPWMTOUT_2	44	GPP22	PD	8mA	GP Input	GP Output	PWM_TOUT_2	–	–	–
XPWMTOUT_3	45	GPP23	PD	8mA	GP Input	GP Output	PWM_TOUT_3	–	–	–
XPWMTOUT_4	40	GPP25	PD	8mA	GP Input	GP Output	PWM_TOUT_5	–	–	–
XPWMTOUT_5	43	GPP26	PD	8mA	GP Input	GP Output	PWM_TOUT_6	–	–	–

UART Interface

Table 8. UART Interface

Pad Name & Default Function	Pad Number	GPIO Name	PU/PD	GPIO Drive	Option 0	Option 1	Option 2	Option 3	Option 4	Option F
XUART0_RXD	47	GPA20	PD	8mA	GP Input	GP Output	UART_0_RXD	–	–	–
XUART0_TXD	46	GPA21	PD	8mA	GP Input	GP Output	UART_0_TXD	–	–	–
XUART1_RXD	53	GPP04	PD	8mA	GP Input	GP Output	UART_1_RXD	UART_2_CTSn	–	–
XUART1_TXD	52	GPP05	PD	8mA	GP Input	GP Output	UART_1_TXD	UART_2_RTSn	–	–
XUART2_RXD	54	GPP06	PD	8mA	GP Input	GP Output	UART_2_RXD	–	–	–
XUART2_TXD	55	GPP07	PD	8mA	GP Input	GP Output	UART_2_TXD	–	–	–
XUART3_RXD	56	GPP16	PD	8mA	GP Input	GP Output	UART_3_RXD	–	–	–
XUART3_TXD	57	GPP17	PD	8mA	GP Input	GP Output	UART_3_TXD	–	–	–

Debug Interface

Table 9. Debug Interface

Pad Name & Default Function	Pad Number	GPIO Name	PU/PD	GPIO Drive	Option 0	Option 1	Option 2	Option 3	Option 4	Option F
XJTAG_TCK	24	–	PD	–	–	–	–	–	–	–
XJTAG_TMS	22	–	PU	–	–	–	–	–	–	–
XJTAG_TDI	23	–	PU	–	–	–	–	–	–	–
XJTAG_TDO	25	–	PD	–	–	–	–	–	–	–
XJTAG_TRST_N	26	–	PD	–	–	–	–	–	–	–
XDEBUG_RXD	38	–	PD	–	–	–	–	–	–	–
XDEBUG_TXD	37	–	PD	–	–	–	–	–	–	–

INT Interface

Table 10. Interrupt Interface

Pad Name & Default Function	Pad Number	GPIO Name	PU/PD	GPIO Drive	Option 0	Option 1	Option 2	Option 3	Option 4	Option F
XEINT_0	28	GPA00	PD	2mA	GP Input	GP Output	–	–	–	NWEINT_GPA0[0]
XEINT_1	30	GPA01	PD	2mA	GP Input	GP Output	–	–	–	NWEINT_GPA0[1]
XEINT_2	29	GPA02	PD	2mA	GP Input	GP Output	–	–	–	NWEINT_GPA0[2]
XGPIO8	63	GPG10	PD	2mA	GP Input	GP Output	SPI_3_CLK	–	–	NWEINT_GPG1[0]
XGPIO9	60	GPG11	PD	2mA	GP Input	GP Output	SPI_3_CSn	–	–	NWEINT_GPG1[1]
XGPIO10	59	GPG12	PD	2mA	GP Input	GP Output	SPI_3_MISO	–	–	NWEINT_GPG1[2]
XGPIO11	61	GPG13	PD	2mA	GP Input	GP Output	SPI_3_MOSI	–	–	NWEINT_GPG1[3]
XGPIO12	58	GPG14	PD	2mA	GP Input	GP Output	–	–	–	NWEINT_GPG1[4]
XGPIO13	10	GPG15	PD	2mA	GP Input	GP Output	–	–	–	NWEINT_GPG1[5]
XGPIO14	9	GPG16	PD	2mA	GP Input	GP Output	–	–	–	NWEINT_GPG1[6]
XGPIO15	12	GPG17	PD	2mA	GP Input	GP Output	–	–	–	NWEINT_GPG1[7]
XGPIO16	11	GPG20	PD	2mA	GP Input	GP Output	–	–	–	NWEINT_GPG2[0]
XGPIO17	8	GPG21	PD	2mA	GP Input	GP Output	–	–	–	NWEINT_GPG2[1]
XGPIO18	7	GPG22	PD	2mA	GP Input	GP Output	–	–	–	NWEINT_GPG2[2]
XGPIO19	6	GPG23	PD	2mA	GP Input	GP Output	–	–	–	NWEINT_GPG2[3]
XGPIO20	13	GPG24	PD	2mA	GP Input	GP Output	–	–	–	NWEINT_GPG2[4]
XGPIO21	5	GPG25	PD	2mA	GP Input	GP Output	–	–	–	NWEINT_GPG2[5]
XGPIO22	19	GPG26	PD	2mA	GP Input	GP Output	–	–	–	NWEINT_GPG2[6]
XGPIO23	18	GPG27	PD	2mA	GP Input	GP Output	–	–	–	NWEINT_GPG2[7]

Reset Interface

Table 11. Reset Interface

Pad Name	Pad Number
XRESET_N	21

Power Interface

Table 12. Power Interface

Pad Name	Pad Number
3V3_EXT_LDO [a]	27
DC_5V_12V	32
GND	[1, 20, 76, 77, 78, 79]

a. Voltage reference only; do not use to power external devices

Electrical Specifications

Absolute Maximum Rating

Table 13. Absolute Maximum Ratings

PAD Number	Symbol	Description	Min	Typ	Max	Units
[32]	V_{IN}	Input voltage V_{IN} on the high-efficiency step-down converter	–	–	20	V
[2-19], [21-26], [28-31], [33-45], [48-75]	$V_{undershoot}$	Undershoot voltage for I/O	-0.3	–	–	V
[31]	PWR_RST	-	-0.3		6	V
[46, 47]	V_{MAX}	Based on 3.3V I/O signaling	–	–	60	V
	I_{MAX}	Continuous	–	–	305	mA
		Pulsed	–	–	800	mA
–	T_A	Storage Temperature	–40		85	°C

Recommended Operating Conditions

The recommended operation of the ARTIK 053/053s Module is based on the operating conditions listed in *Table 14*

Table 14. Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Units
Main Power Supply: PAD: 32	DC_5V_12V	4.75		13.5	V
Operating Temperature	T_c	-20	–	85	°C

DC Electrical Characteristics

Table 15. GPIO DC Electrical Characteristics

PAD Number	Symbol	Description	Condition		Min	Typ	Max	Units
[2-13, 18, 19], [21-26], [28-31], [33-45], [48-75]	V_{TOL}	Tolerant External Voltage	3.3 Power Off and On		–	–	3.6	V
	V_{IH}	High-Level Input Voltage						
		CMOS Interface	–		2.31	–	3.6	V
	V_{IL}	Low-Level Input Voltage						
		CMOS Interface	V_{DD} = 3.3V ± 10%		-0.3	–	0.7	V
	Δ_V	Hysteresis Voltage	–		0.15	–	–	V
	I_{IH}	High-Level Input Current						
		Input Buffer	V_{IN} = 3.3V	V_{DD} = 3.3V Power On	-3	–	3	µA
				V_{DD}= 3.3V Power Off & SNS=0	-5	–	5	
		Input Buffer Pull-Down	V_{IN} = 3.3V	V_{DD} = 3.3V ± 10%	13	40	90	
	I_{IL}	Low-Level Input Current						
		Input Buffer	V_{IN} = 0V	V_{DD} = 3.3V Power On and Off	-3	–	3	µA
		Input Buffer Pull-Down	V_{IN} = 0V	V_{DD} = 3.3V	-13	–	-90	
	V_{OH}	Output High Voltage	I_{OH} = 2.0mA, 4.0mA, 8.0mA and 12.0mA		2.64	–	3.3	V
	V_{OL}	Output Low Voltage	I_{OL} = -2.0mA, -4.0mA, -8.0mA and -12.0mA		0	–	0.66	
	V_{OZ}	Output Hi-Z Current	–		-5	–	5	µA
	C_{IN}	Input Capacitance	Any input and bi-directional buffers		–	–	5	pF
	C_{OUT}	Output Capacitance	Any output buffers		–	–	5	pF

Table 16. GPIO Signal Drive Strengths

State	Currents: Max conditions V_{DD} = 3.3V	Units
0	2	mA
1	4	mA
2	8 (default)	mA
3	12	mA