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SAMSUNG

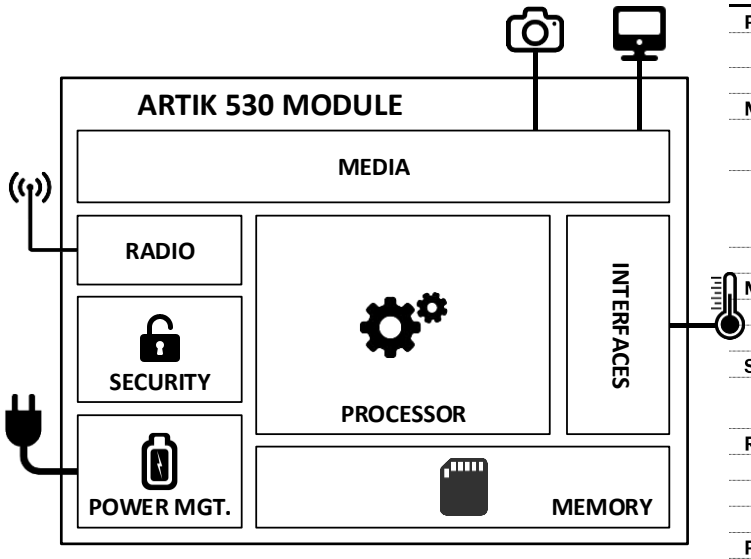
ARTIK™ Modules

5

530 Datasheet

ARTIK 530 Module Top View

The Samsung ARTIK™ 530 Module is a highly-integrated System-in-Module that combines a quad core ARM® Cortex®-A9 processor packaged DRAM and Flash memories; a Secure Element; and a wide range of wireless communication options such as 802.11a/b/g/n, Bluetooth® 4.2 (BLE+Classic), and 802.15.4 for ZigBee®/Thread; all into one 49x36mm footprint. The many standard digital control interfaces support external sensors and higher-performance peripherals to expand the module's capabilities. With the combination of 802.11, Bluetooth® and ZigBee or Thread, the ARTIK 530 Module is the perfect choice for home automation and home hub devices, while also supporting a rich UI/UX capability for camera and display requirements. The inclusion of a hardware-based Secure Element provides end-to-end security.



ARTIK 530 Module Block Diagram

Processor	
CPU	Quad core ARM® Cortex®-A9@1.2GHz
GPU	3D graphics accelerator
Media	
Camera I/F	4-lane MIPI CSI up to 5M (1920x1080@30fps)
Display	4-lane MIPI DSI and HDMI1.4a (1920x1080p@60fps) or LVDS (1280x720p@60fps)
Audio	Two I²S audio input/output
Memory	
DRAM	512MB DDR3
FLASH	4GB eMMC v4.5
Security	
Secure Element	Secure point to point authentication and data transfer
Radio	
WLAN	IEEE 802.11a/b/g/n, dual band SISO
Bluetooth®	4.2 (BLE+Classic)
802.15.4	ZigBee/Thread
Power Management	
PMIC	Provides all power of the ARTIK 530 Module using on board bucks and LDO's
Interfaces	
Ethernet	10/100/1000Base-T MAC (External PHY required)
Analog and Digital I/O	GPIO, UART, I²C, SPI, USB Host, USB OTG, HSIC, ADC, PWM, I²S, JTAG

ARTIK 530 Module Table of Contents

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VERSION HISTORY

Revision	Date	Description	Maturity
V1.0	January 20, 2017	ARTIK 530 datasheet.	Release
V1.01	February 07, 2017	Updated Module PAD's section. Updated look and feel.	Release Update

Block Diagram and Module Features

Figure 1 shows the functional block diagram of the ARTIK 530 Module. It consists of a quad-core ARM® Cortex®-A9 application processor with 512MB of DDR3 and 4GB eMMC, PMIC power management, Secure Element, 802.11/Bluetooth®, 802.15.4 and RF connectors.

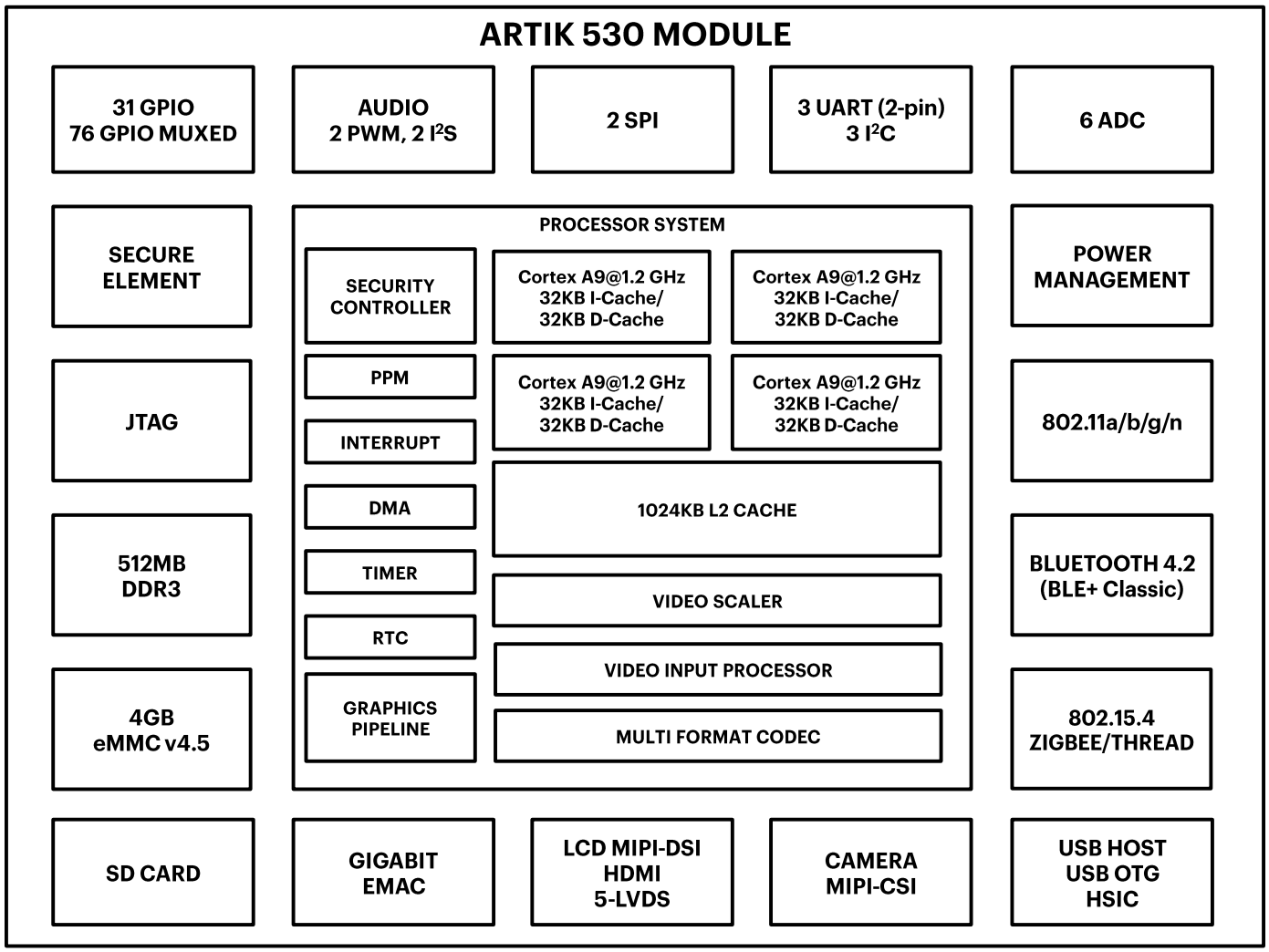

Figure 1. ARTIK 530 Module Functional Block Diagram

Warning : Do not apply power to the ARTIK 530 Module before connecting antennas or damage to the Module may result!

ARTIK 530 Module Features

The sub-sections that will follow describe the functions of the various blocks depicted in *Figure 1* that are present on the ARTIK 530 Module.

GPIO

The ARTIK 530 Module provides a GPIO system with up to 107 GPIOs (76 multiplexed, 31 dedicated) to allow for a wide variety of use cases to be supported. The key features of the GPIO system are:

- Programmable pull-up control
- Both edge detect and level detect functionality
- Support for programmable pull-up resistors
- Support for fast or normal slew operation
- Support for default Drive Strength or High Drive Strength
- Support for interrupt generation that can be triggered on:
  - Rising edge
  - Falling edge
  - High level detection
  - Low level detection
- The I/O data is clocked up to 50MHz

I^2S

The ARTIK 530 Module provides two 5-line Inter-IC Sound (I^2S) channel. I^2S is one of the most popular digital audio interfaces. The I^2S bus handles audio data and other signals, such as sub-coding and control. It is possible to transmit data between two I^2S buses. The key features of the I^2S sub-system are:

- Supports 1-port stereo (1 channel) I^2S-bus for audio with DMA based operation
- Supports serial data transfer of 16/24-bit per channel in Master and Slave mode
- Supports a variety of interface modes:
  - I^2S, Left justified, Right justified, DSP mode

PWM

The ARTIK 530 Module provides two pulse width modulation (PWM) modules. The key features of the PWM modules are:

- Two individual PWM channels with independent duty control and polarity
- Two 32-bit PWM timers, one per channel
- Support for static as well as dynamic setup
- Support for auto-reload and one shot pulse mode
- Dead zone generator
- Level interrupt generation

SPI

The ARTIK 530 Module provides two, Serial Peripheral Interfaces (SPI) that transfers serial data. SPI support includes 8-bit/16-bit shift registers to transmit and receive data. During an SPI transfer, data is simultaneously transmitted (shifted out serially) and received (shifted in serially). The SPI implementation adheres to the protocols described by Texas Instruments Synchronous Serial, National Semiconductor's Microwire and Motorola's Serial Peripheral Interface. The key features of the SPI sub-system are:

- Support for full-duplex
- 8-bit/16-bit shift register for Tx and Rx
- Complies with the SPI protocol described by Texas Instruments, National Semiconductor and Motorola
- Support for independent 16-bit wide transmit and receive FIFOs 8 locations deep
- Supports for master mode and slave mode
- Supports for receive-without-transmit operation
- Max operating frequency :
  - Master Mode : Support Tx up to 50MHz, Rx up to 20MHz

- Slave Mode : Support Tx up to 8MHz, Rx up to 8MHz

UART

The ARTIK 530 Module provides three 2-pin universal asynchronous receiver transmitters (UARTs). The key features of the UART sub-system are:

- Separate 32x8 Tx and 32x12 Rx FIFO memory buffers
- Support for DMA mode (UART0 : [AP_UART_RX0, AP_UART_TX0] only) and interrupt based mode of operation
- All independent channels support IrDA 1.0
- Support for modem control functions CTS, DCD, DSR, RTS, DTR and RI
- Each UART channel contains:
  - Programmable baud-rates
  - 1 or 2 stop bit insertion
  - 5-bit, 6-bit, 7-bit, or 8-bit data width
  - Parity checking

I^2C

The ARTIK 530 Module provides three generic I^2C blocks supporting both 100kb/s and 400kb/s speed modes.
The key features of the I^2C sub-system are:

- Supporting multi-master and slave mode
- 7-bit addressing mode only
- Supports serial, 8-bit oriented and bi-directional data transfer
- Supports up to 100 kb/s in the standard mode
- Supports up to 400 kb/s in the fast mode
- Supports master transmit, master receive, slave transmit, and slave receive operation
- Supports both interrupt and polling events

ADC

The ADC interface controls one 28nm low power CMOS 1.8V 12-bit ADC. The key features of the ADC sub-system are:

- Up to six channels of analog input can be selected
- Converts analog input into 12-bit binary code up to 1MSPS
- Power consumption 1.0mW when running 1MSPS
- Input frequency up to 100kHz

Power Management

The ARTIK 530 Module power requirements are managed using a power management integrated circuit (PMIC). This PMIC device has four fully-integrated fixed-frequency current-mode synchronous PWM step-down converters that can achieve peak efficiencies of up to 97%. In addition it provides seven low-noise LDOs with currents up to 350mA, one always-on LDO and an integrated backup battery charger that will provide all power requirements for the ARTIK 530 Module.

The four DC-DC regulators operate at a fixed high frequency of 2.25MHz, minimizing noise in sensitive applications and allowing the use of small form factor components. These four buck regulators supply up to 3A of output current and can fully satisfy the power and control requirements of the ARTIK 530 Module. Dynamic Voltage Scaling (DVS) of the various core voltages is supported using I^2C control.

For a detailed description see the section on *Power Supply Requirements*.

802.11

The ARTIK 530 Module has a fully-integrated WLAN block covering IEEE 802.11 a/b/g/n. The most important hardware features of the 802.11 module are:

- 802.11 a/b/g/n dual band SISO, 2.4GHz/5GHz compliant
  - 1T1R 2.4GHz/5GHz band

  - Support for 20 and 40MHz bandwidth (72.2/150Mbps PHY rate)
- Enhanced 802.11/Bluetooth® Coexistence control to improve transmission quality in different profiles

BLUETOOTH®

The ARTIK 530 Module has a fully-integrated Bluetooth® block 4.2 (BLE+Classic). The most important hardware features of the Bluetooth® module are:

- Bluetooth® 4.2 (BLE+Classic)
- Enhanced 802.11/Bluetooth® Coexistence control to improve transmission quality in different profiles

802.15.4

The ARTIK 530 Module carries fully-integrated 802.15.4 functionality. The most important hardware features are:

- Fully integrated 2.4 GHz, IEEE 802.15.4 compliant transceiver
- Complete system-on-chip using 32-bit ARM® Cortex®-M4 processor
- Flash and RAM memory and peripherals.
- Extremely low power consumption.
- Excellent RF performance.
- Single-voltage operation.
- Supported Protocols:
  - ZigBee
  - Thread

USB OTG

The ARTIK 530 Module provides one USB2.0 OTG interface supporting both device and host functionality. The key features of the USB2.0 OTG sub-system are:

- In compliance with the USB 2.0 on-the-go specification revision 1.3a and 2.0
- Operates in high speed (480Mbps) mode
- Operates in full speed (12Mbps) mode
- Operates in low speed (1.5Mbps, host only) mode
- Supports session request protocol (SRP) and host negotiation protocol (HNP)
- One control endpoint 0 for control transfer
- Supports up to 15 device-programmable endpoints:
  - Programmable endpoint type: Bulk, Isochronous, Interrupt
  - Programmable In/Out direction
- Supports 16 host channels

USB HOST

The ARTIK 530 Module provides one USB2.0 Host controller that is fully compliant with the USB 2.0 specifications, and the enhanced host controller Interface (EHCI) specification. The key features of the USB2.0 OTG sub-system are:

- Detecting the attachment and removal of USB devices
- Collecting status and activity statistics
- Controlling power supply to attached USB devices
- In compliance with the UTMI+ Level 3 revision 1.0
- Controlling the association to either the open host controller interface (OHCI) or the EHCI via a port router
- Root Hub functionality to support up/down stream port

HSIC

The ARTIK 530 Module provides one high speed inter chip (HSIC) version 1.0 module. The key features of the HSIC sub-system are:

- Support for ping and split transactions
- Up to 30MHz operation for a 16-bit interface
- Up to 60MHz operation for a 8-bit interface

- Support for HSIC version 1.0

MIPI CSI

The ARTIK 530 Module provides one 4-lane mobile industry processor interface (MIPI) interface that complies with the MIPI camera serial interface (CSI) standard specification V1.01r06 and D-PHY standard specification v1.0. The key features of the MIPI CSI sub-system are:

- Supports 1, 2, 3 or 4 data lanes
- Supported image formats are:
  - YUV420, YUV420 (Legacy), YUV420 (CSPS), 8-bit YUV422, 10-bit YUV422
  - User defined Byte based data packet
  - Compatible to PPI (Protocol to PHY interface)

MIPI DSI

The ARTIK 530 Module provides one 4-lane MIPI interface that complies with the MIPI DSI standard specification V1.01r11. The key features of the MIPI DSI sub-system are:

- Maximum resolution ranges up to 1920x1080
- Supports 1, 2, 3 or 4 data lanes
- Supports pixel format:
  - 16bpp, 18bpp packed, 18bpp loosely packed (3 byte), 24bpp
- Supported interfaces are:
    - Protocol-to-PHY Interface (PPI) up to 1.5Gbps, in MIPI D-PHY
    - RGB Interface for video image input from display controller
    - PMS control interface for PLL to configure byte clock frequency
    - Pre-scaler to generate escape clock from byte clock

HDMI

The ARTIK 530 Module provides one HDMI v1.4a interface. The key features of the HDMI sub-system are:

- Support for v1.4a spec
- Up to 1080p video resolution
- HDMI Link + HDMI PHY
- Support for the following video formats:
  - 480p@59.94/60Hz
  - 576p@50Hz
  - 720p@50/59.94/60Hz
  - 1080p@50/59.94/60Hz (No support for interlaced format)
- Support for 4:4:4 RGB
- Support for up to 8-bits per color

LVDS

The ARTIK 530 Module provides five low voltage differential signaling (LVDS) output channels with one clock channel. The key features of the LVDS channel system are:

- Output clock range 30-125MHz
- Support for 630 Mbps per channel
- Up to 393.75MB/s data transport
- Support for power down mode

GIGABIT EMAC

The ARTIK 530 Module provides one Gigabit EMAC interface. The most important features of the Ethernet MAC module are:

- Standard compliance
  - IEEE 802.3az-2010: energy efficient Ethernet (EEE)
  - RGMII v2.6

- MAC supports the following features:
  - 10/100/1000 Mbps data transfer rates with an RGMII interface to communicate with external Gigabit PHY
  - Full duplex operation
  - Half duplex operation
  - Flexible address filtering
  - Additional frame filtering

SD-CARD

The ARTIK 530 Module provides one shared SD-card/MMC interface. The Mobile Storage Host is an interface between the system and the SD-card. The key features of mobile storage host sub-system are:

- Support for Secure Digital I/O (SDIO – version 3.0)
- Support for Secure Digital Memory (SDMEM – version 3.0)
- Support for Consumer Electronics Advanced Transport Architecture (CE-ATA-version 1.1)
- Support 4-bit SDR mode up to 50MHz
- Supports PIO and DMA mode data transfer
- Supports ¼- bit data bus width

MMC

The ARTIK 530 Module provides one shared SD-card/MMC interface. The Mobile Storage Host is an interface between the system and MMC card. The key features of mobile storage host sub-system are:

- Support for Embedded Multimedia Cards (MMC – version 4.41)
- Support for Embedded Multimedia Cards (eMMC – version 4.5)
- Support 4-bit SDR mode up to 50MHz
- Supports PIO and DMA mode data transfer
- Supports ¼- bit data bus width

DDR

The ARTIK 530 Module has DDR memory. The key features of the DDR memory present on the ARTIK 530 Module are:

- One 32-bit DDR3 memory interface
- Two 256MB DDR3 16-bit memory chips, for a total of 512MB
- Up to 800MHz DDR3 speed with a maximum throughput of 6.4GB/s

JTAG

Our JTAG core that is part of the ARTIK 530 Module provides debug capabilities for the developer. The main features of the JTAG module are:

- Compliant with the IEEE 1149 standard
- Can only be used together with the ARTIK 530 Module.

SECURE ELEMENT

The ARTIK 530 Module has a dedicated Secure Element to assure end-to-end authentication and communication between nodes in an IoT setting. The Secure Element provides an ISO/IEC 7816 14443 compliant interface. The most important hardware features of the Secure Element are:

- Dedicated 16-bit SecuCalm CPU core
- Crypto co-processor
  - Modular exponential accelerator
  - RSA 2080 bits
  - ECC 512 bits
- Data security
  - Memory encryption for all memory
  - 256B read only and 256B non erasable flash area
  - Selective reset operation if abnormal voltages/frequencies are detected

- Embedded tamper-free memory
  - 32KB ROM
  - 264KB FLASH
  - (6+2.5)KB Static RAM including 2.5KB crypto memory
- Serial interfaces:
  - ISO 7816-3 compliant interface
  - Asynchronous half-duplex character receive/transmit serial interface

Quad Core Processor System

The processor system architecture that resides on the ARTIK 530 Module is a system-on-a-chip (SoC) based on a 32-bit RISC architecture. Designed using the 28nm low power process, the processor system architecture provides superior performance using a quad-core CPU. The key features of the ARTIK 530 Module are:

- Quad-core ARM® Cortex®-A9, 32-bit RISC architecture
- Maximum core speed 1.2GHz
- 32KB I-Cache per core
- 32KB D-Cache per core
- 1024KB L2-Cache shared between four cores
- Support for dynamic virtual-address mapping

PPM

The ARTIK 530 Module has one pulse period measurement (PPM) IP-block that can measure the duration of a high level or low level from a GPIO pin. The most important features of the PPM block are:

- One 16-bit counter tied to a clock that can vary between 843.75kHz and 13.50MHz

For more details on how to relate a PPM to a GPIO please refer to the ARTIK 530 Module software developer's guide.

Timer

The ARTIK 530 Module has four dedicated timer channels. The most important features of the Timer module are:

- Timer or watchdog timer modes
- Four dedicated Timer channels with watchdog timer
- Normal interval timer mode with interrupt request
- Reset on timer countdown
- Level-triggered interrupt mechanism

Interrupt

The ARTIK 530 Module has one interrupt module. The most important features of the interrupt module are:

- Vectored Interrupt Controller
- Support 64x channel interrupt sources
- For each interrupt source the following properties are available:
  - Fixed hardware interrupt priority level
  - Programmable interrupt priority level
  - Hardware interrupt priority level masking
  - IRQ and FIQ generation
  - Software interrupt generation
  - Test registers
  - Raw interrupt status
  - Interrupt request status

DMA

The ARTIK 530 Module has one scatter-gather DMA module. The most important features of the DMA module are:

- 16x channels of dedicated DMA

- 16x DMA request lines
- Various operating modes
  - Single DMA mode
  - Burst DMA mode
  - Memory to memory transfer
  - Memory to peripheral transfer
  - Peripheral to memory transfer
  - Peripheral to peripheral transfer
- Support for 8/16/32 bit wide transactions
- Big endian and little endian (default) support

RTC

The ARTIK 530 Module has one real time clock (RTC) module. The most important features of the RTC are:

- Four spread spectrum PLLs
- Two external crystals : one 24MHz crystal for PLL, one 32.768KHz crystal for RTC
- 32-bit RTC counter
- Support for alarm interrupt using RTC

Video Input Processor

The ARTIK 530 Module provides one video input processor (VIP). The key features of the VIP sub-system are:

- Support for external 8-bit and 16-bit MIPI-DSI
- Support for internal MIPI-CSI
- Support of images up to 8192x8192
- Support for clipping and scale-down
- Support for YUV420 memory format

Video Scaler

The ARTIK 530 Module provides one universal scaler. The key features of the scaler are:

- Support for different input formats
  - YUV420, YUV422, YUV444
- Flexible size, from 8x8 up to 1920x1080 with a granularity of 8
- Upscale ratio from 8x8 to 1920x1080
- Downscale ratio from 1920x1080 to 8x8
- Low pass filter available after upscale or before downscale
- Horizontal 5-tab filter with 64 sets of coefficients
- Vertical 3-tab filter with 32 sets of coefficients

Multi Format Codec

The ARTIK 530 Module provides one integrated Multi Format Codec (MFC) module. The key features of the MFC sub-system are:

- Decoder
  - H.264 : BP, MP, HP Level 4.2 up to 1920x1080, up to 50MBps
  - MPEG4 : Advanced Simple Profile (ASP) up to 1920x1080, up to 40Mbps
  - H.263 : Profile 3 up to 1920x1080, up to 20Mbps
  - MPEG 1,2 : Main Profile, High Level up to 1920x1080, up to 80MBps
- Encoder
  - H.264 : Baseline profile, Level 4.0 up to 1080p, up to 20Mbps
  - MPEG4 : Simple profile, Level 5.6 up to 1080p, up to 20Mbps
  - H.263 : Profile 3, Level 70 up to 1080p, up to 20Mbps

Graphics Pipeline

The ARTIK 530 Module provides one 2D and 3D graphics pipeline module. The key features of the graphics pipeline are:

- Two pixel processors
  - Tile oriented processing
  - Alpha blending
  - Texture support, non-power-of-2
  - Cube mapping
  - Fast dynamic branching
  - Trigonometric acceleration
  - Full floating point arithmetic
  - Line, quad, triangle and point sprites
  - Perspective correct texturing
  - Point sampling, bilinear and trilinear filtering
  - 8-bit stencil buffering
  - 4-level hierarchical Z and stencil operation
- Geometry processor
  - Programmable vertex shader
  - Flexible input and output formats
  - Autonomous operation tile list generation
  - Indexed and non-indexed geometry input
  - Primitive constructions with points, lines, triangles and quads
- Support for OpenGL ES 1.0 and 2.0

MODULE PADS

The ARTIK 530 Module utilizes 292 signal and ground BALLs providing all the relevant signaling. *Figure 2* shows how the BALLs are oriented and how signal coordinates are assigned to the PADs of the ARTIK 530 Module. *Table 2* - *Table 6* describe the relation between the BALL coordinates and the BALL signal names. These tables also provide detailed characteristics for each BALL signal name.

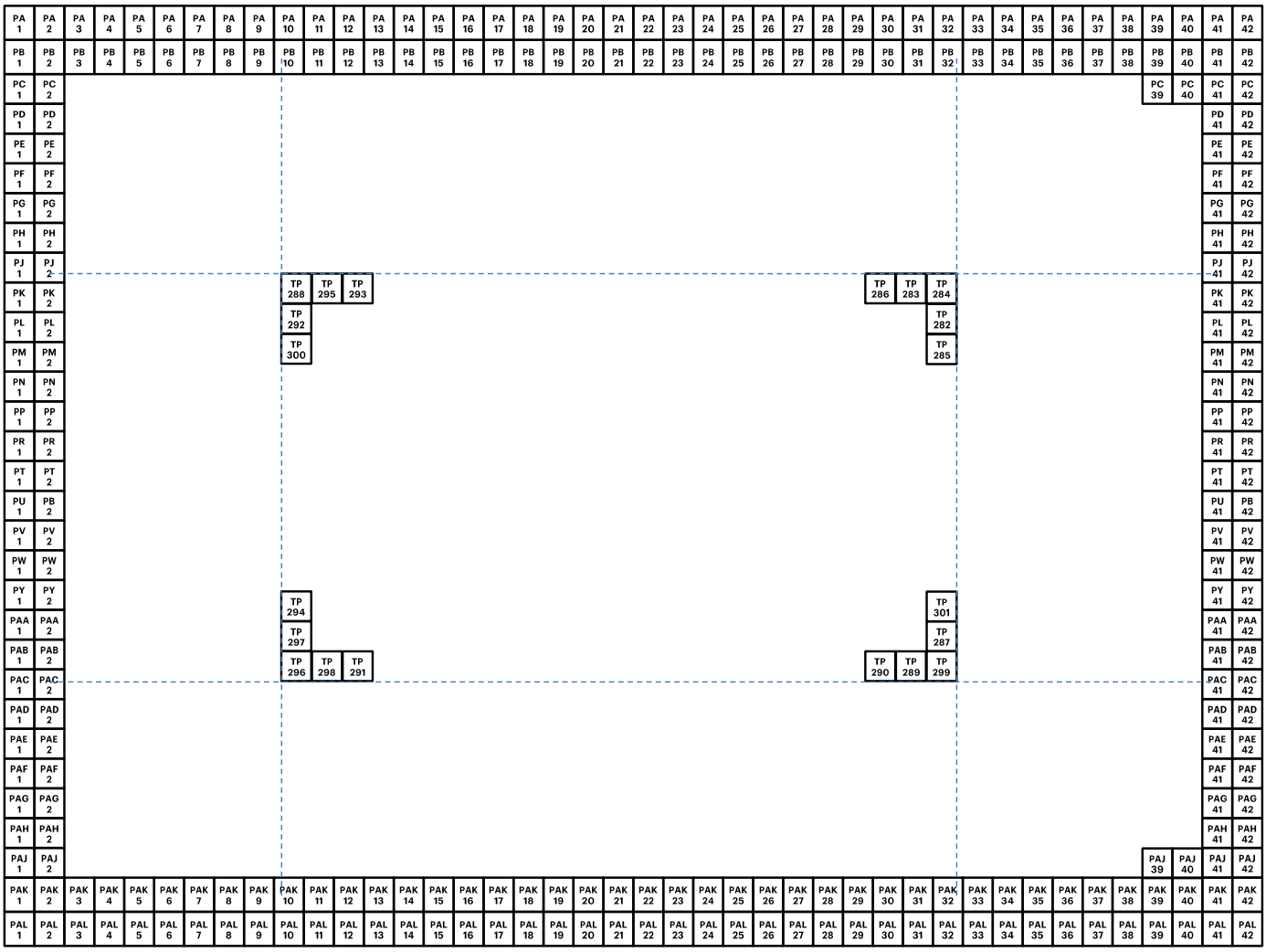

Figure 2. ARTIK 530 Module Top View BALL Organization

Ball Table Column Definitions

The meaning of the various columns used in *Table 2* - *Table 6* is explained in *Table 1*.

Table 1. Ball Table Column Definition

Column Name	Column Definition
Ball Loc	Identifier of the Ball on the ARTIK 530 Module
Ball Name	Default function of the ARTIK 530 Module
Power	Voltage level on the Ball
Default	Internal default function of the main SoC
I/O Type	S=Signal Ball
I/O	I=Input, O=Output, IO=Input/Output
PU/PD	PU=Pull-Up, PD=Pull-Down, N=No Pull-Up or Pull-Down
Group	Default pin group set to work with the Interposer Board. For more information see ARTIK 530 Module Hardware User Guide. Usually the function of the pin can be reprogrammed
Function	Explanation on the function of the ball

NORTH BALL ARRAY

Table 2. NORTH BALL ARRAY

Ball Loc	Ball Name	Power	Default	I/O Type	I/O	PU/PD	Group	Function
PA1	GMAC_TXEN	3V3	GMAC_TXEN	S	IO	N	GMAC	GMAC Transmit Enable
PA2	GMAC_TXD1	3V3	GMAC_TXD1	S	IO	N	GMAC	GMAC Transmit Data 1
PA3	GMAC_TXD3	3V3	GMAC_TXD3	S	IO	N	GMAC	GMAC Transmit Data 3
PA4	NO BALL	-	-	-	-	-	NO BALL	NA
PA5	GMAC_GTXCLK	3V3	GMAC_GTXCLK	S	IO	N	GMAC	GMAC Transmit Clock
PA6	GMAC_RXDV	3V3	GMAC_RXDV	S	IO	N	GMAC	GMAC Receive Enable
PA7	GMAC_RXD2	3V3	GMAC_RXD2	S	IO	N	GMAC	GMAC Receive Data 2
PA8	GMAC_RXD0	3V3	GMAC_RXD0	S	IO	N	GMAC	GMAC Receive Data 0
PA9	GND	0V0	GND	NA	0V0	-	GND	Ground
PA10	AP_MIPICSI_DNCLK	1V8	MIPICSI_DNCLK	S	IO	N	CSI	MIPI CSI Data Negative Clock
PA11	AP_MIPICSI_DN0	1V8	MIPICSI_DN0	S	IO	N	CSI	MIPI CSI Data Negative 0
PA12	AP_MIPICSI_DN1	1V8	MIPICSI_DN1	S	IO	N	CSI	MIPI CSI Data Negative 1
PA13	AP_MIPICSI_DN2	1V8	MIPICSI_DN2	S	IO	N	CSI	MIPI CSI Data Negative 2
PA14	AP_MIPICSI_DN3	1V8	MIPICSI_DN3	S	IO	N	CSI	MIPI CSI Data Negative 3
PA15	GND	0V0	GND	NA	0V0	-	GND	Ground
PA16	AP_MIPIDSI_DNCLK	1V8	MIPIDSI_DNCLK	S	IO	N	DSI	MIPI DSI Data Negative Clock
PA17	AP_MIPIDSI_DN0	1V8	MIPIDSI_DN0	S	IO	N	DSI	MIPI DSI Data Negative 0
PA18	AP_MIPIDSI_DN1	1V8	MIPIDSI_DN1	S	IO	N	DSI	MIPI DSI Data Negative 1
PA19	AP_MIPIDSI_DN2	1V8	MIPIDSI_DN2	S	IO	N	DSI	MIPI DSI Data Negative 2
PA20	AP_MIPIDSI_DN3	1V8	MIPIDSI_DN3	S	IO	N	DSI	MIPI DSI Data Negative 3
PA21	GND	0V0	GND	NA	0V0	-	GND	Ground
PA22	AP_LVDS_TN0	1V8	LVDS_TN0	S	IO	N	LVDS	LVDS Transmit Channel 0 Negative
PA23	AP_LVDS_TN1	1V8	LVDS_TN1	S	IO	N	LVDS	LVDS Transmit Channel 1 Negative
PA24	AP_LVDS_TN2	1V8	LVDS_TN2	S	IO	N	LVDS	LVDS Transmit Channel 2 Negative
PA25	AP_LVDS_TNCLK	1V8	LVDS_TNCLK	S	IO	N	LVDS	LVDS Transmit Negative Clock
PA26	AP_LVDS_TN3	1V8	LVDS_TN3	S	IO	N	LVDS	LVDS Transmit Channel 3 Negative
PA27	AP_LVDS_TN4	1V8	LVDS_TN4	S	IO	N	LVDS	LVDS Transmit Channel 4 Negative
PA28	GND	0V0	GND	NA	0V0	-	GND	Ground
PA29	AP_HDMI_CEC	3V3	SA3	S	IO	N	HDMI	HDMI Consumer Electronics Control
PA30	AP_HDMI_TX2N	1V8	HDMI_TXN2	S	O	N	HDMI	HDMI Transmit Channel 1 Negative
PA31	AP_HDMI_TX1N	1V8	HDMI_TXN1	S	O	N	HDMI	HDMI Transmit Channel 0 Negative
PA32	AP_HDMI_TX0N	1V8	HDMI_TXN0	S	O	N	HDMI	HDMI Transmit Channel 2 Negative
PA33	AP_HDMI_TXCN	1V8	HDMI_TXNCLK	S	O	N	HDMI	HDMI Transmit Negative Clock
PA34	GND	0V0	GND	NA	0V0	-	GND	Ground
PA35	AP_OTG_DM	3V3	USB2.0OTG_DM	S	IO	N	USB OTG	USB OTG Data Minus
PA36	AP_USBH_DM	3V3	USB2.0HOST_DM	S	IO	N	USB HOST	USB HOST Data Plus
PA37	AP_GPA13	3V3	DISD12	S	IO	N	GPIO	Generic GPIO
PA38	AP_HSIC_STROBE	1V2	USBHSIC_STROBE	S	IO	N	HSIC	HSIC Strobe
PA39	AP_GPA14	3V3	DISD13	S	IO	N	GPIO	Generic GPIO
PA40	AP_GPA9	3V3	DISD8	S	IO	N	GPIO	Generic GPIO
PA41	AP_GPA15	3V3	DISD14	S	IO	N	GPIO	Generic GPIO
PA42	AP_GPA12	3V3	DISD11	S	IO	N	GPIO	Generic GPIO
PB1	GND	0V0	GND	NA	0V0	-	GND	Ground
PB2	GMAC_TXD0	3V3	GMAC_TXD0	S	IO	N	GMAC	GMAC Transmit Data 0
PB3	GMAC_TXD2	3V3	GMAC_TXD2	S	IO	N	GMAC	GMAC Transmit Data 2

Ball Loc	Ball Name	Power	Default	I/O Type	I/O	PU/PD	Group	Function
PB4	GMAC_MDC	3V3	GMAC_MDC	S	IO	N	GMAC	GMAC MDC
PB5	GMAC_RXCLK	3V3	GMAC_RXCLK	S	IO	N	GMAC	GMAX Receive Clock
PB6	GMAC_RXD3	3V3	GMAC_RXD3	S	IO	N	GMAC	GMAC Receive Data 3
PB7	GMAC_RXD1	3V3	GMAC_RXD1	S	IO	N	GMAC	GMAC Receive Data 1
PB8	GMAC_MDIO	3V3	GMAC_MDIO	S	IO	N	GMAC	GMAC MDIO
PB9	GND	0V0	GND	NA	0V0	-	GND	Ground
PB10	AP_MIPICSI_DPCLK	1V8	MIPICSI_DPCLK	S	IO	N	CSI	MIPI CSI Data Positive Clock
PB11	AP_MIPICSI_DP0	1V8	MIPICSI_DP0	S	IO	N	CSI	MIPI CSI Data Positive 0
PB12	AP_MIPICSI_DP1	1V8	MIPICSI_DP1	S	IO	N	CSI	MIPI CSI Data Positive 1
PB13	AP_MIPICSI_DP2	1V8	MIPICSI_DP2	S	IO	N	CSI	MIPI CSI Data Positive 2
PB14	AP_MIPICSI_DP3	1V8	MIPICSI_DP3	S	IO	N	CSI	MIPI CSI Data Positive 3
PB15	GND	0V0	GND	NA	0V0	-	GND	Ground
PB16	AP_MIPIDSI_DPCLK	1V8	MIPIDSI_DPCLK	S	IO	N	DSI	MIPI DSI Data Positive Clock
PB17	AP_MIPIDSI_DP0	1V8	MIPIDSI_DP0	S	IO	N	DSI	MIPI DSI Data Positive 0
PB18	AP_MIPIDSI_DP1	1V8	MIPIDSI_DP1	S	IO	N	DSI	MIPI DSI Data Positive 1
PB19	AP_MIPIDSI_DP2	1V8	MIPIDSI_DP2	S	IO	N	DSI	MIPI DSI Data Positive 2
PB20	AP_MIPIDSI_DP3	1V8	MIPIDSI_DP3	S	IO	N	DSI	MIPI DSI Data Positive 3
PB21	GND	0V0	GND	NA	0V0	-	GND	Ground
PB22	AP_LVDS_TP0	1V8	LVDS_TP0	S	IO	N	LVDS	LVDS Transmit Channel 0 Positive
PB23	AP_LVDS_TP1	1V8	LVDS_TP1	S	IO	N	LVDS	LVDS Transmit Channel 1 Positive
PB24	AP_LVDS_TP2	1V8	LVDS_TP2	S	IO	N	LVDS	LVDS Transmit Channel 2 Positive
PB25	AP_LVDS_TPCLK	1V8	LVDS_TPCLK	S	IO	N	LVDS	LVDS Transmit Positive Clock
PB26	AP_LVDS_TP3	1V8	LVDS_TP3	S	IO	N	LVDS	LVDS Transmit Channel 3 Positive
PB27	AP_LVDS_TP4	1V8	LVDS_TP4	S	IO	N	LVDS	LVDS Transmit Channel 4 Positive
PB28	GND	0V0	GND	NA	0V0	-	GND	Ground
PB29	AP_HDMI_HPD	3V3	HDMI_HOT5V	S	I	N	HDMI	HDMI Hot 5V
PB30	AP_HDMI_TX2P	1V8	HDMI_TXP2	S	O	N	HDMI	HDMI Transmit Channel 1 Positive
PB31	AP_HDMI_TX1P	1V8	HDMI_TXP1	S	O	N	HDMI	HDMI Transmit Channel 0 Positive
PB32	AP_HDMI_TX0P	1V8	HDMI_TXP0	S	O	N	HDMI	HDMI Transmit Channel 2 Positive
PB33	AP_HDMI_TXCP	1V8	HDMI_TXPCLK	S	O	N	HDMI	HDMI Transmit Positive Clock
PB34	GND	0V0	GND	NA	0V0	-	GND	Ground
PB35	AP_OTG_DP	3V3	USB2.0OTG_DP	S	IO	N	USB OTG	USB OTG Data Plus
PB36	AP_USBH_DP	3V3	USB2.0HOST_DP	S	IO	N	USB HOST	USB HOST Data Minus
PB37	AP_OTG_ID	-	USB2.0OTG_ID	S	IO	N	USB HOST	USB HOST ID
PB38	AP_HSIC_DATA	1V2	USBHSIC_DATA	S	IO	N	HSIC	HSIC Data
PB39	AP_GPA4	3V3	DISD3	S	IO	N	GPIO	Generic GPIO
PB40	AP_GPA5	3V3	DISD4	S	IO	N	GPIO	Generic GPIO
PB41	AP_GPA16	3V3	DISD15	S	IO	N	GPIO	Generic GPIO
PB42	AP_GPA11	3V3	DISD10	S	IO	N	GPIO	Generic GPIO

SOUTH BALL ARRAY

Table 3. SOUTH BALL ARRAY

Ball Loc	Ball Name	Power	Default	I/O Type	I/O	PU/PD	Group	Function
PAK1	AP_I2S0_DOUT	3V3	I2SDOUT0	S	IO	N	I2S0	I2S 0 Data Out
PAK2	AP_I2S0_BCLK	3V3	I2SBCLK0	S	IO	N	I2S0	I2S 0 Bit Clock
PAK3	AP_GPC11_SPI2_MISO	3V3	SA11	S	IO	N	SPI2	SPI 2 Receive Data
PAK4	AP_GPC9_SPI2_CLK	3V3	SA9	S	IO	N	SPI2	SPI 2 Clock
PAK5	AP_SPI0_MISO	3V3	SPIRXD0	S	IO	N	SPI0	SPI 0 Receive Data
PAK6	AP_SPI0_CLK	3V3	SPICLK0	S	IO	N	SPI0	SPI 0 Clock
PAK7	AP_GPC14_PWM2	3V3	SA14	S	IO	N	PWM	PWM 2
PAK8	AP_GPD6_SCL2	3V3	SCL2	S	IO	N	I2C	I2C SCL
PAK9	AP_GPD4_SCL1	3V3	SCL1	S	IO	N	I2C	I2C SCL 1
PAK10	AP_GPD2_SCL0	3V3	SCL0	S	IO	N	I2C	I2C SCL 0
PAK11	AP_GPA23_HDMI_I2C_SCL	3V3	DISD22	S	IO	N	I2C	HDMI I2C SCL
PAK12	ZB_DEBUG_TDO_SWO	3V3	-	-	-	-	802.15.4	802.15.4 JTAG TMS
PAK13	ZB_PTI_DATA_FRC_DOUT	3V3	-	-	-	-	802.15.4	802.15.4 JTAG TCK
PAK14	ZB_DEBUG_TCK_SWCLK	3V3	-	-	-	-	802.15.4	802.15.4 Control
PAK15	COMBO_ZIG_UART_TXD	3V3	-	-	-	-	802.15.4	802.15.4 Control
PAK16	GND	0V0	GND	NA	0V0	-	GND	Ground
PAK17	VCC3P3_SYS	3V3	-	NA	3V3	-	POWER	0.9-3.5V, 300mA
PAK18	VCC3P3_SYS	3V3	-	NA	3V3	-	POWER	0.9-3.5V, 300mA
PAK19	AP_NBATTF	3V3	AP_nBATTF	-	NA	-	MISC	Battery
PAK20	AP_GPE2	3V3	VID0_6	S	IO	N	MISC	Miscellaneous
PAK21	AP_GPE1	3V3	VID0_5	S	IO	N	MISC	Miscellaneous
PAK22	AP_UART_TX3	3V3	UARTTXD3	S	IO	N	UART	UART Transmit Data 3
PAK23	AP_UART_TX4	3V3	SD13	S	IO	N	UART	UART Transmit Data 4
PAK24	AP_UART_TX0	3V3	UARTTXD0	S	IO	N	UART	UART Transmit Data 5
PAK25	AP_GPB0_VID1_1_I2SLRCK1	3V3	VID1_1	S	IO	N	I2S1	I2S 1 Left Right Clock
PAK26	AP_GPA28_I2SMCLK1	3V3	VICLK1	S	IO	N	I2S1	I2S 1 Master Clock
PAK27	AP_GPA30_VID1_0_I2SBCLK1	3V3	VID1_0	S	IO	N	I2S1	I2S 1 Bit Clock
PAK28	AP_SD0_CMD	3V3	SDCMD0	S	IO	N	SD/MMC	SD Command
PAK29	AP_SD0_D1	3V3	SDDAT0_1	S	IO	N	SD/MMC	SD Data 1
PAK30	AP_SD0_CLK	3V3	SDCLK0	S	IO	N	SD/MMC	SD Clock
PAK31	NC	-	-	-	-	-	NC	Not Connected
PAK32	AP_GPB13_SD0_BOOT	3V3	SD0	S	IO	N	BOOTING	Select Booting Scenario
PAK33	AP_GPC17	3V3	SA17	S	IO	N	GPIO	Generic GPIO
PAK34	AP_GPC0	3V3	SA0	S	IO	N	GPIO	Generic GPIO
PAK35	AP_GPC26	3V3	RDNWR	S	IO	PU	GPIO	Generic GPIO
PAK36	AP_GPB8	3V3	VID1_5	S	IO	N	GPIO	Generic GPIO
PAK37	AP_GPB14	3V3	RNB0	S	IO	N	MISC	Miscellaneous
PAK38	AP_GPA20	3V3	DISD19	S	IO	N	GPIO	Generic GPIO
PAK39	AP_GPA18	3V3	DISD17	S	IO	N	GPIO	Generic GPIO
PAK40	AP_GPA21	3V3	DISD20	S	IO	N	GPIO	Generic GPIO
PAK41	AP_GPA10	3V3	DISD9	S	IO	N	GPIO	Generic GPIO
PAK42	AP_GPA6	3V3	DISD5	S	IO	N	GPIO	Generic GPIO
PAL1	AP_I2S0_DIN	3V3	I2SDIN0	S	IO	N	I2S0	I2S 0 Data In
PAL2	AP_I2S0_MCLK	3V3	I2SMCLK0	S	IO	N	I2S0	I2S 0 Master Clock
PAL3	AP_GPC12_SPI2_MOSI	3V3	SA12	S	IO	N	SPI2	SPI 2 Transmit Data
PAL4	AP_GPC10_SPI2_CS	3V3	SA10	S	IO	PU	SPI2	SPI 2 Frame
PAL5	AP_SPI0_MOSI	3V3	SPITXD0	S	IO	N	SPI0	SPI 0 Transmit Data

Ball Loc	Ball Name	Power	Default	I/O Type	I/O	PU/PD	Group	Function
PAL6	AP_SPI0_CS	3V3	SPIFRM0	S	IO	N	SPI0	SPI 0 Frame
PAL7	AP_GPD1_PWM0	3V3	PWM0	S	IO	N	PWM	PWM 0
PAL8	AP_GPD7_SDA2	3V3	SDA2	S	IO	N	I2C	I2C SDA
PAL9	AP_GPD5_SDA1	3V3	SDA1	S	IO	N	I2C	I2C SDA 1
PAL10	AP_GPD3_SDA0	3V3	SDA0	S	IO	N	I2C	I2C SDA 0
PAL11	AP_GPA24_HDMI_I2C_SDA	3V3	DISD23	S	IO	N	I2C	HDMI I2C SDA
PAL12	ZB_DEBUG_TMS_SWDIO	3V3	-	-	-	-	802.15.4	802.15.4 JTAG TDI
PAL13	ZB_PTI_SYNC_FRC_DFRAME	3V3	-	-	-	-	802.15.4	802.15.4 JTAG TDO
PAL14	PAD_ZB_RSTN	3V3	-	-	-	-	802.15.4	802.15.4 Reset
PAL15	COMBO_ZIG_UART_RXD	3V3	NSCS1	S	IO	PU	802.15.4	802.15.4 Control
PAL16	GND	0V0	GND	NA	0V0	-	GND	Ground
PAL17	VCC3P3_SYS	3V3	-	NA	3V3	-	POWER	0.9-3.5V, 300mA
PAL18	VCC3P3_SYS	3V3	-	NA	3V3	-	POWER	0.9-3.5V, 300mA
PAL19	AP_VDDPWRON	3V3	VDDPWRON	S	O	N	MISC	VDD Power On
PAL20	AP_GPE3	3V3	VID0_7	S	IO	N	MISC	Miscellaneous
PAL21	AP_GPE0	3V3	VID0_4	S	IO	N	MISC	Miscellaneous
PAL22	AP_UART_RX3	3V3	UARTRXD3	S	IO	N	UART	UART Receive Data 3
PAL23	AP_UART_RX4	3V3	SD12	S	IO	N	UART	UART Receive Data 4
PAL24	AP_UART_RX0	3V3	UARTRXD0	S	IO	N	UART	UART Receive Data 5
PAL25	AP_GPD31	3V3	VID0_3	S	IO	N	MISC	Miscellaneous
PAL26	AP_GPB9_I2SDIN1	3V3	VID1_6	S	IO	N	I2S1	I2S 1 Data In
PAL27	AP_GPB6_VID1_4_I2SDOUT1	3V3	VID1_4	S	IO	N	I2S1	I2S 1 Data Out
PAL28	AP_SD0_D3	3V3	SDDAT0_3	S	IO	N	SD/MMC	SD Data 3
PAL29	AP_SD0_D2	3V3	SDDAT0_2	S	IO	N	SD/MMC	SD Data 2
PAL30	AP_SD0_D0	3V3	SDDAT0_0	S	IO	N	SD/MMC	SD Data 0
PAL31	AP_GPB4_VID1_3_BOOT	3V3	VID1_3	S	IO	N	BOOTING	Select Booting Scenario
PAL32	AP_GPB15_SD1_BOOT	3V3	SD1	S	IO	N	BOOTING	Select Booting Scenario
PAL33	AP_GPD8	3V3	PPM	S	IO	N	GPIO	Generic GPIO
PAL34	AP_GPE30	3V3	NSOE	S	IO	PU	GPIO	Generic GPIO
PAL35	AP_GPC27	3V3	NSDQM	S	IO	PU	GPIO	Generic GPIO
PAL36	AP_GPB22	3V3	SD6	S	IO	N	GPIO	Generic GPIO
PAL37	AP_GPB16	3V3	NNFOE0	S	IO	N	MISC	Miscellaneous
PAL38	AP_GPB23	3V3	SD7	S	IO	N	GPIO	Generic GPIO
PAL39	AP_GPA22	3V3	DISD21	S	IO	N	GPIO	Generic GPIO
PAL40	AP_GPA19	3V3	DISD18	S	IO	N	GPIO	Generic GPIO
PAL41	AP_GPA17	3V3	DISD16	S	IO	N	GPIO	Generic GPIO
PAL42	AP_GPA3	3V3	DISD2	S	IO	N	GPIO	Generic GPIO

EAST BALL ARRAY

Table 4. EAST BALL ARRAY

Ball Loc	Ball Name	Power	Default	I/O Type	I/O	PU/PD	Group	Function
PC1	GND	0V0	GND	NA	0V0	-	GND	Ground
PC2	NO BALL	-	-	-	-	-	NO BALL	NA
PD1	GND	0V0	GND	NA	0V0	-	GND	Ground
PD2	NO BALL	-	-	-	-	-	NO BALL	NA
PE1	GND	0V0	GND	NA	0V0	-	GND	Ground
PE2	GND	0V0	GND	NA	0V0	-	GND	Ground
PF1	GND	0V0	GND	NA	0V0	-	GND	Ground
PF2	GND	0V0	GND	NA	0V0	-	GND	Ground
PG1	GND	0V0	GND	NA	0V0	-	GND	Ground
PG2	NO BALL	-	-	-	-	-	NO BALL	NA
PH1	GND	0V0	GND	NA	0V0	-	GND	Ground
PH2	NO BALL	-	-	-	-	-	NO BALL	NA
PJ1	GND	0V0	GND	NA	0V0	-	GND	Ground
PJ2	GND	0V0	GND	NA	0V0	-	GND	Ground
PK1	GND	0V0	GND	NA	0V0	-	GND	Ground
PK2	GND	0V0	GND	NA	0V0	-	GND	Ground
PL1	GND	0V0	GND	NA	0V0	-	GND	Ground
PL2	GND	0V0	GND	NA	0V0	-	GND	Ground
PM1	GND	0V0	GND	NA	0V0	-	GND	Ground
PM2	GND	0V0	GND	NA	0V0	-	GND	Ground
PN1	GND	0V0	GND	NA	0V0	-	GND	Ground
PN2	GND	0V0	GND	NA	0V0	-	GND	Ground
PP1	GND	0V0	GND	NA	0V0	-	GND	Ground
PP2	NO BALL	-	-	-	-	-	NO BALL	NA
PR1	GND	0V0	GND	NA	0V0	-	GND	Ground
PR2	GND	0V0	GND	NA	0V0	-	GND	Ground
PT1	GND	0V0	GND	NA	0V0	-	GND	Ground
PT2	GND	0V0	GND	NA	0V0	-	GND	Ground
PU1	GND	0V0	GND	NA	0V0	-	GND	Ground
PU2	NO BALL	-	-	-	-	-	NO BALL	NA
PV1	GND	0V0	GND	NA	0V0	-	GND	Ground
PV2	NO BALL	-	-	-	-	-	NO BALL	NA
PW1	AP_ADC4	1V8	ADC4	S	IO	N	ADC	ADC Channel 4
PW2	AP_ADC5	1V8	ADC5	S	IO	N	ADC	ADC Channel 5
PY1	AP_ADC0	1V8	ADC0	S	IO	N	ADC	ADC Channel 0
PY2	AP_ADC1	1V8	ADC1	S	IO	N	ADC	ADC Channel 1
PAA1	AP_ADC2	1V8	ADC2	S	IO	N	ADC	ADC Channel 2
PAA2	AP_ADC3	1V8	ADC3	S	IO	N	ADC	ADC Channel 3
PAB1	GND	0V0	GND	NA	0V0	-	GND	Ground
PAB2	GND	0V0	GND	NA	0V0	-	GND	Ground
PAC1	AP_TCK	3V3	TCLK	S	IO	PD	JTAG	JTAG TCK
PAC2	AP_TMS	3V3	TMS	S	IO	PU	JTAG	JTAG TMS
PAD1	AP_TDO	3V3	TDO	S	IO	N	JTAG	JTAG TDO
PAD2	AP_TDI	3V3	TDI	S	IO	PU	JTAG	JTAG TDI
PAE1	AP_NTRST	3V3	NTRST	S	IO	PU	JTAG	JTAG NTRST
PAE2	AP_AGP2_RTC_INT_N	3V3	ALIVEGPIO2	S	IO	N	KEY/ALIVE	Left Key part of AliveGPIO
PAF1	AP_PWRKEY	3V3	ALIVEGPIO0	S	IO	N	KEY/ALIVE	Power Key part of AliveGPIO
PAF2	AP_AGP1_HOMEKEY	3V3	ALIVEGPIO1	S	IO	N	KEY/ALIVE	Home Key part of AliveGPIO

Ball Loc	Ball Name	Power	Default	I/O Type	I/O	PU/PD	Group	Function
PAG1	AP_NRESET	3V3	NRESET	S	I	PU	KEY	Reset
PAG2	AP_GPA25_BACKKEY	3V3	DISVSYNC	S	IO	N	KEY	Back Key
PAH1	AP_GPA26_VOLUP	3V3	DISHSYNC	S	IO	N	KEY	Volume Up
PAH2	AP_GPA0_MENUKEY	3V3	DISCLK	S	IO	N	KEY	Menu Key
PAJ1	AP_I2S0_LRCLK	3V3	I2SLRCLK0	S	IO	N	I2S0	I2S 0 Left Right Clock
PAJ2	AP_GPA27_VOLDOWN	3V3	DISDE	S	IO	N	KEY	Volume Down

WEST BALL ARRAY

Table 5. RIGHT BALL ARRAY

Ball Loc	Ball Name	Power	Default	I/O Type	I/O	PU/PD	Group	Function
PC39	GND	0V0	GND	NA	0V0	-	GND	Ground
PC40	GND	0V0	GND	NA	0V0	-	GND	Ground
PC41	GND	0V0	GND	NA	0V0	-	GND	Ground
PC42	GND	0V0	GND	NA	0V0	-	GND	Ground
PD41	VCC5P0_OTGVBUS	-	-	NA	5V0	-	POWER	USB2.0 OTG BUS Power
PD42	VCC5P0_OTGVBUS	-	-	NA	5V0	-	POWER	USB2.0 OTG BUS Power
PE41	NC	-	-	-	-	-	NC	-
PE42	NC	-	-	-	-	-	NC	-
PF41	NC	-	-	-	-	-	NC	-
PF42	GND	0V0	GND	NA	0V0	-	GND	Ground
PG41	GND	0V0	GND	NA	0V0	-	GND	Ground
PG42	GND	0V0	GND	NA	0V0	-	GND	Ground
PH41	NC	-	-	-		-	NC	-
PH42	NC	-	-	-		-	NC	-
PJ41	NC	-	-	-	-	-	NC	-
PJ42	GND	0V0	-	-	0V0	-	GND	Ground
PK41	GND	0V0	GND	-	0V0	-	GND	Ground
PK42	GND	0V0	GND	-	0V0	-	GND	Ground
PL41	GND	0V0	GND	NA	0V0	-	GND	Ground
PL42	GND	0V0	GND	NA	0V0	-	GND	Ground
PM41	GND	0V0	GND	NA	0V0	-	GND	Ground
PM42	GND	0V0	GND	NA	0V0	-	GND	Ground
PN41	GND	0V0	GND	NA	0V0	-	GND	Ground
PN42	GND	0V0	GND	NA	0V0	-	GND	Ground
PP41	MICOM_INT	3V3	SD14	S	IO	N	MISC	Micom Interrupt
PP42	GND	0V0	GND	NA	0V0	-	GND	Ground
PR41	NC	-	-	-	-	-	NC	-
PR42	NC	-	-	-	-	-	NC	-
PT41	GND	0V0	GND	NA	0V0	-	GND	Ground
PT42	GND	0V0	GND	NA	0V0	-	GND	Ground
PU41	GND	0V0	GND	NA	0V0	-	GND	Ground
PU42	GND	0V0	GND	NA	0V0	-	GND	Ground
PV41	VBAT_MAIN	VBAT	-	NA		-	POWER	Main Power Supply for Module
PV42	VBAT_MAIN	VBAT	-	NA		-	POWER	Main Power Supply for Module
PW41	VBAT_MAIN	VBAT	-	NA		-	POWER	Main Power Supply for Module
PW42	VBAT_MAIN	VBAT	-	NA		-	POWER	Main Power Supply for Module
PY41	VBAT_MAIN	VBAT	-	NA		-	POWER	Main Power Supply for Module
PY42	VBAT_MAIN	VBAT	-	NA		-	POWER	Main Power Supply for Module
PAA41	VBAT_MAIN	VBAT	-	NA		-	POWER	Main Power Supply for Module
PAA42	VBAT_MAIN	VBAT	-	NA		-	POWER	Main Power Supply for Module
PAB41	VBAT_MAIN	VBAT	-	NA		-	POWER	Main Power Supply for Module
PAB42	VBAT_MAIN	VBAT	-	NA		-	POWER	Main Power Supply for Module
PAC41	GND	0V0	GND	NA	0V0	-	GND	Ground
PAC42	GND	0V0	GND	NA	0V0	-	GND	Ground
PAD41	NC	-	-	-	-	-	NC	-
PAD42	NC	-	-	-	-	-	NC	-