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Samsung
ARTIK™

10

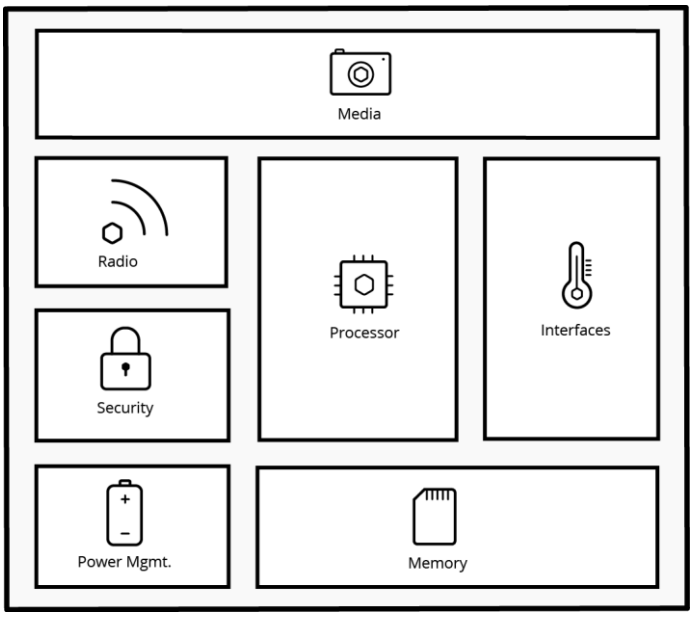
1020 Data Sheet

ARTIK 1020 Module Front View

Samsung's ARTIK™ 1020 Module is the world's highest performance Internet-of-Things (IoT) module. It is based on an octa-core architecture, containing quad ARM® Cortex®-A15 and ARM® quad Cortex®-A7 cores, DRAM and flash memory, camera and display interfaces, a full complement of digital I/O and analog inputs, and world class connectivity with IEEE802.11a/b/g/n/ac, Bluetooth® 4.1 + LE and a ZigBee® radio inside a package that is just 29x39x1.3mm.

The scalable processing power of the ARTIK 1020 Module makes it ideally suited for video and image processing tasks like autonomous vehicle navigation, intensive 3D graphics or large immersive displays.

Alternatively, the small size of the ARTIK 1020 Module enables servicing application domains with a high local computation requirement, like model-based robotic control, virtual reality or image processing. The hardware based Secure Element works with the ARM® TrustZone® and Trustonic's Trusted Execution Environment (TEE) to provide "bank level" security end-to-end.



ARTIK 1020 Module Block Diagram

Processor	
CPU	Quad core ARM® Cortex® A15@1.5GHz, Quad core Cortex® A7@1.3GHz
GPU	Mali™-T628 MP6 core
Media	
Camera I/F	1x 2-Lane MIPI CSI up to 3MP@30fps 1x 4-lane MIPI CSI up to 16MP@30fps (Supports YUV and MJPEG)
Display	4-lane MIPI DSI up to FHD 1920x1200@24bpp simultaneous HDMI 1920x1080@60fps
Audio	1x channel PCM and 2-channel I²S audio interface, supporting 5.1 channel audio
Memory	
DRAM	2GB LPDDR3
FLASH	16GB eMMC
Security	
Secure Element	Secure point to point authentication and data transfer
Trusted Execution Environment	Trustonic TEE (NDA required)
Radio	
WLAN	IEEE802.11a/b/g/n/ac
Bluetooth	4.1 + LE
IEEE802.15.4	ZigBee
Power Management	
PMIC	Provides all power of the ARTIK 1020 module using on board bucks and LDOs
Interfaces	
Analog and Digital I/O	GPIO, Analog Input, UART, I²C, I²S, SPI, USB 2.0, USB 3.0, SDIO, JTAG

Table of Contents

List of Figures

List of Tables

VERSION HISTORY

Revision	Date	Description	Maturity
1.10	October 19, 2016	ARTIK 1020 Module Data Sheet	Release

ARTIK 1020 Module Block Diagram

Figure 1 shows the functional block diagram of the ARTIK 1020 Module. It consists of a quad-core ARM® Cortex®-A15 with a quad-core A7 application processor with 2GB SDRAM and 16GB eMMC Flash, PMIC, Secure Element, Wi-Fi/BT chipset, ZigBee chipset, RF connectors and socket-type connectors.

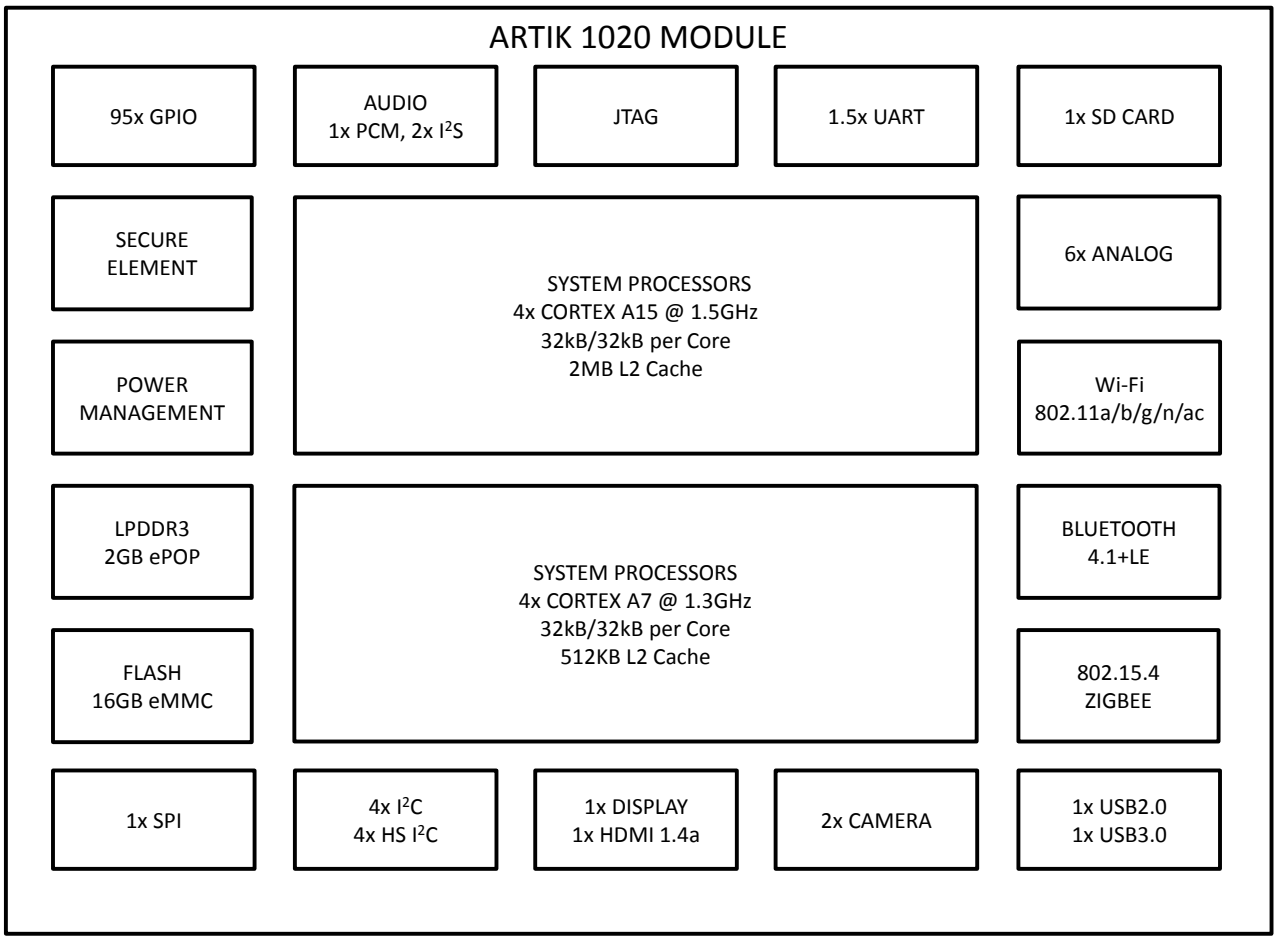


Figure 1. ARTIK 1020 Module Functional Block Diagram

The top side is populated with the ARM® application processor, SE, ZigBee, Wi-Fi/BT combo chipset and RF connectors for Wi-Fi/BT and ZigBee antennas. The bottom side is populated with the PMIC, Memory chipset and Secure Element, two main connectors for function connection to main set and one debug connector for debug interface connection.

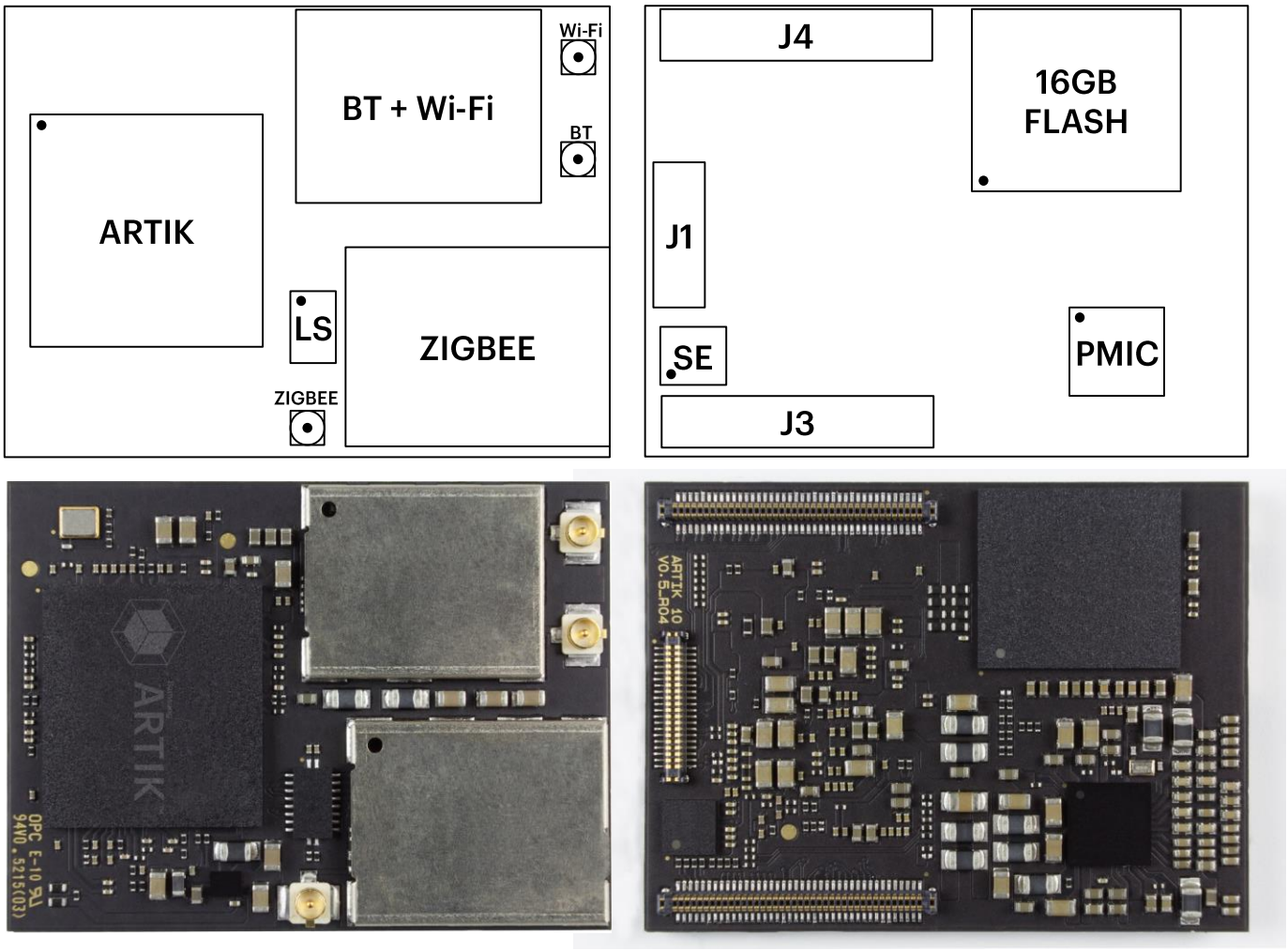


Figure 2. ARTIK 1020 Module – Top View / Bottom View

ARTIK 1020 Module Flash

The ARTIK 1020 Module carries an embedded 16GB Multi Media Card system that is version 5.0 compatible. The most important hardware features of the flash system are:

- Support for eMMC 5.0.
- Backward compatible with older eMMC specifications
- Support for variable databus width 1, 4 and 8 bits
- MMC I/F clock frequency 0-200MHz
- MMC I/F boot frequency 0-52MHz

For more information on KLMAG2GEAC-B002 contact a sales representative from Samsung Semiconductor, Inc.

ARTIK 1020 Module ZigBee

The ARTIK 1020 Module carries a fully integrated ZigBee unit called the Ember® EM3587. It integrates a 2.4 GHz, IEEE 802.15.4-2003-compliant transceiver, 32-bit ARM Cortex-M3 microprocessor, flash and RAM memory, and peripherals. The most important hardware features of the ZigBee module are:

- Complete system on chip using 32-bit ARM Cortex-M3 processor
- Low power consumption:
  - RX current typical 27mA
  - TX current typical 31mA
  - Deep sleep current ≤ 1.25µA
- RF performance:
  - Normal mode link budget up to 110dB
  - RX sensitivity up to 102dBm
- Robust Wi-Fi and Bluetooth coexistence
- Single voltage operation

For more information on EM3587 contact a sales representative from Silicon Laboratories, Inc.

ARTIK 1020 Module ZigBee Front End

The ARTIK 1020 Module carries a fully integrated RF Front-End Module (FEM) designed specifically for ZigBee Smart Energy IoT environments. The device provides integrated and fully matched input baluns, an integrated inter-stage matching and harmonic filter, and digital controls compatible with 1.6 to 3.6V CMOS levels. The RF blocks of the SE2432L support a wide range supply voltage tailored toward battery operated environments. The most important hardware features of the ZigBee front-end are:

- Integrated Power Amplifier up to 24dBm
- Integrated Low Noise Amplifier with programmable bypass
- Integrated antenna switching, with transmit and receive diversity function
- Low NF 2dB typical
- Differential transmit/receive interface with integrated baluns
- Fast switch on/off time ≤ 800ns
- Sleep mode current ≤ 0.05µA

For more information on SE2432L contact a sales representative from Skyworks Solutions, Inc.

ARTIK 1020 Module PMIC

The ARTIK 1020 Module has a fully integrated PMIC containing 10 bucks and 38 LDO's. This unit provides all power requirements for the ARTIK 1020 Module in one compact form factor. The 38 LDO regulators do have 31 PMOS LDOs
and 7NMOS LDOs. LDO28 is available on the debug connector.

For more information on S2MPS11B02 contact a sales representative from Samsung Semiconductor, Inc.

ARTIK 1020 Module Wi-Fi/Bluetooth

The ARTIK 1020 Module has a fully integrated MIMO combo BCM4354 for IEEE 802.11 a/b/g/n/ac wireless LAN with Bluetooth 4.0+LE and FM. The most important hardware features of the Wireless LAN Bluetooth combo module are:

- WLAN 802.11ac compliant:
  - Single stream spatial multiplexing up to 433Mbps
  - Support for 20, 40 and 80 MHz channels with optional SGI (256 QAM modulation)
- WLAN 802.11 a/b/g/n/ac compliant
- Bluetooth 4.0+LE
- 2G and 5G MIMO support
- FM Receiver 65MHz-108MHz bands

For more information on BCM4354 contact a sales representative from Broadcom Ltd.

ARTIK 1020 Module Secure Element

The ARTIK 1020 Module has a dedicated secure element to assure end to end authentication and communication between nodes in an IoT setting. The most important hardware features of the secure element are:

- Dedicated secure CPU SC300
- Crypto Accelerator
  - Hardware based AES/DES/3DES
  - TORNADO-E
  - 5KB crypto RAM
- Crypto co-processor
  - Modular exponential accelerator
  - RSA 4128bits/ECC 544 bits
- Data security
  - Abnormal condition detectors for: reset, interrupt, voltage, temperature, laser exposure, shield removal
  - Random Wait Generator, Random Current Generator
  - Secure optimized layout
  - Dynamic bus encryption
- Embedded tamper free memory
  - 1.5MB flash (program and data)
  - 32KB MASK ROM
  - 48KB Static RAM
  - 5KB Crypto RAM
  - Memory Protection Unit with 4GB addressable space
  - Secure flash write operation with fast page (0.5ms) and sector erase (4ms)
  - 500K erase/write cycles/s
- Serial interfaces:
  - I^2C/SPI/UART (ISO 7816)

- A guaranteed 25 years data retention at room temperature

For more information on S3FV5RP contact a sales representative from Samsung Semiconductor, Inc.

ARTIK 1020 Module Secure JTAG

Our secure JTAG core that is part of the ARTIK 1020 Module provides debug capabilities for the developer. The secure JTAG core authenticates the legal user and in addition it provides an access level that the legal user can operate under. The main features of the secure JTAG core are:

- Dedicated authentication process through password
- Dedicated Hash engine (SHA-1) with hash sequencer
- Two access levels “access-on” and “access-off”
- Industry standard JTAG capabilities

ARTIK 1020 Module Processor System

The processor system that resides on the ARTIK 1020 Module is a system-on-a-chip (SoC) based on a 32-bit RISC processor. Designed using the 28nm low power process the processor system provides superior performance using a quad core Cortex®-A15 and a quad core Cortex®-A7 CPU. The processor system contains WQXGA display capability, 3D graphics hardware, image signal processor hardware and a variety of high-speed interfaces such as eMMC5.0, and USB 3.0.

The ARTIK 1020 Module contains the quad core Cortex®-A15, which has a 40% increase in performance over the Cortex®-A9. It also incorporates a quad core Cortex®-A7 which enables energy efficient computing for less intensive tasks. The ARTIK 1020 Module allows for 14.9GB/s memory bandwidth for heavy traffic operations such as 1080p video en/decoding, 3D graphics display and high resolution image signal processing up to WQXGA resolutions.

The application processor supports dynamic virtual address mapping aiding software engineers to fully utilize the memory resources. The ARTIK 1020 Module 3D core's universal scalable shader engine supports the feature sets in Microsoft VS5.0 and PS5.0. The ARTIK 1020 Module supports Panel-Self-Refresh (PSR) to make a low power system which is important in an IoT environment. The native dual display, in particular, supports WQXGA resolution for the main LCD display and 1080p@60fps HDTV display through HDMI. The key features of the ARTIK 1020 Module are:

- Quad core ARM® Cortex®-A15 with NEON, 32 KB I$/32 KB D$ and 2MB L2 Cache
- Quad core ARM® Cortex®-A7, 32KB I$/32KB D$ and 512KB L2 Cache
- 128-bit Multi-layer Network-on-Chip (NoC) architecture
- Cache Coherent Interface (CCI) among Cortex®-A15 and Cortex®-A7, G2D, G3D and SSS
- Memory Subsystem:
  - 2-ports 32-bit up to 933 MHz LPDDR3/DDR3 Interfaces
  - 2-ports 32-bit up to 533 MHz LPDDR2 Interfaces
- 3D and 2D graphics hardware
- 1x port with 4-lanes MIPI DSI display interface for LCD, supporting up to FHD 1920x1200@24bpp RGB
- 1x HDMI 1.4a interface with on-chip PHY
- 1x port with 4-lanes MIPI CSI2 camera interface
- 1x port with 2-lanes MIPI CSI2 camera interface
- 1x channel USB 3.0 Host or Device (with USB2.0 backward compatibility), supporting SS (5 Gbps) with on-chip PHY
- 1x channel USB 2.0 Host, supporting LS/FS/HS (1.5 Mbps/12 Mbps/480 Mbps) with on-chip PHY
- 1x channel USB2.0 Device
- 1x channel 4-bit SD 3.0
- 1.5x channel high-speed UART (up to 3 Mbps data rate for Bluetooth 2.1 EDR and IrDA 1.0 SIR)

- 1x channel SPI
- 1x channel PCM and 2-channel I²S audio interface, supporting 5.1 channel audio
- 4x channel HS-I²C (up to 3.4 Mbps) for a variety of sensors (such as ambient light sensor, proximity sensor) and PMIC
- 4x channel I²C interface supporting (up to 400 kbps) for HDMI, general-purpose multi-master and ISP
- Security subsystem supporting hardware crypto accelerators, ARM® TrustZone® and TZASC
- 24x channel DMA Controller (8-channel MDMA, 8x2 channel PDMA)
- 87x Configurable Type A GPIOs and 8x Type B GPIOs
- Real time clock, PLLs, timer with PWM, MCT (Multi-Core Timer), and Watchdog timer

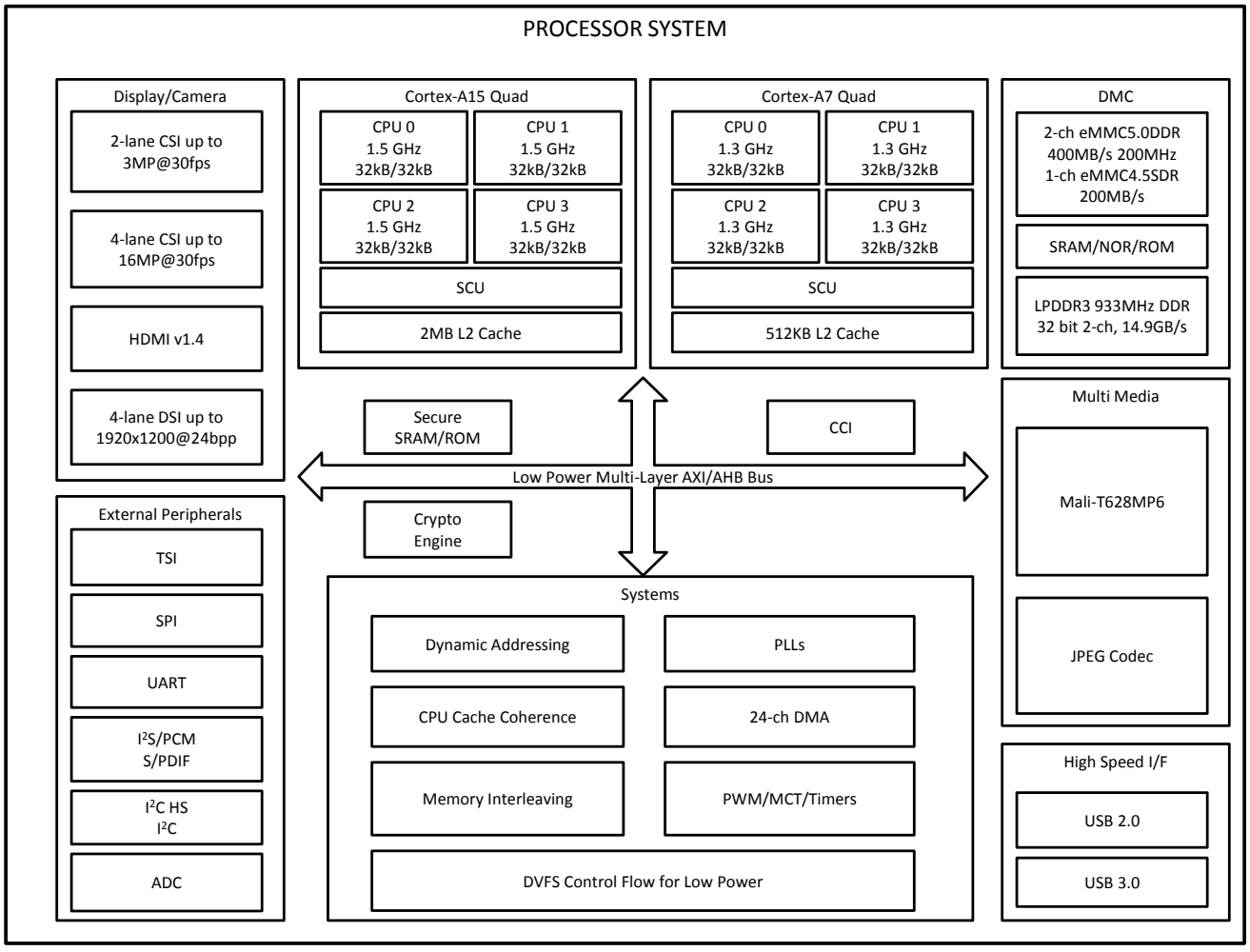


Figure 3. Processor System Block Schematic

Camera ISP

The processor system provides two main camera input channels (1x 4-channels, 1x 2-channels) that can process data up to 1.5 Gbps per channel using a MIPI CSI interface. The key features of the camera sub-system are:

- CAMIF (FIMC-LITE)
- Fully interactive mobile camera interface
- Input data through parallel I/F like ITU R BT-601 standard and MIPI (CSI) Slave I/F
- Consists of one input local path, output local port and output DMA port
- Supports input format of RAW8/10/12/14-bit+YUV422 8bit, MJPEG
- Supports MIPI VCI (virtual channel interleaving) up to 3 channels (single sensor). In dual sensor mode, 2-channel VCI + 1-channel
- 3 CAMIFs for dual sensor operation

HDMI v1.4

The ARTIK 1020 Module provides one HDMIv1.4 (High Definition Multimedia Interface) compliant interface. The key features of the HDMIv1.4 sub-system are:

- HDMI 1.4 with HDCP 1.4
- Support for video formats:
  - 480p@59.94Hz/60Hz, 576p@50Hz
  - 800x600@50Hz/60Hz
  - 720p@50Hz/59.94Hz/60Hz
  - 1280x800@60Hz
  - 1440x480i@60Hz
  - 1440x576i@50Hz
  - 1080i@50Hz/59.94Hz/60Hz
  - 1080p@50Hz/59.94Hz/60Hz
- Support for color formats:
  - RGB888/YCbCr444(YUV444)
  - 8-bit precision per color only
- Support for CEC function
- Includes an integrated high-bandwidth Digital Content Protection (HDCP) encryption engine for audio/video content protection

LCD Display

The ARTIK 1020 Module provides an LCD display capability using 1x MIPI interface that is compliant with the MIPI DSI standard specification V1.01. The key features of the LCD display sub-system are:

- Maximum resolution ranges up to FHD (1920x1200@24bpp)
- Supports 1, 2, 3, or 4 data lanes
- Supports pixel format: 16bpp, 18bpp packed, 18bpp loosely packed (3 byte format), and 24bpp
- Supported interfaces are:
  - Protocol-to-PHY Interface (PPI) in 1.0 Gbps/1.5Gbps MIPI D-PHY
  - RGB Interface for video image input from display controller
  - S-I80 (Synchronous I80) interface for Command Mode Image input from display controller
  - PMS control interface for PLL to configure byte clock frequency
  - Pre-scaler to generate escape clock from byte clock
  - Stereoscopic 3D, proprietary 3D, MIC input

SPI

The ARTIK 1020 Module provides 1x Serial Peripheral Interface (SPI) that transfers serial data. SPI support includes
8-bit/16-bit/32-bit shift registers to transmit and receive data. During a SPI transfer, data is simultaneously transmitted (shifted out serially) and received (shifted in serially). Our SPI implementation adheres to the protocols described
by National Semiconductor, Microwire and Motorola's Serial Peripheral Interface. The key features of the SPI sub-system are:

- Support for full duplex
- 8-bit/16-bit/32-bit shift register for Tx and Rx
- 8-bit/16-bit/32-bit bus interface
- Complies with the SPI protocol described by National Semiconductor, Microwire and Motorola
- Support for 2 independent 32-bit wide transmit and receive FIFOs:
  - Depth 64 in SPI port 0 and depth 16 in SPI port 1 and 2
  - Depth 64 in ISP-SPI port 0 and 1
- Supports for master mode and slave mode
- Supports for receive-without-transmit operation
- Support Tx/Rx up to 50MHz

ADC

The ARTIK 1020 Module provides 6 channels of ADC input that are connected through a multiplexer to 1x12-bit ADC.
The key features of the ADC are:

- Up to 12-bit resolution per channel
- Conversion rate 30kSamples/s-600kSamples/s with a 600kHz-12MHz clock
- Programmable conversion mode (1, 2, 4, 8, 16, 32 or 64 times conversion)

UART

The ARTIK 1020 Module provides 1.5x (1x4-pin, 1x2-pin) independent UART channels and dedicated ISP UART channel.
The key features of the UART sub-system are:

- Both DMA and interrupt based mode of operation supported
- All independent channels support IrDA 1.0
- Each UART channel contains two FIFOs to receive and transmit data:
  - 256 bytes in ch0
  - 64 bytes in ch1
  - 64 bytes in ISP-UART ch0
  - 16 bytes in ch2 and ch3
- Each UART channel contains:
  - Programmable baud-rates
  - One or two stop bit insertion
  - 5-bit, 6-bit, 7-bit, or 8-bit data width
  - Parity checking

I^2S

The ARTIK 1020 Module provides 2x, 3 line Inter-IC Sound (I^2S) channels. The I^2S interface is one of the most popular digital audio interfaces. The I^2S bus handles audio data and other signals such as sub-coding and control. It is possible to transmit data between two I^2S buses. To minimize the number of pins required and to keep wiring simple, a 3-line serial bus is used. The key features of the I^2S sub-system are:

- Mixes up to 2 sound sources
- Drives primary sound source up to 5.1ch using I^2S-bus with external DMA-based operation
- Supports secondary sound source up to stereo with internal or external DMA
- Supports I^2S TDM mode: 1-8 slots (7.1 channels) for transmission (Tx) and 1-2 slots (2 channels) for reception (Rx)
- Supports serial data transfer of 8/16/24-bit per channel
- Supports I^2S, MSB-justified, and LSB-justified data formats
- Supports both master and slave modes
- Supports auxiliary clock out for codec chip

PCM

The ARTIK 1020 Module provides 1x PCM channel. The PCM audio interface provides a bi-directional serial interface
to an external codec. The key features of the PCM sub-system are:

- 16-bit PCM and three ports audio interface
- Supports only Master mode
- All PCM serial timings and strobes are extracted from one master clock
- Supports 1x input (16-bit x 32depth) and 1x output (16-bit x 32 depth) FIFO to buffer data
- DMA interface for Tx or Rx, or both

GPIO

The ARTIK 5 Module provides a GPIO system to allow for a wide variety of use cases to be supported. The key features of the GPIO system are:

- Control for up to 88 external interrupts
  - Falling edge triggered

  - Rising edge triggered
  - Both edge triggered
- Control for up to 25 wake-up interrupts
  - Falling edge triggered
  - Rising edge triggered
  - Both edge triggered
- Control for up to 95 General Purpose IOs
- Controls a variety of pin states in sleep mode

I²C

The ARTIK 1020 Module provides 4x High Speed (HS) I²C channels, in addition it also provides 4x I²C channels. The key features of the I²C module are:

- 4x HS I²C channels up to 3.4Mb/s
- 4x I²C channels up to 400kb/s:
  - Supporting master and slave mode
  - 7-bit addressing mode only
  - Supports serial, 8-bit oriented and bi-directional data transfer
  - Supports up to 100 kb/s in the standard mode
  - Supports up to 400 kb/s in the fast mode
  - Supports master transmit, master receive, slave transmit, and slave receive operation
  - Supports both interrupt and polling events

USB

The ARTIK 1020 Module provides 1x USB2.0 host interface and 1x USB3.0 interface. The key features of the USB2.0 module are:

- In compliance with the Enhanced Host Controller Interface (EHCI) specification, version 1.1 and the Open Host Controller Interface (OHCI) specification, version 1.0a
- In compliance with the USB 2.0 specification
- In compliance with the both the legacy UTMI revision 1.05 and the UTMI+ Level3 revision 1.0
- Supports high-speed, full speed and low speed transfers
- Supports power management features, such as: Suspend/resume functionality, including remote wakeup
- Over-current protection

The key features of the USB3.0 module are:

- In compliance with USB device 3.0 and USB device 2.0
- In compliance with USB host 3.0 and USB host 2.0
- Supports USB device 3.0 interface and USB device 2.0 interface
- Supports USB host 3.0 interface and USB host 2.0 interface
- Supports full-speed (12 Mbps) and high-speed (480 Mbps) modes with USB Device 2.0 interface
- Supports super-speed (5 Gbps) mode with USB device 3.0 interface
- Supports one physical USB port meaning the physical port can be used with either USB 3.0 or USB 2.0
- Supports on-chip USB PHY transceiver
- Supports flexible endpoint configuration
- Supports up to 16 bi-directional endpoints, including control endpoint 0

Mali™-T600 Series

The ARTIK 1020 Module provides 1x instance of the Mali™-T600 GPU series from ARM®. The Mali™-T600 series adds graphics capabilities to the ARTIK 1020 Module. The key features of the Mali™-T600 module are:

- Double precision image processing with FP64 and anti-aliasing
- Coherency aware memory architecture
- Support for EGL 1.4

DMC

The ARTIK 1020 Module provides a Dynamic Memory Controller (DMC) that supports the following memory interfaces:

- 2x channel eMMC5.0 DDR@400MB/s
- 1x channel eMMC4.5 SDR@200MB/s
- SRAM/NOR/ROM interface
- LP-DDR3@933MHz interface
- 2x channel 32-bit DDR3@14.9GB/s

Quad Cortex®-A15 plus Quad Cortex®-A7

The ARTIK 1020 Module provides eight CPU cores which consist of ARM Cortex-A15 quad core processors and ARM Cortex-A7 quad core processors. The Cortex-A15 cores are targeted toward high performance functions while the Cortex-A7 cores are optimized for power efficient computations. For easier and faster CPU core switching, the ARTIK 1020 Module supports a cache coherency interconnect (CCI) bus with L2 cache snooping capability. This hardware automatically assures cache coherency between the 2x L2 caches, so manually synchronizing contents is not needed. The ARM Cortex-A7/A15 octa-core has the following common features:

- Common ARMv7-A Cortex architecture
- Advanced SIMD version 2 with architecture extensions for integer and floating-point vector operations
- Vector floating-point version 4 architecture extensions for floating-point computation that is fully compliant with the IEEE 754 standard
- TrustZone® security technology for ensuring reliable implementation
- Virtualization extensions for the development of virtualized systems that enables the switching of guest operating systems
- Large Physical Address Extension (LPAE) for address translation of up to 40 bits physical address space
- AMBA 4 Cache Coherent Interconnect (CCI)
- ARM NEON™ with 128-bit SIMD
- Multiprocessing extensions for multiprocessing functionality

The ARM Cortex-A15 has the following specific features:

- 3.5 DMIPS per core
- 32KB/32KB I$/D$ and 2MB L2 cache
- 1 TB physical addressing space
- Full hardware virtualization
- ECC and parity protection for all SRAMs
- Advanced power management
- Improved single-thread and MP performance

The ARM Cortex-A7 has the following specific features:

- 1.86 DMIPS per core
- 32KB/32KB I$/D$ cache and 512KB L2 cache
- Rapid switch companion to Cortex-A15

Associated with the eight CPU cores, the ARTIK 1020 Module provides a generic interrupt controller and multi-core timers for each CPU core. The interrupt controller and timer are always-alive even when the CPU cores are power gated. The key features of the generic interrupt controller are:

- Support for three interrupt types:
  - Software Generated Interrupt (SGI)
  - Private Peripheral Interrupt (PPI)
  - Shared Peripheral Interrupt (SPI)
- Programmable interrupts that:
  - Set the security state for an interrupt
  - Set the priority level of an interrupt
  - Enable or disable the interrupt
  - Inform the processors that receives an interrupt
- Enhanced security features

The key features of the multi-core timers are:

- Eight local timers, one for each CPU core containing:
  - A 32-bit counter that generates an interrupt when it reaches zero
  - Single-shot or auto-reload mode
  - Configurable starting value per timer
- A global timer:
  - With a 64-bit incrementing counter and an auto-incrementing feature
  - Accessible to all Cortex-A15/Cortex-A7 processors

ARTIK 1020 Module Connectors

The ARTIK 1020 Module utilizes 2x 80-position and 2x 40-position connectors providing support for GPIO, ADC, SPI, OM, USB, UART, PWM, ISP, I^{2}C, MIPI, HDMI and JTAG. Connector J3 and J4 indicated by AXT480124 are from Panasonic and have 80 pins with a 0.4mm pitch. Connector J1 and J9 indicated by AXT440124 are also from Panasonic and have 40 pins with a 0.4mm pitch. For additional information on both AXT480124 and AXT440124 please contact Panasonic.

In *Figure 4* a listing of all power/signal names that are assigned to physical pins of connector J3 and connector J4 are given. In *Table 1* and *Table 2* the functions and electrical limitations associated with physical behavior of the pins is described. Functionally Connector J3 carries the following interfaces: SPI, I^{2}C, ADC, USB3.0 CH0, I^{2}S/PCM, UART, GPIO and PWM. Functionally Connector J4 carries the following interfaces: ISP, I^{2}C, GPIO, PWM, USB HOST, USB3.0, MMC and MIPI. In general the Interrupts, GPIO and I^{2}C functionality that is present on the connector's might be support for the other interfaces present on the connector.

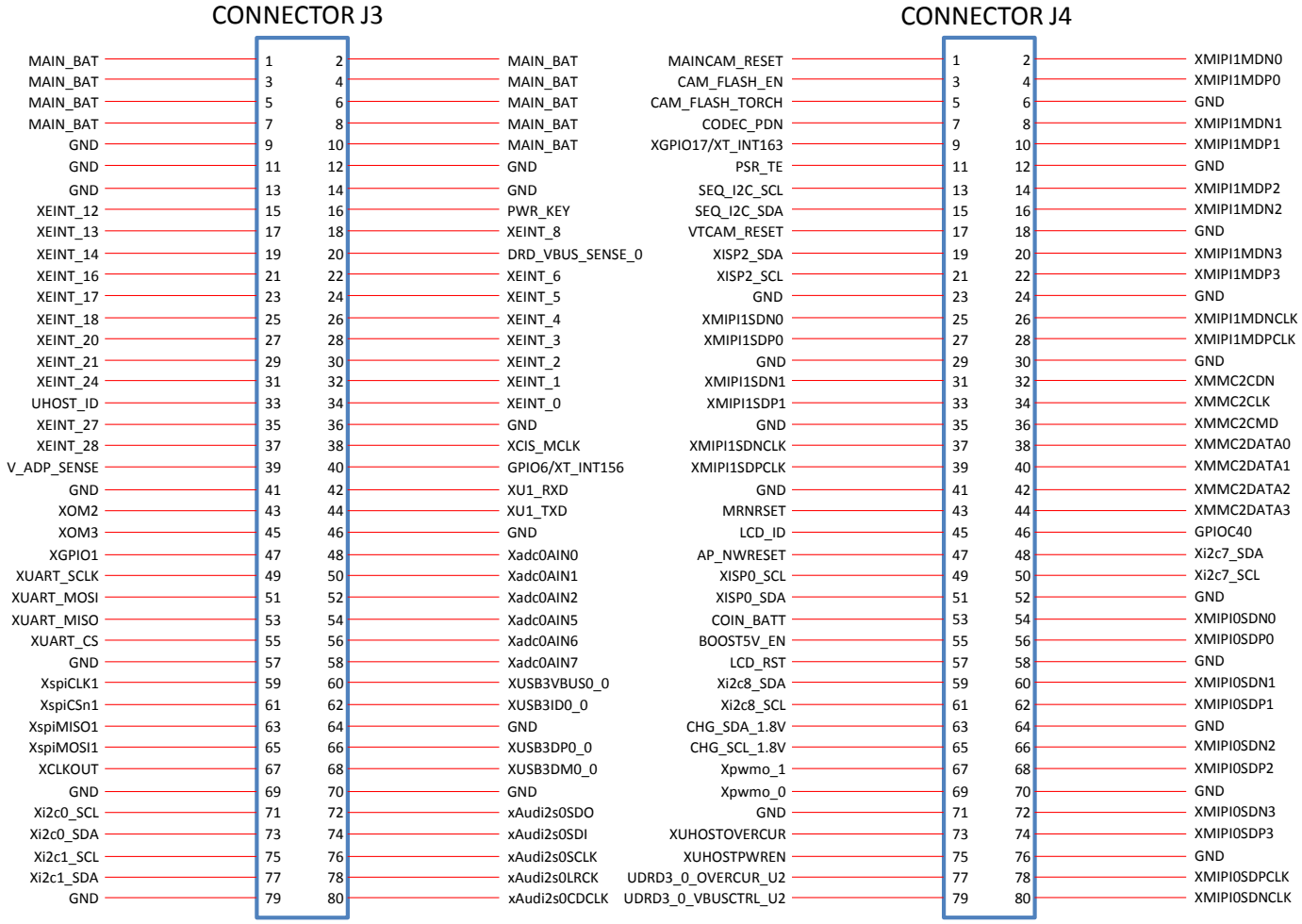


Figure 4. Connector J3, J4 Pin Layout

CONNECTOR J3

Table 1. Connector J3 Pin Description

Connector J3									
Conn#	Pin#	Name	I/O Type	Default	Voltage	DS [mA]	PUD*	Group	Function
J3	1	MAIN_BAT	NA		3V8	NA		BATTERY	Power source (3.8V)
J3	3	MAIN_BAT	NA		3V8	NA		BATTERY	Power source (3.8V)
J3	5	MAIN_BAT	NA		3V8	NA		BATTERY	Power source (3.8V)
J3	7	MAIN_BAT	NA		3V8	NA		BATTERY	Power source (3.8V)
J3	9	GND	NA		0V0	NA		GROUND	Ground
J3	11	GND	NA		0V0	NA		GROUND	Ground
J3	13	GND	NA		0V0	NA		GROUND	Ground
J3	15	XEINT_12	A	I	1V8	2	PDE	LCD	MIPI error detection
J3	17	XEINT_13	A	I	1V8	2	PDE	ARDUINO	GPIO
J3	19	XEINT_14	A	I	1V8	2	PDE	ARDUINO	GPIO
J3	21	XEINT_16	A	I	1V8	2	PDE	Wi-Fi/BT	GPIO
J3	23	XEINT_17	A	I	1V8	2	PDE	POWER/RESET	CHG_IRQ
J3	25	XEINT_18	A	I	1V8	2	PDE	UARTS	XUART_RST
J3	27	XEINT_20	A	I	1V8	2	PDE	UARTS	XUART_IRQ
J3	29	XEINT_21	A	O	1V8	2	PDE	LCD	TP_RST
J3	31	XEINT_24	A	I	1V8	2	PDE	LCD	TP_INT
J3	33	UHOST_ID	A	EXT_INT43[1]	1V8	2	PUDD	NA	UHOST_ID
J3	35	XEINT_27	A	I	1V8	2	PDE	AUDIO	JACK_DET
J3	37	XEINT_28	A	I	1V8	2	PDE	Wi-Fi/BT	LVDS_RST
J3	39	V_ADP_SENSE	A	I	1V8	2	PDE	POWER/RESET	V_ADP_SENSE
J3	41	GND	NA		0V0	NA		GROUND	Ground
J3	43	XOM2	PROCESSOR		1V8	NA		POWER/RESET	SDMMC_CH2 or eMMC44_CH0 boot
J3	45	XOM3	PROCESSOR		1V8	NA		POWER/RESET	SDMMC_CH2 or eMMC44_CH0 boot
J3	47	XGPIO1	A	I	1V8	2	PDE	CAMERA	Power down
J3	49	XUART_SCLK	A	I	1V8	2	PDE	UARTS	GENERIC UART SCLK
J3	51	XUART_MOSI	A	I	1V8	2	PDE	UARTS	GENERIC UART MOSI
J3	53	XUART_MISO	A	I	1V8	2	PDE	UARTS	GENERIC UART MISO
J3	55	XUART_CS	A	I	1V8	2	PDE	UARTS	GENERIC UART CS
J3	57	GND	NA		0V0	NA		GROUND	Ground
J3	59	XspiCLK1	A	I	1V8	2	PDE	Wi-Fi/BT/SIGFOX	SPI CLK
J3	61	XspiCSn1	A	I	1V8	2	PDE	SIGFOX	SPI CSn
J3	63	XspiMISO1	A	I	1V8	2	PDE	Wi-Fi/BT/SIGFOX	SPI MISO
J3	65	XspiMOSI1	A	I	1V8	2	PDE	Wi-Fi/BT/SIGFOX	SPI MOSI
J3	67	XCLKOUT	NA		1V8	NA		AUDIO	24MHz CDCLK
J3	69	GND	NA		0V0	NA		GROUND	Ground
J3	71	Xi2c0_SCL	A	I	1V8	2	PDE	POWER/RESET	SCL
J3	73	Xi2c0_SDA	A	I	1V8	2	PDE	POWER/RESET	SDC
J3	75	Xi2c1_SCL	A	I2C_1_SCL	1V8	2	PUE	Wi-Fi/BT/AUDIO	SCL for BT audio
J3	77	Xi2c1_SDA	A	I2C_1_SDA	1V8	2	PUE	Wi-Fi/BT/AUDIO	SDA for BT audio
J3	79	GND	NA		0V0	NA		GROUND	Ground
J3	2	MAIN_BAT	NA		3V8	NA		BATTERY	Power source (3.8V)
J3	4	MAIN_BAT	NA		3V8	NA		BATTERY	Power source (3.8V)

Connector J3									
Conn#	Pin#	Name	I/O Type	Default	Voltage	DS [mA]	PUD*	Group	Function
J3	6	MAIN_BAT	NA		3V8	NA		BATTERY	Power source (3.8V)
J3	8	MAIN_BAT	NA		3V8	NA		BATTERY	Power source (3.8V)
J3	10	MAIN_BAT	NA		3V8	NA		BATTERY	Power source (3.8V)
J3	12	GND	NA		0V0	NA		GROUND	Ground
J3	14	GND	NA		0V0	NA		GROUND	Ground
J3	16	PWR_KEY	PMIC		1V8	NA		POWER/RESET	power on, high active
J3	18	XEINT_8	A	I	1V8	2	PDE	ARDUINO	GPIO
J3	20	DRD_VBUS_SENSE_0	A	EXT_INT40[7]	1V8	2	PDE	USB3.0	DRD_VBUS_SENSE_0
J3	22	XEINT_6	A	I	1V8	2	PDE	ARDUINO	GPIO
J3	24	XEINT_5	A	I	1V8	2	PDE	ARDUINO	GPIO
J3	26	XEINT_4	A	I	1V8	2	PDE	ARDUINO	GPIO
J3	28	XEINT_3	A	I	1V8	2	PDE	ARDUINO	GPIO
J3	30	XEINT_2	A	I	1V8	2	PDE	ARDUINO	GPIO
J3	32	XEINT_1	A	I	1V8	2	PDE	ARDUINO	GPIO
J3	34	XEINT_0	A	I	1V8	2	PDE	ARDUINO	GPIO
J3	36	GND	NA		0V0	NA		GROUND	Ground
J3	38	XCIS_MCLK	A	I	1V8	2	PDE	CAMERA	MCLK
J3	40	GPIO6/XT_INT156	A	I	1V8	2	PDE	CAMERA	MCLK
J3	42	Xu1_RXD	A	UART_1_RXD	1V8	2	PUDD	ARDUINO	UART RXD
J3	44	Xu1_TXD	A	UART_1_TXD	1V8	2	PUDD	ARDUINO	UART TXD
J3	46	GND	NA		0V0	NA		GROUND	Ground
J3	48	Xadc0AIN0	Analog		1V8	NA		ARDUINO	ADC
J3	50	Xadc0AIN1	Analog		1V8	NA		ARDUINO	ADC
J3	52	Xadc0AIN2	Analog		1V8	NA		ARDUINO	ADC
J3	54	Xadc0AIN5	Analog		1V8	NA		ARDUINO	ADC
J3	56	Xadc0AIN6	Analog		1V8	NA		ARDUINO	ADC
J3	58	Xadc0AIN7	Analog		1V8	NA		ARDUINO	ADC
J3	60	XUSB3VBUS0_0	USB3.0		3V3	NA		USB3.0	USB3.0 DRD channel 0
J3	62	XUSB3ID0_0	A/USB3.0/ADC	EXT_INT43[5]	1V8	2	PUE	USB3.0	Identification USB3.0 DRD channel 0
J3	64	GND	NA		0V0	NA		GROUND	Ground
J3	66	XUSB3DP0_0	USB3.0		3V3	NA		USB3.0	USB2.0 backward compatible P channel in USB3.0
J3	68	XUSB3DM0_0	USB3.0		3V3	NA		USB3.0	USB2.0 backward compatible M channel in USB3.0
J3	70	GND	NA		0V0	NA		GROUND	Ground
J3	72	xAudi2s0SDO	A		1V8			Wi-Fi/BT/AUDIO	Audio SDO
J3	74	xAudi2s0SDI	A		1V8			Wi-Fi/BT/AUDIO	Audio SDI
J3	76	xAudi2s0SCLK	A		1V8			Wi-Fi/BT/AUDIO	Audio SCLK
J3	78	xAudi2s0LRCK	A		1V8			Wi-Fi/BT/AUDIO	Audio LRCK
J3	80	xAudi2s0CDCLK	A		1V8			Wi-Fi/BT/AUDIO	Audio DCLK

* The PUD variables have the following meaning:
PUDD = Power Up Down Disabled, PDE = Power Down Enabled, PUE = Power Up Enabled, R = Reserved.

CONNECTOR J4

Table 2. Connector J4 Pin Description

Connector J4									
Conn#	Pin#	Name	I/O Type	Default	Voltage	DS [mA]	PUD*	Group	Function
J4	1	MAINCAM_RESET	A	I	1V8	2	PDE	CAMERA	Reset
J4	3	CAM_FLASH_EN	A	O	1V8	2	PDE	CAMERA	Flash
J4	5	CAM_FLASH_TORCH	A	O	1V8	2	PDE	CAMERA	Flash torch
J4	7	CODEC_PDN	A	O	1V8	2	PDE	Wi-Fi/BT/AUDIO	Codec Power Down
J4	9	XGPIO17/XT_INT163	A	I	1V8	2	PDE	SIGFOX	Low power control
J4	11	PSR_TE	A	I	1V8	2	PDE	ISP	Display sync
J4	13	SEQ_I2C_SCL	A	I	1V8	2	PDE	SPI	SCL
J4	15	SEQ_I2C_SDA	A	I	1V8	2	PDE	SPI	SDA
J4	17	VTCAM_RESET	A	I	1V8	2	PDE	CAMERA	Reset
J4	19	XISP2_SDA	A	I	1V8	2	PDE	CAMERA	SDA
J4	21	XISP2_SCL	A	I	1V8	2	PDE	CAMERA	SCL
J4	23	GND	NA		0V0	NA		GROUND	Ground
J4	25	XMIPI1SDN0	MIPI		1V0	NA		CAMERA	CSI1 SDN0 CHANNEL 0
J4	27	XMIPI1SDP0	MIPI		1V0	NA		CAMERA	CSI1 SDP0 CHANNEL 0
J4	29	GND	NA		0V0	NA		GROUND	Ground
J4	31	XMIPI1SDN1	MIPI		1V0	NA		CAMERA	CSI1 SDN1 CHANNEL 1
J4	33	XMIPI1SDP1	MIPI		1V0	NA		CAMERA	CSI1 SDP1 CHANNEL 1
J4	35	GND	NA		0V0	NA		GROUND	Ground
J4	37	XMIPI1SDNCLK	MIPI		1V0	NA		CAMERA	CSI1 SDNCLK
J4	39	XMIPI1SDPCLK	MIPI		1V0	NA		CAMERA	CSI1 SDPCLK
J4	41	GND	NA		0V0	NA		GROUND	Ground
J4	43	MRNRESET	PROCESSOR /PMIC		1V8	NA		POWER/RESET/ARDUINO/ SENSOR/ Wi-Fi/BT	PMIC resets Processor Subsystem
J4	45	LCD_ID	A	I	1V8	2	PDE	SIGFOX	Vsync
J4	47	AP_NWRESET	PROCESSOR	I	1V8	-	-	NA	Warm Reset
J4	49	XISP0_SCL	A	I	1V8	2	PDE	CAMERA	SCL
J4	51	XISP0_SDA	A	I	1V8	2	PDE	CAMERA	SDA
J4	53	COIN_BATT	NA	NA	3V3	-	-	NA	Coin Battery Power Supply
J4	55	BOOST5V_EN	A	O	1V8	2	PDE	USB3.0	USB3.0
J4	57	LCD_RST	A	O	1V8	2	PUE	LCD	Reset
J4	59	Xi2c8_SDA	A	I	1V8	2	PDE	LCD	SCL
J4	61	Xi2c8_SCL	A	I	1V8	2	PDE	LCD	SDA
J4	63	CHG_SDA_1.8V	A	I	1V8	2	PUE	POWER/RESET	Change I2C to 1V8 signaling
J4	65	CHG_SCL_1.8V	A	I	1V8	2	PUE	POWER/RESET	Change I2C to 1V8 signaling
J4	67	Xpwmo_1	A	I	1V8	2	PDE	ARDUINO	PWM On/Off control
J4	69	Xpwmo_0	A	I	1V8	2	PDE	ARDUINO	PWM On/Off control
J4	71	GND	NA		0V0	NA		GROUND	Ground
J4	73	XUHOSTOVERCUR	USB HOST		1V8	NA		NA	
J4	75	XUHOSTPWREN	USB HOST		1V8	NA		USB/ETHERNET	USB
J4	77	UDRD3_0_OVERCUR_U2	USB3.0		1V8	NA		USB3.0	Control for USB3.0 DRD channel 0
J4	79	UDRD3_0_VBUSCTRL_U2	USB3.0		1V8	NA		USB3.0	Control for USB3.0 DRD channel 0
J4	2	XMIPI1MDN0	MIPI		1V0	NA		LCD	DSI1 DN0 CHANNEL 0
J4	4	XMIPI1MDP0	MIPI		1V0	NA		LCD	DSI1 DP0 CHANNEL 0

Connector J4									
Conn#	Pin#	Name	I/O Type	Default	Voltage	DS [mA]	PUD*	Group	Function
J4	6	GND	NA		0V0	NA		GROUND	Ground
J4	8	XMIPI1MDN1	MIPI		1V0	NA		LCD	DSI1 DN1 CHANNEL 1
J4	10	XMIPI1MDP1	MIPI		1V0	NA		LCD	DSI1 DP1 CHANNEL 1
J4	12	GND	NA		0V0	NA		GROUND	Ground
J4	14	XMIPI1MDP2	MIPI		1V0	NA		LCD	DSI1 DP2 CHANNEL 2
J4	16	XMIPI1MDN2	MIPI		1V0	NA		LCD	DSI1 DN2 CHANNEL 2
J4	18	GND	NA		0V0	NA		GROUND	Ground
J4	20	XMIPI1MDN3	MIPI		1V0	NA		LCD	DSI1 DN3 CHANNEL 3
J4	22	XMIPI1MDP3	MIPI		1V0	NA		LCD	DSI1 DP3 CHANNEL 3
J4	24	GND	NA		0V0	NA		GROUND	Ground
J4	26	XMIPI1MDNCLK	MIPI		1V0	NA		LCD	DSI1 NCLK
J4	28	XMIPI1MDPCLK	MIPI		1V0	NA		LCD	DSI1 PCLK
J4	30	GND	NA		0V0	NA		GROUND	Ground
J4	32	XMMC2CDN	B		2V8	8	PUE	SD CARD	CDN card detect
J4	34	XMMC2CLK	B		2V8	8	PUDD	SD CARD	CLK
J4	36	XMMC2CMD	B		2V8	8	PUDD	SD CARD	CMD
J4	38	XMMC2DATA0	B		2V8	8	PUE	SD CARD	DATA0
J4	40	XMMC2DATA1	B		2V8	8	PUE	SD CARD	DATA1
J4	42	XMMC2DATA2	B		2V8	8	PUE	SD CARD	DATA2
J4	44	XMMC2DATA3	B		2V8	8	PUE	SD CARD	DATA3
J4	46	GPIOC40	B	I	2V8	2	PDE	POWEWR/RESET	GPIO
J4	48	Xi2c7_SDA	A	I	1V8	2	PDE	HDMI	SCL
J4	50	Xi2c7_SCL	A	I	1V8	2	PDE	HDMI	SDA
J4	52	GND	NA	-	0V0	NA		GROUND	Ground
J4	54	XMIPI0SDN0	MIPI	-	1V0	NA		CAMERA	CSI0 DN0 CHANNEL 0
J4	56	XMIPI0SDP0	MIPI	-	1V0	NA		CAMERA	CSI0 DP0 CHANNEL 0
J4	58	GND	NA	-	0V0	NA		GROUND	Ground
J4	60	XMIPI0SDN1	MIPI	-	1V0	NA		CAMERA	CSI0 DN1 CHANNEL 1
J4	62	XMIPI0SDP1	MIPI	-	1V0	NA		CAMERA	CSI0 DP1 CHANNEL 1
J4	64	GND	NA	-	0V0	NA		GROUND	Ground
J4	66	XMIPI0SDN2	MIPI	-	1V0	NA		CAMERA	CSI0 DN2 CHANNEL 2
J4	68	XMIPI0SDP2	MIPI	-	1V0	NA		CAMERA	CSI0 DP2 CHANNEL 2
J4	70	GND	NA	-	0V0	NA		GROUND	Ground
J4	72	XMIPI0SDN3	MIPI	-	1V0	NA		CAMERA	CSI0 DN3 CHANNEL 3
J4	74	XMIPI0SDP3	MIPI	-	1V0	NA		CAMERA	CSI0 DP3 CHANNEL 3
J4	76	GND	NA	-	0V0	NA		GROUND	Ground
J4	78	XMIPI0SDPCLK	MIPI	-	1V0	NA		CAMERA	CSI0 PCLK
J4	80	XMIPI0SDNCLK	MIPI	-	1V0	NA		CAMERA	CSI0 NCLK

In *Figure 5* a listing of all power/signal names that are assigned to physical pins of connector J1 and connector J9 are given. In *Table 3* and *Table 4* the functions and electrical limitations associated with physical behavior of the pins is described. Functionally Connector J1 carries the following interfaces: USB3.0 DRD, USB HOST, MMC, I^2C and HDMI. Functionally Connector J9 carries JTAG functionality for the various devices. Again as with previous connectors the Interrupts, GPIO and I^2C functionality that is present on the connector's might be support for other interfaces present on the connector.

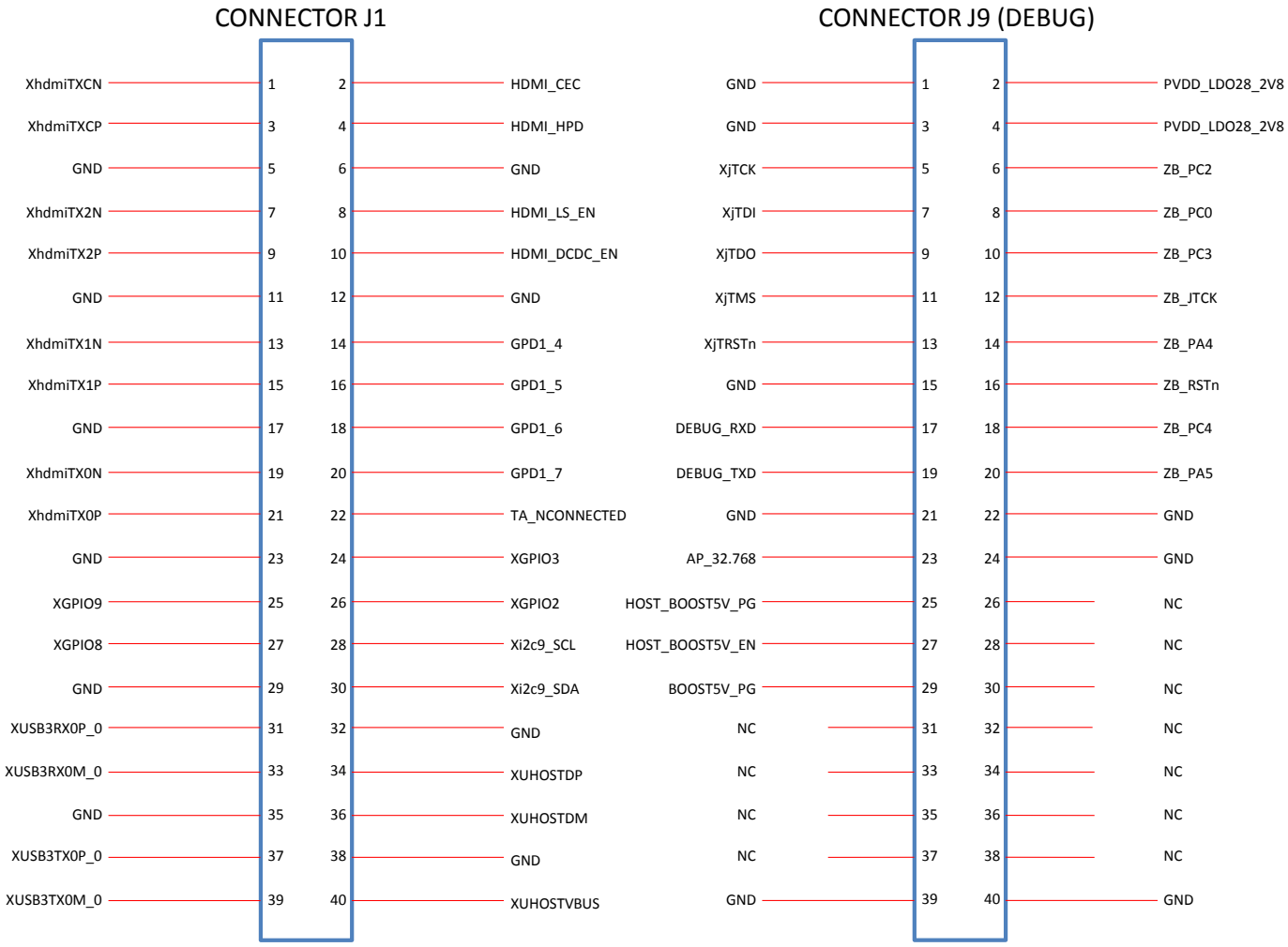


Figure 5. Connector J1, J9 Pin Layout

CONNECTOR J1

Table 3. Connector J1 Pin Description

Connector J1									
Conn#	**Pin#**	**Name**	**I/O Type**	**Default**	**Voltage**	**DS [mA]**	**PUD***	**Group**	**Function**
J1	1	XhdmiTXCN	HDMI	-	1V0	NA		HDMI	TXCN
J1	3	XhdmiTXCP	HDMI	-	1V0	NA		HDMI	TXCP
J1	5	GND	NA	-	0V0	NA		GROUND	Ground
J1	7	XhdmiTX2N	HDMI	-	1V0	NA		HDMI	TX2N
J1	9	XhdmiTX2P	HDMI	-	1V0	NA		HDMI	TX2P
J1	11	GND	NA	-	0V0	NA		GROUND	Ground
J1	13	XhdmiTX1N	HDMI	-	1V0	NA		HDMI	TX1N
J1	15	XhdmiTX1P	HDMI	-	1V0	NA		HDMI	TX1P
J1	17	GND	NA	-	0V0	NA		GROUND	Ground
J1	19	XhdmiTX0N	HDMI	-	1V0	NA		HDMI	TXON
J1	21	XhdmiTX0P	HDMI	-	1V0	NA		HDMI	TXOP
J1	23	GND	NA	-	0V0	NA		GROUND	Ground
J1	25	XGPIO9	A	I	1V8	2	PDE	SIGFOX	Power enable
J1	27	XGPIO8	A	I	1V8	2	PDE	ZWAVE	Reset
J1	29	GND	NA	-	0V0	NA		GROUND	Ground
J1	31	XUSB3RX0P_0	USB3.0	-	1V0	NA		USB3.0	USB3.0 DRD channel 0 receive plus
J1	33	XUSB3RX0M_0	USB3.0	-	1V0	NA		USB3.0	USB3.0 DRD channel 0 receive minus
J1	35	GND	NA	-	0V0	NA		GROUND	Ground
J1	37	XUSB3TX0P_0	USB3.0	-	1V0	NA		USB3.0	USB3.0 DRD channel 0 transmit plus
J1	39	XUSB3TX0M_0	USB3.0	-	1V0	NA		USB3.0	USB3.0 DRD channel 0 transmit minus
J1	2	HDMI_CEC	A	I	1V8	2	PDE	HDMI	HDMI_CEC
J1	4	HDMI_HPD	A	EXT_INT43[7]	1V8	2	PDE	HDMI	HDMI_HPD
J1	6	GND	NA	-	0V0	NA		GROUND	Ground
J1	8	HDMI_LS_EN	A	O	1V8	2	PDE	HDMI	HDMI_LS_EN
J1	10	HDMI_DCDC_EN	A	O	1V8	2	PDE	HDMI	HDMI_DCDC_EN
J1	12	GND	NA		0V0	NA		GROUND	Ground
J1	14	GPD1_4	A	I	1V8	2	PDE	PROCESSOR	GENERIC DATA0
J1	16	GPD1_5	A	I	1V8	2	PDE	PROCESSOR	GENERIC DATA1
J1	18	GPD1_6	A	I	1V8	2	PDE	PROCESSOR	GENERIC DATA2
J1	20	GPD1_7	A	O	1V8	2	PDE	PROCESSOR	GENERIC DATA3
J1	22	TA_nCONNECTED	PMIC	-	1V8	NA		PMIC	Power up event
J1	24	XGPIO3	A	I	1V8	2	PDE	SIGFOX	GENERIC GPIO
J1	26	XGPIO2	A	I	1V8	2	PDE	CAMERA	GENERIC GPIO
J1	28	Xi2c9_SCL	A	I	1V8	2	PDE	Wi-Fi/BT	GENERIC SCL
J1	30	Xi2c9_SDA	A	I	1V8	2	PDE	Wi-Fi/BT	GENERIC SDA
J1	32	GND	NA	-	0V0	NA		GROUND	Ground
J1	34	XUHOSTDP	USB HOST	-	3V3	NA		USB/ETHERNET	USB data plus
J1	36	XUHOSTDM	USB HOST	-	3V3	NA		USB/ETHERNET	USB data minus
J1	38	GND	NA	-	0V0	NA		GROUND	Ground
J1	40	XUHOSTVBUS	USB HOST	-	3V3	NA		USB	USB vbus