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SAMSUNG

ARTIK™ Modules 5

ARTIK 530s Development Kit Overview

Version History 2
ARTIK 530s Development Kit Contents 3
ARTIK 530s Additional Documentation 3
Additional Materials 3
ARTIK 530s Development Kit Overview 4
    Development Kit Block Diagram 5
ARTIK 530s Development Kit Interposer Board 6
ARTIK 530s Interposer Board Interfaces 7
    USB OTG 7
    HDMI 7
    Reset Pushbutton Switch 10
    Power-Key Pushbutton Switch 10
    Boot Mode DIP Switches 11
    Interposer to Platform Board Connectors 11
ARTIK 530s Development Kit Platform Board 14
    SD Card Interface 15
    Audio Interface 15
    USB Host 2.0 Interface 17
    ARTIK JTAG 17
    Power Jack 17
    Power Switch 18
    GPIO Test Header Interface to I/O Expander Board 18
ARTIK 530s Development Kit I/O Expander Board 20
    I/O Expander Board Power Source 21
ARTIK 530s Configuration 22
    Selecting the Development Kit Power Source 22
    ARTIK 530s Development Kit Boot Mode Configuration 23
    ARTIK 530s Software Configuration 25
        Powering On the ARTIK Development Kit 25
        Windows Based Configuration 25
        Linux Based Configuration 28
Mechanical Specifications 30

List of Figures

Figure 1. ARTIK 530s Development Kit Contents 4
Figure 2. ARTIK 530s Development Platform System Block Diagram 5
Figure 3. ARTIK 530s Interposer Board (Left - Top Side, Right - Bottom Side) 6
Figure 4. Location of USB OTG Port on the Interposer Board 7
Figure 5. Location of HDMI Port on Interposer Board 8
Figure 6. Location of LVDS Connection on the Interposer Board 8
Figure 7. Location of Ethernet Port on the Interposer Board 9
Figure 8. Location of Antennas on the Interposer Board 9
Figure 9. Location of PWR_KEY Pushbutton Switch on the Interposer Board 10
Figure 10. ARTIK 530s Development Kit Platform Board (Left - Bottom Side, Right - Top Side 14
Figure 11. Location of SD Card Interface on the Platform Board 15
Figure 12. Location of the Audio Jack on the Platform Board 15
Figure 13. Location of MIPI DSI Connector on the Platform Board 16
Figure 14. Location of MIPI CSI Connector on the Platform Board 16
Figure 15. Location of the USB2.0 Interface Ports on the Platform Board 17
Figure 16. Location of the 5V DC Power Supply Jack on the Platform Board 17
Figure 17. Location of Power Switch on the Platform Board 18
Figure 18. ARTIK 530s Development Kit I/O Expander Board 20
Figure 19. Location of Jumpers JP1 - JP4 on the Platform Board 22
Figure 20. Location of Boot Configuration DIP Switches on the Interposer Board 23
Figure 21. ARTIK 530s Interposer and Platform Board Mechanical Specifications 30

Version History

Revision	Date	Description
V1.0	November 30, 2017	Initial draft of ARTIK 530s Development Kit Overview.

This document describes the ARTIK 530s Development Kit.

ARTIK 530s Development Kit Contents

The ARTIK 530s development kit consists of the following components:

- ARTIK 530s Interposer board (contains ARTIK 530s module)
- ARTIK 530s Platform board (connected to the Interposer board at the factory)
- ARTIK 530s I/O Expander board (connects to the Platform board for I/O expansion)
- Bluetooth/WiFi antenna (for general purpose wireless communication)
- Zigbee antenna (for low-power, low-speed close proximity wireless communication)

Each of these components is described in the following subsections.

ARTIK 530s Additional Documentation

The following documents provide additional information on the ARTIK 530s development environment.

- ARTIK 530s Data Sheet
- ARTIK 530s Hardware User Guide
- ARTIK 530s/710s System Design Guide
- ARTIK PCB Design Guide
- ARTIK 530s Interposer board schematics
- ARTIK 530s Platform board schematics
- ARTIK 530s I/O Expander board schematics
- ARTIK 530s Bill of Materials

Additional Materials

Depending on the system environment, the following components may be required when interfacing to the ARTIK 530s Development Platform.

- 5V DC, 24W power supply for connecting to the DC power jack on the Platform board. Note that the 5V DC jack is identical to a 12V DC jack. Ensure that the power supply is 5V, not 12V.
- microUSB cable for connecting an external host or when transferring data over the USB OTG port.
- USB-A cables for interfacing to one of two USB Host ports on the Platform board.
- HDMI micro-to-standard cable for connection to an HDMI display.
- Ethernet cable for direct connection to a local area network.
- Connection to a local WiFi network via the Bluetooth/WiFi antenna on the Interposer board.

ARTIK 530s Development Kit Overview

The ARTIK 530s Development Board consists of one Interposer Board, one Platform Board and one I/O Expander board. The Interposer board includes the ARTIK 530s module which is soldered to the board at the factory.

The ARTIK 530s Development Platform is an affordable approach for developing an IoT solution. The ARTIK 530s module is designed for IoT devices and it contains hardware functions based on a Linux® system. Some of hardware functions include multimedia and network such as 802.11 and ZigBee®. In addition the ARTIK 530s Module has mass storage capability.

Figure 1 shows the three boards that make up the ARTIK 530s Development Kit.

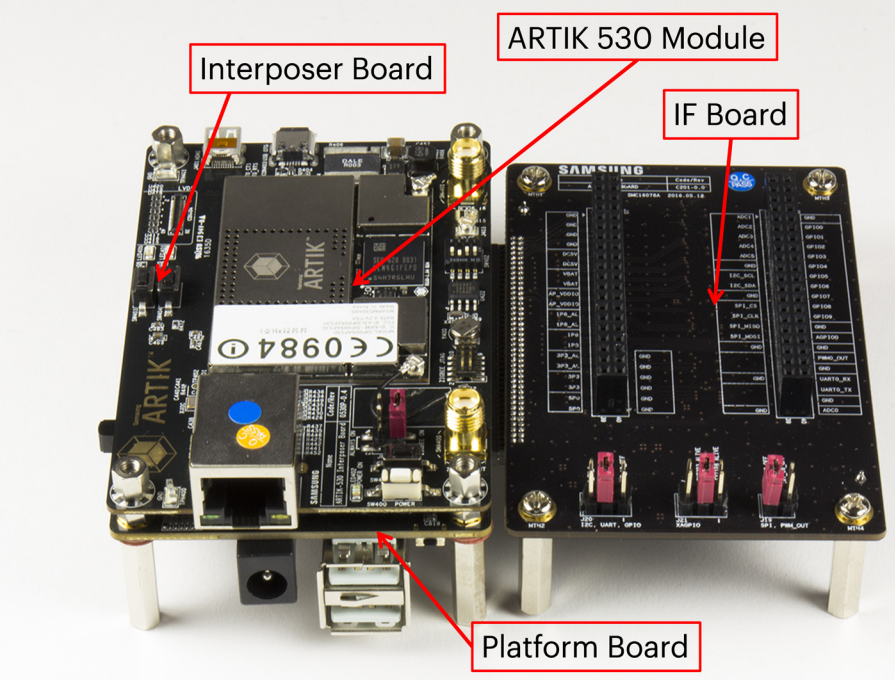

Figure 1. ARTIK 530s Development Kit Contents

Development Kit Block Diagram

Figure 2 shows a system block diagram of the three boards in the ARTIK 530s module development platform and the relative location of each interface.

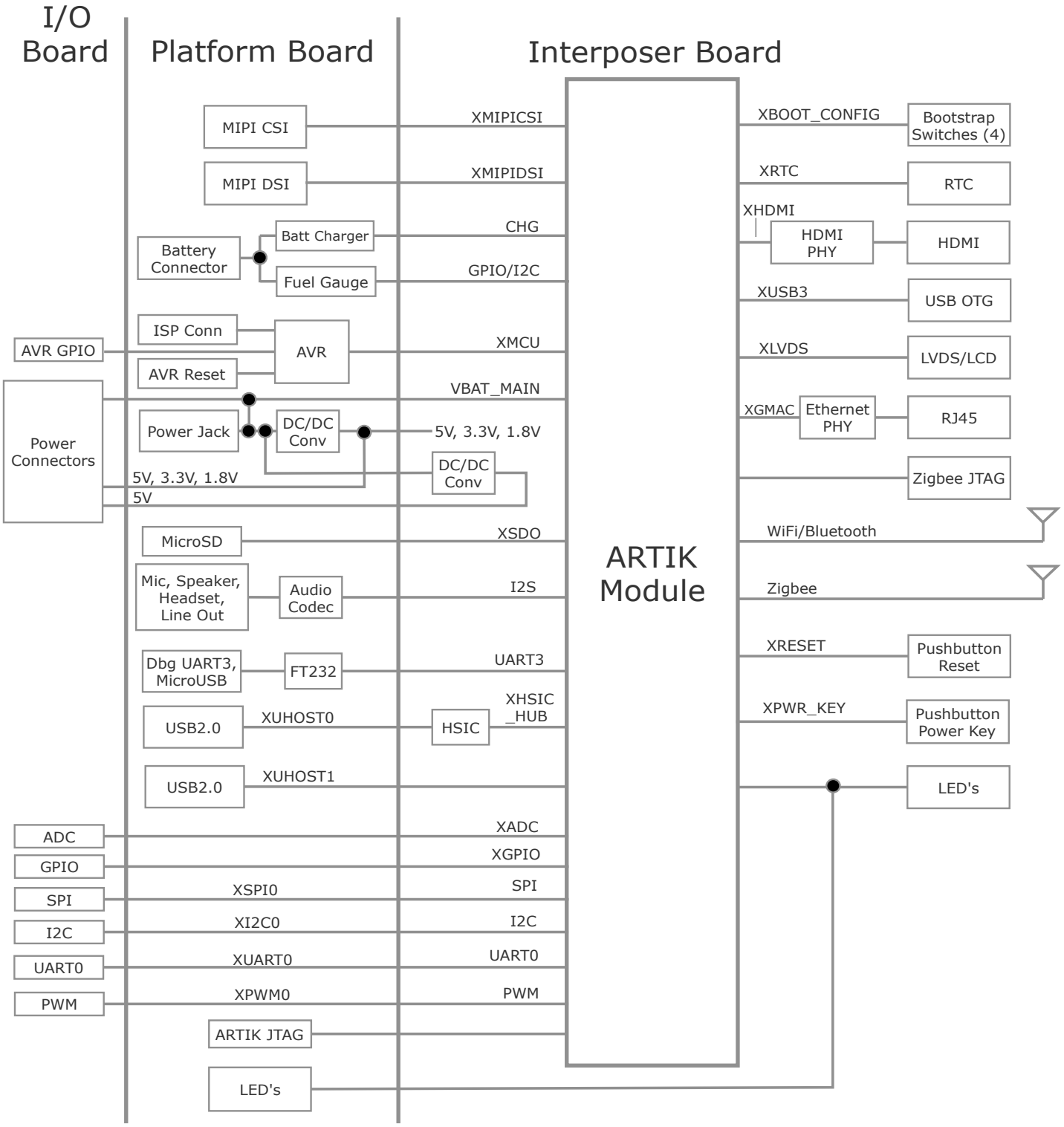

Figure 2. ARTIK 530s Development Platform System Block Diagram

ARTIK 530s Development Kit Interposer Board

The ARTIK 530s Interposer Board interfaces are shown in *Figure 3*.

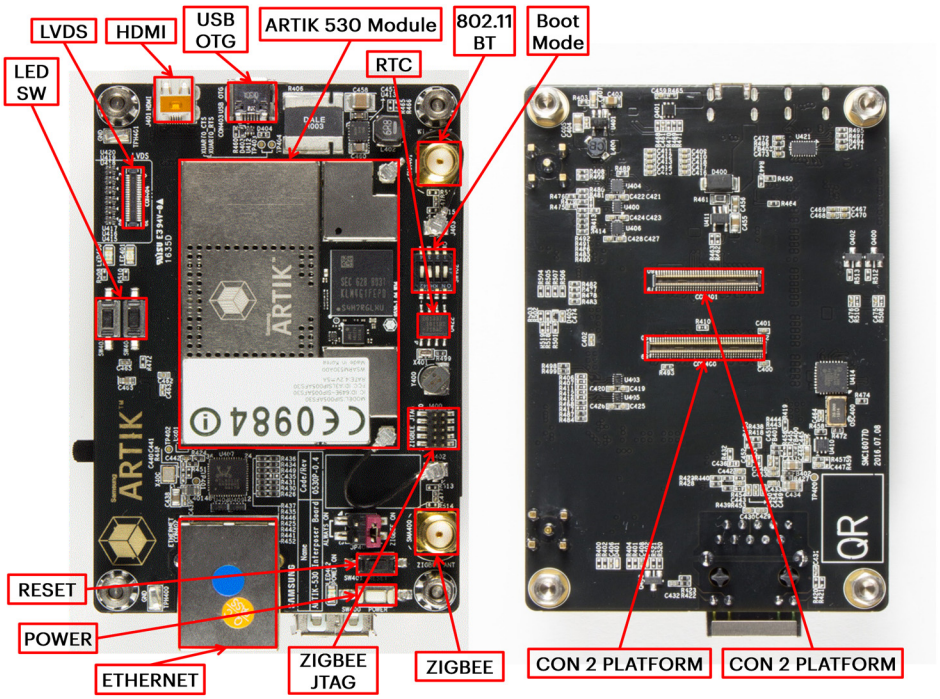

Figure 3. ARTIK 530s Interposer Board (Left - Top Side, Right - Bottom Side)

The ARTIK 530s Development Platform contains the ARTIK 530s module that is soldered to the Interposer board. *Table 1*shows the main features of the ARTIK 530s module. For more information on the ARTIK 530s module please consult the ARTIK 530s module datasheet.

Table 1. ARTIK 530s Module Main Features

Feature	Description
CPU	Quad-core ARM Cortex A9 @ 1.2 GHz
GPU	3D graphics accelerator
Camera Interface	4-lane MIPI CSI up to 5M (1920 x 1080 @ 30 fps)
Display interface	4-lane MIPI DSI and HDMI 1.4a (1920 x 1080p @ 60 fps), or LVDS (1280 x 720p @ 60 fps)
Audio	Two I2S audio channels (input/output)
DRAM	512 MB DDR3
Flash	4 GB eMMC 4.5
Secure Element	Secure point to point authentication and data transfer
Trustware	Trusted execution environment
WLAN	IEEE 802.11a/b/g/n, dual-band SISO
Bluetooth	4.2 (BLE + Classic)
802.15.	Zigbee/Thread

Table 1. ARTIK 530s Module Main Features (Continued)

Feature	Description
Power Management	PMIC, integrated into the ARTIK module. Provides all power to the ARTIK 530s module.
Ethernet	10/100/1000Base-T MAC (external PHY required)
Analog and Digital I/O	GPIO, UART, I2C, SPI, USB host, USB OTG, HSIC, ADC, PWM, I2S, JTAG

ARTIK 530s Interposer Board Interfaces

The following subsections describe the various interfaces present on the ARTIK 530s Interposer board.

USB OTG

The Interposer board has one USB OTG connector located as can be seen in *Figure 4*. The USB OTG port can be used to program the module.

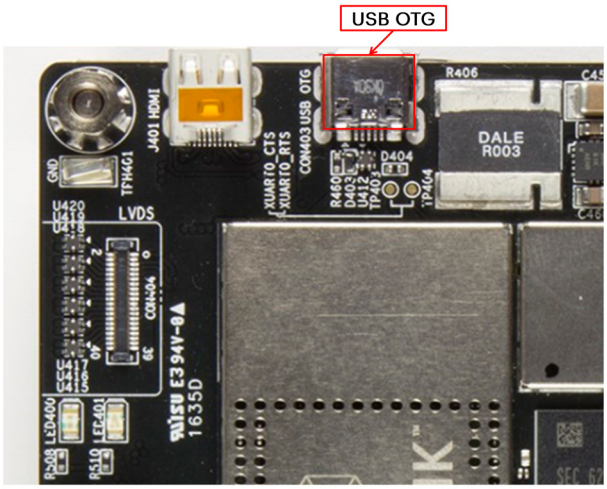

Figure 4. Location of USB OTG Port on the Interposer Board

HDMI

The Interposer board has one HDMI 1.4a connector (Micro D-Type) located as can be seen in *Figure 5*. The following video formats are supported:

- 480p/480i @59.94Hz/60Hz, 576p/576i@50Hz
- 720p/720i @50Hz/59.94Hz/60Hz
- 1080p/1080i @50Hz/59.94Hz/60Hz

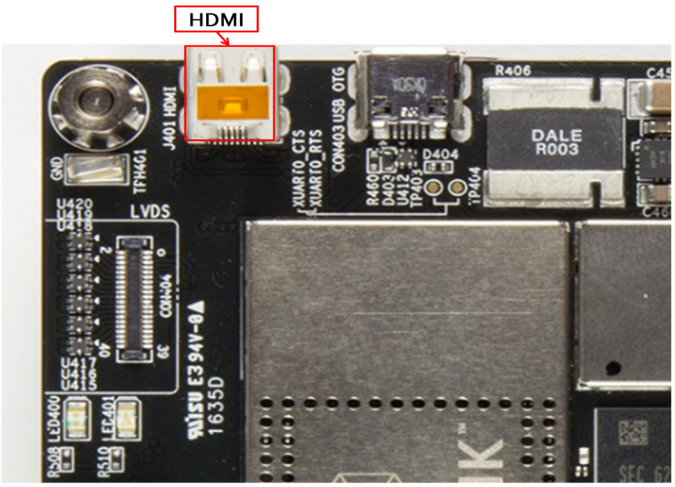

Figure 5. Location of HDMI Port on Interposer Board

LVDS

The Interposer board has one LVDS Interface containing 5x data channels and one clock channel, its location can be seen in ***Figure 6***. The available maximum resolution is 1920 x 1080 @ 60fps.

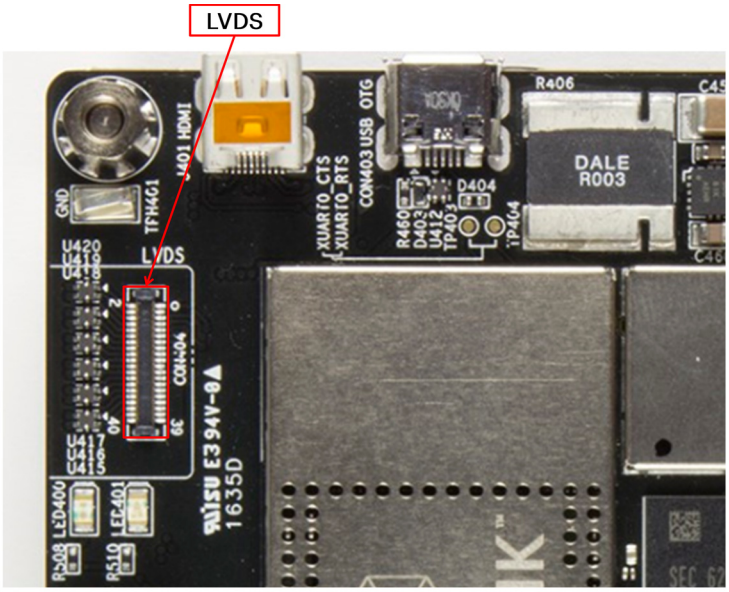

Figure 6. Location of LVDS Connection on the Interposer Board

Ethernet

The Interposer board has one Ethernet Interface, its location are shown in ***Figure 7***. The Ethernet interface is based on 802.3az-2010 and is compliant with the Energy Efficient Ethernet (EEE) standard. The maximum theoretical speed of the interface is 1000 Mbps.

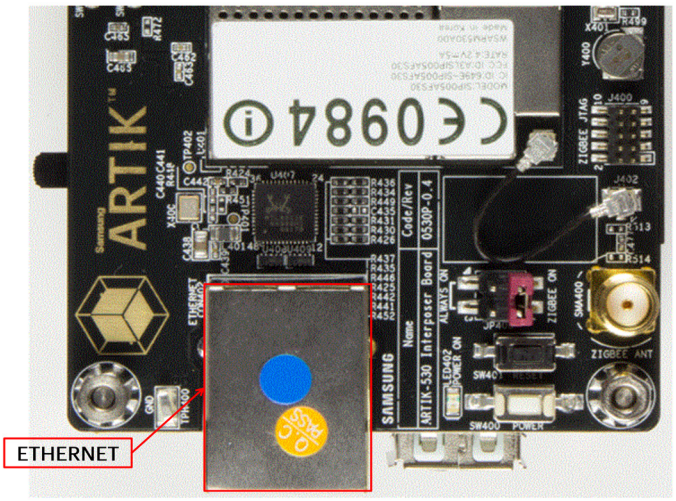

Figure 7. Location of Ethernet Port on the Interposer Board

Antennas

If 802.11, Bluetooth®, or Zigbee functionality is required, two antennas are included as part of the ARTIK 530s Development Kit. These antennas are attached to coaxial connectors on the Interposer board as shown in ***Table 2***. More details on the antenna specifications are shown in ***Figure 8***.

Table 2. Antenna Specifications

Property	Description
Antenna Type	Dipole antenna
Antenna Peak Gain	+1.43 (2.4GHz)/ +0.91 (5GHz)
Frequency	2.4GHz, 5GHz (for 802.11, Bluetooth®, ZigBee®)
Connector Type	SMA-M
Antenna Size	108.7 mm

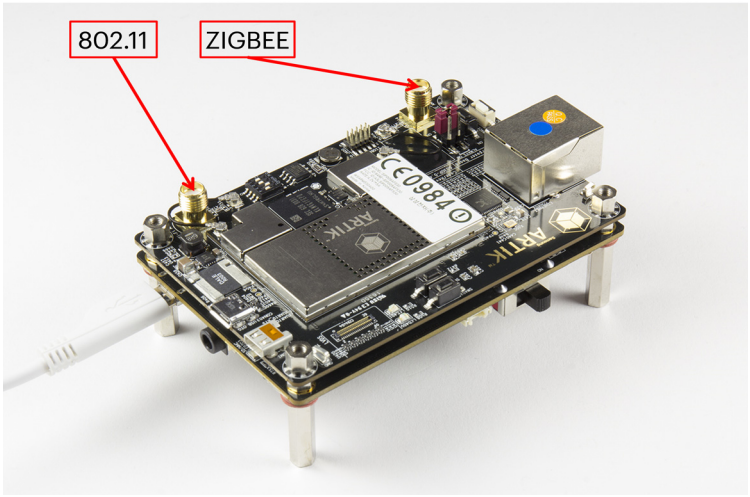

Figure 8. Location of Antennas on the Interposer Board

Zigbee JTAG

The Interposer board contains a dedicated Zigbee JTAG connector. This connector is used only for debug of the on-board Zigbee controller in case the Flashing of firmware to the controller is required. As such, this connector cannot be used for system debug.

Reset Pushbutton Switch

Reset of the ARTIK module is accomplished by depressing the RESET button located on the Interposer board. This button is located near the RJ45 Ethernet jack right next to the PWR_KEY button shown in *Figure 3*. The button is indicated as RESET on the silkscreen. When this button is depressed, the entire development platform is reset, except for the power controller (PMIC) on the ARTIK module, and all data is lost.

Power-Key Pushbutton Switch

The PWR_KEY pushbutton switch located on the Interposer board performs the following functions:

- System Power Up: Pressing and holding the PWR_KEY button until the red LED illuminates causes the system to power-up the board.
- System Power Down: Pressing and holding the PWR_KEY button until the red LED goes off causes the system to turn off.

The location of the PWR_KEY pushbutton switch is shown in *Figure 9*.

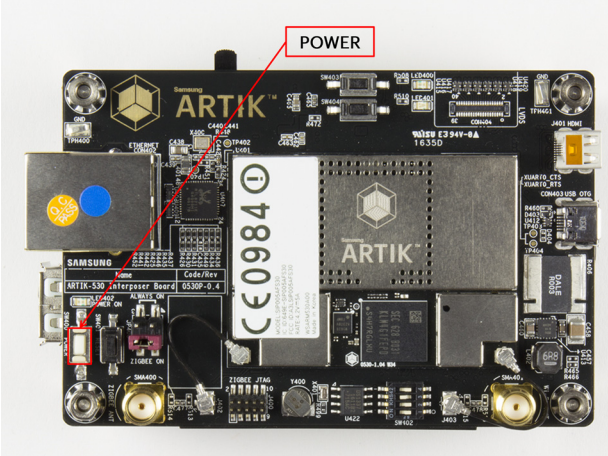

Figure 9. Location of PWR_KEY Pushbutton Switch on the Interposer Board

The Interposer board also contains a 4-pin jumper (JP400) that allows the system to boot automatically once power is applied, effectively bypassing the PWR_KEY button by grounding the AP_PWRKEY pin on the ARTIK module. This jumper is located right next to the Reset button as shown on the Interposer board in *Figure 9*. When pins 1 and 3 of this jumper are connected, the PWR_KEY LED turns on and boot-up commences once power is applied to the board. When this jumper is inserted, pressing and holding the PWR_KEY button as described above is not required. Note that pins 2 and 4 of this jumper are used for Zigbee JTAG and are not used for PWR_KEY purposes.

Boot Mode DIP Switches

The Interposer board contains 4 DIP switches that are used to configure the system to boot from on-module eMMC memory, SD card, or the USB OTG port. For more information, refer to the section entitled *ARTIK 530s Development Kit Boot Mode Configuration*.

Interposer to Platform Board Connectors

Two HIROSE connectors are used to transfer signals between the Interposer and Platform boards. One connector (CON700) contains 90 pins, and the second connector (CON701) contains 80 pins. The following tables show the relationship between the connector pinout and pin names, and the associated module pin names and numbers.

Table 3. CON400 HIROSE Connector to ARTIK Module Pin Mapping

Left Side of Connector (odd numbered pins)					Right Side of Connector (even numbered pins)			
Module Pin Name	Module Pin Number	HIROSE Connector Name	HIROSE Connector Pin #		HIROSE Connector Pin #	HIROSE Connector Name	Module Pin Number	Module Pin Name
N/A[a]	N/A	VDD_AP_IO_3P3	1		2	VDD_AP_IO_3P3	N/A	N/A
N/A	N/A	GND	3		4	GND	N/A	N/A
AP_MIPICSI1_DN3	PA14	XMIPICSI1_DN3	5		6	XCAM_LDO_EN	PAK42	AP_GPA6
AP_MIPICSI1_DP3	PB14	XMIPICSI1_DP3	7		8	XCAM_STBY_1.8V	PAL42	AP_GPA3
N/A	N/A	GND	9		10	XCAM_RESET	PAL41	AP_GPA17
AP_MIPICSI1_DN2	PA13	XMIPICSI1_DN2	11		12	XCAM_SCL_1.8V[b]	PAK10	AP_GPD2_SCL0
AP_MIPICSI1_DP2	PB13	XMIPICSI1_DP2	13		14	XCAM_SDA_1.8V	PAL10	AP_GPD2_SDA0
N/A	N/A	GND	15		16	GND	N/A	N/A
AP_MIPICSI1_DN1	PA12	XMIPICSI1_DN1	17		18	XSD0_CDN	PAK37	AP_GPB16
AP_MIPICSI1_DP1	PB12	XMIPICSI1_DP1	19		20	XSD0_D1	PAK29	AP_SD0_D1
N/A	N/A	GND	21		22	XSD0_D0	PAL30	AP_SD0_D0
AP_MIPICSI1_DN0	PA11	XMIPICSI1_DN0	23		24	XSD0_CLK	PAK30	AP_SD0_CLK
AP_MIPICSI1_DP0	PB11	XMIPICSI1_DP0	25		26	XSD0_CMD	PAK28	AP_SD0_CMD
N/A	N/A	GND	27		28	XSD0_D3	PAL28	AP_SD0_D3
AP_MIPICSI1_DNCLK	PA10	XMIPICSI1_DNCLK	29		30	XSD0_D2	PAKL9	AP_SD0_D2
AP_MIPICSI1_DPCLK	PB10	XMIPICSI1_DPCLK	31		32	GND	N/A	N/A
N/A	N/A	GND	33		34	XCHG_INT	PAK41	AP_GPA10
AP_UART_TX4	PAK23	XUART0_TX	35		36	XCHG_SCL	PAK38	AP_GPA20
AP_UART_RX4	PAL23	XUART0_RX	37		38	XCHG_SDA	PAL40	AP_GPA19
N/A	N/A	GND	39		40	GND	N/A	N/A
AP_UART_TX3	PAK22	XDEBUG_TXD	41		42	XFUEL_SCL	PA40	AP_GPA9
AP_UART_RX3	PAL22	XDEBUG_RXD	43		44	XFUEL_SDA	PA37	AP_GPA13
N/A	N/A	GND	45		46	XFUEL_INT	PAK19	AP_GPD28
AP_USBH_DP	PB36	XUHOST1_DP	47		48	GND	N/A	N/A
AP_USBH_DM	PA36	XUHOST1_DM	49		50	XSPI0_CS	PAL4	AP_GPC10_SPI2_CS
N/A	N/A	GND	51		52	XSPI0_CLK	PAK4	AP_GPC9_SPI2_CLK
N/A	N/A	XUHOST0_DP	53		54	XSPI0_MISO	PAK3	AP_GPC11_SPI2_MISO

Table 3. CON400 HIROSE Connector to ARTIK Module Pin Mapping (Continued)

Left Side of Connector (odd numbered pins)				Right Side of Connector (even numbered pins)			
Module Pin Name	Module Pin Number	HIROSE Connector Name	HIROSE Connector Pin #	HIROSE Connector Pin #	HIROSE Connector Name	Module Pin Number	Module Pin Name
N/A	N/A	XUHOST0_DM	55	56	XSPI0_MOSI	PAL3	AP_GPC12_SPI2_MOSI
N/A	N/A	GND	57	58	GND	N/A	N/A
AP_TMS	PAC2	XJTAG_TMS	59	60	XADC0	AP_ADC0	PY1
AP_TCK	PAC1	XJTAG_TCK	61	62	XADC1	AP_ADC1	PY2
AP_TDI	PAD2	XJTAG_TDI	63	64	XADC2	AP_ADC2	PAA1
AP_TDO	PAD1	XJTAG_TDO	65	66	XADC3	AP_ADC3	PAA2
AP_TNTRST	PAE1	XJTAG_RSTN	67	68	XADC4	AP_ADC4	PW1
N/A	N/A	GND	69	70	XADC5	AP_ADC5	PW2
AP_NRESET	PAG1	XRESET	71	72	GND	N/A	N/A
N/A	N/A	GND	73	74	XPWM0_OUT	PAK7	AP_GPC14_PWM2
VCC_3P3_SYS[4:1]	PAL18, 17 PAK18, 17	VSYS_IO_3P3	75	76	GND	N/A	N/A
N/A	N/A	GND	77	78	XI2C0_SCL	PAK9	AP_GPD4_SCL1
N/A	N/A	LCD2_ID	79	80	Xi2C0_SDA	PAL9	AP_GPD5_SDA1
N/A	N/A	N/C	81	82	GND	N/A	N/A
N/A	N/A	GND	83	84	GND	N/A	N/A
AP_GPA16	PB41	XUHOST_VBUSCTRL	85	86	GND	N/A	N/A
N/A	N/A	GND	87	88	GND	N/A	N/A
AP_GPB30	PP41	MICOM_INT	89	90	GND	N/A	N/A

a. N/A indicates that the connector pin does not connect to the ARTIK module.
b. All pins ending in '_1.8V' pass through level translators in the Interposer board before connecting to the ARTIK module.

Table 4. CON401 HIROSE Connector to ARTIK Module Pin Mapping

Left Side of Connector (odd numbered pins)				Right Side of Connector (even numbered pins)			
Module Pin Name	Module Pin Number	HIROSE Connector Name	HIROSE Connector Pin #	HIROSE Connector Pin #	HIROSE Connector Name	Module Pin Number	Module Pin Name
N/A[a]	N/A	GND	1	2	GND	N/A	N/A
AP_MIPIDSI1_DN3	PA20	XMIPIDSI1_DN3	3	4	XLCD_PMWOUT_1.8V[b]	PAL7	AP_GPD1_PWM0
AP_MIPIDSI1_DP3	PB20	XMIPIDSI1_DP3	5	6	XLCD_RESET_1.8V	PAL34	AP_GPE30
N/A	N/A	GND	7	8	XLCD_GPIO_1.8V	PAK34	AP_GPC0
AP_MIPIDSI1_DN2	PA19	XMIPIDSI1_DN2	9	10	GND	N/A	N/A
AP_MIPIDSI1_DP2	PB19	XMIPIDSI1_DP2	11	12	XTSP_SCL_1.8V	PAK8	AP_GPD6_SCL2
N/A	N/A	GND	13	14	XTSP_SDA_1.8V	PAL8	AP_GPD7_SDA2
AP_MIPIDSI1_DN1	PB17	XMIPIDSI1_DN1	15	16	XTSP_RESET_1.8V	PAH41	AP_GPC25
AP_MIPIDSI1_DP1	PB18	XMIPIDSI1_DP1	17	18	GND	N/A	N/A
N/A	N/A	GND	19	20	XLCD1_GPIO1_1.8V	PAH42	AP_GPE31
AP_MIPIDSI1_DN0	PA17	XMIPIDSI1_DN0	21	22	XTSP1_GPIO1_1.8V	PAL35	AP_GPC27

Table 4. CON401 HIROSE Connector to ARTIK Module Pin Mapping (Continued)

Left Side of Connector (odd numbered pins)				Right Side of Connector (even numbered pins)			
Module Pin Name	Module Pin Number	HIROSE Connector Name	HIROSE Connector Pin #	HIROSE Connector Pin #	HIROSE Connector Name	Module Pin Number	Module Pin Name
AP_MIPIDSI1_DP0	PB17	XMIPIDSI1_DP0	23	24	XTSP_INT_1.8V	PAL36	AP_GPB22
N/A	N/A	GND	25	26	GND	N/A	N/A
AP_MIPIDSI1_DNCLK	PA16	XMIPIDSI1_DNCLK	27	28	XAUDIO_SCL	PB39	AP_GPA4
AP_MIPIDSI1_DPCLK	PB16	XMIPIDSI1_DPCLK	29	30	XAUDIO_SDA	PB40	AP_GPA5
N/A	N/A	GND	31	32	XAUDIO_IRQ	PAL33	AP_GPD8
AP_GPE0	PAL21	XGPIO0	33	34	GND	N/A	N/A
AP_GPE1	PAK21	XGPIO1	35	36	XAUDIO_I2S0_CDCLK	PAL2	AP_I2S0_MCLK
AP_GPE2	PAK20	XGPIO2	37	38	XAUDIO_I2S0_LRCLK	PAJ1	AP_I2S0_LRCLK
AP_GPB14	PAK37	XGPIO3	39	40	XAUDIO_I2S0_SCLK	PAK2	AP_I2S0_BCLK
AP_GPA14	PA39	XGPIO4	41	42	XAUDIO_I2S0_DIN	PAL1	AP_I2S0_DIN
AP_GPB9_I2SDIN1	PAL26	XGPIO5	43	44	XAUDIO_I2S0_DOUT	PAK1	AP_I2S0_DOUT
AP_GPA25	PAG2	XGPIO6	45	46	GND	N/A	N/A
AP_GPA0	PAH2	XGPIO7	47	48	BT_PCM_LRCLK	PAJ42	BT_PCM_LRCLK
AP_GPA26	PAH1	XGPIO8	49	50	BT_PCM_CLK	PAJ39	BT_PCM_CLK
AP_GP27	PAJ2	XGPIO9	51	52	BT_PCM_DOUT	PAJ41	BT_PCM_D_OUT
AP_AGP1	PAF2	XAGPIO0	53	54	BT_PCM_DIN	PAJ40	BT_PCM_D_IN
N/A	N/A	GND	55	56	GND	N/A	N/A
AP_GPB11	PAG41	XMCU_SCL	57	58	GND	N/A	N/A
AP_GPB18	PAG42	XMCU_SDA	59	60	GND	N/A	N/A
N/A	N/A	GND	61	62	V_MAIN	PV42	VIN1[c]
VCC3P3_SYS[4:1]	PAL18, 17 PAK18, 17	VSYS_IO_3P3	63	64	V_MAIN	PV41	VIN2
N/A	N/A	VDD_EXT3P3_ALIVE	65	66	V_MAIN	PW42	VIN3
N/A	N/A	VDD_EXT3P3_ALIVE	67	68	V_MAIN	PW41	VIN4
N/A	N/A	VDD_EXT3P3	69	70	V_MAIN	PY42	VIN5
N/A	N/A	VDD_EXT3P3	71	72	V_MAIN	PY41	VIN6
N/A	N/A	VDD_EXT1P8_ALIVE	73	74	V_MAIN	PAA42	VIN7
N/A	N/A	VDD_EXT1P8_ALIVE	75	76	V_MAIN	PAA41	VIN8
N/A	N/A	VDD_EXT1P8	77	78	V_MAIN	PAB42	VIN9
N/A	N/A	VDD_EXT1P8	79	80	V_MAIN	PAB41	VIN10

a. N/A indicates that the particular connector pin does not connect to the ARTIK module.
b. All pins that end in '_1.8V' connect to the ARTIK module through level translators on the Interposer board.
c. All VIN[10:1] pins are connected together at the ARTIK module and are collectively called V_MAIN.

ARTIK 530s Development Kit Platform Board

The main components of the Platform board is shown in *Figure 10*.

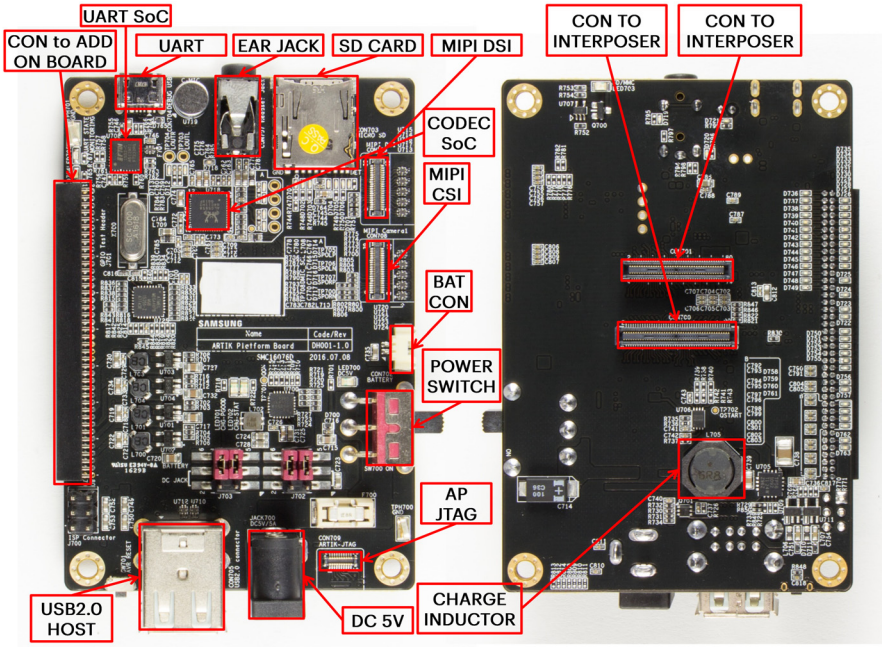

Figure 10. ARTIK 530s Development Kit Platform Board (Left - Bottom Side, Right - Top Side

SD Card Interface

The Platform board has one SD-CARD interface supporting SD3.0 located as shown in *Figure 11*.

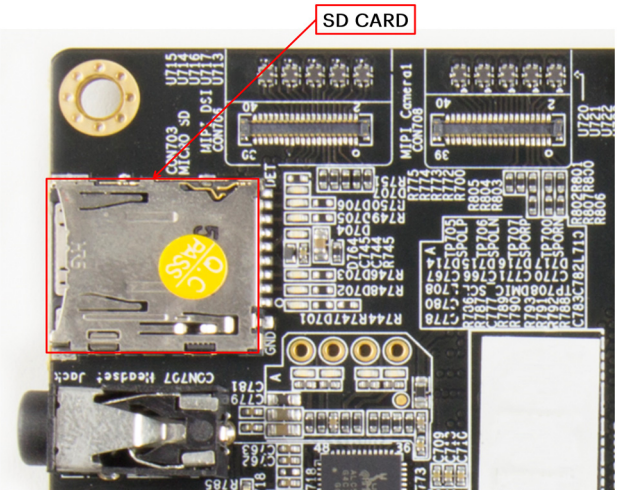

Figure 11. Location of SD Card Interface on the Platform Board

Audio Interface

The Platform board has one 4-pin audio jack interface supporting stereo audio as shown in *Figure 12*.

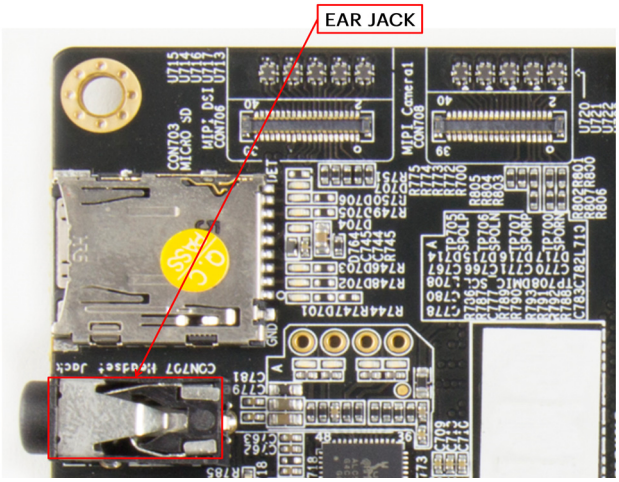

Figure 12. Location of the Audio Jack on the Platform Board

MIPI CSI/DSI Interface

The Platform board has one MIPI DSI and one MIPI CSI interface. The location of the DSI Display interface is shown in *Figure 13*. The location of the MIPI CSI interface is shown in *Figure 14*.

The MIPI DSI interface can operate at a maximum resolution of WUXGA (1920 x 1200), whereas the MIPI CSI interface can have a static resolution of 5M pixels or a dynamic resolution for video capturing of 1080P.

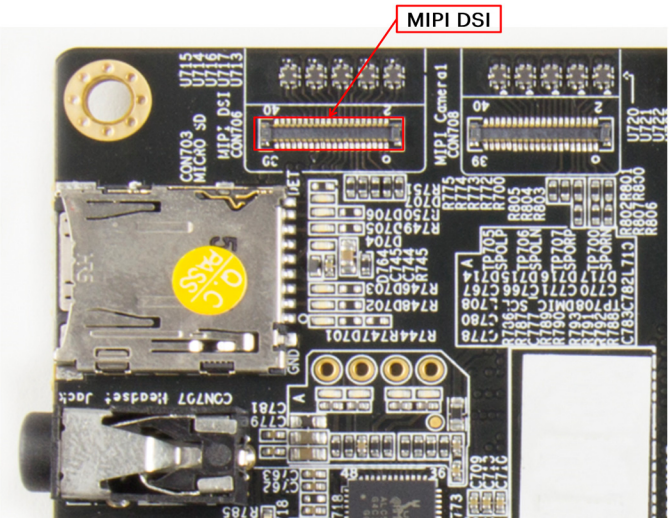

Figure 13. Location of MIPI DSI Connector on the Platform Board

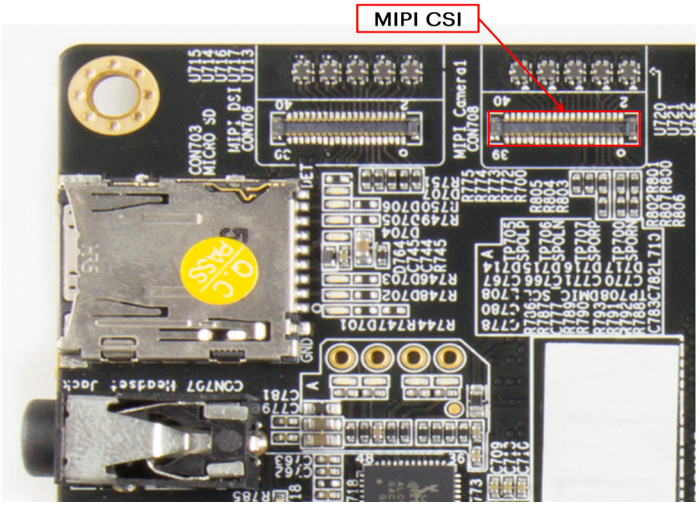

Figure 14. Location of MIPI CSI Connector on the Platform Board

USB Host 2.0 Interface

The Platform board has two USB 2.0 Interfaces. The location of these interfaces is shown in *Figure 15*.

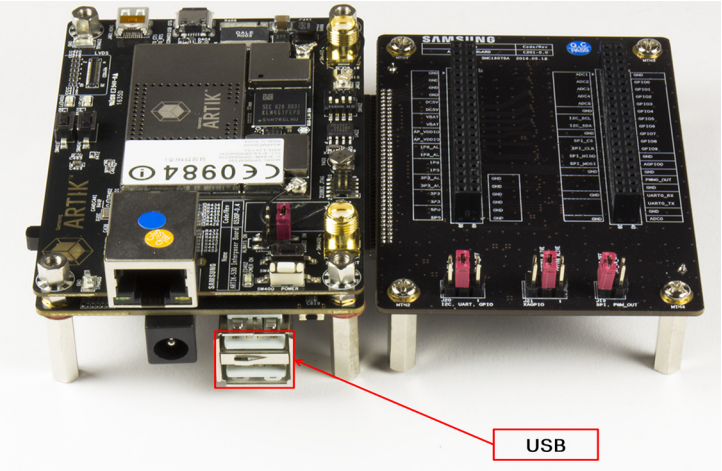

Figure 15. Location of the USB2.0 Interface Ports on the Platform Board

ARTIK JTAG

The Platform board contains a JTAG port for communication with an external JTAG debugger. This connector is located right next to the DC power jack.

Power Jack

The Platform board can receive power from the following two sources.

- 5V DC power jack
- Battery

The 5V DC jack is located next to the Ethernet connector as shown in *Figure 10*. The battery connector is located next to the power-on switch and can be connected as shown in *Figure 16*.

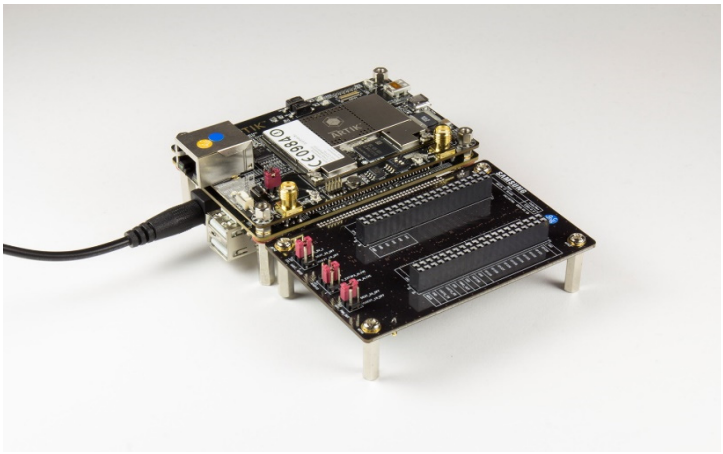

Figure 16. Location of the 5V DC Power Supply Jack on the Platform Board

Power Switch

The power switch is used to distribute power from either the DC jack or the battery to the rest of the ARTIK 530sdevelopment platform. When this switch is in the ON position, power is applied to the development platform, as well as the internal power controller (PMIC) on the ARTIK module. However, pressing and holding the PWR_KEY pushbutton switch is required to power up the ARTIK module. For more information, refer to the section entitled *Power-Key Pushbutton Switch*. *Figure 17* shows the location of the power switch on the Platform board.

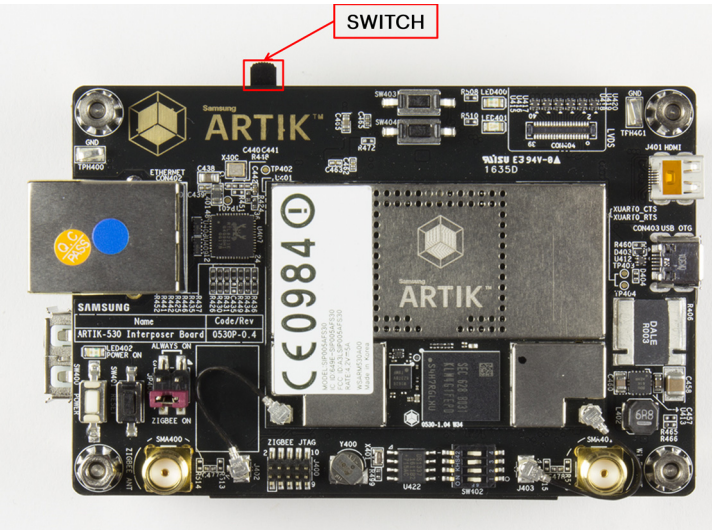

Figure 17. Location of Power Switch on the Platform Board

GPIO Test Header Interface to I/O Expander Board

The Platform board has one 80-pin dual-row expansion header that is used to connect to the I/O Expansion board. The pinout of this connector is shown in *Table 5*, along with a mapping to the ARTIK module pinout where applicable. The pin assignments are noted on the silkscreen of the Platform board. The odd-numbered pins are closest to the edge of the board.

Table 5. ARTIK 530s GPIO Expansion Header Pinout

ARTIK Module Pin Name	Module Pin Number	Header Pin Name	Header Pin Number	Header Pin Number	Header Pin Name	Module Pin Number	ARTIK Module Pin Name
N/A[a]	N/A	GND	1	2	MICOM_GPIO2[b]	N/A	N/A
AP_GPE0	PAL21	XGPIO0	3	4	MICOM_GPIO3	N/A	N/A
AP_GPE1	PAK21	XGPIO1	5	6	MICOM_GPIO4	N/A	N/A
AP_GPE2	PAK20	XGPIO2	7	8	MICOM_GPIO5	N/A	N/A
AP_GPB14	PAK37	XGPIO3	9	10	MICOM_GPIO6	N/A	N/A
AP_GPA14	PA39	XGPIO4	11	12	MICOM_GPIO7	N/A	N/A
AP_GPB9_I2SDIN1	PAL26	XGPIO5	13	14	MICOM_GPIO8	N/A	N/A
AP_GPA25	PAG2	XGPIO6	15	16	MICOM_GPIO9	N/A	N/A
AP_GPA0	PAH2	XGPIO7	17	18	MICOM_GPIO10	N/A	N/A
AP_GPA26	PAH1	XGPIO8	19	20	MICOM_GPIO11	N/A	N/A
AP_GPA27	PAJ2	XGPIO9	21	22	MICOM_GPIO12	N/A	N/A

Table 5. ARTIK 530s GPIO Expansion Header Pinout (Continued)

ARTIK Module Pin Name	Module Pin Number	Header Pin Name	Header Pin Number	Header Pin Number	Header Pin Name	Module Pin Number	ARTIK Module Pin Name
N/A	N/A	GND	23	24	MICOM_GPIO13	N/A	N/A
AP_AGP1	PAF2	XAGPIO0	25	26	MICOM_GPIO14	N/A	N/A
N/A	N/A	GND	27	28	MICOM_GPIO15	N/A	N/A
AP_GPC14_PWM2	PAK7	XPWM0_OUT	29	30	GND	N/A	N/A
N/A	N/A	GND	31	32	GND	N/A	N/A
AP_UART_RX4	PAL23	XUART0_RX	33	34	GND	N/A	N/A
AP_UART_TX4	PAK23	XUART0_TX	35	36	GND	N/A	N/A
N/A	N/A	GND	37	38	GND	N/A	N/A
AP_ADC0	PY1	XADC0	39	40	GND	N/A	N/A
AP_ADC1	PY2	XADC1	41	42	GND	N/A	N/A
AP_ADC2	PAA1	XADC2	43	44	GND	N/A	N/A
AP_ADC3	PAA2	XADC3	45	46	GND	N/A	N/A
AP_ADC4	PW1	XADC4	47	48	GND	N/A	N/A
AP_ADC5	PW2	XADC5	49	50	DC5V	N/A	N/A
N/A	N/A	GND	51	52	DC5V	N/A	N/A
AP_GPD4_SCL1	PAK9	XI2C0_SCL	53	54	VBAT_MAIN[c]	N/A	N/A
AP_GPD5_SDA1	PAL9	XI2C0_SDA	55	56	VBAT_MAIN	N/A	N/A
N/A	N/A	GND	57	58	AP_VDDIO	N/A	N/A
AP_GPC10_SPI2_CS	PAL6	XSPI0_CS	59	60	AP_VDDIO	N/A	N/A
AP_GPC9_SPI2_CLK	PAK4	XSPI0_CLK	61	62	VDD_EXT1P8_ALIVE	N/A	N/A
AP_GPC11_SPI2_MISO	PAK3	XSPI0_MISO	63	64	VDD_EXT1P8_ALIVE	N/A	N/A
AP_GPC10_SPI2_MOSI	PAL5	XSPI0_MOSI	65	66	VDD_EXT1P8	N/A	N/A
N/A	N/A	GND	67	68	VDD_EXT1P8	N/A	N/A
N/A	N/A	MICOM_GPIO0	69	70	VDD_EXT3P3_ALIVE	N/A	N/A
N/A	N/A	MICOM_GPIO1	71	72	VDD_EXT3P3_ALIVE	N/A	N/A
N/A	N/A	GND	73	74	VDD_EXT3P3	N/A	N/A
N/A	N/A	NC	75	76	VDD_EXT3P3	N/A	N/A
N/A	N/A	NC	77	78	VDD_EXT5P0_1	N/A	N/A
N/A	N/A	GND	79	80	VDD_EXT5P0_1	N/A	N/A

a. An N/A designation indicates that the pin in question does not originate from the ARTIK module.

b. All pins that start with 'MICOM_' originate from the AVR MICOM device located on the Platform board. See the Platform board schematics for more information.

c. All power pins (even pins 54 – 80) originate from DC/DC converter circuits on the Platform board. See the Platform board schematics for more information.

ARTIK 530s Development Kit I/O Expander Board

Figure 18 shows the highlights of the I/O Expander board. The I/O Expander board interfaces to the Platform board using the 80-pin GPIO test header located at connector J701 as described abopve. The I/O Expander board contains two additional 40-pin headers shown below that can be used to connect to external devices.

Table 6 and *Table 7* show the pinouts of the J2 and J3 connectors respectively. Note that for the J3 connector, no pins of this connector originate from the ARTIK module. Hence there is no connector pin to module pin mapping shown.

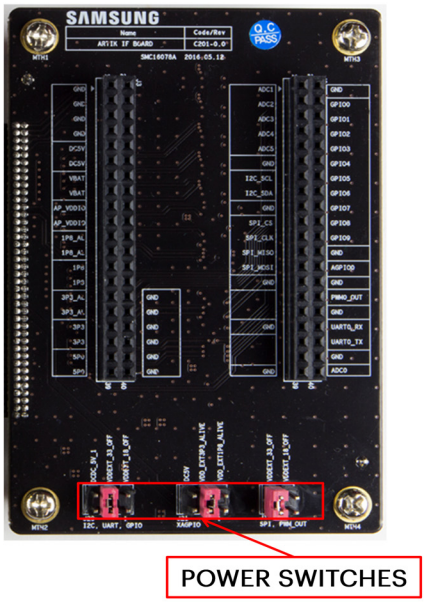

Figure 18. ARTIK 530s Development Kit I/O Expander Board

Table 6. I/O Expander Board J2 Connector Pinout

ARTIK Module Pin Name	Module Pin Number	Pin Name	Pin Number	Pin Number	Pin Name	Module Pin Number	ARTIK Module Pin Name
AP_ADC1	PY2	XADC1	1	2	GND	N/A	N/A
AP_ADC2	PAA1	XADC2	3	4	ADD_XGPIO0	PAL21	AP_GPE0
AP_ADC3	PAA2	XADC3	5	6	ADD_XGPIO1	PAK21	AP_GPE1
AP_ADC4	PW1	XADC4	7	8	ADD_XGPIO2	PAK20	AP_GPE2
AP_ADC5	PW2	XADC5	9	10	ADD_XGPIO3	PAK37	AP_GPB14
N/A	N/A	GND	11	12	ADD_XGPIO4	PA39	AP_GPA14
AP_GPD4_SCL1	PAK9	ADD_XI2C0_SCL	13	14	ADD_XGPIO5	PAL26	AP_GPB9_I2SDIN1
AP_GPD5_SDA1	PAL9	ADD_XI2C0_SDA	15	16	ADD_XGPIO6	PAG2	AP_GPA25
N/A	N/A	GND	17	18	ADD_XGPIO7	PAH2	AP_GPA0
AP_GPC10_SPI2_CS	PAL6	ADD_XSPI0_CS	19	20	ADD_XGPIO8	PAH1	AP_GPA26
AP_GPC9_SPI2_CLK	PAK4	ADD_XSPI0_CLK	21	22	ADD_XGPIO9	PAJ2	AP_GPA27
AP_GPC11_SPI2_MISO	PAK3	ADD_XSPI0_MISO	23	24	GND	N/A	N/A
AP_GPC10_SPI2_MOSI	PAL5	ADD_XSPI0_MOSI	25	26	ADD_XAGPIO0	PAF2	AP_AGP1
N/A	N/A	GND	27	28	GND	N/A	N/A
N/A	N/A	NC	29	30	ADD_XPWM0_OUT	PAK7	AP_GPC14_PWM2

Table 6. I/O Expander Board J2 Connector Pinout (Continued)

ARTIK Module Pin Name	Module Pin Number	Pin Name	Pin Number	Pin Number	Pin Name	Module Pin Number	ARTIK Module Pin Name
N/A	N/A	MICOM_GPIO1	31	32	GND	N/A	N/A
N/A	N/A	GND	33	34	ADD_XUART0_RX	PAL23	AP_UART_RX4
N/A	N/A	NC	35	36	ADD_XUART0_TX	PAK23	AP_UART_TX4
N/A	N/A	NC	37	38	GND	N/A	N/A
N/A	N/A	GND	39	40	XADC0	PY1	AP_ADC0

Table 7. I/O Expander Board J3 Connector

Pin Name	Pin Number	Pin Number	Pin Name
GND	1	2	MICOM_GPIO1
GND	3	4	MICOM_GPIO2
GND	5	6	MICOM_GPIO3
GND	7	8	MICOM_GPIO4
DC5V	9	10	MICOM_GPIO5
	11	12	MICOM_GPIO6
VBAT_MAIN	13	14	MICOM_GPIO7
	15	16	MICOM_GPIO8
AP_VDDIO	17	18	MICOM_GPIO9
	19	20	MICOM_GPIO10
VDD_EXT1P8_ALIVE	21	22	MICOM_GPIO11
	23	24	MICOM_GPIO12
VDD_EXT1P8	25	26	MICOM_GPIO13
	27	28	MICOM_GPIO14
VDD_EXT3P3_ALIVE	29	30	GND
	31	32	GND
VDD_EXT3P3	33	34	GND
	35	36	GND
VDD_EXT5P0_1	37	38	GND
	39	40	GND

I/O Expander Board Power Source

Jumpers J20 and J21 are used to select the I/O power source (I^2C, UART GPIO) or XGPIO of either, 1.8V, 3.3V or 5V. *Table 8* shows how to set the various jumpers to switch between power sources.

Table 8. Configuration of Power Jumpers J20 and J21

Interface	Power Source	Jumper Placement
I2C, UART, GPIO	DCDC_5V_1	Place Jumper J20 on pins 1 - 2
	VDDEXT_33_OFF (default)	Place Jumper J20 on pins 3 - 4
	VDDEXT_18_OFF	Place Jumper J20 on pins 5 - 6
XGPIO	DC5V	Place Jumper J21 on pins 1 - 2
	VDD_EXT3P3_ALIVE (default)	Place Jumper J21 on pins 3 - 4
	VDD_EXT1P8_ALIVE	Place Jumper J21 on pins 5 - 6

The jumpers are located on the I/O Expander board as shown in *Figure 18*.

ARTIK 530s Configuration

This section discusses some of the configuration options of the ARTIK 530s development platform.

Selecting the Development Kit Power Source

The power source is selected using jumpers JP1 - JP4, located on J702 and J703 of the Platform board. When power is provided from a DC-5V Adapter OR a Battery, all jumpers are in the 1-2 position. When power is provided from the DC-5V Adapter and at the same time a battery is connected that is being charged (Battery Charging Mode), all jumpers are in the 2-3 position.

When the jumpers JP1 - JP4 are in the 1-2 position, either a battery OR the DC-5V adapter can be connected, but NEVER both at the same time. When the jumpers JP1-JP4 are in the 2-3 position, (Battery Charging Mode) both a battery and the DC-5V Adapter can be connected at the same time.

Figure 19 shows the default settings and how to switch between the settings. When the ARTIK 530s Development Board is used with an external power adapter make certain that you use a 5V, 5A adapter with a 2.1 x 5.5mm plug.

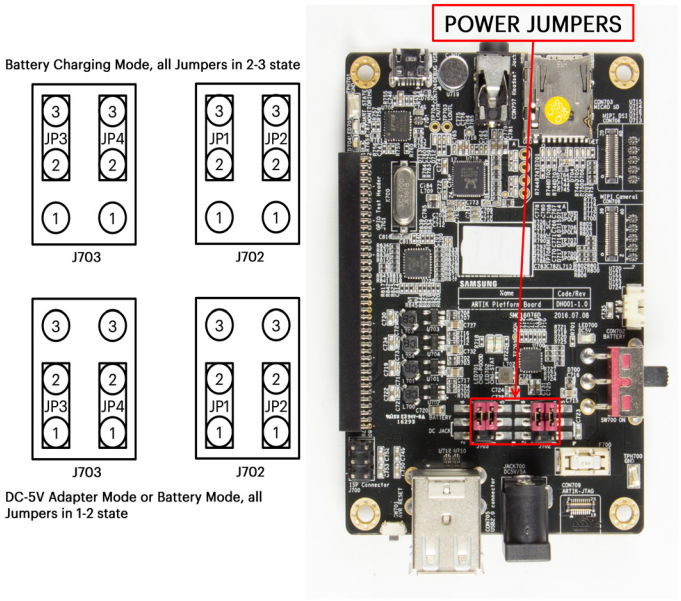

Figure 19. Location of Jumpers JP1 - JP4 on the Platform Board

ARTIK 530s Development Kit Boot Mode Configuration

The ARTIK 530s Interposer board contains a 4-position DIP switch that is used to select the boot source. The location of this switch is shown in *Figure 20*.

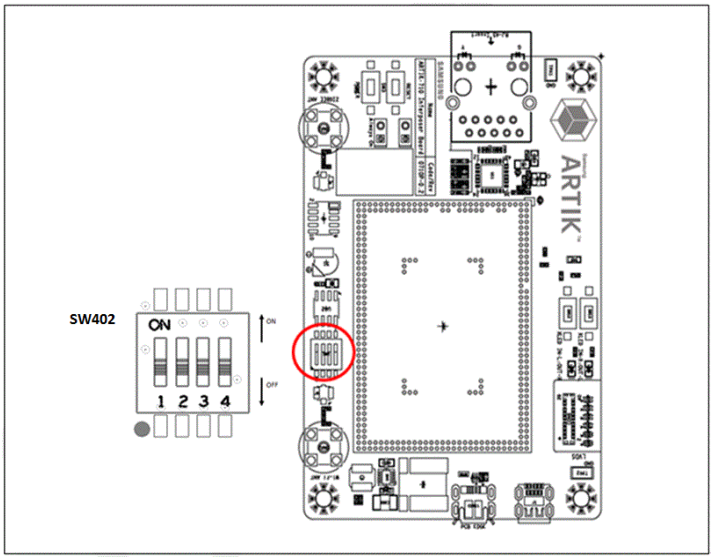

Figure 20. Location of Boot Configuration DIP Switches on the Interposer Board

The ARTIK 530s development platform provides numerous boot-up options for configuring the device. Boot devices include a 4-GByte eMMC Flash memory device located inside the ARTIK module, as well as the microSD and USB OTG connectors for external boot.

On initial power-up of the ARTIK platform, the eMMC memory may or may not have the latest version of the software and hence may require an update. If an update is required, this can be accomplished by first loading the image through either the microSD or USB OTG interfaces. The 4-position DIP switch described above is used to set the boot priorities.

Table 9 shows the various boot options.

Table 9. Setting the Boot Priority Switches

SW402	eMMC Boot	SD Card Boot	USB OTG Boot
1	OFF	OFF	ON
2	OFF	OFF	ON
3	X	X	X
4	OFF	ON	X

When power is applied, the board attempts to boot from one of three primary boot options as shown in the table above depending on the DIP switch settings. If that option is not available, it will try and boot from the next option. This concept is shown in the table below.