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Email & Skype: info@chipsmall.com Web: www.chipsmall.com
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SAMSUNG

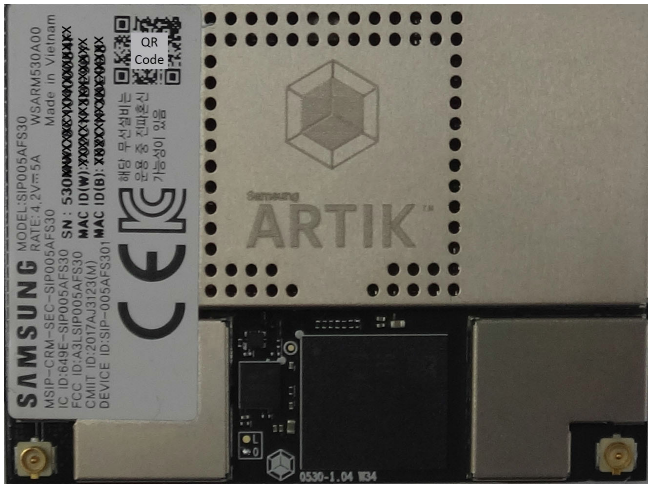
ARTIK™ Modules

5

ARTIK 530/530s Module Datasheet

1 Module Overview

ARTIK 530



The Samsung ARTIK™ 530/530s Module is a highly-integrated System-in-Module that combines a quad-core ARM® Cortex®-A9 processor packaged with 512MB or 1GB DRAM and Flash memory, a Security Subsystem, and a wide range of wireless communication options—such as 802.11a/b/g/n for Wi-Fi®, Bluetooth® 4.2 (BLE+Classic), and 802.15.4 for Zigbee—all into one 49×36mm footprint. The many standard digital control interfaces support external sensors and higher performance peripherals to expand the module's capabilities. With the combination of 802.11, Bluetooth, and 802.15.4, the ARTIK 530/530s Module is the perfect choice for home automation and home hub devices, while also supporting a rich UI/UX capability for camera and display requirements. The inclusion of a hardware-based Secure Element provides end-to-end security.

ARTIK 530s and ARTIK 530s 1G

Figure 1. ARTIK™ 530/530s Module Top View

Processor	
CPU	Quad-core ARM® Cortex®-A9@1.2GHz
GPU	3D graphics accelerator
Media	
Camera I/F	4-lane MIPI CSI up to 5M (1920x1080@30fps)
Display	4-lane MIPI DSI and HDMI1.4a (1920x1080p@60fps) or LVDS (1280×720p@60fps)
Audio	Two I^2S audio interfaces
Memory	
DRAM	512MB or 1GB DDR3 @ 800MHz
FLASH	4GB eMMC v4.5
Security	
Secure Element	Secure point-to-point authentication and data transfer
Trusted Execution Environment	Trustware
Radio	
WLAN	IEEE 802.11a/b/g/n, dual-band SISO
Bluetooth	4.2 (Classic+BLE)
LR_WPAN	IEEE 802.15.4
Power Management	
PMIC	Provides all power of the ARTIK 530/530s Module using onboard bucks and LDOs
Interfaces	
Ethernet	10/100/1000Base-T MAC (External PHY required)
Analog and Digital I/O	GPIO, UART, I^2C, SPI, SDIO, USB OTG, USB Host/HSIC, ADC, PWM, I^2S, JTAG

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2 Version History

Revision	Date	Description
V1.0	January 20, 2017	First release.
V1.01	February 07, 2017	Updated Module PAD's section. Updated look and feel.
V1.02	April 12, 2017	Updated default behavior of GPIO pins to latest software release. Updated Booting Sequence section. 802.15.4 RF Specifications section. Updated Tables 1–36. Updated SD/MMC AC Electrical Characteristics section. Updated Recommended Operating Conditions section. Updated ESD section. Updated Power management section.
V1.03	November 20, 2017	In *Table 1*, definition of PU/PD and I/O columns for ballout and signal-description tables more explicitly defined. Characteristics for LDO3 (VCC3P3_SYS) removed, as using the output to drive external ICs is highly discouraged. Descriptions of other LDOs was removed, as they are not available externally. In *Functional Interfaces*, each subsection describing an interface that has alternate functions clarifies which are selected by hardware at power-on reset. Cross references added to the appropriate tables in *GPIO Alternate Functions*. Changed format of default functions in tables of *GPIO Alternate Functions* to make it easier to see which function number is the default. *Booting Selection* section rewritten for clarity. Power Sequence section divided into *Power Sequence* and *Power States*. Simplified power management state diagram, *Figure 5*. *Power/Current Consumption* section added.
V1.04	November 30,2017	Added ARTIK 530s and ARTIK 530s 1G features in *Module Overview*, *Block Diagram and Module Features*, and *Security Subsystem*. Caution after block diagram in *Block Diagram and Module Features* about not applying power before connecting antennas was deemed unnecessary and removed.
V1.05	November 30,2017	*Ordering Information*: Added ordering part numbers for ARTIK 530s 1G and its associated development kit.
V1.06	December 20, 2017	USB HOST/USB OTG: Changed function description of AP_OTG_ID signal. HSIC: Changed function descriptions for balls PAK12–14 and PAL12–14. *Mechanical Specifications*: Changed ball names in *Figure 13* and *Table 60* to correlate with ball organization shown in *Figure 3*. Note that the changes address a labeling consistency issue only; no electrical or layout changes are required.
V1.07	February 2, 2018	*CE*: Radio Equipment Directive (RED) certification update.
V1.08	April 5, 2018	*I^2C*: Removed support for slave mode. *Table 3*, *Table 9*: Marked pad PAL15 for internal use only. *Table 30*: Removed pad PAL15 from GPIO function table because it is reserved for internal use. Added *Temperature Thresholds for Operating Frequency Throttling* under new section *Thermal and Environmental Specifications*.
V1.09	May 29, 2018	*Figure 2*: Changed functional blocks for USB and HSIC. Changed *HSIC* to be a subheading to *USB HOST* to reflect hardware hierarchy. In *Functional Interfaces*, split USB OTG from USB Host and combined USB Host with HSIC. *Table 60*: Corrected X-locations of center pads. *Recommended Operating ConditionsRecommended Operating Conditions*: Added footnote about reduced retention time for Flash stored for an extended period of time at temperatures about 30°C. *Legal Information*: Clarified policy regarding third-party registered trademarks. General: Changed headings to a numbered format.
V1.10	June 25, 2018	*Figure 3*: Missing ball column 20 inserted..

3 Block Diagram and Module Features

Figure 2 shows the functional block diagram of the ARTIK 530/530s Module. It consists of a quad-core ARM® Cortex®-A9 application processor with 512MB or 1GB of DDR3 and 4GB eMMC Flash, PMIC power management, Security Subsystem, 802.11 for Wi-Fi®, Bluetooth®, 802.15.4 for Zigbee, and RF connectors.

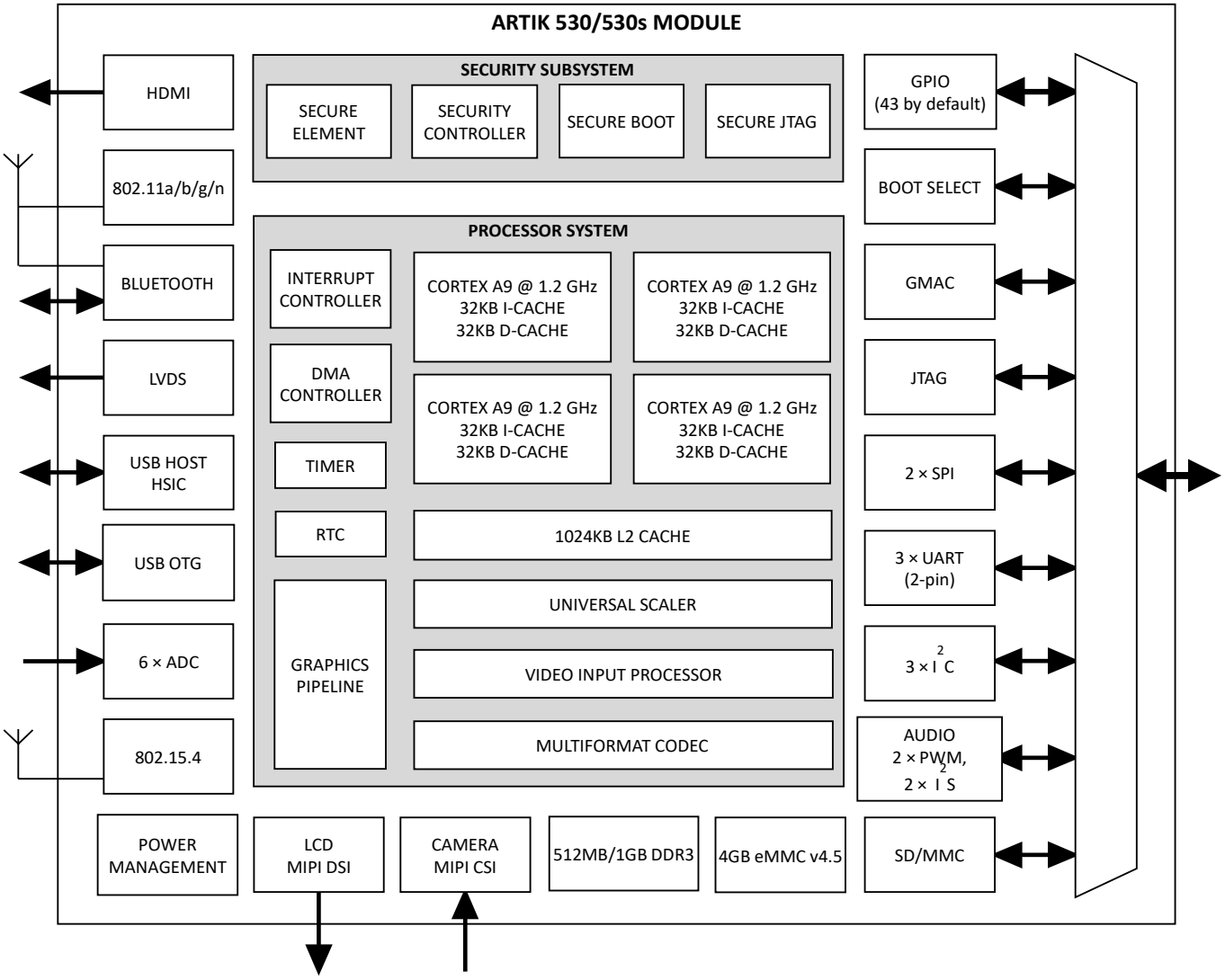

Figure 2. ARTIK 530/530s Module Functional Block Diagram

3.1 ARTIK 530/530s Module Features

The following subsections describe the functions of the various ARTIK 530/530s Module blocks depicted in *Figure 2*.

3.1.1 Quad-Core Processor System

The processor system architecture that resides on the ARTIK 530/530s Module is a system-on-a-chip (SoC) based on a 32-bit RISC architecture. Designed using the 28nm low power process, the processor system architecture provides superior performance using a quad-core CPU. The key features of the ARTIK 530/530s Module are

- Quad-core ARM® Cortex®-A9, 32-bit RISC architecture
- Maximum core speed 1.2GHz
- 32KB I-Cache per core
- 32KB D-Cache per core
- 1024KB L2-Cache shared between four cores
- Support for dynamic virtual-address mapping

3.1.2 Memory Controller

The ARTIK 530/530s Module has one DDR3 memory interface. The key features are

- One 32-bit DDR3 memory interface
- Two 256MB or two 512MB DDR3 16-bit memory chips, for a total of 512MB or 1GB
- Up to 800MHz DDR3 speed with a maximum throughput of 6.4GB/s

3.1.3 Power Management

The ARTIK 530/530s Module power requirements are managed using a power management integrated circuit (PMIC). This PMIC device has four fully-integrated fixed-frequency current-mode synchronous PWM step-down converters that can achieve peak efficiencies of up to 97%.The regulators operate at a fixed high frequency, minimizing noise in sensitive applications and allowing the use of small form factor components. These four regulators fully satisfy the power and control requirements of the ARTIK 530/530s Module. Dynamic Voltage Scaling (DVS) of the various core voltages is supported using I^2C control.

3.1.4 Wi-Fi

The ARTIK 530/530s Module has a fully integrated WLAN block covering IEEE 802.11 a/b/g/n. The most important hardware features of the module are

- 802.11 a/b/g/n dual-band SISO that is 2.4GHz/5GHz-compliant
- 1T1R 2.4GHz/5GHz band
- Support for 20MHzand 40MHz bandwidth (72.2/150Mbps PHY rate)
- Enhanced 802.11/Bluetooth coexistence control to improve transmission quality in different profiles
- Use of an SDIO interface

3.1.5 Bluetooth®

The ARTIK 530/530s Module has a fully integrated 4.2 block (BLE+Classic). The most important hardware features of the module are

- Bluetooth 4.2 (BLE+Classic)
- Enhanced 802.11/Bluetooth Coexistence control to improve transmission quality in different profiles

3.1.6 802.15.4 for Zigbee

The ARTIK 530/530s Module carries fully-integrated 802.15.4 functionality. The most important hardware features are

- Fully integrated 2.4 GHz, IEEE 802.15.4-compliant transceiver
- Complete system-on-chip using 32-bit ARM® Cortex®-M4 processor
- Flash and RAM memory and peripherals.
- Extremely low power consumption.
- Excellent RF performance.

3.1.7 USB OTG

The ARTIK 530/530s Module provides one USB 2.0 OTG interface supporting both device and host functionality. The key features of the USB 2.0 OTG sub-system are

- Compliant with the USB 2.0 on-the-go specification revision 1.3a and 2.0
- High-speed (480Mbps) mode
- Full-speed (12Mbps) mode
- Low-speed (1.5Mbps) mode (host only)
- Support for session request protocol (SRP) and host negotiation protocol (HNP)
- One control endpoint 0 for control transfer
- Up to 15 device-programmable endpoints:
  - Programmable endpoint type: Bulk, Isochronous, Interrupt
  - Programmable In/Out direction
- 16 host channels

3.1.8 USB HOST

The ARTIK 530/530s Module provides one USB 2.0 controller that is fully compliant with the USB 2.0 Host specifications, and the enhanced host controller Interface (EHCI) specification. The key features of the USB 2.0 Host sub-system are

- Detecting the attachment and removal of USB devices
- Collecting status and activity statistics
- Controlling power supply to attached USB devices

- In compliance with the UTMI+ Level 3 revision 1.0
- Controlling the association to either the open host controller interface (OHCI) or the EHCI via a port router
- Root Hub functionality to support upstream/downstream port

3.1.8.1 HSIC

The ARTIK 530/530s Module provides one high-speed inter-chip (HSIC) version 1.0 module, controlled by the USB Host Controller. The key features of the HSIC sub-system are

- Support for ping and split transactions
- Up to 30MHz operation for a 16-bit interface
- Up to 60MHz operation for a 8-bit interface
- Support for HSIC version 1.0

3.1.9 Gigabit EMAC

The ARTIK 530/530s Module provides one Gigabit EMAC interface. The most important features of the Ethernet MAC module are

- Standard compliance
  - IEEE 802.3az-2010: energy efficient Ethernet (EEE)
  - RGMII v2.6
- MAC supports the following features:
  - 10/100/1000 Mbps data transfer rates with an RGMII interface to communicate with external Gigabit PHY
  - Full duplex operation
  - Half duplex operation
  - Flexible address filtering
  - Additional frame filtering

3.1.10 SD/MMC

The ARTIK 530/530s Module provides one SD/MMC interface. The Mobile Storage Host is an interface between the system and the SD/MMC. The key features of mobile storage host sub-system are as follows:

3.1.10.1 SD

- Support for Secure Digital I/O (SDIO – version 3.0)
- Support for Secure Digital Memory (SDMEM – version 3.0)
- Consumer Electronics Advanced Transport Architecture (CE-ATA-version 1.1)
- Support 4-bit SDR mode up to 50MHz
- Support for PIO and DMA mode data transfer
- Support for 4- bit data bus width

3.1.10.2 MMC

- Support for Multimedia Cards (MMC – version 4.41)
- Support for Embedded Multimedia Cards (eMMC – version 4.5)
- Support for 4-bit SDR mode up to 50MHz
- Support for PIO and DMA mode data transfer
- Support for 4- bit data bus width

3.1.11 PCM

The ARTIK 530/530s Module provides one PCM channel. The PCM interface provides a bi-directional serial interface that can be connected to an external audio . The key features of the PCM subsystem are

- Supports both Master and Slave mode external audio codecs
- Supports both short and long frame synchronization
- Supports a variety of data formats with a default format of 13-bit 2's complement, left justified, clock MSB first

3.1.12 MIPI CSI

The ARTIK 530/530s Module provides one 4-lane mobile industry processor interface (MIPI) interface that complies with the MIPI camera serial interface (CSI) standard specification V1.01r06 and D-PHY standard specification v1.0. The key features of the MIPI CSI sub-system are

- 1, 2, 3 or 4 data lanes
- Support for the following image formats:
  - YUV420, YUV420 (Legacy), YUV420 (CSPS), 8-bit YUV422, 10-bit YUV422
  - User-defined byte-based data packet
  - Compatible to PPI (Protocol to PHY interface)

3.1.13 MIPI DSI

The ARTIK 530/530s Module provides one 4-lane MIPI interface that complies with the MIPI DSI standard specification V1.01r11. The key features of the MIPI DSI sub-system are

- Maximum resolution ranges up to WUXGA 1920 × 1200
- Supports 1, 2, 3 or 4 data lanes
- Supports pixel format:
  - 16bpp, 18bpp packed, 18bpp loosely packed (3 byte), 24bpp
- Supported interfaces are
  - Protocol-to-PHY Interface (PPI) up to 1.5Gbps, in MIPI D-PHY
  - RGB Interface for video image input from display controller
  - PMS control interface for PLL to configure byte clock frequency
  - Prescaler to generate escape clock from byte clock

3.1.14 HDMI

The ARTIK 530/530s Module provides one HDMI v1.4a interface. The key features of the HDMI sub-system are

- Support for v1.4a spec
- Up to 1080p video resolution
- HDMI Link + HDMI PHY
- Support for the following video formats:
  - 480p@59.94/60Hz
  - 576p@50Hz
  - 720p@50/59.94/60Hz
  - 1080p@50/59.94/60Hz (No support for interlaced format)
- Support for 4:4:4 RGB
- Support for up to 8-bits per color

3.1.15 LVDS

The ARTIK 530/530s Module provides five low voltage differential signaling (LVDS) output channels with one clock channel. The key features of the LVDS channel system are

- Output clock range 30–125MHz
- Support for 630 Mbps per channel
- Up to 393.75MB/s data transport
- Support for power down mode

3.1.16 Video Input Processor

The ARTIK 530/530s Module provides one video input processor (VIP). The key features of the VIP sub-system are

- Support for external 8-bit and 16-bit MIPI
- Support for internal MIPI-CSI
- Support for images up to 8192×8192
- Support for clipping and scale-down
- Support for YUV420 memory format

3.1.17 Scaler

The ARTIK 530/530s Module provides one universal scaler. The key features of the scaler are

- Support for different input formats:
  - YUV420, YUV422, YUV444
- Flexible size, from 8×8 up to 1920×1080 with a granularity of 8
- Upscale ratio from 8×8 to 1920×1080
- Downscale ratio from 1920×1080 to 8×8

- Low pass filter available after upscale or before downscale
- Horizontal 5-tab filter with 64 sets of coefficients
- Vertical 3-tab filter with 32 sets of coefficients

3.1.18 Multiformat Codec

The ARTIK 530/530s Module provides one integrated Multiformat Codec (MFC) module. The key features of the MFC sub-system are

- Decoder:
  - H.264 : BP, MP, HP Level 4.2 up to 1920×1080, up to 50MBps
  - MPEG4 : Advanced Simple Profile (ASP) up to 1920×1080, at up to 40Mbps
  - H.263 : Profile 3 up to 1920×1080, up to 20Mbps
  - MPEG 1,2 : Main Profile, High Level up to 1920×1080, up to 80MBps
- Encoder:
  - H.264 : Baseline profile, Level 4.0 up to 1080p, up to 20Mbps
  - MPEG4 : Simple profile, Level 5.6 up to 1080p, up to 20Mbps
  - H.263 : Profile 3, Level 70 up to 1080p, up to 20Mbps

3.1.19 Graphics Pipeline

The ARTIK 530/530s Module provides one 2D and 3D graphics pipeline module. The key features of the graphics pipeline are

- Two pixel processors:
  - Tile oriented processing
  - Alpha blending
  - Texture support, non-power-of-2
  - Cube mapping
  - Fast dynamic branching
  - Trigonometric acceleration
  - Full floating-point arithmetic
  - Line, quad, triangle and point sprites
  - Perspective correct texturing
  - Point sampling, bilinear and trilinear filtering
  - 8-bit stencil buffering
  - 4-level hierarchical Z and stencil operation
- Geometry processor:
  - Programmable vertex shader
  - Flexible input and output formats
  - Autonomous operation tile list generation
  - Indexed and non-indexed geometry input
  - Primitive constructions with points, lines, triangles and quads

- Support for OpenGL ES 1.0 and 2.0

3.1.20 ADC

The ADC interface controls one 28nm low-power CMOS 1.8V 12-bit ADC. The key features of the ADC sub-system are

- Up to six channels of analog input can be selected
- Conversion of analog input into 12-bit binary code up to 1 Mega Sample Per Second (MSPS)
- 1.0mW power consumption when running 1MSPS
- Input frequency up to 100kHz

3.1.21 GPIO

The ARTIK 530/530s Module provides a GPIO system with up to 107 GPIOs multiplexed with other I/O interface lines, as shown in *Figure 2* to support a wide variety of use-cases. The key features of the GPIO system are as follows:

- Both edge detect and level detect functionality
- Support for programmable pull-up/pull-down resistors
- Support for fast or normal slew operation
- Drive strength can be set from a register:

Value	Drive Strength *
0	2.6mA approximately (default)
1	5.2mA approximately
2	10.4mA approximately
3	15.6mA approximately

*. Assumes the reference I/O voltage is 3.3V. All drive-strength values are approximate. This value represents the current drive capability of GPIO pad only. Do not use GPIO as a current source.

- Support for interrupt generation that can be triggered on one of the following:
  - Rising edge
  - Falling edge
  - High level detection
  - Low level detection
- The I/O data is clocked up to 50MHz

3.1.22 I^2S

The ARTIK 530/530s Module provides two 5-line Inter-IC Sound (I^2S) channels. I^2S is one of the most popular digital audio interfaces. The I^2S bus handles audio data and other signals, such as subcoding and control. It is possible to transmit data between two I^2S buses. The key features of the I^2S sub-system are

- One-port stereo (1 channel) I^2S-bus for audio with DMA based operation
- Serial data transfer of 16/24 bits per channel in Master and Slave mode
- A variety of interface modes:
  - I^2S, Left justified, Right justified, DSP mode

3.1.23 Timer

The ARTIK 530/530s Module has four dedicated timer channels. The most important features of the Timer module are

- Timer or watchdog timer modes
- Four dedicated Timer channels with watchdog timer
- Normal interval timer mode with interrupt request
- Reset on timer countdown
- Level-triggered interrupt mechanism

3.1.23.1 PWM

The ARTIK 530/530s Module provides two pulse width modulation (PWM) instances with the following key features:

- Two individual PWM channels with independent duty control and polarity
- Two 32-bit PWM timers, one per channel
- Support for static as well as dynamic setup
- Support for auto-reload and one-shot pulse mode
- Dead zone generator
- Level interrupt generation

3.1.24 SPI

The ARTIK 530/530s Module provides two Serial Peripheral Interface (SPI) portsthat transfer serial data. SPI support includes 8-bit/16-bit shift registers to transmit and receive data. During an SPI transfer, data is simultaneously transmitted (shifted out serially) and received (shifted in serially). The SPI implementation adheres to the protocols described by Texas Instruments Synchronous Serial Interface, National Semiconductor's Microwire, and Motorola's Serial Peripheral Interface. The key features of the SPI sub-system are

- Support for full-duplex
- 8-bit/16-bit shift register for Tx and Rx
- Compliant with the SPI protocol described by Texas Instruments, National Semiconductor and Motorola
- Support for independent 16-bit wide transmit and receive FIFOs 8 locations deep

- Support for master mode and slave mode
- Support for receive-without-transmit operation
- Max operating frequency :
  - Master Mode : Supports Tx up to 50MHz, Rx up to 20MHz
  - Slave Mode : Supports Tx up to 8MHz, Rx up to 8MHz

3.1.25 UART

The ARTIK 530/530s Module provides three 2-pin universal asynchronous receiver transmitters (UARTs). The key features of the UART sub-system are

- Separate 64×8 Tx and 64×8 Rx FIFO memory buffers
- Support for DMA-mode and interrupt-based mode of operation
- All independent channels support IrDA 1.0
- Each UART channel contains:
  - Programmable baud-rates
  - 1 or 2 stop bit insertion
  - 5-bit, 6-bit, 7-bit, or 8-bit data width
  - Parity checking

3.1.26 I^2C

The ARTIK 530/530s Module provides three generic I^2C blocks supporting both 100kb/s and 400kb/s speed modes. The key features of the I^2C sub-system are

- Support for multi-master mode
- 7-bit addressing mode only
- Serial, 8-bit oriented and bi-directional data transfer
- Up to 100 kb/s in the standard mode
- Up to 400 kb/s in the fast mode
- Support for both interrupt and polling events

3.1.27 JTAG

The JTAG core provides debug capabilities for the developer and is compliant with the IEEE 1149 standard.

3.1.28 Interrupt Controller

The ARTIK 530/530s Module has one interrupt controller module. The most important features of the interrupt module are

- Vectored interrupt controller
- Support for 64 channel-interrupt sources

- For each interrupt source the following properties are available:
  - Fixed hardware interrupt priority level
  - Programmable interrupt priority level
  - Hardware interrupt priority level masking
  - IRQ and FIQ generation
  - Software interrupt generation
  - Test registers
  - Raw interrupt status
  - Interrupt request status

3.1.29 DMA

The ARTIK 530/530s Module has one scatter-gather DMA module. The most important features of the DMA module are

- 16 channels of dedicated DMA
- 16 DMA request lines
- Various operating modes
  - Single DMA mode
  - Burst DMA mode
  - Memory-to-memory transfer
  - Memory-to-peripheral transfer
  - Peripheral-to-memory transfer
  - Peripheral-to-peripheral transfer
- Support for 8/16/32 bit wide transactions
- Big endian and little endian (default) support

3.1.30 RTC

The ARTIK 530/530s Module has one real time clock (RTC) module. The most important features are

- Four spread-spectrum PLLs
- Two external crystals: one 24MHz crystal for the PLLs and one 32.768KHz crystal for the RTC
- One 32-bit RTC counter
- Support for alarm interrupt using RTC
  -

3.1.31 Security Subsystem

In addition to the Secure Element, the main processor on the module provides additional security features. The key features of the Security Controller sub-system are

- Secure 128-bit die ID (available to the ARTIK 530s Modules only)

- Secure JTAG featuring a secure 128-bit JTAG ID (available to the ARTIK 530s Modules only)
- Secure boot featuring a 128-bit boot ID (available to the ARTIK 530s Modules only)
- Security Controller (available to the ARTIK 530s Modules only)
- Secure Element (all features in ARTIK 530s Modules; limited features in ARTIK 530 Module)

3.1.31.1 Security Controller

The Security Controller provides a Trusted Execution Environment (TEE) and hardware cryptographic accelerators as follows:

- TEE
  - Register Protection Controller
  - Memory Protection Controller
- Hardware cryptographic accelerators
  - DES, Triple DES
  - AES
  - SHA-1
  - MD5

3.1.31.2 Secure Element

The ARTIK 530/530s Module has a dedicated Secure Element to assure end-to-end authentication and communication between nodes in an IoT setting. The most important hardware features of the Secure Element are

- An ISO/IEC 7816 14443-compliant interface.
- Dedicated 16-bit SecuCalm CPU core
- Crypto co-processor
  - Modular exponential accelerator
  - RSA 2080 bits
  - ECC 512 bits
- Data security
  - Memory encryption for all memory
  - 256B read-only and 256B nonerasable Flash area
  - Selective reset operation if abnormal voltages/frequencies are detected
- Embedded tamper-free memory
  - 32KB ROM
  - 264KB Flash
  - 2.5KB cryptographic memory
- Serial interfaces:
  - ISO 7816-3-compliant interface
  - Asynchronous half-duplex character receive/transmit serial interface

4 Module Pads

The ARTIK 530/530s Module utilizes 292 signal and ground balls providing all the relevant signaling. *Figure 3* shows how the balls are oriented and how signal coordinates are assigned to the PADs of the ARTIK 530/530s Module. *Table 2*–*Table 6* describe the relation between the ball coordinates and the ball signal names. These tables also provide detailed characteristics for each ball signal name.

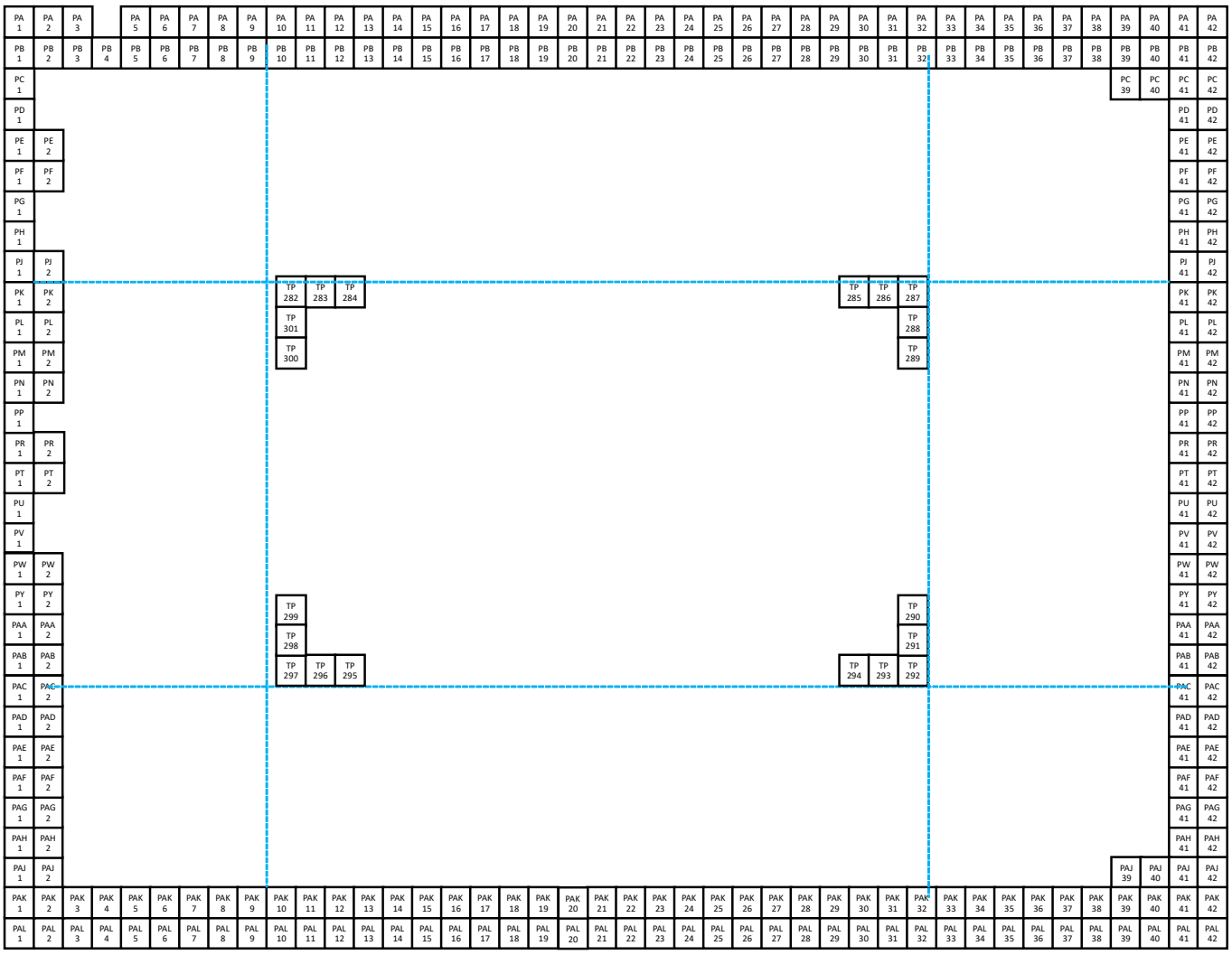

Figure 3. ARTIK 530/530s Module Top View Ball Organization

4.1 Ball Table Column Definitions

The meaning of the various columns used in *Table 2* - *Table 6* is explained in *Table 1*.

Table 1. Ball Table Column Definition

Column Name	Column Definition
Ball Loc.	Ball location on the ARTIK 530/530s Module as shown in *Figure 3*.
Ball Name	The ball name on the ARTIK 530/530s Module.
Voltage	Voltage level on the ball.
Default	Default function of the main SoC at hardware power-on.
Type	S: Signal ball, P: Power ball, G: GND ball.
I/O	I: Input, O: Output, IO: Input/Output to/from module
PU/PD	Indicates the presence of module-internal pull-up or pull-down. PU: Pull-Up, PD: Pull-Down, N: No Pull-Up/Pull-Down.
Group	Nominal function group set according to pad name. For more information see the ARTIK 530/530s Module Hardware User Guide. Usually the function of the pin can be reprogrammed.
Function	Explanation on the function of the ball.

4.1.1 North Ball Array

Table 2. North Ball Array

Ball Loc.	Ball Name	Voltage	Type	I/O	PU/PD	Group	Function
PA1	GMAC_TXEN	3.3V	S	IO	N	GMAC	GMAC Transmit Enable
PA2	GMAC_TXD1	3.3V	S	IO	N	GMAC	GMAC Transmit Data 1
PA3	GMAC_TXD3	3.3V	S	IO	N	GMAC	GMAC Transmit Data 3
PA4	NO BALL	–	–	–	–	NO BALL	–
PA5	GMAC_GTXCLK	3.3V	S	IO	N	GMAC	GMAC Transmit Clock
PA6	GMAC_RXDV	3.3V	S	IO	N	GMAC	GMAC Receive Enable
PA7	GMAC_RXD2	3.3V	S	IO	N	GMAC	GMAC Receive Data 2
PA8	GMAC_RXD0	3.3V	S	IO	N	GMAC	GMAC Receive Data 0
PA9	GND	0.0V	G	–	–	GND	Ground
PA10	AP_MIPICSI_DNCLK	1.8V	S	IO	N	CSI	MIPI CSI Data Negative Clock
PA11	AP_MIPICSI_DN0	1.8V	S	IO	N	CSI	MIPI CSI Data Negative 0
PA12	AP_MIPICSI_DN1	1.8V	S	IO	N	CSI	MIPI CSI Data Negative 1
PA13	AP_MIPICSI_DN2	1.8V	S	IO	N	CSI	MIPI CSI Data Negative 2
PA14	AP_MIPICSI_DN3	1.8V	S	IO	N	CSI	MIPI CSI Data Negative 3
PA15	GND	0.0V	G	–	–	GND	Ground
PA16	AP_MIPIDSI_DNCLK	1.8V	S	IO	N	DSI	MIPI DSI Data Negative Clock
PA17	AP_MIPIDSI_DN0	1.8V	S	IO	N	DSI	MIPI DSI Data Negative 0
PA18	AP_MIPIDSI_DN1	1.8V	S	IO	N	DSI	MIPI DSI Data Negative 1
PA19	AP_MIPIDSI_DN2	1.8V	S	IO	N	DSI	MIPI DSI Data Negative 2
PA20	AP_MIPIDSI_DN3	1.8V	S	IO	N	DSI	MIPI DSI Data Negative 3
PA21	GND	0.0V	G	–	–	GND	Ground
PA22	AP_LVDS_TN0	1.8V	S	O	N	LVDS	LVDS Transmit Channel 0 Negative
PA23	AP_LVDS_TN1	1.8V	S	O	N	LVDS	LVDS Transmit Channel 1 Negative

Table 2. North Ball Array (Continued)

Ball Loc.	Ball Name	Voltage	Type	I/O	PU/PD	Group	Function
PA24	AP_LVDS_TN2	1.8V	S	O	N	LVDS	LVDS Transmit Channel 2 Negative
PA25	AP_LVDS_TNCLK	1.8V	S	O	N	LVDS	LVDS Transmit Negative Clock
PA26	AP_LVDS_TN3	1.8V	S	O	N	LVDS	LVDS Transmit Channel 3 Negative
PA27	AP_LVDS_TN4	1.8V	S	O	N	LVDS	LVDS Transmit Channel 4 Negative
PA28	GND	0.0V	G	–	–	GND	Ground
PA29	AP_HDMI_CEC	3.3V	S	IO	N	HDMI	HDMI Consumer Electronics Control
PA30	AP_HDMI_TX2N	1.8V	S	O	N	HDMI	HDMI Transmit Channel 2 Negative
PA31	AP_HDMI_TX1N	1.8V	S	O	N	HDMI	HDMI Transmit Channel 1 Negative
PA32	AP_HDMI_TX0N	1.8V	S	O	N	HDMI	HDMI Transmit Channel0 Negative
PA33	AP_HDMI_TXCN	1.8V	S	O	N	HDMI	HDMI Transmit Negative Clock
PA34	GND	0.0V	G	–	–	GND	Ground
PA35	AP_OTG_DM	3.3V	S	IO	N	USB OTG	USB OTG Data Minus
PA36	AP_USBH_DM	3.3V	S	IO	N	USB HOST	USB HOST Data Minus
PA37	AP_GPA13	3.3V	S	IO	N	GPIO	Generic GPIO
PA38	AP_HSIC_STROBE	1.2V	S	IO	N	HSIC	HSIC Strobe
PA39	AP_GPA14	3.3V	S	IO	N	GPIO	Generic GPIO
PA40	AP_GPA9	3.3V	S	IO	N	GPIO	Generic GPIO
PA41	AP_GPA15	3.3V	S	IO	N	GPIO	Generic GPIO
PA42	AP_GPA12	3.3V	S	IO	N	GPIO	Generic GPIO
PB1	GND	0.0V	G	–	–	GND	Ground
PB2	GMAC_TXD0	3.3V	S	IO	N	GMAC	GMAC Transmit Data 0
PB3	GMAC_TXD2	3.3V	S	IO	N	GMAC	GMAC Transmit Data 2
PB4	GMAC_MDC	3.3V	S	IO	N	GMAC	GMAC MDC
PB5	GMAC_RXCLK	3.3V	S	IO	N	GMAC	GMAX Receive Clock
PB6	GMAC_RXD3	3.3V	S	IO	N	GMAC	GMAC Receive Data 3
PB7	GMAC_RXD1	3.3V	S	IO	N	GMAC	GMAC Receive Data 1
PB8	GMAC_MDIO	3.3V	S	IO	N	GMAC	GMAC MDIO
PB9	GND	0.0V	G	–	–	GND	Ground
PB10	AP_MIPICSI_DPCLK	1.8V	S	IO	N	CSI	MIPI CSI Data Positive Clock
PB11	AP_MIPICSI_DP0	1.8V	S	IO	N	CSI	MIPI CSI Data Positive 0
PB12	AP_MIPICSI_DP1	1.8V	S	IO	N	CSI	MIPI CSI Data Positive 1
PB13	AP_MIPICSI_DP2	1.8V	S	IO	N	CSI	MIPI CSI Data Positive 2
PB14	AP_MIPICSI_DP3	1.8V	S	IO	N	CSI	MIPI CSI Data Positive 3
PB15	GND	0.0V	G	–	–	GND	Ground
PB16	AP_MIPIDSI_DPCLK	1.8V	S	IO	N	DSI	MIPI DSI Data Positive Clock
PB17	AP_MIPIDSI_DP0	1.8V	S	IO	N	DSI	MIPI DSI Data Positive 0
PB18	AP_MIPIDSI_DP1	1.8V	S	IO	N	DSI	MIPI DSI Data Positive 1
PB19	AP_MIPIDSI_DP2	1.8V	S	IO	N	DSI	MIPI DSI Data Positive 2
PB20	AP_MIPIDSI_DP3	1.8V	S	IO	N	DSI	MIPI DSI Data Positive 3
PB21	GND	0.0V	G	–	–	GND	Ground
PB22	AP_LVDS_TP0	1.8V	S	O	N	LVDS	LVDS Transmit Channel 0 Positive
PB23	AP_LVDS_TP1	1.8V	S	O	N	LVDS	LVDS Transmit Channel 1 Positive

Table 2. North Ball Array (Continued)

Ball Loc.	Ball Name	Voltage	Type	I/O	PU/PD	Group	Function
PB24	AP_LVDS_TP2	1.8V	S	O	N	LVDS	LVDS Transmit Channel 2 Positive
PB25	AP_LVDS_TPCLK	1.8V	S	O	N	LVDS	LVDS Transmit Positive Clock
PB26	AP_LVDS_TP3	1.8V	S	O	N	LVDS	LVDS Transmit Channel 3 Positive
PB27	AP_LVDS_TP4	1.8V	S	O	N	LVDS	LVDS Transmit Channel 4 Positive
PB28	GND	0.0V	G	–	–	GND	Ground
PB29	AP_HDMI_HPD	3.3V	S	I	N	HDMI	HDMI Hot Plug Detect
PB30	AP_HDMI_TX2P	1.8V	S	O	N	HDMI	HDMI Transmit Channel 2 Positive
PB31	AP_HDMI_TX1P	1.8V	S	O	N	HDMI	HDMI Transmit Channel 1 Positive
PB32	AP_HDMI_TX0P	1.8V	S	O	N	HDMI	HDMI Transmit Channel 0 Positive
PB33	AP_HDMI_TXCP	1.8V	S	O	N	HDMI	HDMI Transmit Positive Clock
PB34	GND	0.0V	G	–	–	GND	Ground
PB35	AP_OTG_DP	3.3V	S	IO	N	USB OTG	USB OTG Data Plus
PB36	AP_USBH_DP	3.3V	S	IO	N	USB HOST	USB HOST Data Plus
PB37	AP_OTG_ID	–	S	I	N	USB HOST	USB HOST ID
PB38	AP_HSIC_DATA	1.2V	S	IO	N	HSIC	HSIC Data
PB39	AP_GPA4	3.3V	S	IO	N	GPIO	Generic GPIO
PB40	AP_GPA5	3.3V	S	IO	N	GPIO	Generic GPIO
PB41	AP_GPA16	3.3V	S	IO	N	GPIO	Generic GPIO
PB42	AP_GPA11	3.3V	S	IO	N	GPIO	Generic GPIO

4.1.2 South Ball Array

Table 3. South Ball Array

Ball Loc.	Ball Name	Voltage	Type	I/O	PU/PD	Group	Function
PAK1	AP_I2S0_DOUT	3.3V	S	IO	N	I2S0	I^2S 0 Data Out
PAK2	AP_I2S0_BCLK	3.3V	S	IO	N	I2S0	I^2S 0 Bit Clock
PAK3	AP_GPC11_SPI2_MISO	3.3V	S	IO	N	SPI2	SPI 2 Receive Data
PAK4	AP_GPC9_SPI2_CLK	3.3V	S	IO	N	SPI2	SPI 2 Clock
PAK5	AP_SPI0_MISO	3.3V	S	IO	N	SPI0	SPI 0 Receive Data *
PAK6	AP_SPI0_CLK	3.3V	S	IO	N	SPI0	SPI 0 Clock *
PAK7	AP_GPC14_PWM2	3.3V	S	IO	N	PWM	PWM 2
PAK8	AP_GPD6_SCL2	3.3V	S	IO	PU	I^2C	I^2C SCL 2
PAK9	AP_GPD4_SCL1	3.3V	S	IO	PU	I^2C	I^2C SCL 1
PAK10	AP_GPD2_SCL0	3.3V	S	IO	PU	I^2C	I^2C SCL 0
PAK11	AP_GPA23_HDMI_I2C_SCL	3.3V	S	IO	N	I^2C	HDMI I^2C SCL *
PAK12	ZB_DEBUG_TDO_SWO	3.3V	–	–	–	802.15.4	802.15.4 JTAG TMS
PAK13	ZB_PTI_DATA_FRC_DOUT	3.3V	–	–	–	802.15.4	802.15.4 JTAG TCK
PAK14	ZB_DEBUG_TCK_SWCLK	3.3V	–	–	–	802.15.4	802.15.4 Control
PAK15	COMBO_ZIG_UART_TXD	3.3V	S	IO	–	802.15.4	802.15.4 UART
PAK16	GND	0.0V	G	–	–	GND	Ground