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SiT5356

1 – 60 MHz, ±0.1 to ±0.25 ppm, Stratum 3, Elite Platform™ Precision Super-TCXO

Description

The SiT5356 is a ±100 ppb precision MEMS Super-TCXO that is fully compliant to Telcordia GR-1244-CORE Stratum 3 oscillator specifications. Engineered for best dynamic performance, the SiT5356 is ideal for high reliability telecom, wireless and networking, industrial, precision GNSS and audio/video applications.

Leveraging SiTime's unique DualMEMS™ temperature sensing and TurboCompensation™ technologies, the SiT5356 delivers the best dynamic performance for timing stability in the presence of environmental stressors due to air flow, temperature perturbation, vibration, shock, and electromagnetic interference. This device also integrates multiple on-chip regulators to filter power supply noise, eliminating the need for a dedicated external LDO.

The SiT5356 offers three device configurations that can be ordered using Ordering Codes for:

1) TCXO with non-pullable output frequency,
2) VCTCXO allowing voltage control of output frequency, and
3) DCTCXO, enabling digital control of output frequency using an I^2C interface, pullable to 5 ppt (parts per trillion) resolution.

The SiT5356 can be factory programmed for any combination of frequency, stability, voltage, and pull range. Programmability enables designers to optimize clock configurations while eliminating long lead times and customization costs associated with quartz devices where each frequency is custom built.

Refer to Manufacturing Guideline for proper reflow profile and PCB cleaning recommendations to ensure best performance.

Features

- Any frequency from 1 MHz to 60 MHz in 1 Hz steps
- Factory programmable options for low lead time
- Best dynamic stability under airflow, thermal shock
  - ±100 ppb stability across temperature
  - ±1 ppb/°C typical frequency slope (ΔF/ΔT)
  - 3e-11 ADEV at 10 second averaging time
- -40°C to +105°C operating temperature
- No activity dips or micro jumps
- Resistant to shock, vibration and board bending
- On-chip regulators eliminate the need for external LDOs
- Digital frequency pulling (DCTCXO) via I^2C
  - Digital control of output frequency and pull range
  - Up to ±3200 ppm pull range
  - Frequency pull resolution down to 5 ppt
- 2.5V, 2.8V, 3.0V and 3.3V supply voltage
- LVCMOS or clipped sinewave output
- RoHS and REACH compliant
- Pb-free, Halogen-free, Antimony-free

Applications

- 4G/5G radio, Small cell
- IEEE1588 boundary and grandmaster clocks
- Carrier-grade routers and switches
- Synchronous Ethernet
- Optical transport – SONET/SDH, OTN, Stratum 3
- DOCSIS 3.x remote PHY
- GPS disciplined oscillators
- Precision GNSS systems
- Test and measurement

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Block Diagram

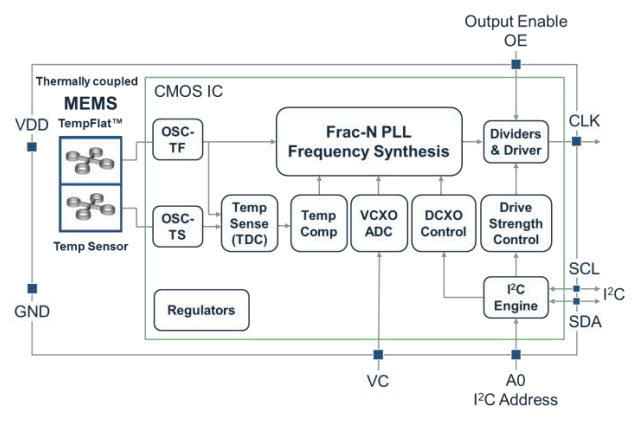


Figure 1. SiT5356 Block Diagram

5.0 x 3.2 mm² Package Pinout

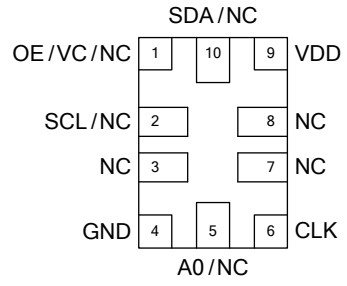
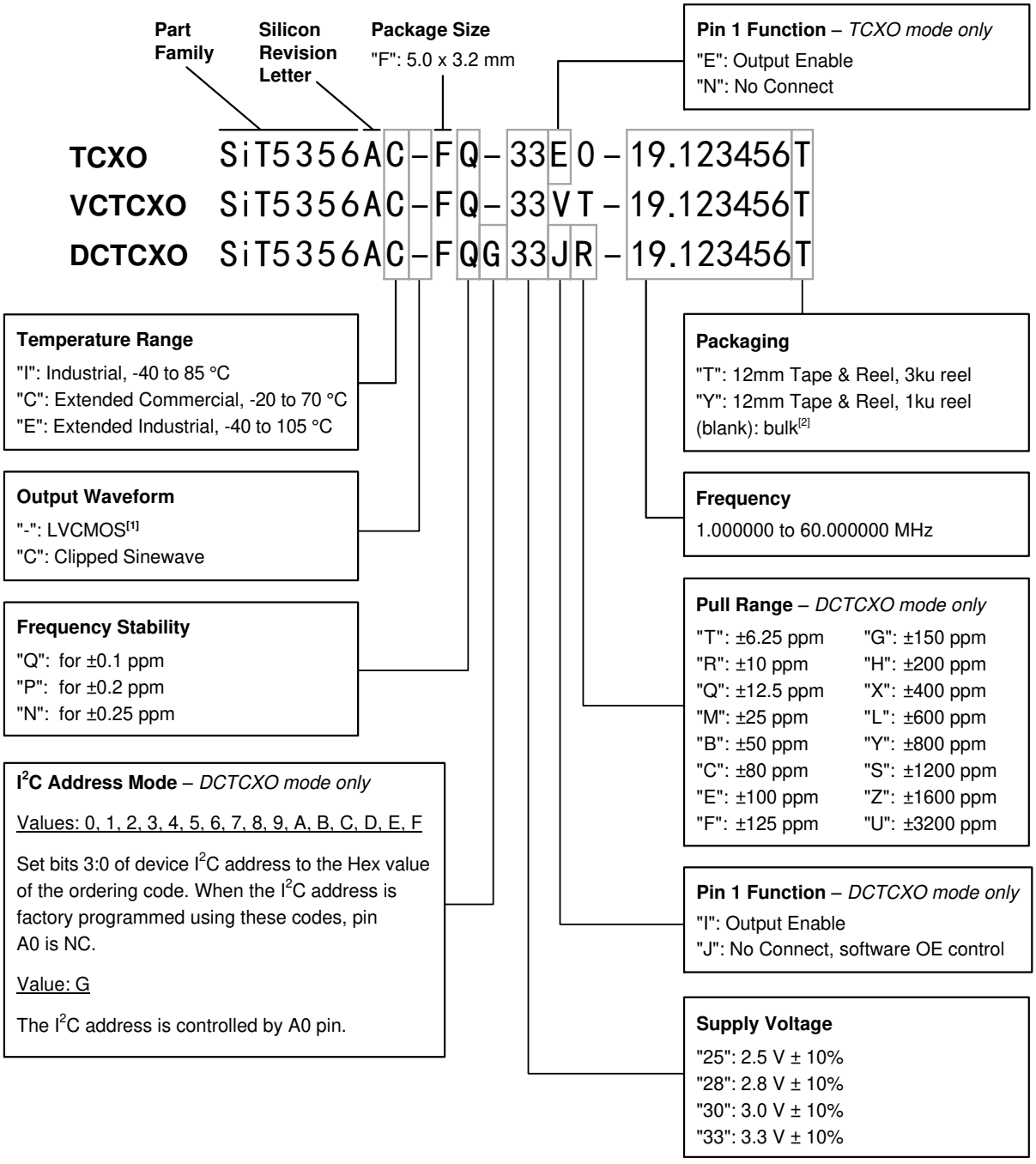


Figure 2. Pin Assignments (Top view)
(Refer to Table 13 for Pin Descriptions)

Ordering Information

The following part number guide is for reference only. To customize and build an exact part number, use the SiTime Part Number Generator. To validate the part number, use the SiTime Part Number Decoder.



Notes:

1. "-" corresponds to the default rise/fall time for LVCMOS output as specified in Table 1 (Electrical Characteristics). Contact SiTime for other rise/fall time options for best EMI.
2. Bulk is available for sampling only

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Electrical Characteristics

All Min and Max limits are specified over temperature and rated operating voltage with 15 pF output load unless otherwise stated. Typical values are at 25°C and 3.3V Vdd.

Table 1. Output Characteristics

Parameters	Symbol	Min.	Typ.	Max.	Unit	Condition
Frequency Coverage						
Nominal Output Frequency Range	F_nom	1	–	60	MHz	
Temperature Range						
Operating Temperature Range	T_use	-20	–	+70	°C	Extended Commercial, ambient temperature
		-40	–	+85	°C	Industrial, ambient temperature
		-40	–	+105	°C	Extended Industrial, ambient temperature
Frequency Stability - Stratum 3+ Grade						
Initial Tolerance	F_init	-0.5	–	+0.5	ppm	Initial frequency at 25°C inclusive of solder-down shift at 48 hours after 2 reflows
Supply Voltage Sensitivity	F_Vdd	-2.5	±0.5	+2.5	ppb	Vdd ±5%
Output Load Sensitivity	F_load	-0.4	±0.05	+0.4	ppb	LVCMOS output, 15 pF ±10%. Clipped sinewave output, 10kΩ || 10 pF ±10%
Frequency Stability over Temperature	F_stab	-0.1	–	+0.1	ppm	Referenced to (max frequency + min frequency)/2 over the rated temperature range, in TCXO, DCTCXO, or VCTCXO (VCTCXO with ±6.25 ppm pull range)
Frequency vs. Temperature Slope	ΔF/ΔT	-2	±0.9	+2	ppb/°C	-20 to 85 °C
		-3.5	±1	+3.5	ppb/°C	-40 to -20 °C
		–	±0.9	–	ppb/°C	85 to 105 °C
Dynamic Frequency Change during Temperature Ramp	F_dynamic	-0.02	±0.008	+0.02	ppb/s	0.5°C/min temperature ramp rate, -20 to 85 °C
		-0.035	±0.01	-0.035	ppb/s	0.5°C/min temperature ramp rate, -40 to -20 °C
			±0.008	–	ppb/s	0.5°C/min temperature ramp rate, 85 to 105 °C
24-hour holdover stability	F_24_Hold	-0.15	–	+0.15	ppm	Inclusive of over-temp frequency variation
Hysteresis Over Temperature	F_hys	–	±25	–	ppb	-40 to 105 °C, 0.5°C/min ramp rate
		–	±15	–	ppb	-40 to 85 °C, 0.5°C/min ramp rate
		–	±10	–	ppb	-20 to 70 °C, 0.5°C/min ramp rate
One-Day Aging	F_1d	–	±1	–	ppb	At 25°C, after 30-days of continued operation. Aging is measured with respect to day 31
One-Year Aging	F_1y	–	±0.3	–	ppm	At 25°C, after 2-days of continued operation. Aging is measured with respect to day 3.
20-Year Aging	F_20y	–	±0.5	–	ppm	
Frequency Stability - Stratum 3 Grade						
Initial Tolerance	F_init	-1	–	+1	ppm	Initial frequency at 25°C inclusive of solder-down shift at 48 hours after 2 reflows
Supply Voltage Sensitivity	F_Vdd	-6.5	±4.2	+6.5	ppb	Vdd ±5%
Output Load Sensitivity	F_load	-1.1	±0.3	+1.1	ppb	LVCMOS output, 15 pF ±10%. Clipped sinewave output, 10kΩ || 10 pF ±10%.
Frequency Stability over Temperature	F_stab	-0.2	–	+0.2	ppm	Referenced to (max frequency + min frequency)/2 over the rated temperature range. Vc=Vdd/2 for VCTCXO.
		-0.25	–	+0.25	ppm	
Frequency vs. Temperature Slope	ΔF/ΔT	-10	±6.4	+10	ppb/°C	-40 to 105 °C
Dynamic Frequency Change during Temperature Ramp	F_dynamic	-0.8	±0.05	+0.08	ppb/s	0.5°C/min temperature ramp rate
24-hour holdover stability	F_24_Hold	-0.32	–	+0.32	ppm	Inclusive of over-temperature frequency variation
One-Day Aging	F_1d	-5	±3	+5	ppb	At 25°C, after 30-days of continued operation. Aging is measured with respect to day 31.
One-Year Aging	F_1y	–	±1	–	ppm	At 25°C, after 2-days of continued operation. Aging is measured with respect to day 3.
20-Year Aging	F_20y	–	±2	–	ppm	
20-Year Total Stability	F_tot_20y	-4.6	–	+4.6	ppm	Complies with Stratum 3 per GR-1244-CORE. Actual performance is better.
LVCMOS Output Characteristics						
Duty Cycle	DC	45	–	55	%	
Rise/Fall Time	Tr, Tf	0.8	1.2	1.9	ns	10% - 90% Vdd
Output Voltage High	VOH	90%	–	–	Vdd	IOH = +3mA
Output Voltage Low	VOL	–	–	10%	Vdd	IOL = -3mA
Clipped Sinewave Output Characteristics						
Output Voltage Swing	V_out	0.8	–	1.2	V	Clipped sinewave output, 10kΩ || 10 pF ±10%
Rise/Fall Time	Tr, Tf	–	3.5	4.6	ns	20% - 80% Vdd, F_nom = 19.2 MHz

Table 1. Output Characteristics (continued)

Parameters	Symbol	Min.	Typ.	Max.	Unit	Condition
Start-up Characteristics						
Start-up Time	T_start	–	2.5	3.5	ms	Time to first pulse, measured from the time Vdd reaches 90% of its final value. Vdd ramp time = 100 µs from 0V to Vdd
Output Enable Time	T_oe	–	–	680	ns	F_nom = 10 MHz. See Timing Diagrams section below.
First Pulse Accuracy	T_stability	–	5	45	ms	Time to first accurate pulse within rated stability, measured from the time Vdd reaches 90% of its final value. Vdd ramp time = 100 µs

Table 2. DC Characteristics

Parameters	Symbol	Min.	Typ.	Max.	Unit	Condition
Supply Voltage						
Supply Voltage	Vdd	2.25	2.5	2.75	V	Contact SiTime for 2.25V to 3.63V continuous supply voltage support.
		2.52	2.8	3.08	V	
		2.7	3.0	3.3	V	
		2.97	3.3	3.63	V	
Current Consumption						
Current Consumption	Idd	–	44	53	mA	F_nom = 19.2 MHz, No Load, TCXO and DCTCXO modes
		–	48	57	mA	F_nom = 19.2 MHz, No Load, VCTCXO mode
OE Disable Current	I_od	–	43	51	mA	OE = GND, output weakly pulled down. TCXO, DCTCXO
		–	47	55	mA	OE = GND, output weakly pulled down. VCTCXO mode

Table 3. Input Characteristics

Parameters	Symbol	Min.	Typ.	Max.	Unit	Condition
Input Characteristics – OE Pin						
Input Impedance	Z_in	75	–	–	kΩ	Internal pull up to Vdd
Input High Voltage	VIH	70%	–	–	Vdd	
Input Low Voltage	VIL	–	–	30%	Vdd	
Frequency Tuning Range – Voltage Control or I^2C mode						
Pull Range	PR	±6.25	–	–	ppm	VCTCXO mode. Contact SiTime for ±12.5 and ±25 ppm.
		±6.25 ±10 ±12.5 ±25 ±50 ±80 ±100 ±125 ±150 ±200 ±400 ±600 ±800 ±1200 ±1600 ±3200	–	–	ppm	DCTCXO mode
Absolute Pull Range[0]	APR	±5.15	–	–	ppm	±0.1 ppm F_stab, DCTCXO, VCTCXO for PR = ±6.25 ppm
		±3.05	–	–	ppm	±0.2 ppm F_stab, DCTCXO, VCTCXO for PR = ±6.25 ppm
		±3.00	–	–	ppm	±0.25 ppm F_stab, DCTCXO, VCTCXO for PR = ±6.25 ppm
Upper Control Voltage	VC_U	90%	–	–	Vdd	VCTCXO mode
Lower Control Voltage	VC_L	–	–	10%	Vdd	VCTCXO mode
Control Voltage Input Impedance	VC_z	8	–	–	MΩ	VCTCXO mode
Control Voltage Input Bandwidth	VC_bw	–	10	–	kHz	VCTCXO mode. Contact SiTime for other bandwidth options.
Frequency Control Polarity	F_pol		Positive			VCTCXO mode
Pull Range Linearity	PR_lin	–	0.5	1.0	%	VCTCXO mode
I^2C Interface Characteristics, 200 Ohm, 550 pF (Max I^2C Bus Load)						
Bus Frequency	F_I2C	–	100	–	kHz	-40 to 105 °C
		–	400	–	kHz	-40 to 105 °C
		–	1000	–	kHz	-40 to 85 °C
Input Voltage Low	VIL_I2C	–	–	30%	Vdd	DCTCXO mode
Input Voltage High	VIH_I2C	70%	–	–	Vdd	DCTCXO mode
Output Voltage Low	VOL_I2C	–	–	0.4	V	DCTCXO mode
Input Leakage current	I_L	0.5	–	24	µA	0.1 V_{DD}< VOUT < 0.9 $V_{DD.}$ Includes typical leakage current from 200 kΩ pull resister to VDD. DCTCXO mode
Input Capacitance	C_{IN}	–	–	5	pF	DCTCXO mode

Note:

3. APR = PR – initial tolerance – 20-year aging – frequency stability over temperature. Refer to Table 17 for APR with respect to other pull range options.

Table 4. Jitter & Phase Noise – LVCMOS, -40 to 85 °C

Parameters	Symbol	Min.	Typ.	Max.	Unit	Condition
Jitter						
RMS Phase Jitter (random)	T_phj	–	0.31	0.48	ps	F_nom = 10 MHz, Integration bandwidth = 12 kHz to 5 MHz
		–	0.31	0.48	ps	F_nom = 50 MHz, Integration bandwidth = 12 kHz to 20 MHz
RMS Period Jitter	T_jitt_per	–	0.8	1.1	ps	F_nom = 10 MHz, population 10k
Peak Cycle-to-Cycle Jitter	T_jitt_cc	–	6	9	ps	F_nom = 10 MHz, population 1k, measured as absolute value
Phase Noise						
1 Hz offset		–	-80	-74	dBc/Hz	F_nom = 10 MHz TCXO and DCTCXO modes, and VCTCXO mode with ±6.25 ppm pull range
10 Hz offset		–	-108	-102	dBc/Hz	
100 Hz offset		–	-127	-123	dBc/Hz	
1 kHz offset		–	-148	-145	dBc/Hz	
10 kHz offset		–	-154	-151	dBc/Hz	
100 kHz offset		–	-154	-150	dBc/Hz	
1 MHz offset		–	-167	-163	dBc/Hz	
5 MHz offset		–	-168	-164	dBc/Hz	
Spurious	T_spur	–	-112	-105	dBc	F_nom = 10 MHz, 1 kHz to 5 MHz offsets

Table 5. Jitter & Phase Noise – Clipped Sinewave, -40 to 85 °C

Parameters	Symbol	Min.	Typ.	Max.	Unit	Condition
Jitter						
RMS Phase Jitter (random)	T_phj	–	0.31	0.45	ps	F_nom = 19.2 MHz, Integration bandwidth = 12 kHz to 5 MHz
		–	0.31	0.48	ps	F_nom = 60 MHz, Integration bandwidth = 12 kHz to 20 MHz
Phase Noise						
1 Hz offset		–	-74	-68	dBc/Hz	F_nom = 19.2 MHz TCXO and DCTCXO modes, and VCTCXO mode with ±6.25 ppm pull range
10 Hz offset		–	-102	-97	dBc/Hz	
100 Hz offset		–	-121	-117	dBc/Hz	
1 kHz offset		–	-142	-140	dBc/Hz	
10 kHz offset		–	-148	-146	dBc/Hz	
100 kHz offset		–	-149	-145	dBc/Hz	
1 MHz offset		–	-162	-158	dBc/Hz	
5 MHz offset		–	-164	-159	dBc/Hz	
Spurious	T_spur	–	-109	-104	dBc	F_nom = 19.2 MHz, 1 kHz to 5 MHz offsets

Table 6. Jitter & Phase Noise – LVCMOS, -40 to 105 °C

Parameters	Symbol	Min.	Typ.	Max.	Unit	Condition
Jitter						
RMS Phase Jitter (random)	T_phj	–	0.31	0.48	ps	F_nom = 10 MHz, Integration bandwidth = 12 kHz to 5 MHz
		–	0.31	0.50	ps	F_nom = 50 MHz, Integration bandwidth = 12 kHz to 20 MHz
RMS Period Jitter	T_jitt_per	–	0.8	1.1	ps	F_nom = 10 MHz, population 10k
Peak Cycle-to-Cycle Jitter	T_jitt_cc	–	6	9	ps	F_nom = 10 MHz, population 1k, measured as absolute value
Phase Noise						
1 Hz offset		–	-80	-74	dBc/Hz	F_nom = 10 MHz TCXO and DCTCXO modes, and VCTCXO mode with ±6.25 ppm pull range
10 Hz offset		–	-108	-102	dBc/Hz	
100 Hz offset		–	-127	-123	dBc/Hz	
1 kHz offset		–	-148	-145	dBc/Hz	
10 kHz offset		–	-154	-151	dBc/Hz	
100 kHz offset		–	-154	-150	dBc/Hz	
1 MHz offset		–	-167	-162	dBc/Hz	
5 MHz offset		–	-168	-163	dBc/Hz	
Spurious	T_spur	–	-112	-101	dBc	F_nom = 10 MHz, 1 kHz to 5 MHz offsets, Vdd=2.5V
		–	-112	-106	dBc	F_nom = 10 MHz, 1 kHz to 5 MHz offsets, Vdd=2.8V, 3.0V, 3.3V

Table 7. Jitter & Phase Noise – Clipped Sinewave, -40 to 105 °C

Parameters	Symbol	Min.	Typ.	Max.	Unit	Condition
Jitter						
RMS Phase Jitter (random)	T_phj	–	0.31	0.46	ps	F_nom = 19.2 MHz, Integration bandwidth = 12 kHz to 5 MHz
		–	0.31	0.50	ps	F_nom = 60 MHz, Integration bandwidth = 12 kHz to 20 MHz
Phase Noise						
1 Hz offset		–	-74	-68	dBc/Hz	F_nom = 19.2 MHz TCXO and DCTCXO modes, and VCTCXO mode with ±6.25 ppm pull range
10 Hz offset		–	-102	-97	dBc/Hz	
100 Hz offset		–	-121	-117	dBc/Hz	
1 kHz offset		–	-142	-140	dBc/Hz	
10 kHz offset		–	-148	-146	dBc/Hz	
100 kHz offset		–	-149	-145	dBc/Hz	
1 MHz offset		–	-162	-158	dBc/Hz	
5 MHz offset		–	-164	-159	dBc/Hz	
Spurious	T_spur	–	-109	-103	dBc	F_nom = 19.2 MHz, 1 kHz to 5 MHz offsets

Table 8. Absolute Maximum Limits

Attempted operation outside the absolute maximum ratings may cause permanent damage to the part.
Actual performance of the IC is only guaranteed within the operational specifications, not at absolute maximum ratings.

Parameter	Test Conditions	Value	Unit
Storage Temperature		-65 to 125	°C
Continuous Power Supply Voltage Range (Vdd)		-0.5 to 4	V
Human Body Model (HBM) ESD Protection	JESD22-A114	2000	V
Soldering Temperature (follow standard Pb-free soldering guidelines)		260	°C
Junction Temperature[4]		130	°C

Note:
4. Exceeding this temperature for an extended period of time may damage the device.

Table 9. Thermal Considerations[5]

Package	θJA (°C/W)	θJC, Bottom (°C/W)
Ceramic 5.0 x 3.2 mm²	54	15

Note:
5. Measured in still air.

Table 10. Maximum Operating Junction Temperature[6]

Max Operating Temperature (ambient)	Maximum Operating Junction Temperature
70°C	**80°C**
85°C	**95°C**
105°C	**115°C**

Note:
6. Datasheet specifications are not guaranteed if junction temperature exceeds the maximum operating junction temperature.

Table 11. Environmental Compliance

Parameter	Test Conditions	Value	Unit
Mechanical Shock Resistance	**MIL-STD-883F, Method 2002**	**10000**	*g*
Mechanical Vibration Resistance	**MIL-STD-883F, Method 2007**	**70**	*g*
Temperature Cycle	**JESD22, Method A104**	–	–
Solderability	**MIL-STD-883F, Method 2003**	–	–
Moisture Sensitivity Level	**MSL1 @260°C**	–	–

Device Configurations and Pin-outs

Table 12. Device Configurations

Configuration	Pin 1	Pin 5	I²C Programmable Parameters
TCXO	OE/NC	NC	–
VCTCXO	VC	NC	–
DCTCXO	OE/NC	A0/NC	Frequency Pull Range, Frequency Pull Value, Output Enable control.

Pin-out Top Views

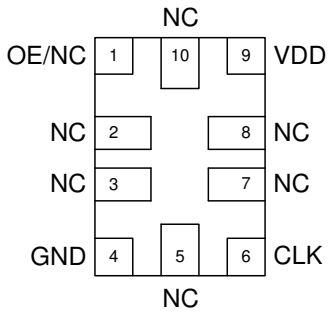


Figure 3. TCXO

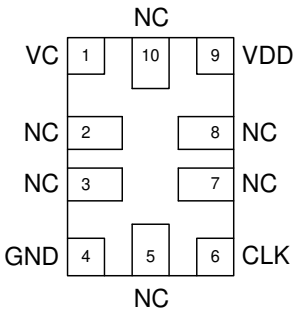


Figure 4. VCTCXO

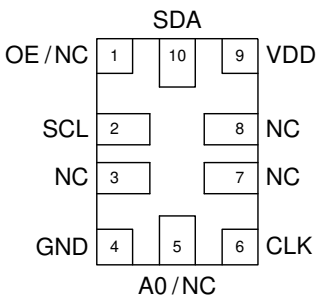


Figure 5. DCTCXO

Table 13. Pin Description

Pin	Symbol	I/O	Internal Pull-up/Pull Down Resistor	Function
1	OE/NC/VC	OE – Input	100 kΩ Pull-Up	H[7]: specified frequency output L: output is high impedance. Only output driver is disabled.
		NC[8] – No Connect	–	H or L or Open: No effect on output frequency or other device functions
		VC – Input	–	Control Voltage in VCTCXO Mode
2	SCL / NC[8]	SCL – Input	200 kΩ Pull-Up	I²C serial clock input.
		No Connect		H or L or Open: No effect on output frequency or other device functions
3	NC[8]	No Connect	–	H or L or Open: No effect on output frequency or other device functions
4	GND	Power	–	Connect to ground
5	A0 / NC[8]	A0 – Input	100 kΩ Pull-Up	Device I²C address when the address selection mode is via the A0 pin. This pin is NC when the I²C device address is specified in the ordering code. A0 Logic Level / I²C Address 0 / 1100010 1 / 1101010
		NC – No Connect	–	H or L or Open: No effect on output frequency or other device functions.
6	CLK	Output	–	LVCMOS, or clipped sinewave oscillator output
7	NC[8]	No Connect	–	H or L or Open: No effect on output frequency or other device functions
8	NC[8]	No Connect	–	H or L or Open: No effect on output frequency or other device functions
9	VDD	Power	–	Connect to VDD[8]
10	SDA / NC[8]	SDA – Input/Output	200 kΩ Pull Up	I²C Serial Data.
		NC – No Connect	–	H or L or Open: No effect on output frequency or other device functions.

Notes:

7. In OE mode for noisy environments, a pull-up resistor of 10 kΩ or less is recommended if pin 1 is not externally driven. If pin 1 needs to be left floating, use the NC option.
8. A 0.1 µF capacitor in parallel with a 10 µF capacitor are required between Vdd and GND. The 0.1 µF capacitor is recommended to place close to the device, and place the 10 µF capacitor less than 2 inches away.
9. All NC pins can be left floating and do not need to be soldered down.

Test Circuit Diagrams for LVCMOS and Clipped Sinewave Outputs

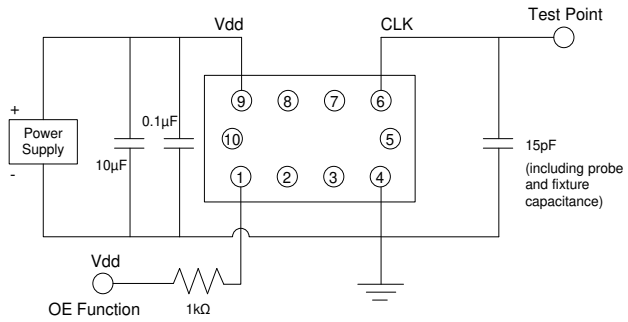


Figure 6. LVCMOS Test Circuit (OE Function)

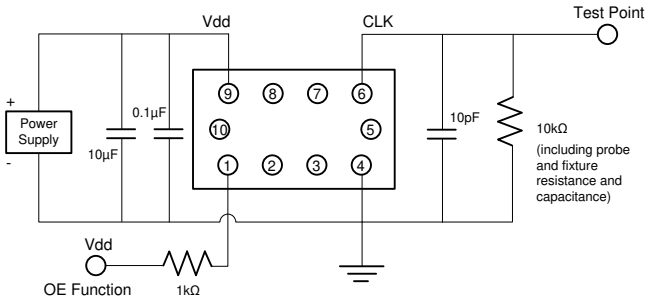


Figure 7. Clipped Sinewave Test Circuit (OE Function) for AC and DC Measurements

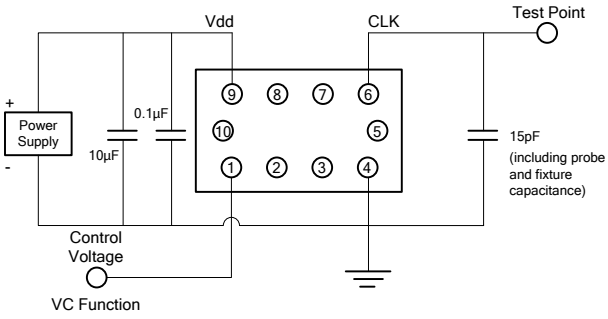


Figure 8. LVCMOS Test Circuit (VC Function)

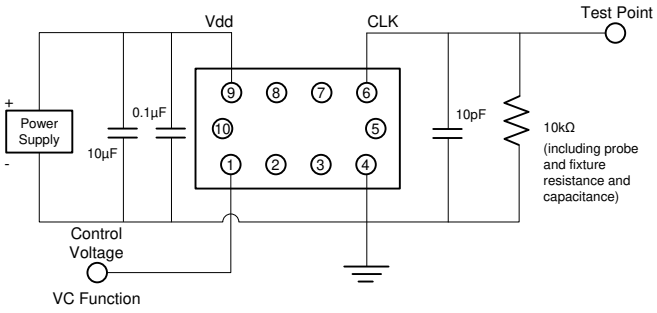


Figure 9. Clipped Sinewave Test Circuit (VC Function) for AC and DC Measurements

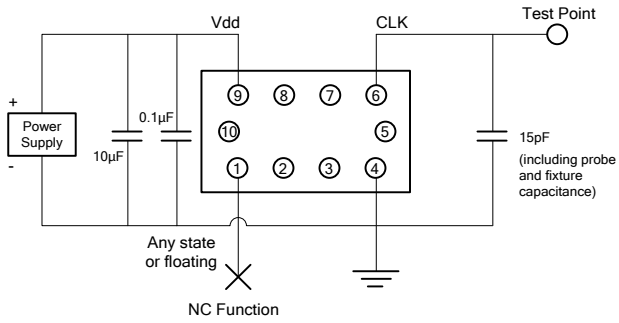


Figure 10. LVCMOS Test Circuit (NC Function)

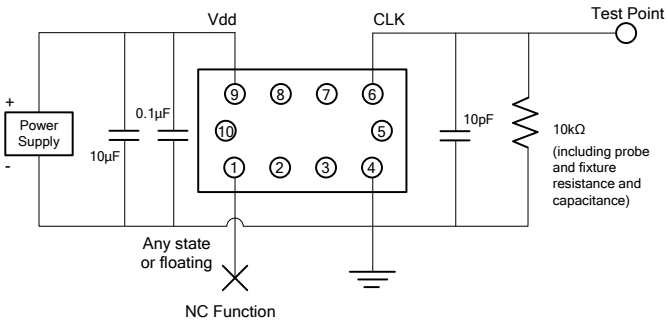


Figure 11. Clipped Sinewave Test Circuit (NC Function) for AC and DC Measurements

Test Circuit Diagrams for LVCMOS and Clipped Sinewave Outputs (continued)

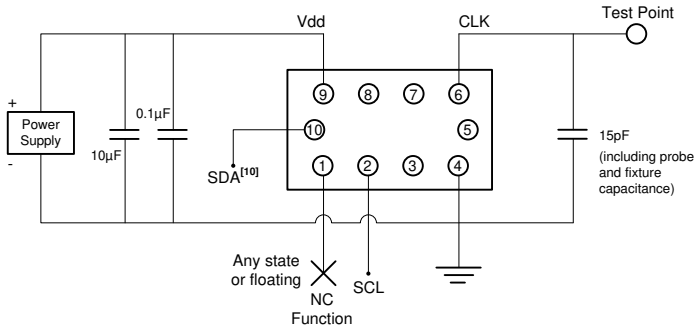


Figure 12. LVCMOS Test Circuit (I²C Control), DCTCXO mode

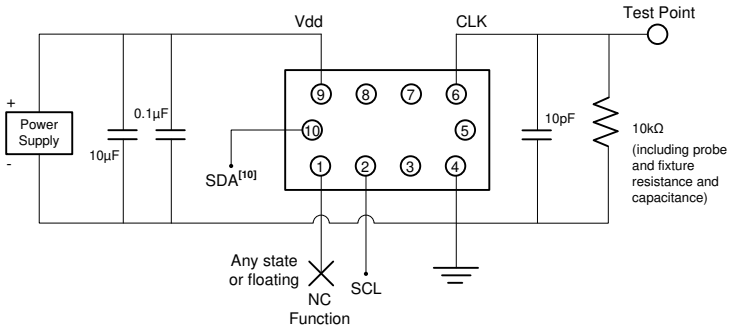


Figure 13. Clipped Sinewave Test Circuit (I²C Control), DCTCXO mode for AC and DC Measurements

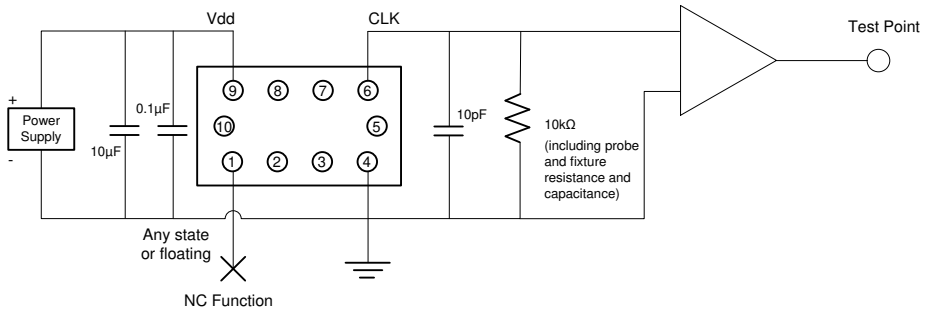


Figure 14. Clipped Sinewave Test Circuit for Phase Noise Measurements, Applies to All Configurations (NC Function shown for example only)

Note:
10. SDA is open-drain and may require pull-up resistor if not present in I²C test setup.

Waveforms

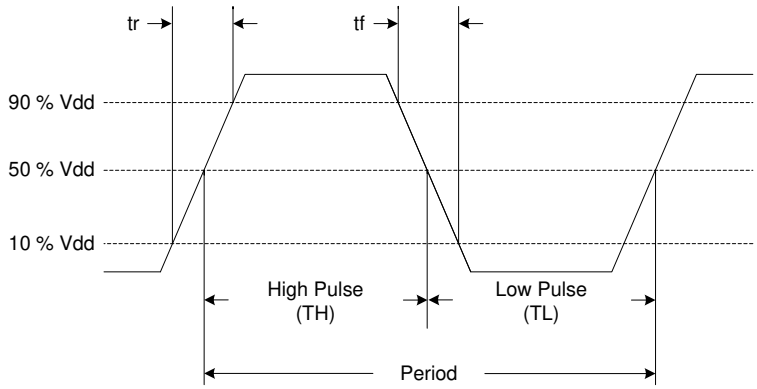


Figure 15. LVCMOS Waveform Diagram[11]

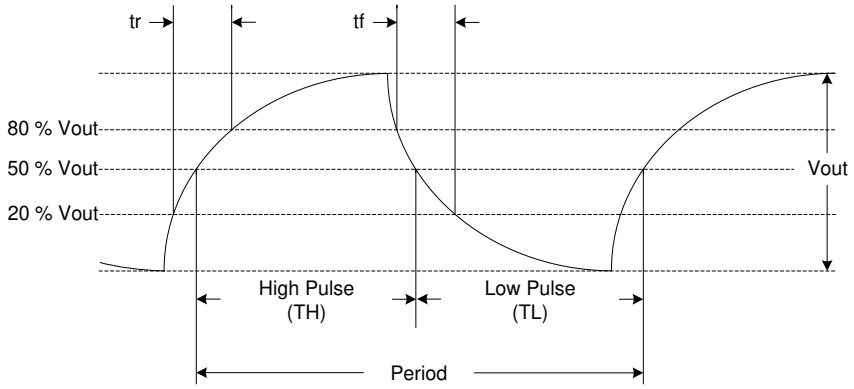
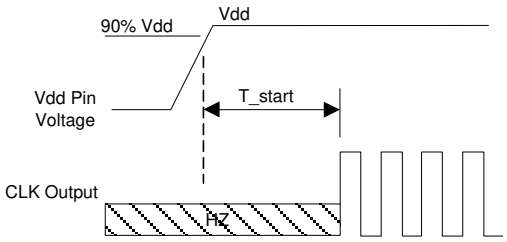


Figure 16. Clipped Sinewave Waveform Diagram[11]

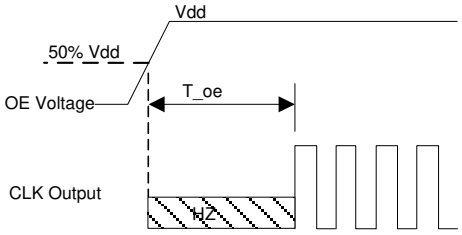
Note:
11. Duty Cycle is computed as Duty Cycle = TH/Period.

Timing Diagrams



T_start: Time to start from power-off

Figure 17. Startup Timing



T_oe: Time to re-enable the clock output

Figure 18. OE Enable Timing (OE Mode Only)

Typical Performance Plots

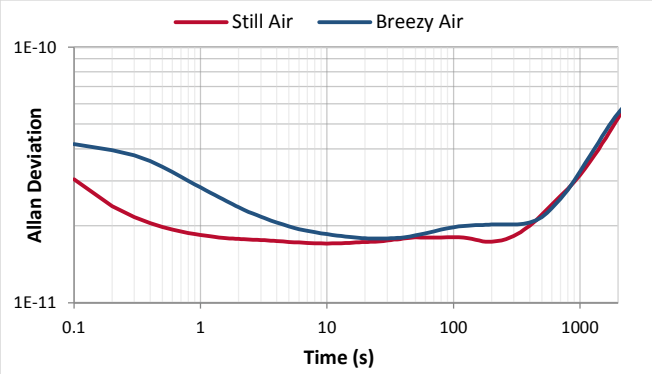


Figure 19. ADEV (±0.1 ppm)

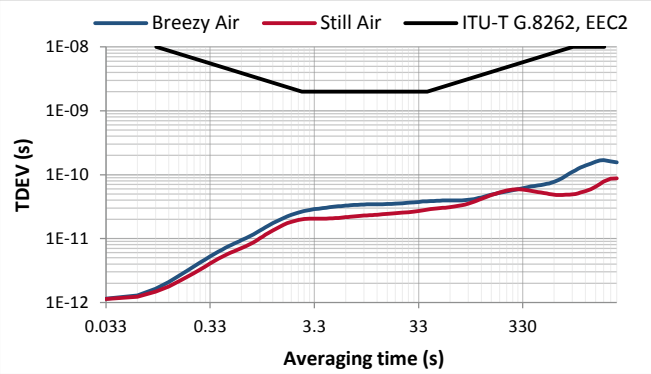


Figure 20. TDEV (0.1 Hz loop bandwidth, ±0.1 ppm)

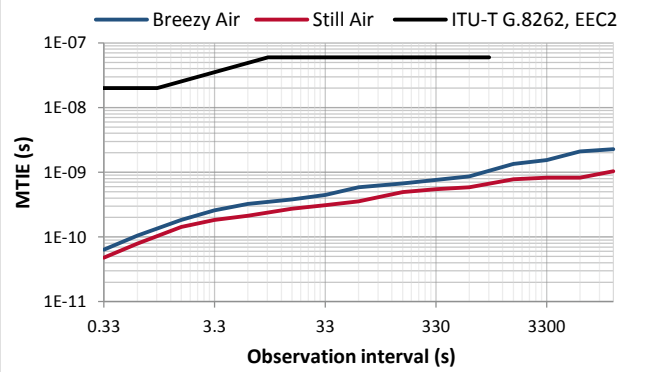


Figure 21. MTIE (0.1 Hz loop bandwidth, ±0.1 ppm)

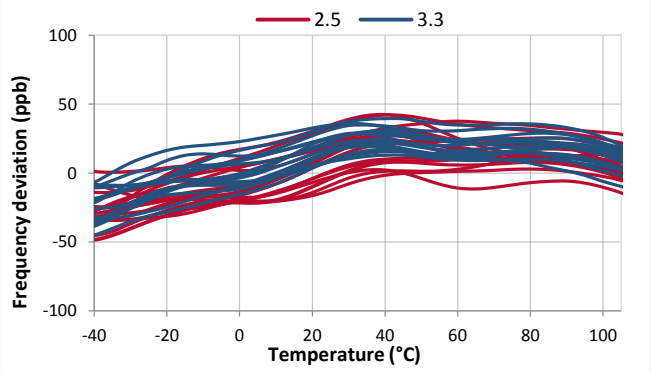


Figure 22. Frequency vs Temperature (±0.1 ppm), 105°C

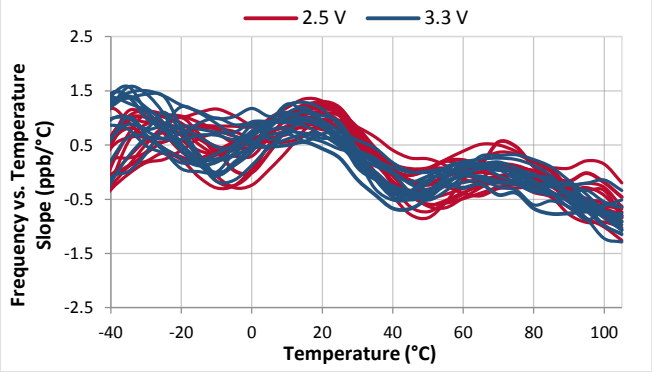


Figure 23. Freq. vs. Temp. Slope (ΔF/ΔT), ±0.1 ppm device

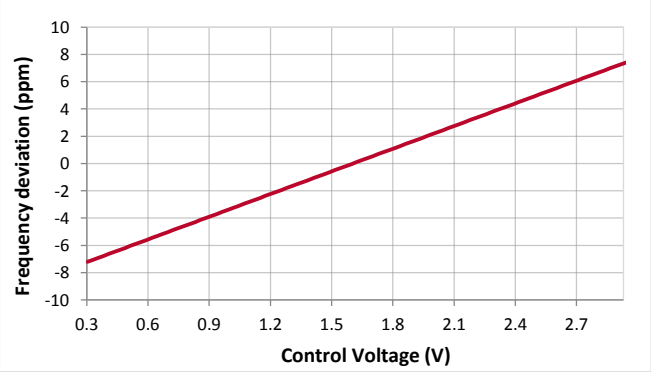


Figure 24. VCTCXO frequency pull characteristic

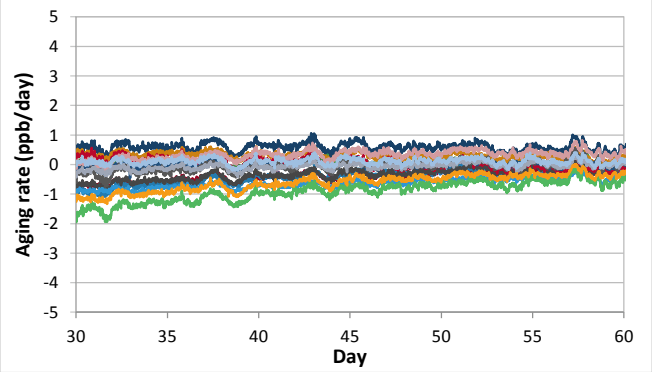


Figure 25. 1-day aging rate (to 62 days), ±0.1 ppm device

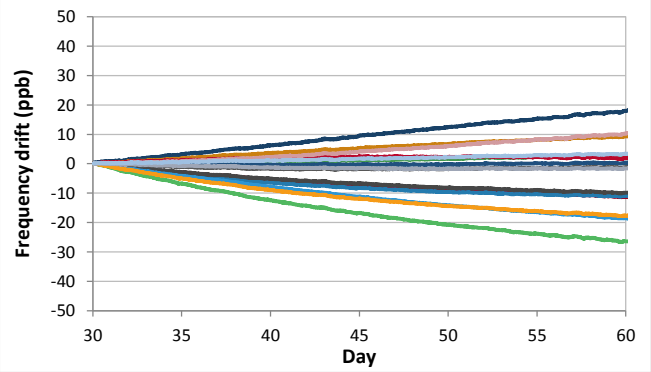


Figure 26. Drift over 30 days relative to the first reading

Typical Performance Plots (continued)

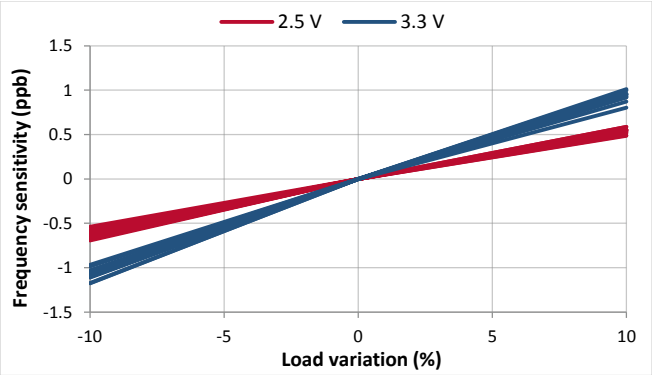


Figure 27. Load sensitivity (±0.1 ppm)

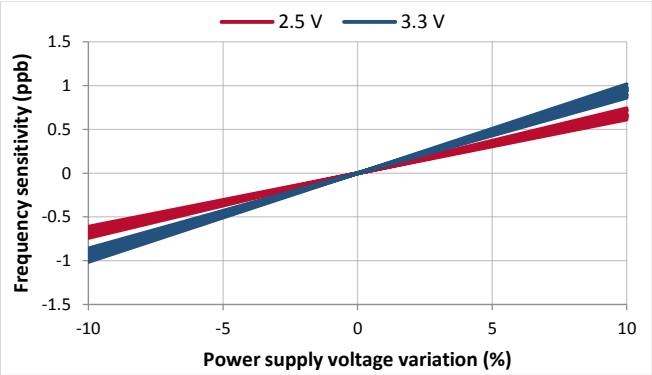


Figure 28. VDD sensitivity (±0.1 ppm)

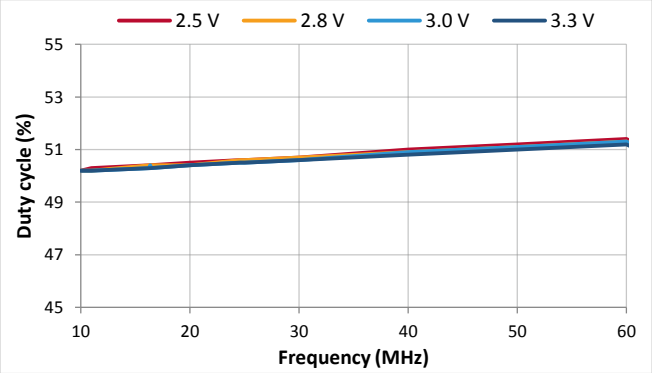


Figure 29. Duty Cycle (LVCMOS)

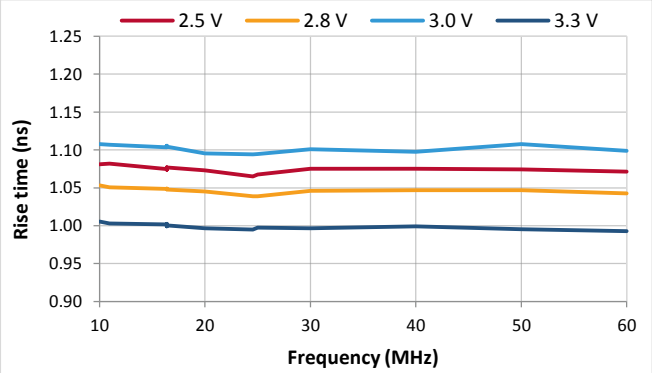


Figure 30. Rise Time (LVCMOS)

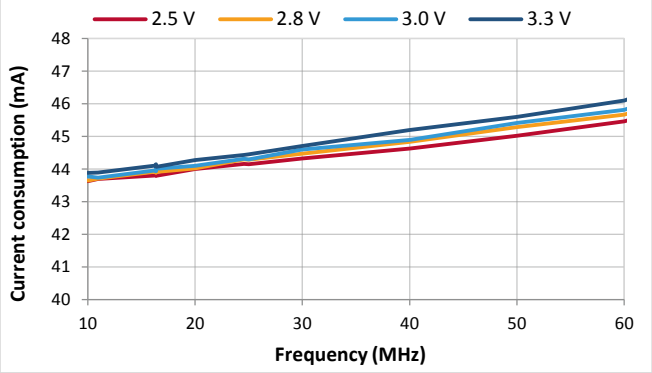


Figure 31. IDD TCXO (LVCMOS)

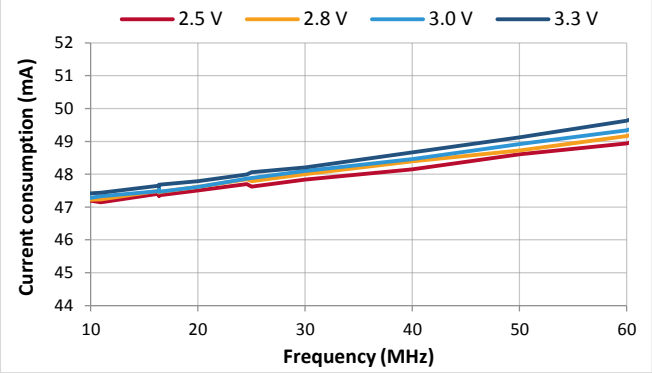


Figure 32. IDD VCTCXO (LVCMOS)

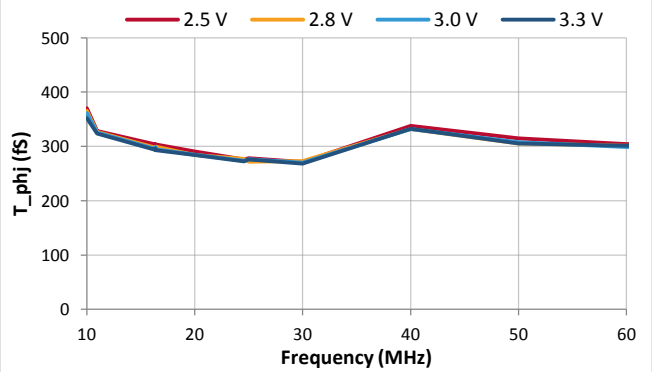


Figure 33. T_phj, RMS Random, (DC)TCXO (LVCMOS)

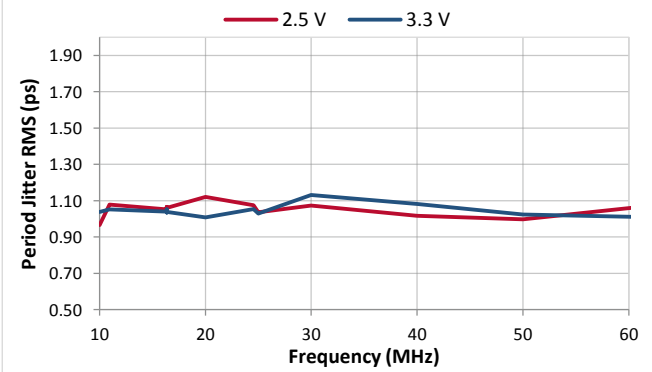


Figure 34. Period Jitter, RMS (LVCMOS)

Typical Performance Plots (continued)

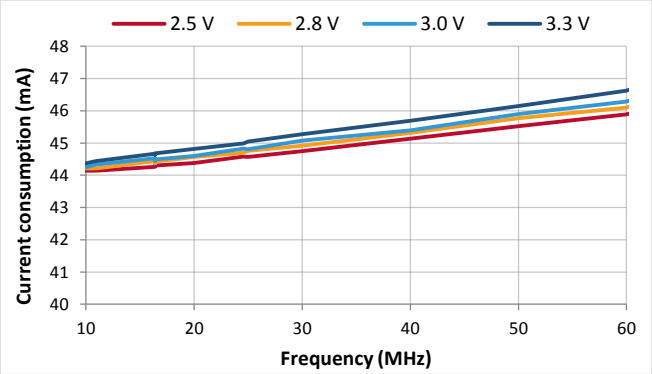


Figure 35. IDD DCTCXO (LVCMOS)

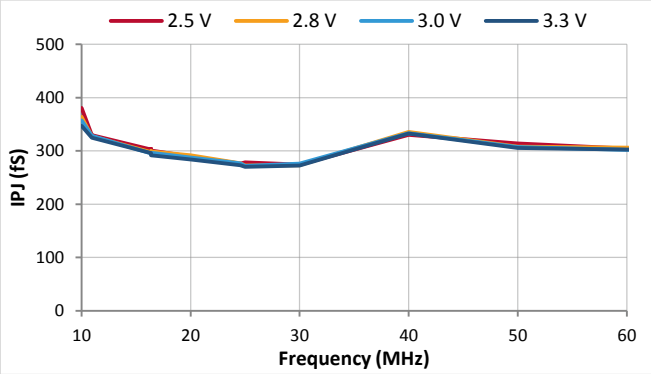


Figure 36. T_phj, RMS Random, VCTCXO (LVCMOS)

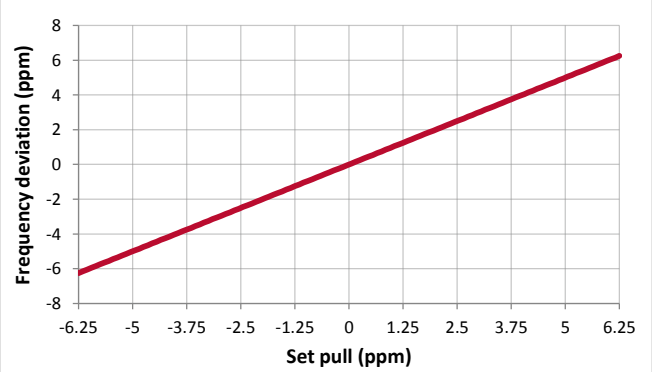


Figure 37. DCTCXO frequency pull characteristic

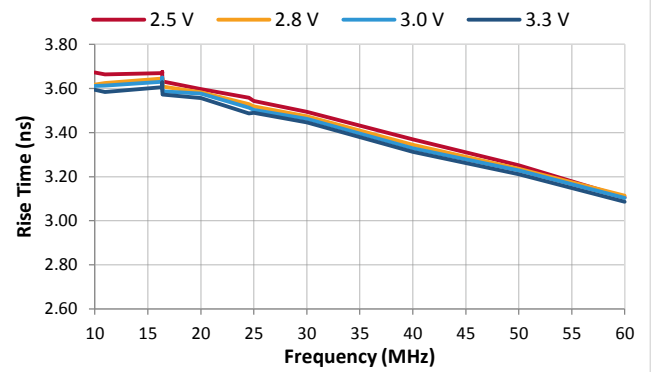


Figure 38. Rise Time (Clipped Sinewave)

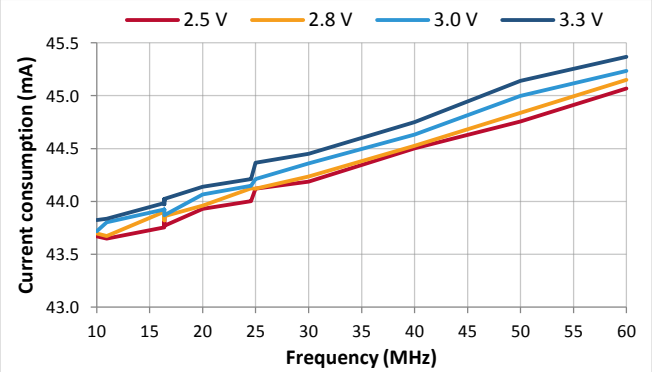


Figure 39. IDD TCXO (Clipped Sinewave)

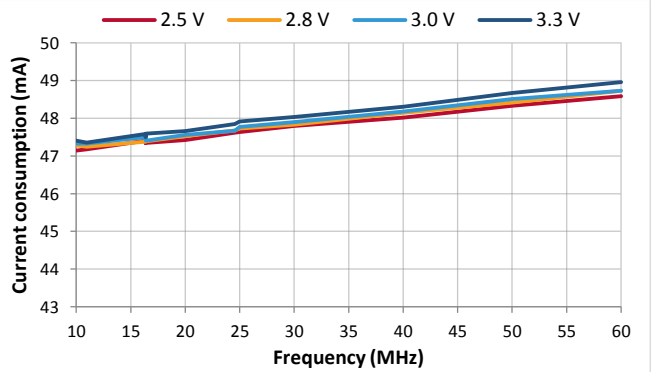


Figure 40. IDD VCTCXO (Clipped Sinewave)

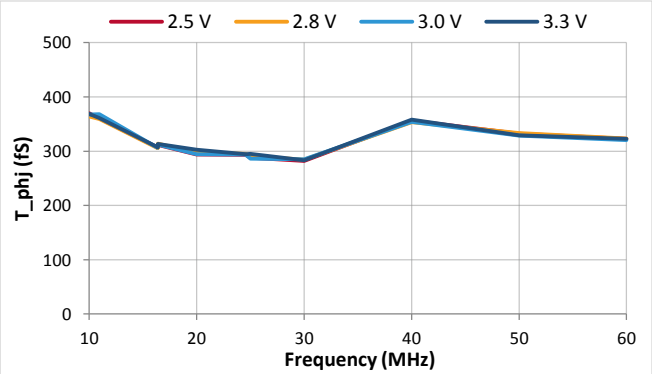


Figure 41. T_phj, RMS Random, (DC)TCXO (Clipped Sine)

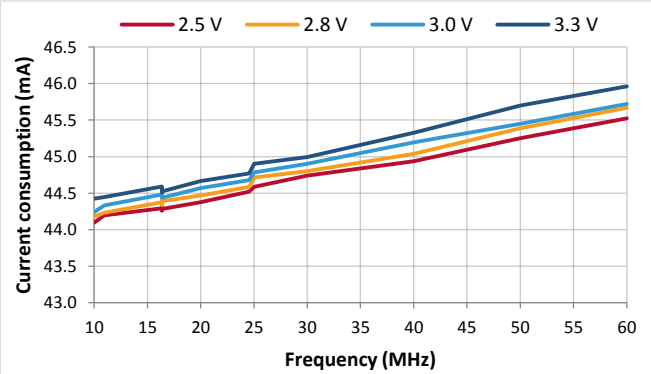


Figure 42. IDD DCTCXO (Clipped Sinewave)

Typical Performance Plots (continued)

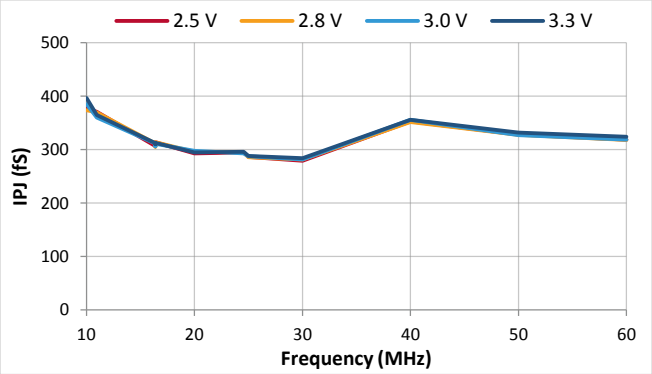


Figure 43. T_phj, RMS Random, VCTCXO (Clipped Sine)

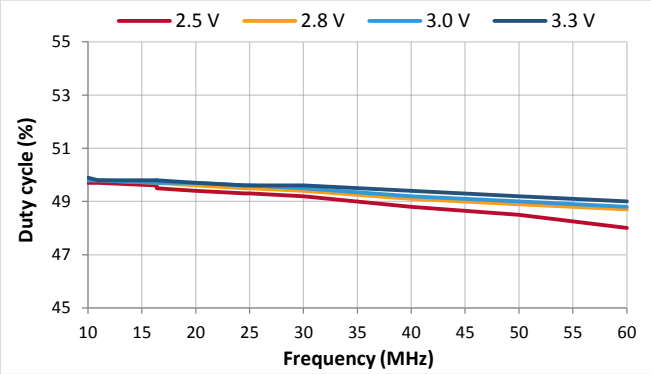


Figure 44. Duty Cycle (Clipped Sinewave)

Architecture Overview

Based on SiTime's innovative Elite Platform™, the SiT5356 delivers exceptional dynamic performance, i.e. resilience to environmental stressors such as shock, vibration, and fast temperature transients. Underpinning the Elite platform are SiTime's unique DualMEMS™ temperature sensing architecture and TurboCompensation™ technologies.

DualMEMS is a noiseless temperature compensation scheme. It consists of two MEMS resonators fabricated on the same die substrate. The TempFlat™ resonator is designed with a flat frequency characteristic over temperature whereas the temperature sensing resonator is by design sensitive to temperature changes. The ratio of frequencies between these two resonators provides an accurate reading of the resonator temperature with 20 µK resolution.

By placing the two MEMS resonators on the same die, this temperature sensing scheme eliminates any thermal lag and gradients between resonator and temperature sensor, thereby overcoming an inherent weakness of legacy quartz TCXOs.

The DualMEMS temperature sensor drives a state-of-the-art CMOS temperature compensation circuit. The TurboCompensation design, with >100 Hz compensation bandwidth, achieves a dynamic frequency stability that is far superior to any quartz TCXO. The digital temperature compensation enables additional optimization of frequency stability and frequency slope over temperature within any chosen temperature range for a given system design.

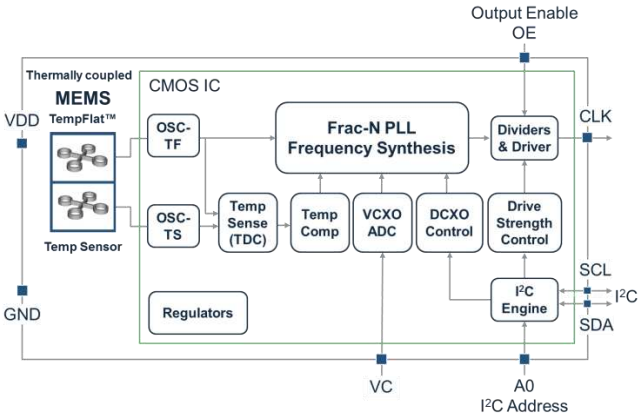


Figure 45. Elite Architecture

The Elite platform also incorporates a high resolution, low noise frequency synthesizer along with the industry standard I²C bus. This unique combination enables system designers to digitally control the output frequency in steps as low as 5 ppt and over a wide range up to ±3200 ppm.

For more information regarding the Elite platform and its benefits please visit:

- SiTime's breakthroughs section
- TechPaper: DualMEMS Temperature Sensing Technology
- TechPaper: DualMEMS Resonator TDC

Functional Overview

The SiT5356 is designed for maximum flexibility with an array of factory programmable options, enabling system designers to configure this precision device for optimal performance in a given application.

Frequency Stability

The SiT5356 comes in two factory-trimmed stability grades that are optimized for different applications. Both Stratum 3+ and Stratum 3 devices are compliant with Stratum 3 stability of ±4.6 ppm over 20 years.

Table 14. Stability Grades vs. Ordering Codes

Grade	Frequency Slope (ΔF/ΔT)	Frequency Stability Over Temperature	Ordering Code
Stratum 3+	±3.5 ppb/°C	±0.1 ppm	Q
Stratum 3	±10 ppb/°C	±0.2 ppm	P
		±0.25 ppm	N

- Stratum 3+ grade with ΔF/ΔT of ±3.5 ppb/°C is engineered to provide significantly better performance than legacy quartz TCXOs in time and phase synchronization applications such as IEEE1588, small cells, and 5G C-RAN (cloud RAN).
- Stratum 3 grade is designed to replace classic Stratum 3 TCXOs in applications such as SyncE with better dynamic performance and shorter lead time.

Output Frequency and Format

The SiT5356 can be factory programmed for an output frequency without sacrificing lead time or incurring an upfront customization cost typically associated with custom-frequency quartz TCXOs.

The device supports both LVCMOS and clipped sinewave output. Ordering codes for the output format are shown below:

Table 15. Output Formats vs. Ordering Codes

Output Format	Ordering Code
LVCMOS	"-"
Clipped Sinewave	"C"

Output Frequency Tuning

In addition to the non-pullable TCXO, the SiT5356 can also support output frequency tuning through either an analog control voltage (VCTCXO), or I²C interface (DCTCXO). The I²C interface enables 16 factory programmed pull-range options from ±6.25 ppm to ±3200 ppm. The pull range can also be reprogrammed via I²C to any supported pull-range value.

Refer to Device Configuration section for details.

Pin 1 Configuration (OE, VC, or NC)

Pin 1 of the SiT5356 can be factory programmed to support three modes: Output Enable (OE), Voltage Control (VC), or No Connect (NC).

Table 16. Pin Configuration Options

Pin 1 Configuration	Operating Mode	Output
OE	TCXO/DCTCXO	Active or High-Z
NC	TCXO/DCTCXO	Active
VC	VCTCXO	Active

When pin 1 is configured as OE pin, the device output is guaranteed to operate in one of the following two states:

- Clock output with the frequency specified in the part number when Pin 1 is pulled to logic high
- Hi-Z mode with weak pull down when pin 1 is pulled to logic low.

When pin 1 is configured as NC, the device is guaranteed to output the frequency specified in the part number at all times, regardless of the logic level on pin 1.

In the VCTCXO configuration, the user can fine-tune the output frequency from the nominal frequency specified in the part number by varying the pin 1 voltage. The guaranteed allowable variation of the output frequency is specified as pull range. A VCTCXO part number must contain a valid pull-range ordering code.

Device Configurations

The SiT5356 supports 3 device configurations – TCXO, VCTCXO, and DCTCXO. The TCXO and VCTCXO options are directly compatible with the quartz TCXO and VCTCXO. The DCTCXO configuration provides performance enhancement by eliminating VCTCXO's sensitivity to control voltage noise with an I^2C digital interface for frequency tuning.

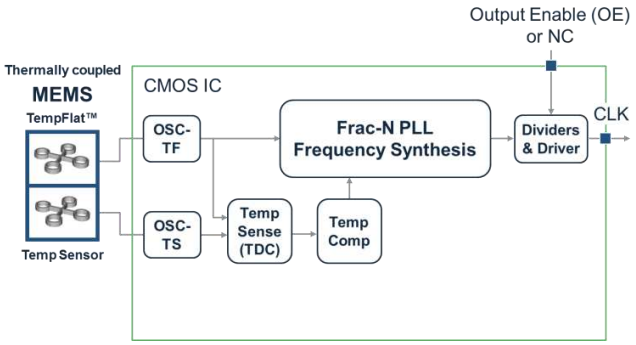


Figure 46. Block Diagram – TCXO

TCXO Configuration

The TCXO configuration generates a fixed frequency output, as shown in Figure 46. The frequency is specified by the user in the frequency field of the device ordering code and then factory programmed. Other factory programmable options include supply voltage, output types (LVCMOS or clipped sinewave), and pin 1 functionality (OE or NC).

Refer to the Ordering Information section at the end of the datasheet for a list of all ordering options.

VCTCXO Configuration

A VCTCXO, shown in Figure 47, is a frequency control device whose output frequency is an approximately linear function of control voltage applied to the voltage control pin. VCTCXOs have a number of use cases including the VCO portion of a jitter attenuation/jitter cleaner PLL Loop.

The SiT5356 achieves a 10x better pull range linearity of <0.5% via a high-resolution fractional PLL compared with 5% to 10% typical of quartz VCTCXOs that rely on pulling a resonator. By contrast, quartz-based VCTCXOs change output frequency by varying the capacitive load of a crystal resonator using varactor diodes, which results in poor linearity.

Note that the output frequency of the VCTCXO is proportional to the analog control voltage applied to pin 1. Because this control signal is analog and directly controls the output frequency, care must be taken to minimize noise on this pin.

The nominal output frequency is factory programmed per the customer's request to 6 digits of precision and is defined as the output frequency when the control voltage equals Vdd/2. The maximum output frequency variation from this nominal value is set by the pull range, which is also factory programmed to the customer's desired value and specified by the ordering code. The Ordering Information section shows all ordering options and associated ordering codes.

Refer to VCTCXO-Specific Design Considerations for more information on critical VCTCXO parameters including pull range linearity, absolute pull range, control voltage bandwidth, and Kv.

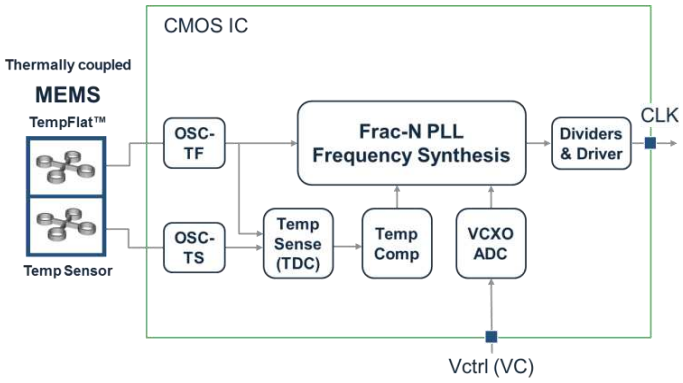


Figure 47. Block Diagram – VCTCXO

DCTCXO Configuration

The SiT5356 offers digital control of the output frequency, as shown in Figure 48. The output frequency is controlled by writing frequency control words over the I^2C interface.

There are several advantages of DCTCXOs relative to VCTCXOs:

1) Frequency control resolution as low as 5 ppt. This high resolution minimizes accumulated time error in synchronization applications.
2) Lower system cost – A VCTCXO may need a Digital to Analog Converter (DAC) to drive the control voltage input. In a DCTXCO, the frequency control is achieved digitally by register writes to the control registers via I^2C, thereby eliminating the need for a DAC.
3) Better noise immunity – The analog signal used to drive the voltage control pin of a VCTCXO can be sensitive to noise, and the trace over which the signal is routed can be susceptible to noise coupling from the system. The DCTCXO does not suffer from analog noise coupling since the frequency control is performed digitally through I^2C.
4) No frequency-pull non-linearity – The frequency pulling is achieved via fractional feedback divider of the PLL, eliminating any pull non-linearity concerns typical of quartz-based VCTCXOs. This improves dynamic performance in closed-loop applications.
5) Programmable wide pull range – The DCTCXO pulling mechanism is via the fractional feedback divider and is therefore not constrained by resonator pullability as in quartz-based solutions. The SiT5356 offers 16 frequency pull-range options from ±6.25ppm to ±3200ppm, providing system designers great flexibility.

Refer to DCTCXO-Specific Design Considerations for more information on critical DCTCXO parameters including pull range, absolute pull range, frequency output, and I^2C control registers.

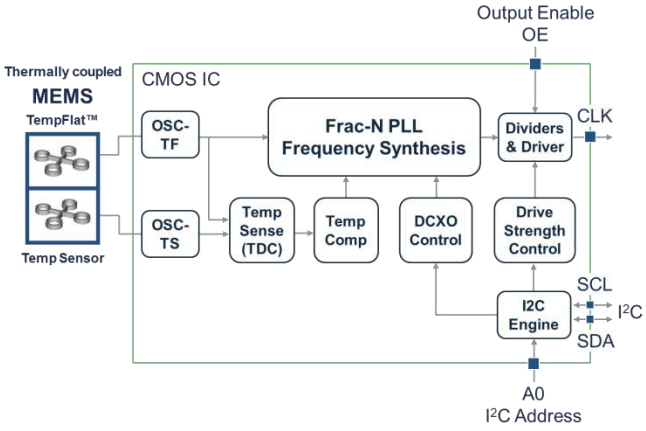


Figure 48. Block Diagram

VCTCXO-Specific Design Considerations

Linearity

In any VCTCXO, there will be some deviation of the frequency-voltage (FV) characteristic from an ideal straight line. Linearity is the ratio of this maximum deviation to the total pull range, expressed as a percentage. Figure 49 below shows the typical pull linearity of a SiTime VCTCXO. The linearity is excellent (1% maximum) relative to most quartz offerings because the frequency pulling is achieved with a PLL rather than varactor diodes.

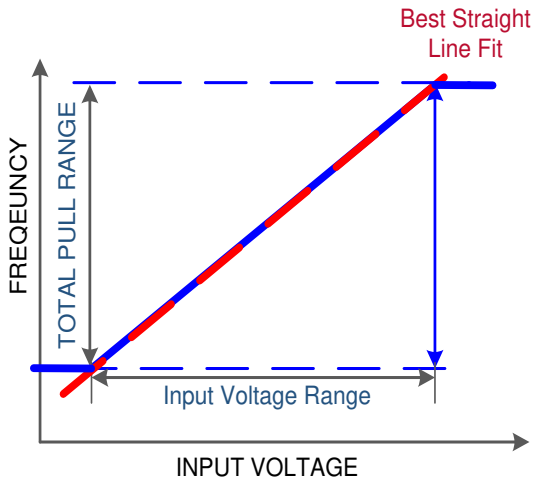


Figure 49. Typical SiTime VCTCXO Linearity

Control Voltage Bandwidth

Control voltage bandwidth, sometimes called “modulation rate” or “modulation bandwidth”, indicates how fast a VCO can respond to voltage changes at its input. The ratio of the output frequency variation to the input voltage variation, previously denoted by K_V, has a low-pass characteristic in most VCTCXOs. The control voltage bandwidth equals the modulating frequency where the output frequency deviation equals 0.707 (e.g. -3 dB) of its DC value, for DC inputs swept in the same voltage range.

For example, a part with a ±6.25 ppm pull range and a 0-3V control voltage can be regarded as having an average KV of 4.17 ppm/V (12.5 ppm/3V = 4.17 ppm/V). Applying an input of 1.5V DC ± 0.5V (1.0 V to 2.0V) causes an output frequency change of 4.17 ppm (±2.08 ppm). If the control voltage bandwidth is specified as 10 kHz, the peak-to-peak value of the output frequency change will be reduced to 4.33 ppm/√2 or 2.95 ppm, as the frequency of the control voltage change is increased to 10 kHz.

FV Characteristic Slope K_V

The slope of the FV characteristic is a critical design parameter in many low bandwidth PLL applications. The slope is the derivative of the FV characteristic – the deviation of frequency divided by the control voltage change needed to produce that frequency deviation, over a small voltage span, as shown below:

$$K_V = \frac{\Delta f_{out}}{\Delta V_{in}}$$

It is typically expressed in kHz/Volt, MHz/Volt, ppm/Volt, or similar units. This slope is usually called “K_V” based on terminology used in PLL designs.

The extreme linear characteristic of the SiTime SiT5356 VCTCXO family means that there is very little K_V variation across the whole input voltage range (typically <1%), significantly reducing the design burden on the PLL designer. Figure 50 below illustrates the typical K_V variation.

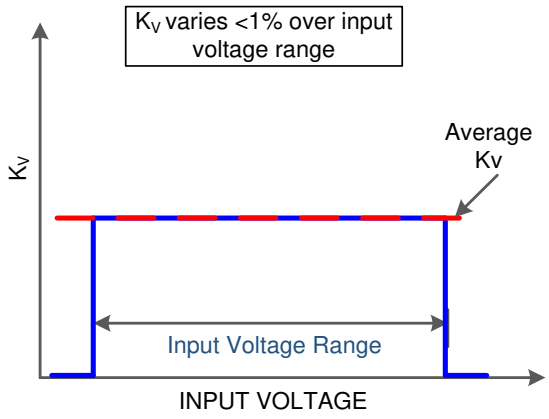


Figure 50. Typical SiTime K_V Variation

Pull Range, Absolute Pull Range

Pull range (PR) is the amount of frequency deviation that will result from changing the control voltage over its maximum range under nominal conditions.

Absolute pull range (APR) is the guaranteed controllable frequency range over all environmental and aging conditions. Effectively, it is the amount of pull range remaining after taking into account frequency stability, tolerances over variables such as temperature, power supply voltage, and aging, i.e.:

$$APR = PR - F_{stability} - F_{aging}$$

where $F_{stability}$ is the device frequency stability due to initial tolerance and variations on temperature, power supply, and load.

Figure 51 shows a typical SiTime VCTCXO FV characteristic. The FV characteristic varies with conditions, so that the frequency output at a given input voltage can vary by as much as the specified frequency stability of the VCTCXO. For such VCTCXOs, the frequency stability and APR are independent of each other. This allows very wide range of pull options without compromising frequency stability.

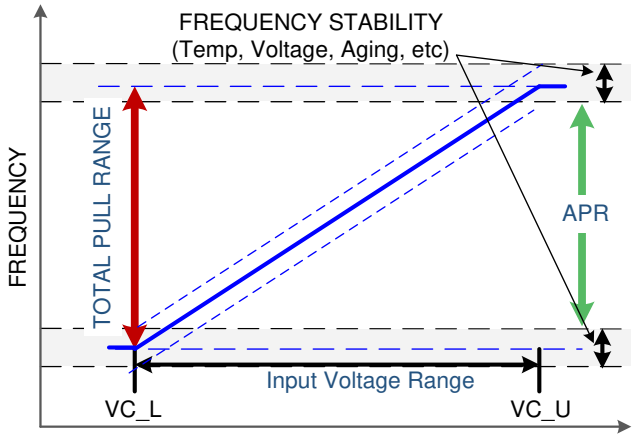


Figure 51. Typical SiTime VCTCXO FV Characteristic

The upper and lower control voltages are the specified limits of the input voltage range as shown in Figure 51 above. Applying voltages beyond the upper and lower voltages do not result in noticeable changes of output frequency. In other words, the FV characteristic of the VCTCXO saturates beyond these voltages. Figures 1 and 2 show these voltages as Lower Control Voltage (VC_L) and Upper Control Voltage (VC_U).

Table 17 below shows the pull range and corresponding APR values for each of the frequency vs. temperature ordering options.

Table 17. VCTCXO Pull Range, APR Options[12] Typical unless specified otherwise. Pull range (PR) is ±6.25 ppm.

Pull Range Ordering Code	Device Option(s)	APR ppm ±0.1 ppm option ±0.5 ppm 20-year aging	APR ppm ±0.2 ppm option ±2 ppm 20-year aging	APR ppm ±0.25 ppm option ±2 ppm 20-year aging
T	VCTCXO	±5.15	±3.05	±3.0

Notes:
12. APR includes initial tolerance, frequency stability vs. temperature, and the corresponding 20-year aging.

DCTCXO-Specific Design Considerations

Pull Range and Absolute Pull Range

Pull range and absolute pull range are described in the previous section. Table 18 below shows the pull range and corresponding APR values for each of the frequency vs. temperature ordering options.

Table 18. APR Options[13]

Pull Range Ordering Code	Pull Range ppm	APR ppm ±0.1 ppm option ±0.5 ppm 20-year aging	APR ppm ±0.2 ppm option ±2 ppm 20-year aging	APR ppm ±0.25 ppm option ±2 ppm 20-year aging
T	±6.25	±5.15	±3.05	±3.0
R	±10	±8.90	±6.80	±6.75
Q	±12.5	±11.4	±9.3	±9.25
M	±25	±23.9	±21.8	±21.75
B	±50	±48.9	±46.8	±46.75
C	±80	±78.9	±76.8	±76.75
E	±100	±98.9	±96.8	±96.75
F	±125	±123.9	±121.8	±121.75
G	±150	±148.9	±146.8	±146.75
H	±200	±198.9	±196.8	±196.75
X	±400	±398.9	±396.8	±396.75
L	±600	±598.9	±596.8	±596.75
Y	±800	±798.9	±796.8	±796.75
S	±1200	±1198.9	±1196.8	±1196.75
Z	±1600	±1598.9	±1596.8	±1596.75
U	±3200	±3198.9	±3196.8	±3196.75

Notes:
13. APR includes initial tolerance, frequency stability vs. temperature, and the corresponding 20-year aging.