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SJA1105P/Q/R/S

Rev. 1 — 1 November 2017 Objective short data sheet

1 Features and benefits

1.1 General features

- 5-port store and forward architecture
- Each port individually configurable for 10/100 Mbit/s when operated as MII/RMII and 10/100/1000 Mbit/s when operated as RGMII or SGMII
- Independent I/O voltage domains: selectable 1.8/2.5/3.3 V operation for MII/RMII/RGMII; selectable 1.8/2.5/3.3 V for host interfacing; 1.2 V core voltage domains
- Small footprint: LFBGA159 (12 mm × 12 mm) package
- Automotive Grade 2 ambient operating temperature: -40 °C to +105 °C
- Automotive product qualification in accordance with AEC-Q100 Rev-H

1.2 Ethernet switching and AVB features

- IEEE 802.3 compliant
- IEEE 802.1Q defined tag support
- 4096 VLANs supported
- Priority-based QoS handling as specified in IEEE 802.1Q
- Hardware support for IEEE 802.1AS timestamping and IEEE 802.1Qav AVB traffic shaping
- 16 credit-based shapers available according to IEEE 802.1Qav; shapers can be freely allocated to any priority queue on a per port basis
- Support for SR Class A, Class B, and Class C traffic
- IEEE 1588v2 one-step sync forwarding in hardware
- Statistics for dropped frames and buffer load

1.3 Interface features

- MII/RMII for interfacing with 10/100 Mbit/s PHYs/host processor (Fast Ethernet)
- RGMII for interfacing with 10/100/1000 Mbit/s PHYs/host processor/cascading (Gigabit Ethernet); internal delay for interface connection without external delay components
- SGMII for interfacing with 10/100/1000 Mbit/s PHYs/host processor/cascading
- MAC and PHY modes for interfacing (MII/RMII/RGMII/SGMII) directly with another switch or host processor
- Programmable drive strength for MII/RMII/RGMII interfaces
- SPI for host processor access

1.4 Other features

- 25 MHz system clock input from crystal oscillator or AC-coupled single-ended clock
- 25 MHz reference clock output
- Device reset input from host processor
- Synchronization output for cascading devices
- IEEE 1149.1/1149.6 compliant JTAG interface for TAP controller access and BSCAN

2 Related documentation

For the full data sheet and application hints, please register with DocStore at https://www.docstore.nxp.com.

3 Ordering information

Table 1. Ordering information

Type number	Package		
	Name	Description	Version
SJA1105PEL [1]	LFBGA159	plastic low profile fine-pitch ball grid array package; 159 balls	SOT1427-1
SJA1105QEL [1]			
SJA1105REL			
SJA1105SEL			

[1] Pin compatible with SJA1105 and SJA1105T.

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NXP SJA1105 Ethernet Switch Series Selection Table

	Features	SJA1105	SJA1105T	SJA1105P	SJA1105Q	SJA1105R	SJA1105S	Benefits
Package and Interfaces	Operating temperature range: −40°C to +105°C (Automotive Grade 2)	●	●	●	●	●	●	Flexible ECU design by: • support for any type of Ethernet PHY such as 100/1000BASE-T1 and 1000BASE-TX • up to four cascaded switches controlled by a single host
	LFBGA159 12x12mm2, 0,8mm pitch	●	●	●	●	●	●	
	MII (3V3)/RMII (3V3)/RGMII (3V3) interfaces	●	●					
	MII/RMII/RGMII (all 1V8, 2V5, 3V3) interfaces			●	●	●	●	
	RGMII internal delay line			●	●	●	●	
	SGMII interface					●	●	
	Pin compatibility	●	●	●	●	○	○	
	Software compatibility	●	●	○	○	○	○	
Switching	Hash-based L2 look-up table	●	●					• Fine-grained control forwarding decisions in the network • Powerful debugging and diagnostic capabilities
	TCAM-based frame filtering			●	●	●	●	
	Double VLAN tagging support			●	●	●	●	
	RMON RFC 2819 Ethernet counters			●	●	●	●	
	VLAN-based egress tagging/un-tagging	●	●	●	●	●	●	
	Frame mirroring and diagnostic features	●	●	●	●	●	●	
AVB/TSN	Credit-based shaping blocks for IEEE802.1Qav	10	10	16	16	16	16	Key hardware features to enable the implementation of a fully synchronized network for: • lip-synched playback of audio and video streams • data-transmission scheduling for TSN networks
	IEEE802.1AS time stamping support	●	●	●	●	●	●	
	TSN IEEE802.1Qbv: time-aware shaping		●		●		●	
	TSN IEEE802.1Qci (pre-standard): per-stream policing*		●		●		●	
Security	Ingress rate limiting on a per-port and per-priority basis for unicast/multicast and broadcast traffic	●	●	●	●	●	●	Provisions for: • authentication of the nodes connected to the network • limit the data generated by one or more connected devices.
	Port reachability limitation and disabling address learning setting	●	●	●	●	●	●	
	MAC address white & black Listing			●	●	●	●	
	Support for IEEE 802.1X-based authentication mechanism	●	●	●	●	●	●	
	Learn process with “one-shot “option			●	●	●	●	

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4 Legal information

4.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
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