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DATA SHEET

SKY13278-313LF: GaAs SPDT Switch 100 MHz–2.5 GHz

Features

- Broadband: 100 MHz–2.5 GHz
- Very low insertion loss: 0.4 dB typ. @ 900 MHz
- High isolation: 26 dB typ. @ 900 MHz
- Low current consumption: <100 µA @ 3 V
- Miniature QFN-6 2 x 3 mm package
- Lead (Pb)-free and RoHS-compliant MSL-1 @ 260 °C per JEDEC J-STD-020

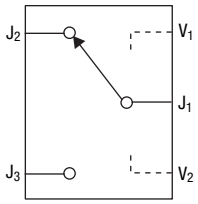
Description

The SKY13278-313LF is a pHEMT GaAs FET IC high linearity SPDT switch. This wideband switch has been designed for use from 100 MHz to 2.5 GHz, where extremely high linearity, low control voltage, high isolation, low insertion loss and ultra-miniature package size are required. It can be controlled with positive, negative or a combination of both voltages. The RF signal paths within the SKY13278-313LF are fully bilateral.

Some standard implementations include T/R switching and diversity switching over 3 W. The SKY13278-313LF switch can be used in many analog and digital wireless communication systems including cellular, GSM and UMTS applications.

Switching is controlled via two control voltage inputs. Depending upon the voltage level applied to the control voltage pins, the common RF port (J_1) is connected to one of two RF ports (J_2 or J_3) via a low insertion loss path, while the path between J_1 and the other RF port is in its isolation state. When the control voltages are toggled, the states between J_1 and J_2, as wells as J_1 and J_3, are also toggled.

Function Block Diagram



The SKY13278-313LF is available in a lead(Pb)-free, RoHS-compliant, QFN-6 2 x 3 mm plastic package.

An evaluation board is available upon request.

NEW Skyworks offers lead (Pb)-free, RoHS (Restriction of Hazardous Substances)-compliant packaging.

Electrical Specifications

V_{CTL} = 0/3 V, T = 25 °C, P_{INPUT} = 0 dBm, Z_0 = 50 Ω unless otherwise noted

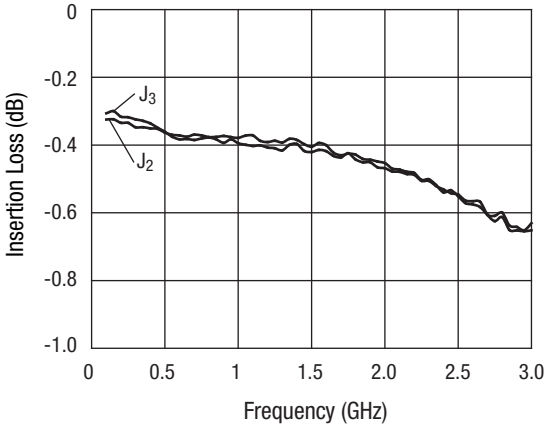
Parameter	Frequency	Min.	Typ.	Max.	Unit
Insertion loss	0.1–0.5 GHz		0.40	0.5	dB
	0.5–1.0 GHz		0.40	0.5	dB
	1.0–2.0 GHz		0.45	0.6	dB
	2.0–2.5 GHz		0.55	0.7	dB
Isolation	0.1–0.5 GHz	29	32		dB
	0.5–1.0 GHz	23	26		dB
	1.0–2.0 GHz	17	20		dB
	2.0–2.5 GHz	15	18		dB
Return loss (insertion loss state)	0.1–0.5 GHz		20		dB
Lower frequency return loss is dependent on DC blocks	1.0–2.0 GHz		20		dB

Operating Characteristics

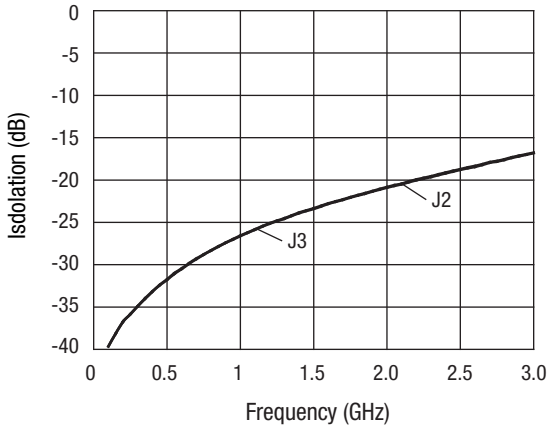
V_{CTL} = 0/3 V, T = 25 °C, P_{INPUT} = 0 dBm, Z_0 = 50 Ω unless otherwise noted

Parameter	Condition	Frequency	Min.	Typ.	Max.	Unit
Switching characteristics Rise, fall On, off	 10/90% or 90/10% RF 50% CTL to 90/10% RF			 650 800		 ns ns
Input power for 0.1 dB compression		900 MHz		40		dBm
Second, third harmonics	P_{IN} = 34.5 dBm, f_{IN} = 900 MHz			-75		dBc
Second, third harmonics	P_{IN} =32 dBm, f_{IN}= 1800 MHz			-70		dBc
Blocker performance	T_1 = 1950 MHz @ 20 dBm T_2 = 1760 MHz @ -15 dBm IMD3 measured at 2140 MHz			-105		dBm
Thermal resistance				45		°C/W
Control voltages	V_{LOW} = 0 V @ 20 µA maximum V_{HIGH} = 2.8 V @ 100 µA maximum to 5 V @ 200 µA maximum					

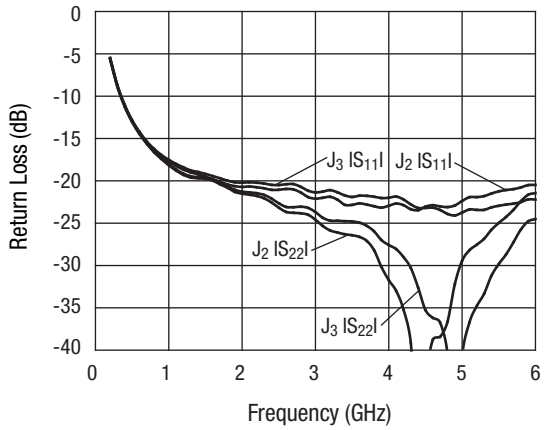
Typical Performance Data



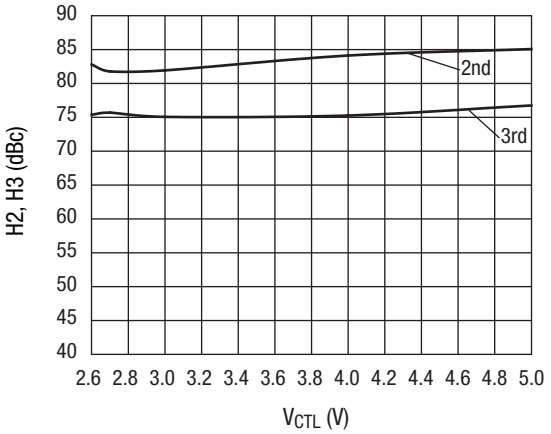
Insertion Loss vs. Frequency



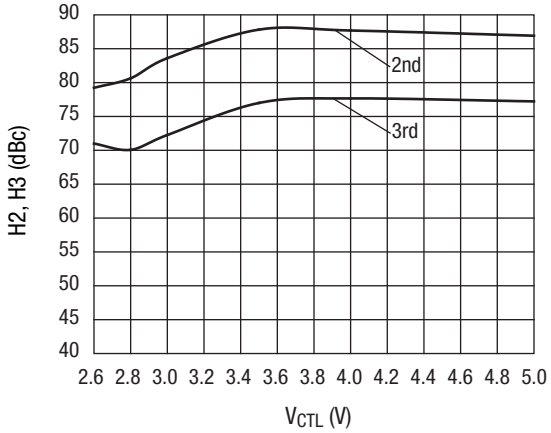
Isolation vs. Frequency



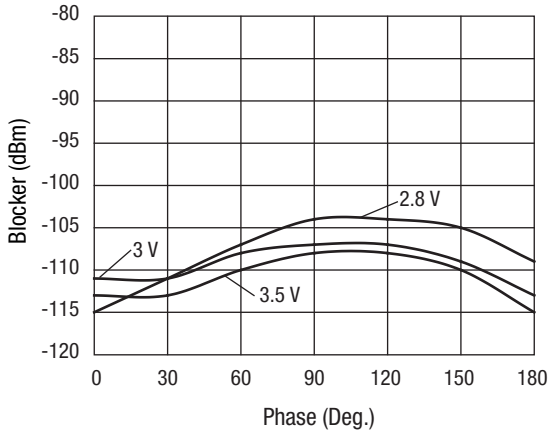
Return Loss vs. Frequency



Second and Third Harmonics vs. Control Voltage
F_{IN} = 900 MHz P_{IN} = 34.5 dBm



Second and Third Harmonics vs. Control Voltage
F_{IN} = 1800 MHz P_{IN} = 32 dBm



Blocker Performance vs. Phase
f1 = 1950 MHz, P_{IN} = +20 dBm
f2 = 1760 MHz, P_{IN} = -15 dBm
Blocker Measured at 2140 MHz

Truth Table

V_1	V_2	J_1–J_2	J_1–J_3
V_{LOW}	V_{HIGH}	Isolation	Insertion loss
V_{HIGH}	V_{LOW}	Insertion loss	Isolation
V_{LOW}	V_{LOW}	Not recommended(1)	
V_{HIGH}	V_{HIGH}	Not recommended(1)	

$2.8\ V \leq V_{HIGH} \leq 5\ V$, $0 \leq V_{LOW} \leq 0.2\ V$.
1. Switch is in an undefined state.

Recommended Solder Reflow Profiles

Refer to the *"Recommended Solder Reflow Profile"* Application Note.

Tape and Reel Information

Refer to the *"Discrete Devices and IC Switch/Attenuators Tape and Reel Package Orientation"* Application Note.

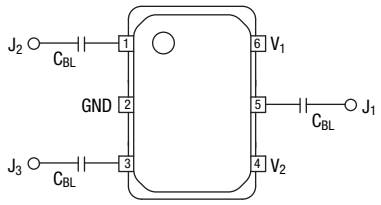
Absolute Maximum Ratings

Characteristic	Value
RF input power @ 5 V	10 W, f > 900 MHz @ 25 °C
Control voltage	$-0.2 \leq V_1, V_2 \leq 8\ V$
Operating temperature	-40 °C to +85 °C
Storage temperature	-65 °C to +150 °C

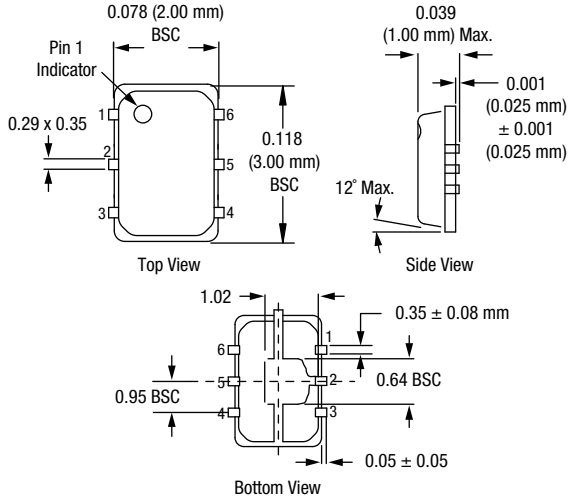
Performance is guaranteed only under the conditions listed in the specifications table and is not guaranteed under the full range(s) described by the Absolute Maximum specifications. Exceeding any of the absolute maximum/minimum specifications may result in permanent damage to the device and will void the warranty.

CAUTION: *Although this device is designed to be as robust as possible, ESD (Electrostatic Discharge) can damage this device. This device must be protected at all times from ESD. Static charges may easily produce potentials of several kilovolts on the human body or equipment, which can discharge without detection. Industry-standard ESD precautions must be employed at all times.*

Pin Out



QFN-6



Pin Descriptions

Pin Number	Pin Name	Description
1	J_2	RF Input/Output – RF input/output port which is either connected to J_1 via a low insertion loss path or isolated from J_1, according to the logic voltage levels applied to V_1 and V_2.
2	GND	Equipotential Point – Internal circuit common, which must be connected to the pcb ground or common via the lowest possible impedance.
3	J_3	RF Input/Output – RF input/output port which is either connected to J_1 via a low insertion loss path or isolated from J_1, according to the logic voltage levels applied to V_1 and V_2.
4	V_2	Control Voltage 2 – Control voltage input #2. The logic voltage level applied to this pin, along with the voltage level applied to V_1 (pin 6), determines the states of the RF paths between J_1–J_2 and J_1–J_3.
5	J_1	RF Common Input/Output – RF common input/output port which is either connected to J_2 or to J_3 via a low insertion loss and isolated from the other RF port, according to the logic voltage levels applied to V_1 and V_2.
6	V_1	Control Voltage 1 – Control voltage input #1. The logic voltage level applied to this pin, along with the voltage level applied to V_2 (pin 4), determines the states of the RF paths between J_1–J_2 and J_1–J_3.

Evaluation Board

The evaluation board for the SKY13278-313 allows the switch to be fully exercised. The RF common port is marked "J_1", and the two switched RF ports are marked "J_2" and "J_3". All of the RF ports have SMA connectors mounted. The control voltage inputs are marked "V_1" and "V_2".

The printed circuit board material is FR4. The RF dielectric layer is 0.012 inches thick, ½ oz. copper. The RF transmission lines are each 50 Ω (nominal) microstrip.

There are three DC blocking capacitors on the board, C_1, C_2 and C_3, each of which is in series with one of the RF ports. These capacitors are 47 pF. For improved insertion loss at signal frequencies below approximately 500 MHz these capacitors should be replaced with larger capacitance capacitors, such as 1000 pF.

Item	Description	Comments
C_1, C_2, C_3	DC Blocking Capacitor, 47 pF	0402
J_1, J_2, J_3	SMA Connector, Edge Mount	
U1	SKY13278-313	
Printed Circuit Board	Skyworks SK39990