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DATA SHEET

SKY72300-362: Spur-Free, 2.1 GHz Dual Fractional-N Frequency Synthesizer

Applications

- General purpose RF systems
- 2.5G and 3G wireless infrastructure
- Broadband wireless access
- Low bit rate wireless telemetry
- Instrumentation
- L-band receivers
- Satellite communications

Features

- Spur-free operation
- 2.1 GHz maximum operating frequency
- 500 MHz maximum auxiliary synthesizer
- Ultra-fine step size, 100 Hz or less
- High internal reference frequency enables large loop bandwidth implementations
- Very fast switching speed (e.g., below 100 μs)
- Phase noise to –91 dBc/Hz inside the loop filter bandwidth @ 1800 MHz
- Software programmable power-down modes
- High-speed serial interface up to 100 Mbps
- Three-wire programming
- Programmable division ratios on reference frequency
- Phase detectors with programmable gain to provide a programmable loop bandwidth
- Frequency power steering further enhances rapid acquisition time
- On-chip crystal oscillator
- Frequency adjust for temperature compensation

NEW

Skyworks offers lead (Pb)-free RoHS (Restriction of Hazardous Substances) compliant packaging.

- Direct digital modulation
- 3 V operation
- 5 V output to loop filter
- QFN (24-pin, 4 x 4 mm) Pb-free (MSL3, 260 °C per JEDEC J-STD-020) package

Description

Skyworks SKY72300-362 direct digital modulation fractional-N frequency synthesizer provides ultra-fine frequency resolution, fast switching speed, and low phase-noise performance. This synthesizer is a key building block for high-performance radio system designs that require low power and fine step size.

The ultra-fine step size of less than 100 Hz allows this synthesizer to be used in very narrowband wireless applications. With proper temperature sensing or through control channels, the synthesizer's fine step size can compensate for crystal oscillator or Intermediate Frequency (IF) filter drift. As a result, crystal oscillators or crystals can replace temperature-compensated or ovenized crystal oscillators, reducing parts count and associated component cost. The device's fine step size can also be used for Doppler shift corrections.

The SKY72300-362 has a phase noise floor of –90 dBc/Hz up to 2.1 GHz operation as measured inside the loop bandwidth. This is permitted by the on-chip low noise dividers and low divide ratios provided by the device's high fractionality.

Reference crystals or oscillators up to 50 MHz can be used with the SKY72300-362. The crystal frequency is divided down by independent programmable dividers (1 to 32) for the main and auxiliary synthesizers. The phase detectors can operate at a maximum speed of 25 MHz, which allows better phase noise due to the lower division value. With a high reference frequency, the loop bandwidths can also be increased. Larger loop bandwidths improve the settling times and reduce in-band phase noise. Therefore, typical switching times of less than 100 s can be achieved. The lower in-band phase noise also permits the use of lower cost Voltage Controlled Oscillators (VCOs) in customer applications.

The SKY72300-362 has a frequency power steering circuit that helps the loop filter to steer the VCO when the frequency is too fast or too slow, further enhancing acquisition time.

The unit operates with a three-wire, high-speed serial interface. A combination of large bandwidth, fine resolution, and the three-wire, high-speed serial interface allows for a direct frequency modulation of the VCO. This supports any continuous phase, constant envelope modulation scheme such as Frequency Modulation (FM), Frequency Shift Keying (FSK), Minimum Shift Keying (MSK), or Gaussian Minimum Shift Keying (GMSK).

This capability can eliminate the need for In-phase and Quadrature (I/Q) Digital-to-Analog Converters (DACs), quadrature upconverters, and IF filters from the transmitter portion of the radio system.

Figure 1 shows a functional block diagram for the SKY72300-362. The device package and pinout for the 24-pin Quad Flat No-Lead (QFN) package are shown in Figure 2.

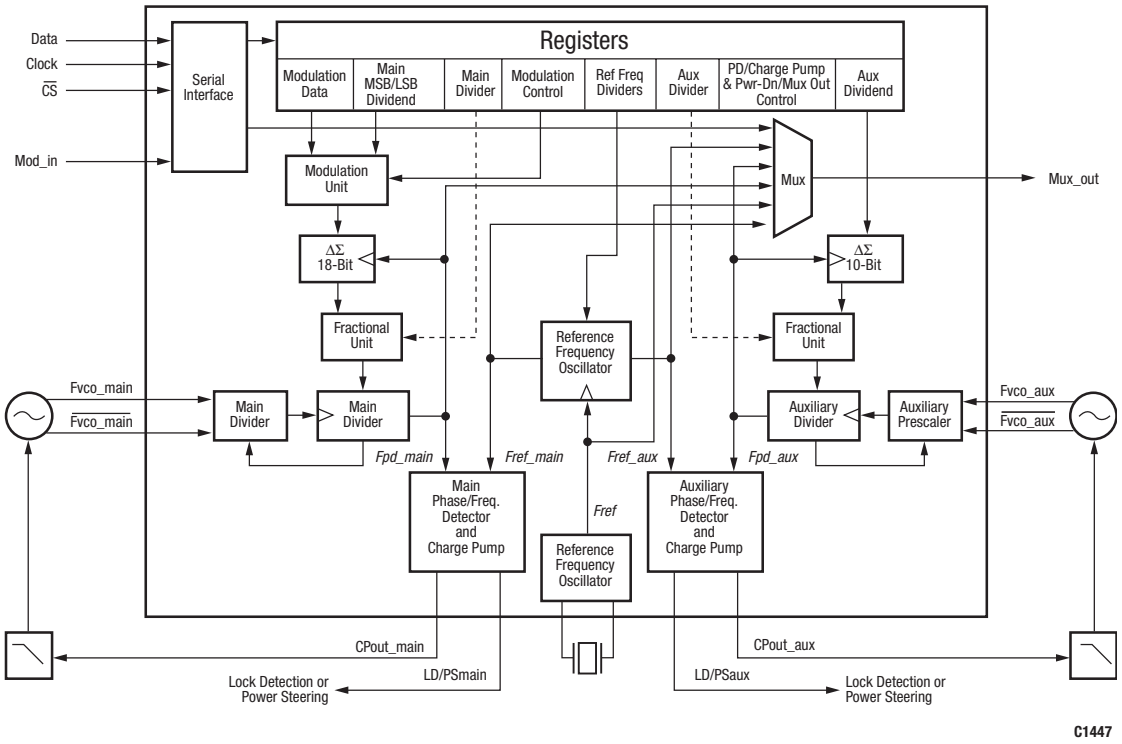

Figure 1. SKY72300-362 Functional Block Diagram

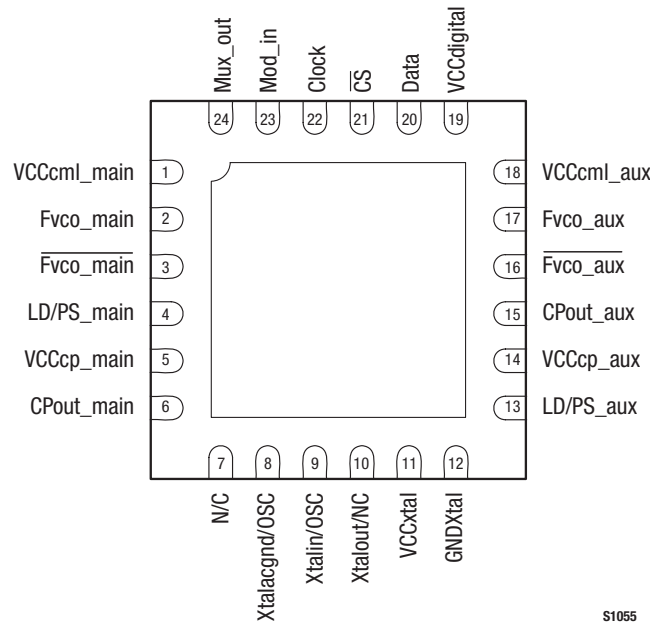

Figure 2. SKY72300-362 Pinout, 24-Pin QFN

Technical Description

The SKY72300-362 is a fractional-N frequency synthesizer using a $\Delta\Sigma$ modulation technique. The fractional-N implementation provides low in-band noise by having a low division ratio and fast frequency settling time. In addition, the SKY72300-362 provides arbitrarily fine frequency resolution with a digital word, so that the frequency synthesizer can be used to compensate for crystal frequency drift in the RF transceiver.

Serial Interface

The serial interface is a versatile three-wire interface consisting of three pins: Clock (serial clock), Data (serial input), and $\overline{CS}$ (chip select). It enables the SKY72300-362 to operate in a system where one or multiple masters and slaves are present. To perform a loopback test at startup and to check the integrity of the board and processor, the serial data is fed back to the master device (e.g., a microcontroller or microprocessor unit) through a programmable multiplexer. This facilitates hardware and software debugging.

Registers

There are ten 16-bit registers in the SKY72300-362. For more information, see the Register Descriptions section of this document.

Main and Auxiliary $\Delta\Sigma$ Modulators

The fractionality of the SKY72300-362 is accomplished by the use of a proprietary, configurable 10-bit or 18-bit $\Delta\Sigma$ modulator for the main synthesizer and 10-bit $\Delta\Sigma$ modulator for the auxiliary synthesizer.

Main and Auxiliary Fractional Units

The SKY72300-362 provides fractionality through the use of main and auxiliary $\Delta\Sigma$ modulators. The output from the modulators is combined with the main and auxiliary divider ratios through their respective fractional units.

VCO Prescalers

The VCO prescalers provide low-noise signal conditioning of the VCO signals. They translate from an off-chip, single-ended or differential signal to an on-chip differential Current Mode Logic (CML) signal. The SKY72300-362 has independent main and auxiliary VCO prescalers.

Main and Auxiliary VCO Dividers

The SKY72300-362 provides programmable dividers that control the CML prescalers and supply the required signals to the charge pump phase detectors. Programmable divide ratios ranging from 38 to 537 are possible in fractional-N mode and from 32 to 543 in integer-N mode.

Reference Frequency Oscillator

The SKY72300-362 has a self-contained, low-noise crystal oscillator. This crystal oscillator is followed by the clock generation circuitry that generates the required clock for the programmable reference frequency dividers.

Reference Frequency Dividers

The crystal oscillator signal can be divided by a ratio of 1 to 32 to create the reference frequencies for the phase detectors. The SKY72300-362 has both a main and an auxiliary frequency synthesizer, and provides independently configurable dividers of the crystal oscillator frequency for both the main and auxiliary phase detectors. The divide ratios are programmed by the Reference Frequency Dividers Register.

NOTE: *The divided crystal oscillator frequencies (which are the internal reference frequencies), Fref_main and Fref_aux, are referred to as reference frequencies throughout this document.*

Phase Detectors and Charge Pumps

The SKY72300-362 uses a separate charge pump phase detector for each synthesizer which provides a programmable gain, Kd, from 31.25 to 1000 $\mu A/2\pi$ radians in 32 steps programmed using the Phase Detector/Charge Pump Control Register.

Frequency Steering

When programmed for frequency power steering, the SKY72300-362 has a circuit that helps the loop filter steer the VCO, through the LD/PSmain signal (pin 4). In this configuration, the LD/PSmain signal can provide for more rapid acquisition.

When programmed for lock detection, internal frequency steering is implemented and provides frequency acquisition times comparable to conventional phase/frequency detectors.

Lock Detection

When programmed for lock detection, the SKY72300-362 provides an active low, pulsing open collector output using the LD/PSmain signal (pin 4) to indicate the out-of-lock condition. When locked, the LD/PSmain signal is tri-stated (high impedance).

Power Down

The SKY72300-362 supports a number of power-down modes through the serial interface. For more information, see the Register Descriptions section of this document.

Serial Interface Operation

The serial interface consists of three pins: Clock (pin 22), Data (pin 20), and $\overline{CS}$ (pin 21). The Clock signal controls data on the two serial data lines (Data and $\overline{CS}$). The Data pin bits shift into a temporary register on the rising edge of Clock. The $\overline{CS}$ line allows individual selection transfers that synchronize and sample the information of slave devices on the same bus.

Figure 3 depicts how a serial transfer takes place functionally.

A serial transfer is initiated when a microcontroller or microprocessor forces the $\overline{CS}$ line to a low state. This is followed immediately by an address/data stream sent to the Data pin that coincides with the rising edges of the clock presented on the Clock line.

Each rising edge of the Clock signal shifts in one bit of data on the Data line into a shift register. At the same time, one bit of data is shifted out of the Mux_out pin (if the serial bit stream is selected) at each falling edge of Clock. To load any of the registers, 16 bits of address or data must be presented to the Data line with the LSB last while the $\overline{CS}$ signal is low. If the $\overline{CS}$ signal is low for more than 16 clock cycles, only the last address or data bits are used to load the registers.

If the $\overline{CS}$ signal is brought to a high state before the 13th Clock edge, the bit stream is assumed to be modulation data samples. In this case, it is assumed that no address bits are present and that all the bits in the stream should be loaded into the Modulation Data Register.

Register Programming

Register programming equations, described in this section, use the following variables and constants:

$N_{fractional}$	Desired VCO division ratio in fractional-N applications. This is a real number and can be interpreted as the reference frequency (F_{ref}) multiplying factor such that the resulting frequency is equal to the desired VCO frequency.
$N_{integer}$	Desired VCO division ratio in integer-N applications. This number is an integer and can be interpreted as the reference frequency (F_{ref}) multiplying factor so that the resulting frequency is equal to the desired VCO frequency.
N_{reg}	Nine-bit unsigned input value to the divider ranging from 0 to 511 (integer-N mode) and from 6 to 505 (fractional-N mode).
divider	This constant equals 262144 when the $\Delta\Sigma$ modulator is in 18-bit mode, and 1024 when the $\Delta\Sigma$ modulator is in 10-bit mode.
dividend	When in 18-bit mode, this is the 18-bit signed input value to the $\Delta\Sigma$ modulator, ranging from –131072 to +131071 and providing 262144 steps, each step equal to $F_{div\_ref}/2^{18}$ Hz. When in 10-bit mode, this is the 10-bit signed input value to the $\Delta\Sigma$ modulator, ranging from –512 to +511 and providing 1024 steps, each step equal to $F_{div\_ref}/2^{10}$ Hz.

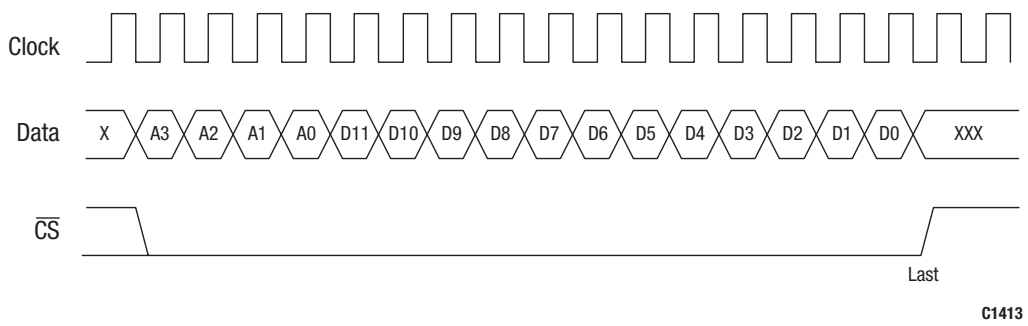

Figure 3. Serial Transfer Timing Diagram

F_{VCO} Desired VCO frequency (either F_{vco_main} or F_{vco_aux}).

F_{div_ref} Divided reference frequency presented to the phase detector (either F_{ref_main} or F_{ref_aux}).

Fractional-N Applications. The desired division ratio for the main and auxiliary synthesizers is given by:

$$N_{fractional} = \frac{F_{VCO}}{F_{div\_ref}}$$

where $N_{fractional}$ must be between 37.5 and 537.5.

The value to be programmed by the Main or Auxiliary Divider Register is given by:

$$N_{reg} = Round(N_{fractional}) - 32$$

NOTE: *The Round function rounds the number to the nearest integer.*

When in fractional mode, allowed values for N_{reg} are from 6 to 505 inclusive.

The value to be programmed by either of the MSB/LSB Dividend Registers or the Auxiliary Dividend Register is given by:

$$dividend = Round[divider \times (N_{fractional} - N_{reg} - 32)]$$

where the divider is either 1024 in 10-bit mode or 262144 in 18-bit mode. Therefore, the dividend is a signed binary value either 10 or 18 bits long.

NOTE: *Because of the high fractionality of the SKY72300-362, there is no practical need for any integer relationship between the reference frequency and the channel spacing or desired VCO frequencies.*

Sample calculations for two fractional-N applications are provided in Figure 4.

Integer-N Applications. The desired division ratio for the main or auxiliary synthesizer is given by:

$$N_{integer} = \frac{F_{vco\_main}}{F_{div\_ref}}$$

where $N_{integer}$ is an integer number from 32 to 543.

The value to be programmed by the Main or Auxiliary Divider Register is given by:

$$N_{reg} = N_{integer} - 32$$

When in integer mode, allowed values for N_{reg} are from 0 to 511 for both the main and auxiliary synthesizers.

NOTE: *As with all integer-N synthesizers, the minimum step size is related to the crystal frequency and reference frequency division ratio.*

A sample calculation for an integer-N application is provided in Figure 5.

Register Loading Order. In applications where the main synthesizer is in 18-bit mode, the Main Dividend MSB Register holds the 10 MSBs of the dividend and the Main Dividend LSB Register holds the 8 LSBs of the dividend. The registers that control the main synthesizer's divide ratio are to be loaded in the following order:

- Main Divider Register
- Main Dividend LSB Register
- Main Dividend MSB Register (at which point the new divide ratio takes effect)

In applications where the main synthesizer is in 10-bit mode, the Main Dividend MSB Register holds the 10 bits of the dividend. The registers that control the main synthesizer's divide ratio are to be loaded in the following order:

- Main Divider Register
- Main Dividend MSB Register (at which point the new divide ratio takes effect)

Case 1: To achieve a desired F_{vco_main} frequency of 902.4530 MHz using a crystal frequency of 40 MHz with operation of the synthesizer in 18-bit mode. Since the maximum internal reference frequency (F_{div_ref}) is 25 MHz, the crystal frequency is divided by 2 to obtain a F_{div_ref} of 20 MHz. Therefore:

$$N_{fractional} = \frac{F_{vco\_main}}{F_{div\_ref}}$$

$$= \frac{902.4530}{20}$$

$$= 45.12265$$

The value to be programmed in the Main Divider Register is:

$$N_{reg} = \text{Round}[N_{fractional}] - 32$$

$$= \text{Round}[45.12265] - 32$$

$$= 45 - 32$$

$$= 13 \text{ (decimal)}$$

$$= 000001101 \text{ (binary)}$$

With the modulator in 18-bit mode, the value to be programmed in the Main Dividend Registers is:

$$\text{dividend} = \text{Round}[\text{divider} \times (N_{fractional} - N_{reg} - 32)]$$

$$= \text{Round}[262144 \times (45.12265 - 13 - 32)]$$

$$= \text{Round}[262144 \times (0.12265)]$$

$$= \text{Round}[32151.9616]$$

$$= 32152 \text{ (decimal)}$$

$$= 000111110110011000 \text{ (binary)}$$

where 00 0111 1101 is loaded in the MSB of the Main Dividend Register and 1001 1000 is loaded in the LSB of the Main Dividend Register.

Summary:

- Main Divider Register = 0 0000 1101
- Main Dividend Register, LSB = 1001 1000
- Main Dividend Register, MSB = 00 0111 1101
- The resulting main VCO frequency is 902.453 MHz
- Step size is 76.3 Hz

Note: The frequency step size for this case is 20 MHz divided by 2^{18}, giving 76.3 Hz.

C1414

Figure 4. Fractional-N Applications: Sample Calculation (1 of 2)

Case 2: To achieve a desired F_{vco_main} frequency of 917.7786 MHz using a crystal frequency of 19.2 MHz with operation of the synthesizer in 10-bit mode. Since the maximum internal reference frequency (F_{div_ref}) is 25 MHz, the crystal frequency does not require the internal division to be greater than 1, which makes F_{div_ref} = 19.2 MHz. Therefore:

$$N_{fractional} = \frac{F_{vco\_main}}{F_{div\_ref}}$$

$$= \frac{917.7786}{19.2}$$

$$= 47.80097$$

The value to be programmed in the Main Divider Register is:

$$N_{reg} = \text{Round}[N_{fractional}] - 32$$

$$= \text{Round}[47.80087] - 32$$

$$= 48 - 32$$

$$= 16 \text{ (decimal)}$$

$$= 000010000 \text{ (binary)}$$

With the modulator in 10-bit mode, the value to be programmed in the Main Dividend Registers is:

$$\text{dividend} = \text{Round}[\text{divider} \times (N_{fractional} - N_{reg} - 32)]$$

$$= \text{Round}[1024 \times (47.80087 - 16 - 32)]$$

$$= \text{Round}[1024 \times (-0.1990312)]$$

$$= \text{Round}[-203.808]$$

$$= 204 \text{ (decimal)}$$

$$= 1100110100 \text{ (binary)}$$

where 11 0011 0100 is loaded in the MSB of the Main Dividend Register.

Summary:

- Main Divider Register = 0 0001 0000
- Main Dividend Register, MSB = 11 0011 0100
- The resulting main VCO frequency is 917.775 MHz
- Step size is 18.75 kHz

Note: The frequency step size for this case is 19.2 MHz divided by 2^{10}, giving 18.75 kHz.

C1415

Figure 4. Fractional-N Applications: Sample Calculation (2 of 2)

Case 1: To achieve a desired F_{vco_aux} frequency of 400 MHz using a crystal frequency of 16 MHz. Since the minimum divide ratio is 32, the reference frequency (F_{div_ref}) must be a maximum of 12.5 MHz. Choosing a reference frequency divide ratio of 2 provides a reference frequency of 8 MHz. Therefore:

$$N_{integer} = \frac{F_{vco\_aux}}{F_{div\_ref}}$$

$$= \frac{400}{8}$$

$$= 50$$

The value to be programmed in the Auxiliary Divider Register is:

$$N_{reg} = N_{integer} - 32$$

$$= 50 - 32$$

$$= 18 \text{ (decimal)}$$

$$= 000010010 \text{ (binary)}$$

Summary:

- Auxiliary Divide Register = 0 0001 0010

C1416

Figure 5. Integer-N Applications: Sample Calculation

For the auxiliary synthesizer, the Auxiliary Dividend Register holds the 10 bits of the dividend. The registers that control the auxiliary synthesizer's divide ratio are to be loaded in the following order:

- Auxiliary Divider Register
- Auxiliary Dividend Register (at which point the new divide ratio takes effect)

NOTE: *When in integer mode, the new divide ratios take effect as soon as the Main or Auxiliary Divider Register is loaded.*

Direct Digital Modulation

The high fractionality and small step size of the SKY72300-362 allow the user to tune to practically any frequency in the VCO's operating range. This allows direct digital modulation by programming the different desired frequencies at precise instants. Typically, the channel frequency is programmed by the Main Divider and MSB/LSB Dividend Registers, and the instantaneous frequency offset from the carrier is programmed by the Modulation Data Register.

The Modulation Data Register can be accessed in three ways as defined in the following subsections.

Normal Register Write. A normal 16-bit serial interface write occurs when the $\overline{CS}$ signal is 16 clock cycles wide. The corresponding 16-bit modulation data is simultaneously presented to the Data pin. The content of the Modulation Data Register is passed to the modulation unit at the next falling edge of the divided main VCO frequency (F_{pd_main}).

Short $\overline{CS}$ Through Data Pin (No Address Bits Required). A shortened serial interface write occurs when the $\overline{CS}$ signal is from 2 to 12 clock cycles wide. The corresponding modulation data (2 to 12 bits) is simultaneously presented to the Data pin. The Data pin is the default pin used to enter modulation data directly in the Modulation Data Register with shortened $\overline{CS}$ strobes.

This method of data entry eliminates the register address overhead on the serial interface. All serial interface bits are re-synchronized internally at the reference oscillator frequency. The content of the Modulation Data Register is passed to the modulation unit at the next falling edge of the divided main VCO frequency (F_{pd_main}).

Short $\overline{CS}$ Through Mod_in Pin (No Address Bits Required). A shortened serial interface write occurs when the $\overline{CS}$ signal is from 2 to 12 clock cycles wide. The corresponding modulation data (2 to 12 bits) is simultaneously presented on the Mod_in pin, an alternate pin used to enter modulation data directly into the Modulation Data Register with shortened $\overline{CS}$ strobes. This mode is selected through the Modulation Control Register.

Table 1. SKY72300-362 Register Map

Address (Hex)	Register (Note 1)	Length (Bits)	Address (Bits)
0	Main Divider Register	12	4
1	Main Dividend MSB Register	12	4
2	Main Dividend LSB Register	12	4
3	Auxiliary Divider Register	12	4
4	Auxiliary Dividend Register	12	4
5	Reference Frequency Dividers Register	12	4
6	Phase Detector/Charge Pump Control Register	12	4
7	Power Down/Multiplexer Output Select Control Register	12	4
8	Modulation Control Register	12	4
9	Modulation Data Register	12	4
—	Modulation Data Register (Note 2) — direct input	2 ≤ length ≤ 12 bits	0

Note 1: All registers are write only.

Note 2: No address bits are required for modulation data. Any serial data between 2 and 12 bits long is considered modulation data.

This method of data entry also eliminates the register address overhead on the serial interface and allows a different device than the one controlling the channel selection to enter the modulation data (e.g., a microcontroller for channel selection and a digital signal processor for modulation data).

All serial interface bits are internally re-synchronized at the reference oscillator frequency and the content of the Modulation Data Register is passed to the modulation unit at the next falling edge of the divided main VCO frequency (F_{pd_main}).

Modulation data samples in the Modulation Data Register can be from 2 to 12 bits long, and enable the user to select how many distinct frequency steps are to be used for the desired modulation scheme.

The user can also control the frequency deviation through the modulation data magnitude offset in the Modulation Control Register. This allows shifting of the modulation data to accomplish a 2^m multiplication of frequency deviation.

NOTE: *The programmable range of –0.5 to +0.5 of the main ΔΣ modulator can be exceeded up to the condition where the sum of the dividend and the modulation data conform to:*

$$-0.5625 \le (N_{mod} + dividend) \le +0.5625$$

When the sum of the dividend and modulation data lie outside this range, the value of $N_{integer}$ must be changed.

For a more detailed description of direct digital modulation functionality, refer to the Skyworks Application Note, *Direct Digital Modulation Using the SKY72300, SKY72301, and SKY72302 Dual Synthesizers/PLLs* (document number 101349).

Register Descriptions

Table 1 lists the 10 16-bit registers that are used to program the SKY72300-362. All register writes are programmed address first, followed directly with data. MSBs are entered first. On power up, all registers are reset to 0x000 except registers at addresses 0x0 and 0x3, which are set to 0x006.

Main Synthesizer Registers

The Main Divider Register contains the integer portion closest to the desired fractional-N (or the integer-N) value minus 32 for the main synthesizer. This register, in conjunction with the Main Dividend MSB and LSB Registers (which control the fraction offset from –0.5 to +0.5), allows selection of a precise frequency. As shown in Figure 6, the value to be loaded is:

- Main Synthesizer Divider Index = Nine-bit value for the integer portion of the main synthesizer dividers. Valid values for this register are from 6 to 505 (fractional-N) or 0 to 511 (integer-N).

The Main Dividend MSB and LSB Registers control the fraction part of the desired fractional-N value and allow an offset of –0.5 to +0.5 to the main integer selected through the Main Divider Register. As shown in Figures 7 and 8, values to be loaded are:

- Main Synthesizer Dividend (MSBs) = Ten-bit value for the MSBs of the 18-bit dividend for the main synthesizer.
- Main Synthesizer Dividend (LSBs) = Eight-bit value for the LSBs of the 18-bit dividend for the main synthesizer.

The Main Dividend Register MSB and LSB values are 2's complement format.

NOTE: *When in 10-bit mode, the Main Dividend LSB Register is not required.*

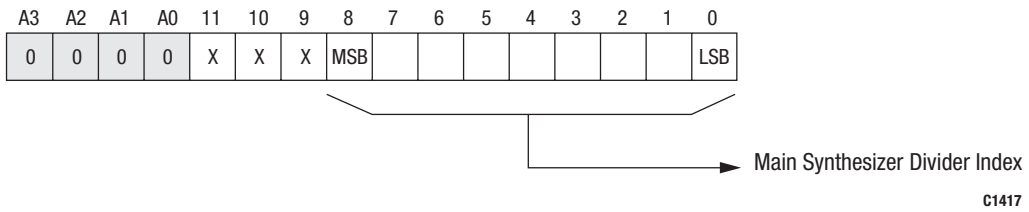

Figure 6. Main Divider Register (Write Only)

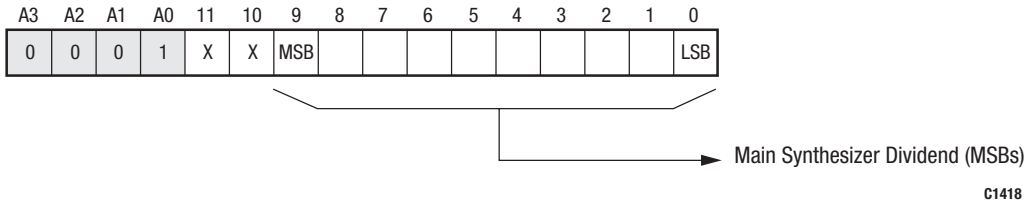

Figure 7. Main Dividend MSB Register (Write Only)

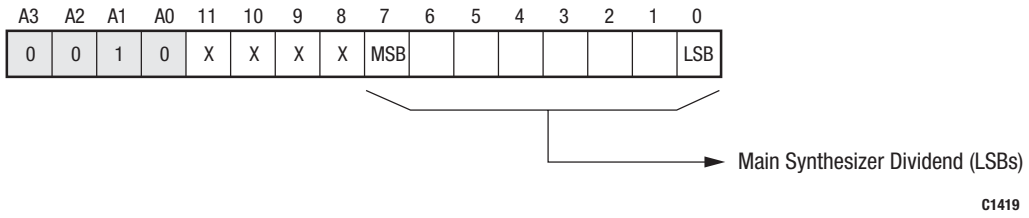

Figure 8. Main Dividend LSB Register (Write Only)

Auxiliary Synthesizer Registers

The Auxiliary Divider Register contains the integer portion closest to the desired fractional-N (or integer-N) value minus 32 for the auxiliary synthesizer. This register, in conjunction with the Auxiliary Dividend Register (which controls the fraction offset from –0.5 to +0.5), allows selection of a precise frequency. As shown in Figure 9, the value to be loaded is:

Auxiliary Synthesizer Divider Index = Nine-bit value for the integer portion of the auxiliary synthesizer dividers. Valid values for this register are from 6 to 505 (fractional-N) or from 0 to 511 (integer-N).The Auxiliary Dividend Register controls the fraction part of the desired fractional-N value and allows an offset of –0.5 to +0.5 to the auxiliary integer selected through the Auxiliary Divider Register. As shown Figure 10, the value to be loaded is:

- Auxiliary Synthesizer Dividend = Ten-bit value for the auxiliary synthesizer dividend.

General Synthesizer Registers

The dual-programmable reference frequency dividers provide the reference frequencies to the phase detectors by dividing the crystal oscillator frequency. The lower five bits hold the reference frequency divide index for the main phase detector. The next five bits hold the reference frequency divide index for the auxiliary phase detector. Divide ratios from 1 to 32 are possible for each reference frequency divider (see Tables 2 and 3).

The Reference Frequency Dividers Register configures the dual-programmable reference frequency dividers for the main and auxiliary synthesizers. As shown in Figure 11, the values to be loaded are:

- Main Reference Frequency Divider Index = Desired main oscillator frequency division ratio –1. Default value on power up is 0, signifying that the reference frequency is not divided for the main phase detector.
- Auxiliary Reference Frequency Divider Index = Desired auxiliary oscillator frequency division ratio –1. Default value on power up is 0, signifying that the reference frequency is not divided for the auxiliary phase detector.

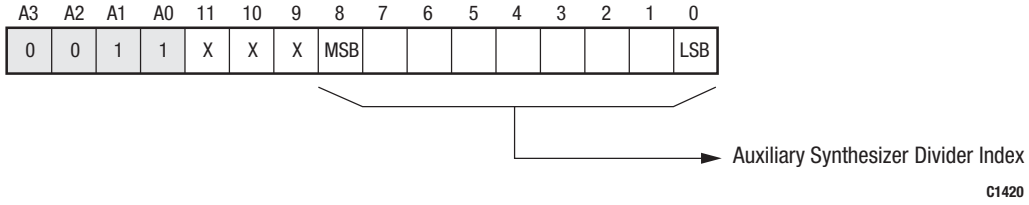

Figure 9. Auxiliary Divider Register (Write Only)

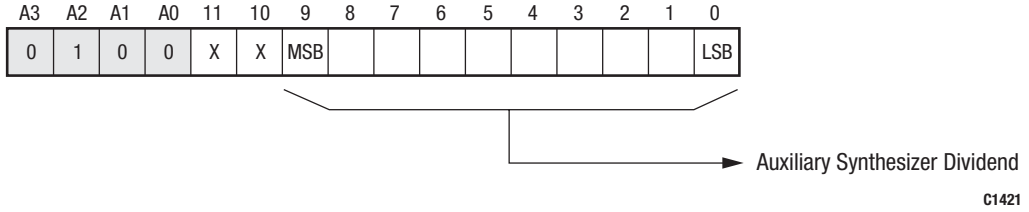

Figure 10. Auxiliary Dividend Register (Write Only)

Table 2. Programming the Main Reference Frequency Divider

Decimal	Bit 4 (MSB)	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)	Reference Divider Ratio
0	0	0	0	0	0	1
1	0	0	0	0	1	2
2	0	0	0	1	0	3
—	—	—	—	—	—	—
—	—	—	—	—	—	—
—	—	—	—	—	—	—
31	1	1	1	1	1	32

Table 3. Programming the Auxiliary Reference Frequency Divider

Decimal	Bit 9 (MSB)	Bit 8	Bit 7	Bit 6	Bit 5 (LSB)	Reference Divider Ratio
0	0	0	0	0	0	1
1	0	0	0	0	1	2
2	0	0	0	1	0	3
—	—	—	—	—	—	—
—	—	—	—	—	—	—
—	—	—	—	—	—	—
31	1	1	1	1	1	32

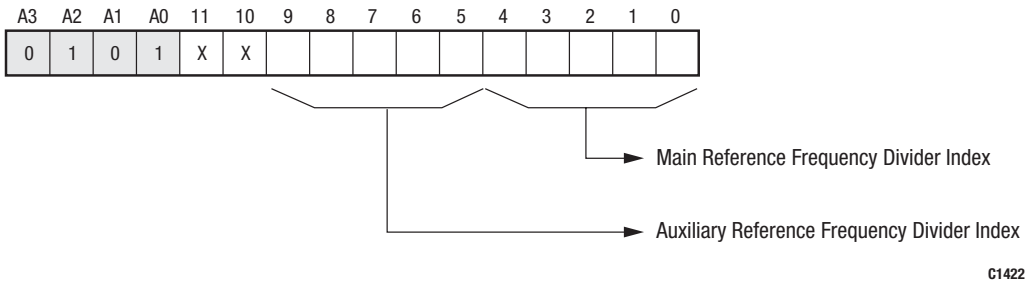

Figure 11. Reference Frequency Dividers Register (Write Only)

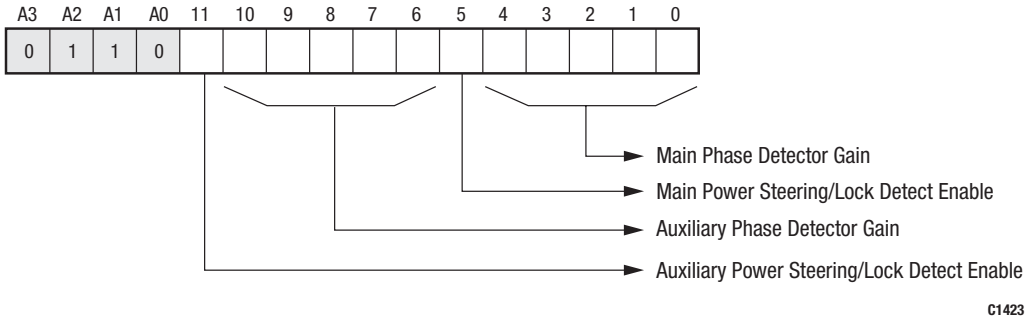

Figure 12. Phase Detector/Charge Pump Control Register (Write Only)

The Phase Detector/Charge Pump Control Register allows control of the gain for both phase detectors and configuration of the LD/PSmain and LD/PSaux signals for frequency power steering or lock detection. As shown in Figure 12, the values to be loaded are:

- Main Phase Detector Gain = Five-bit value for programmable main phase detector gain. Range is from 0 to 31 decimal for 31.25 to 1000 μA/ 2π radian, respectively.
- Main Power Steering Enable = One-bit flag to enable the frequency power steering circuitry of the main phase detector. When this bit is cleared, the LD/PSmain pin is configured to be a lock detect, active low, open collector pin. When this bit is set, the LD/PSmain pin is configured to be a frequency power steering pin and can be used to bypass the external main loop filter to provide faster frequency acquisition.
- Auxiliary Phase Detector Gain = Five-bit value for programmable auxiliary phase detector gain. Range is from 0 to 31 decimal for 31.25 to 1000 μA/2π radians, respectively.
- Auxiliary Power Steering Enable = One-bit flag to enable the frequency power steering circuitry of the auxiliary phase detector. When this bit is cleared, the LD/PSaux pin is configured to be a lock detect, active low, open collector pin. When this bit is set, the LD/PSaux pin is configured to be a frequency power steering pin and may be used to bypass the external auxiliary loop filter to provide faster frequency acquisition.

The Power Down/Multiplexer Output Select Control Register allows control of the power-down modes, internal multiplexer output, and main ΔΣ synthesizer fractionality. As shown in Figure 13, the values to be loaded are:

- Full Power Down = One-bit flag to power down the SKY72300-362 except for the reference oscillator and the serial interface. When this bit is cleared, the SKY72300-362 is powered up. When this bit is set, the SKY72300-362 is in full power-down mode excluding the Mux_out signal (pin 24).
- Main Synthesizer Power Down = One-bit flag to power down the main synthesizer. When this bit is cleared, the main synthesizer is powered up. When this bit is set, the main synthesizer is in power-down mode.
- Main Synthesizer Mode = One-bit flag to power down the main synthesizer's ΔΣ modulator and fractional unit to operate as an integer-N synthesizer. When this bit is cleared, the main synthesizer is in fractional-N mode. When this bit is set, the main synthesizer is in integer-N mode.

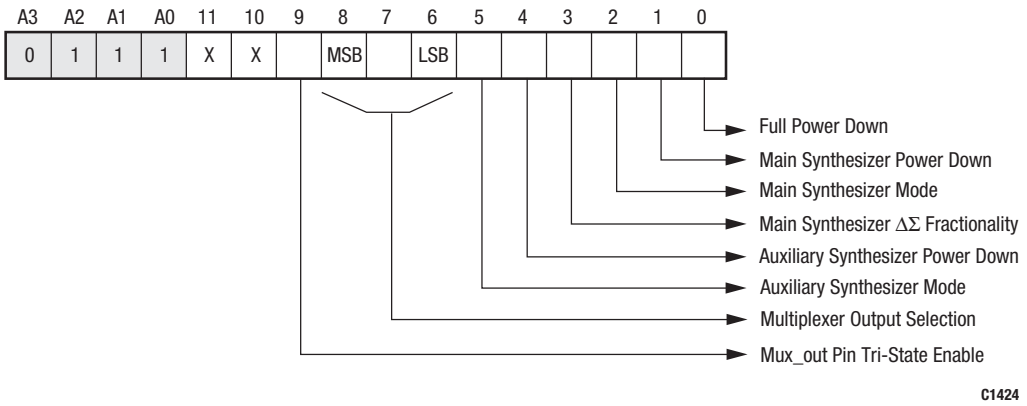

Figure 13. Power Down and Multiplexer Output Register (Write Only)

Table 4. Multiplexer Output

Multiplexer Output Select (Bit 8)	Multiplexer Output Select (Bit 7)	Multiplexer Output Select (Bit 6)	Multiplexer Output (Mux_out)
0	0	0	Reference Oscillator
0	0	1	Auxiliary Reference Frequency (F_{ref_aux})
0	1	0	Main Reference Frequency (F_{ref_main})
0	1	1	Auxiliary Phase Detector Frequency (F_{pd_aux})
1	0	0	Main Phase Detector Frequency (F_{pd_main})
1	0	1	Serial data out
1	1	0	Serial interface test output
1	1	1	Unused

- Main Synthesizer $\Delta\Sigma$ Fractionality = One-bit flag to configure the size of the main $\Delta\Sigma$ modulator. This has a direct effect on power consumption, and on the level of fractionality and step size. When this bit is cleared, the main $\Delta\Sigma$ modulator is 18-bit with a fractionality of 2^{18} and a step size of F_{ref_main}/262144. When this bit is set, the main $\Delta\Sigma$ modulator is 10-bit with a fractionality of 2^{10} and a step size of F_{ref_main}/1024.
- Auxiliary Synthesizer Power Down = One-bit flag to power down the auxiliary synthesizer. When this bit is cleared, the auxiliary synthesizer is powered up. When this bit is set, the auxiliary synthesizer is in power-down mode.
- Auxiliary Synthesizer Mode = One-bit flag to power down the auxiliary synthesizer's $\Delta\Sigma$ modulator and fractional unit to operate as an integer-N synthesizer. When this bit is cleared, the auxiliary synthesizer is in fractional-N mode. When this bit is set, the auxiliary synthesizer is in integer-N mode.

NOTE: *There are no special power-up sequences required for the SKY72300-362.*

- Multiplexer Output Selection = Three-bit value that selects which internal signal is output to the Mux_out pin. The following internal signals are available on this pin:
  - Reference oscillator: F_{ref}
  - Main or auxiliary divided reference (post-reference frequency main or auxiliary dividers): F_{ref_main} or F_{ref_aux}
  - Main or auxiliary phase detector frequency (post-main or auxiliary frequency dividers): F_{pd_main} or F_{pd_aux}
  - Serial data out for loop-back and test purposes

  Refer to Table 4 for more information.
- Mux_out Pin Tri-State Enable = One-bit flag to tri-state the Mux_out pin. When this bit is cleared, the Mux_out pin is enabled. When this bit is set, the Mux_out pin is tri-stated.

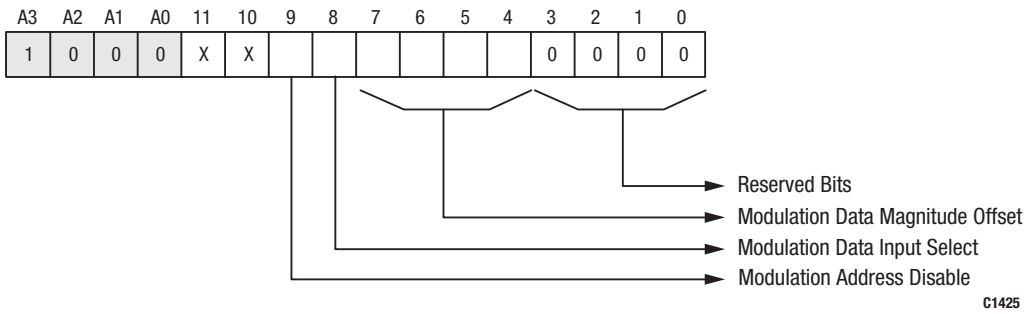

Figure 14. Modulation Control Register (Write Only)

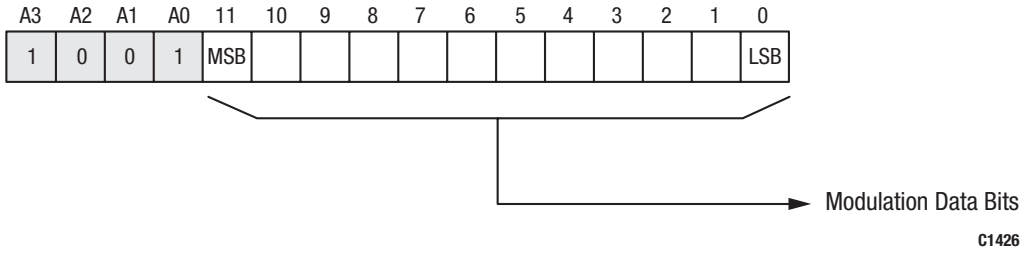

Figure 15. Modulation Data Register (Write Only)

The Modulation Control Register is used to configure the modulation unit of the main synthesizer. The modulation unit adds or subtracts a frequency offset to the selected center frequency at which the main synthesizer operates. The size of the modulation data sample, controlled by the duration of the $\overline{CS}$ signal, can be from 2 to 12 bits wide to provide from 4 to 4096 selectable frequency offset steps.

The modulation data magnitude offset selects the magnitude multiplier for the modulation data and can be from 0 to 8. As shown in Figure 14, the values to be loaded are:

- Modulation Data Magnitude Offset = Four-bit value that indicates the magnitude multiplier (m) for the modulation data samples. Valid values range from 0 to 13, effectively providing a 2^m multiplication of the modulation data sample.
- Modulation Data Input Select = One-bit flag to indicate the pin on which modulation data samples are serially input when the $\overline{CS}$ signal is between 2 and 12 bits long. When this bit is cleared, modulation data samples are to be presented on the Data pin. When this bit is set, modulation data samples are to be presented on the Mod_in pin.
- Modulation Address Disable = One-bit flag to indicate the presence of the address as modulation data samples are presented on either the Mod_in or Data pins. When this bit is cleared, the address is presented with the modulation data samples (i.e., all transfers are 16 bits long). When this bit is set, no address is presented with the modulation data samples (i.e., all transfers are 2 to 12 bits long).

The Modulation Data Register is used to load the modulation data samples to the modulation unit. These values are transferred to the modulation unit on the falling edge of F_{pd_main} where they are passed to the main $\Delta\Sigma$ modulator at the selected magnitude offset on the next falling edge of F_{pd_main}. Modulation Data Register values are 2's complement format. As shown in Figure 15, the value to be loaded is:

- Modulation Data Bits = Modulation data samples that represent the instantaneous frequency offset to the selected main synthesizer frequency (selected channel) before being affected by the modulation data magnitude offset.

Package and Handling Information

Since the device package is sensitive to moisture absorption, it is baked and vacuum packed before shipping. Instructions on the shipping container label regarding exposure to moisture after the container seal is broken must be followed. Otherwise, problems related to moisture absorption may occur when the part is subjected to high temperature during solder assembly.

The SKY72300-362 is rated to Moisture Sensitivity Level 3 (MSL3) at 260 °C. It can be used for lead or lead-free soldering.

Care must be taken when attaching this product, whether it is done manually or in a production solder reflow environment.

Production quantities of this product are shipped in a standard tape and reel format. For packaging details, refer to the Skyworks Application Note, Tape and Reel, document number 101568.

Electrical and Mechanical Specifications

The SKY72300-362 is supplied as a 24-pin QFN. The exposed pad is located on the bottom side of the package and must be connected to ground for proper operation. The exposed pad should be soldered directly to the circuit board.

Signal pin assignments and functional pin descriptions are described in Table 5. The absolute maximum ratings of the SKY72300-362 are provided in Table 6. The recommended operating conditions are specified in Table 7 and electrical specifications are provided in Table 8.

Figure 16 provides a schematic diagram for the SKY72300-362. Figure 17 shows the package dimensions for the 24-pin QFN and Figure 18 provides the tape and reel dimensions.

Electrostatic Discharge (ESD) Sensitivity

The SKY72300-362 is a static-sensitive electronic device. Do not operate or store near strong electrostatic fields. Take proper ESD precautions.

Table 5. SKY72300-362 Signal Descriptions (1 of 2)

Pin #	Pin Name	Type	Description
1	VCCcml_main	Power and ground	Emitter Coupled Logic/Current Mode Logic (ECL/CML), 3 V. Removing power safely powers down the associated divider chain and charge pump.
2	Fvco_main	Input	Main VCO differential input.
3	$\overline{\text{Fvco\_main}}$	Input	Main VCO complimentary differential input.
4	LD/PS_main	Analog output	Programmable output pin. Indicates phase detector out-of-lock as an active low pulsing open collector output (high impedance when lock is detected), or helps the loop filter steer the VCO. This pin is configured using the Phase Detector/Charge Pump Control Register.
5	VCCcp_main (Note 1)	Power and ground	Charge pump supply, 3 to 5 V. Removing power safely powers down the associated divider chain and charge pump.
6	CPout_main	Analog output	Charge pump output. The gain of the charge pump phase detector is controlled by the Phase Detector/Charge Pump Control Register.
7	N/C	–	No connection
8	Xtalacgnd/OSC	Ground/input	Reference crystal AC ground or external oscillator differential input.
9	Xtalin/OSC	Input	Reference crystal input or external oscillator differential input.
10	Xtalout/NC	Input	Reference crystal output or no connect.
11	VCCxtal	Power and ground	Crystal oscillator ECL/CML, 3 V.
12	GNDxtal	Power and ground	Crystal oscillator ground.
13	LD/PS_aux	Analog output	Programmable output pin. Indicates auxiliary phase detector out-of-lock as an active low pulsing open collector output (high impedance when lock is detected), or helps the loop filter steer the auxiliary VCO. This pin is configured using the Phase Detector/Charge Pump Control Register.
14	VCCcp_aux (Note 1)	Power and ground	Auxiliary charge pump supply, 3 to 5 V. Removing power safely powers down the associated divider chain and charge pump.
15	CPout_aux	Analog output	Auxiliary charge pump output. The gain of the auxiliary charge pump phase detector is controlled by the Phase Detector/Charge Pump Control Register.
16	$\overline{\text{Fvco\_aux}}$	Input	Auxiliary VCO complimentary differential input.
17	Fvco_aux	Input	Auxiliary VCO differential input.
18	VCCcml_aux (Note 1)	Power and ground	ECL/CML, 3 V. Removing power safely powers down the associated divider chain and charge pump.
19	VCCdigital (Note 1)	Power and ground	Digital supply, 3 V.
20	Data	Digital input	Serial address and data input pin. Address bits are followed by data bits.

Table 5. SKY72300-362 Signal Descriptions (2 of 2)

Pin #	Pin Name	Type	Description
21	$\overline{CS}$	Digital input	Active low enable pin. Enables loading of address and data on the Data pin on the rising edge of Clock. When $\overline{CS}$ goes high, data is transferred to the register indicated by the address. Subsequent clock edges are ignored.
22	Clock	Digital input	Clock signal pin. When $\overline{CS}$ is low, the register address and data are shifted in address bits first on the Data pin on the rising edge of Clock.
23	Mod_in	Digital input	Alternate serial modulation data input pin. Address bits are followed by data bits.
24	Mux_out	Digital output	Internal multiplexer output. Selects from oscillator frequency, reference frequency, divided VCO frequency, serial data out, or testability signals. This pin can be tri-stated from the synthesizer registers.

Note 1: Associated pairs of power and ground pins must be decoupled using 0.1 µF capacitors.

Table 6. Absolute Maximum Ratings

Parameter	Min	Max	Units
Maximum analog RF supply voltage		3.6	VDC
Maximum digital supply voltage		3.6	VDC
Maximum charge pump supply voltage		5.25	VDC
Storage temperature	–65	+150	°C
Operating temperature	–40	+85	°C

Note: Exposure to maximum rating conditions for extended periods may reduce device reliability. There is no damage to device with only one parameter set at the limit and all other parameters set at or below their nominal values.

Table 7. Recommended Operating Conditions

Parameter	Min	Max	Units
Analog RF supplies	2.7	3.3	VDC
Digital supply	2.7	3.3	VDC
Charge pump supplies	2.7	5.0 (Note 1)	VDC
Operating temperature (T_A)	–40	+85	°C

Note 1: When power steering is enabled, the charge pump must be 4.5 V maximum.

Table 8. Electrical Characteristics (1 of 2)
(VDD = 3 V, T_A = 25 °C, Unless Otherwise Noted)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Power Consumption						
Total power consumption	P_{TOTAL}	Charge pump currents of 200 µA. Both synthesizers fractional, F_{REF_MAIN} = 20 MHz, F_{REF_AUX} = 1 MHz		37.5		mW
		Auxiliary synthesizer power down		27		mW
Power-down current	I_{CC_PWDN}			10 (Note 1)		µA
Reference Oscillator						
Reference oscillator frequency	F_{OSC}				50	MHz
Oscillator sensitivity (as a buffer)	V_{OSC}	AC coupled, single-ended	0.1		2.0	Vpp
Frequency shift versus supply voltage	F_{SHIFT_SUPPLY}	2.7 V ≤ V_{XTAL} ≤ 3.3 V			±0.3	ppm

Table 8. Electrical Characteristics (2 of 2)
(VDD = 3 V, T_A = 25 °C, Unless Otherwise Noted)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
VCOs						
Main synthesizer operating frequency	F_{VCO_MAIN}	Sinusoidal, –40 °C to +85 °C	100 (Note 2)		2100	MHz
Auxiliary synthesizer operating frequency	F_{VCO_AUX}	Sinusoidal, –40 °C to +85 °C	100 (Note 2)		500	MHz
RF input sensitivity	V_{VCO}	AC coupled	50		250	mV_{PEAK}
RF input impedance	Z_{VCO_IN}			94 – j140 @ 1200 MHz		Ω
Main fractional-N tuning step size	ΔF_{STEP_MAIN}		$F_{REF\_MAIN}/2^{18}$ or $F_{REF\_MAIN}/2^{10}$			Hz
Auxiliary fractional-N tuning step size	ΔF_{STEP_AUX}		$F_{REF\_AUX}/2^{10}$			Hz
Noise						
Phase noise floor	P_{NF}	Measured inside the loop bandwidth using 25 MHz reference frequency, –40 °C to +85 °C		–128 + 20 Log (N)		dBc/Hz
Phase Detectors and Charge Pumps						
Main phase detector frequency	F_{REF_MAIN}	–40 °C to +85 °C			25	MHz
Auxiliary phase detector frequency	F_{REF_AUX}	–40 °C to +85 °C			25	MHz
Charge pump output source current	$I_{CP\text{-}SOURCE}$	V_{CP} = 0.5 VCC_{CP}	125		1000	µA
Charge pump output sink current	$I_{CP\text{-}SINK}$	V_{CP} = 0.5 VCC_{CP}	–125		–1000	µA
Charge pump accuracy	$I_{CP\text{-}ACCURACY}$			±20		%
Charge pump output voltage linearity range	I_{CP} vs V_{CP}	0.5 V ≤ V_{CP} ≤ (VCC_{CP} – 0.5 V)	GND + 400		VCC_{CP} – 400	mV
Charge pump current versus temperature	I_{CP} vs T	V_{CP} = 0.5 VCC_{CP} –40 °C < T < +85 °C			5	%
Charge pump current versus voltage	I_{CP} vs V_{CP}	0.5 V ≤ V_{CP} ≤ (VCC_{CP} – 0.5 V)			8	%
Digital Pins						
High level input voltage	V_{IH}		0.7 $V_{DIGITAL}$			V
Low level input voltage	V_{IL}				0.3 $V_{DIGITAL}$	V
High level output voltage	V_{OH}	I_{OH} = –2 mA	$V_{DIGITAL}$ –0.2			V
Low level output voltage	V_{OL}	I_{OL} = +2 mA			GND + 0.2	V
Timing – Serial Interface						
Clock frequency	f_{CLOCK}				100	MHz
Data and $\overline{CS}$ set up time to Clock rising	t_{SU}		3			ns
Data and $\overline{CS}$ hold time after Clock rising	t_{HOLD}		0			ns

Note 1: A 5 V charge pump power supply (on pin 5) results in higher power-down leakage current.

Note 2: The minimum synthesizer frequency is 12 x F_{OSC}, where F_{OSC} is the frequency at the Xtalin/OSC pin.

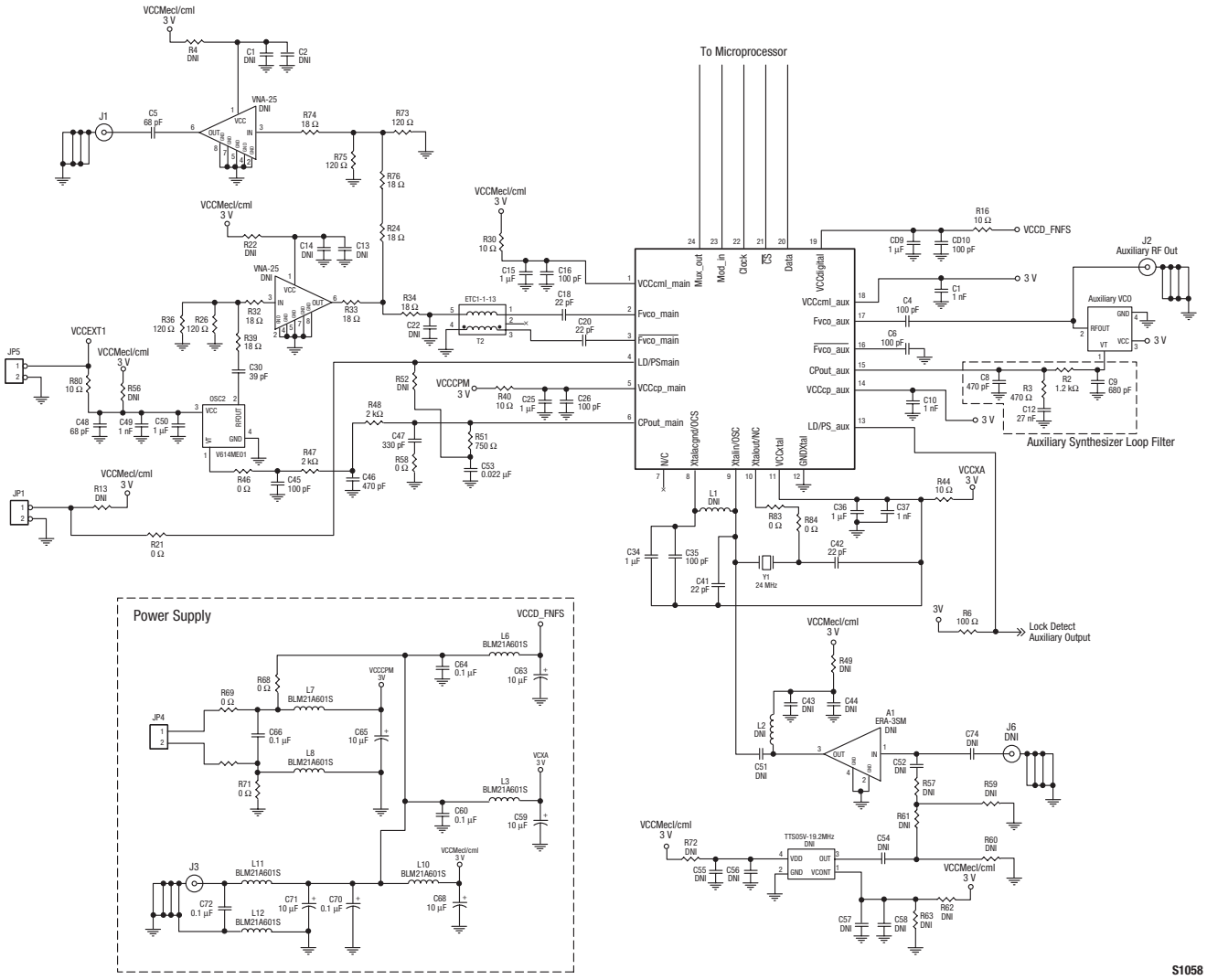

Figure 16. SKY72300-362 Application Schematic

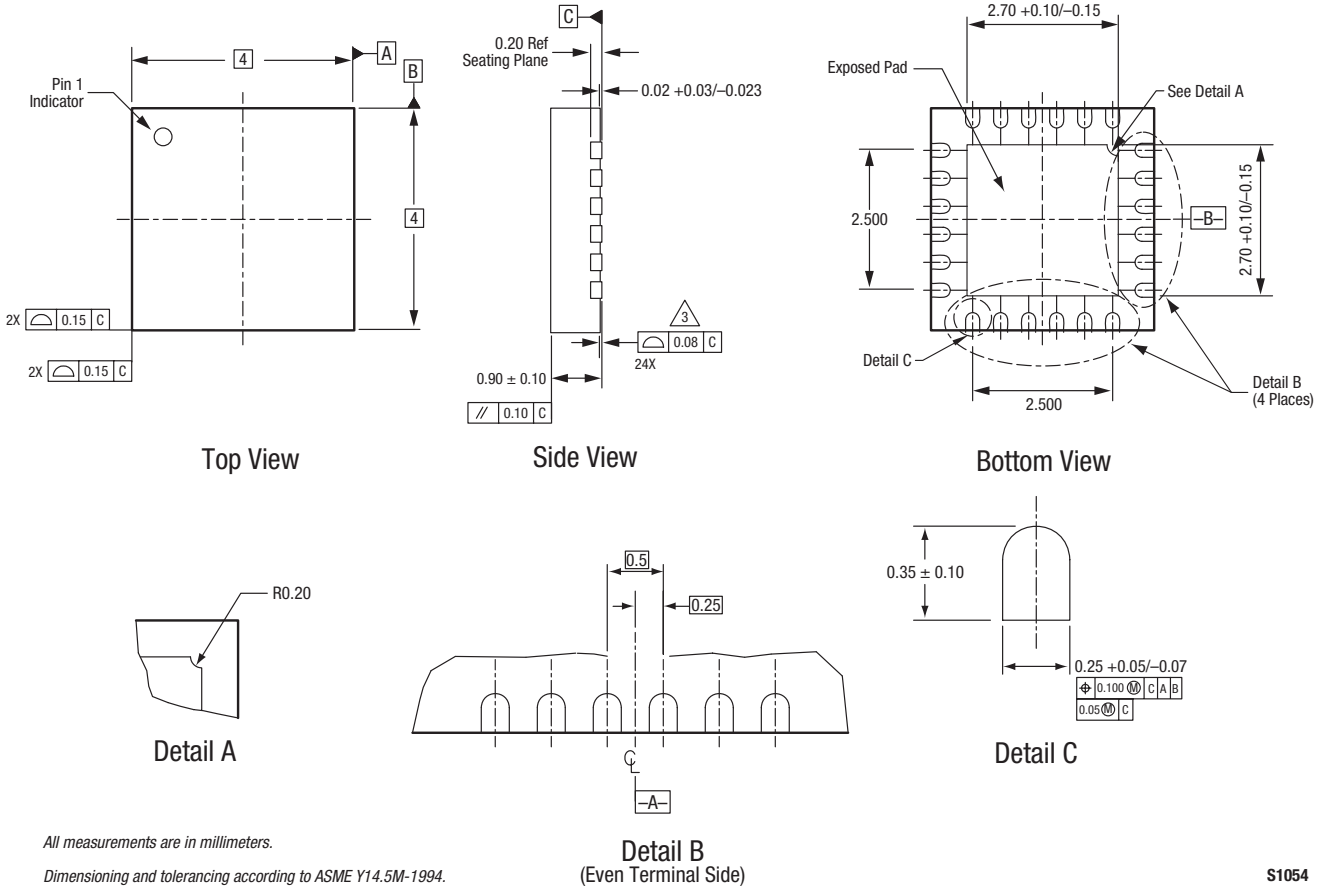

Figure 17. SKY72300-362 24-Pin QFN Package Dimensions

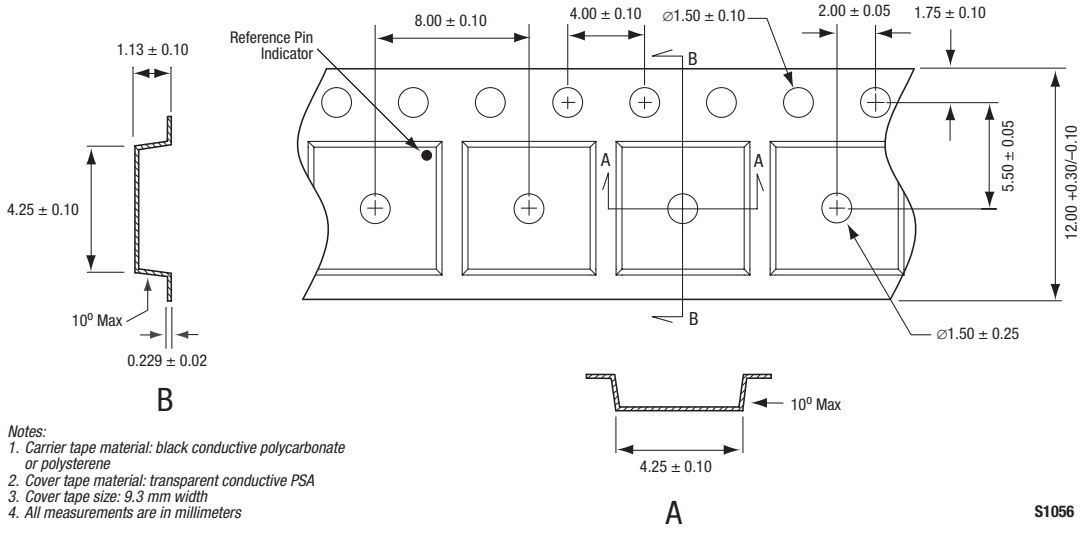

Figure 18. SKY72300-362 Tape and Reel Dimensions

Ordering Information

Model Name	Manufacturing Part Number	Evaluation Kit Part Number
SKY72300-362 2.1 GHz Frequency Synthesizer	SKY72300-362 (Pb-free package)	TW14-D790