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SL28EB742

EPROCLOCK® GENERATOR FOR INTEL® CK505 COMPLIANCE

Features

- Compliant Intel CK505 Clock spec
- Low power push-pull type differential output buffers
- Integrated resistors on differential clocks
- Wireless friendly 3-bits slew rate control on single-ended clocks
- Differential CPU clocks with pin selectable frequency
- 100 MHz Differential SRC clocks
- Selectable Differential SATA or SRC clocks
- 96 MHz Differential DOT clock
- 48 MHz USB clock
- Selectable 12 or 48 MHz clock
- 25 MHz ouput
- Buffered Reference Clock 14.318 MHz
- 14.318 MHz Crystal Input or Clock input
- I^2C support with readback capabilities
- Triangular Spread Spectrum profile for maximum electromagnetic interference (EMI) reduction
- Industrial Temperature: –40 to 85 °C
- 3.3 V power supply
- 56-pin QFN package

Ordering Information:
See page 39

Selectable Differential SRC or CPU Clock

CPU	SRC	SATA	DOT96	48M	48M/ 12M	33M	25M	14.318M
x2/x3	x4/x7	x0/x1	x1	x1/2	x1	x2	x1	x1

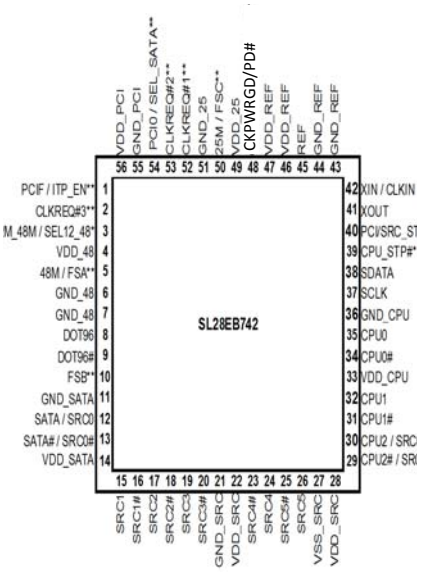
EProClock® Programmable Technology

- > 4000 bits of configurations
- Can be configured through SMBus or hard coded
- Custom frequency sets
- Differential skew control on true or compliment or both
- Differential duty cycle control on true or compliment or both
- Differential amplitude control
- Differential and single-ended slew rate control
- Program Internal or External series resistor on single-ended clocks
- Program different spread profiles
- Program different spread modulation rate

Selectable Differential SRC or CPU Clock

CPU	SRC	SATA	DOT96	48M	48M/ 12M	33M	25M	14.318M
x2/x3	x4/x7	x0/x1	x1	x1/2	x1	x2	x1	x1

Pin Assignments



* Internal 100K-ohm pull-up resistor
** Internal 100K-ohm pull down resistor

Patents pending

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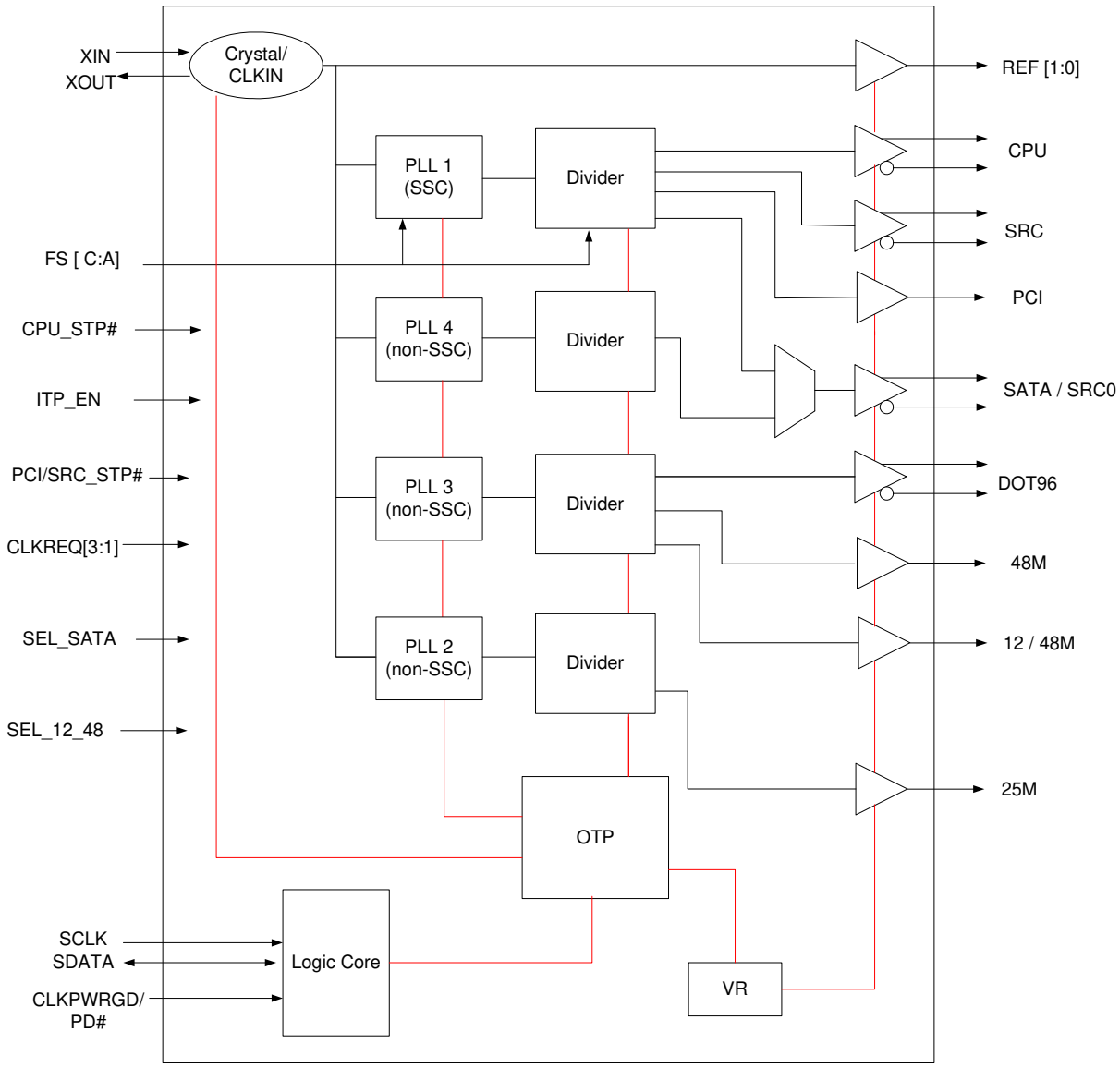
This information applies to a product under development. Its characteristics and specifications are subject to change without notice.

Description

The SL28EB742 is a high-performance clock generator supporting Intel Cedarview platforms. The SL28EB742 is rated to support extended grade temperature. Utilizing an inexpensive 14.318 MHz crystal, it is capable of supporting multiple frequencies from four PLLs. The CPU clock can support a frequency range from 83.33 to 166 MHz by configuration of two strap pins. With a combination of strap pins and an I^2C interface, the device allows maximum configurability.

EProClock® is the world's first non-volatile programmable clock. The EProClock® technology allows board designer to promptly achieve optimum compliance and clock signal integrity; historically, attainable typically through device and/or board redesigns. EProClock® technology can be configured through SMBus or hard coded.

Functional Block Diagram



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1. Electrical Specifications

Table 1. Recommended Operating Conditions

(VDD = 3.3 V, T_A = 25 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Supply Voltage (extended)	$VDD_{(industrial)}$	3.3 V ±5%	3.13	3.3	3.46	V
Supply Voltage (commercial)	$VDD_{(commercial)}$	3.3 V ±10%	2.97	3.3	3.63	V

Table 2. DC Electrical Specifications

Parameter	Symbol	Test Condition	Min	Max	Unit
3.3 V Operating Voltage	VDD core	3.3 ± 5%	3.135	3.465	V
3.3 V Input High Voltage (SE)	V_{IH}		2.0	V_{DD} + 0.3	V
3.3 V Input Low Voltage (SE)	V_{IL}		V_{SS} – 0.3	0.8	V
Input High Voltage	V_{IHI2C}	SDATA, SCLK	2.2	—	V
Input Low Voltage	V_{ILI2C}	SDATA, SCLK	—	1.0	V
FS Input High Voltage	V_{IH_FS}		0.7	VDD+0.3	V
FS Input Low Voltage	V_{IL_FS}		V_{SS} – 0.3	0.35	V
Input High Leakage Current	I_{IH}	Except internal pull-down resistors, $0 < V_{IN} < V_{DD}$	—	5	µA
Input Low Leakage Current	I_{IL}	Except internal pull-up resistors, $0 < V_{IN} < V_{DD}$	–5	—	µA
3.3 V Output High Voltage (SE)	V_{OH}	I_{OH} = –1 mA	2.4	—	V
3.3 V Output Low Voltage (SE)	V_{OL}	I_{OL} = 1 mA	—	0.4	V
High-impedance Output Current	I_{OZ}		–10	10	µA
Input Pin Capacitance	C_{IN}		1.5	5	pF
Output Pin Capacitance	C_{OUT}			6	pF
Pin Inductance	L_{IN}		—	7	nH
Power Down Current	IDD_PD		—	1	mA
Dynamic Supply Current	$IDD\_3.3\ V$	All outputs enabled. SE clocks with 5” traces. Differential clocks with 5” traces. Loading per CK505 spec.	—	115	mA

Table 3. AC Electrical Specifications

Parameter	Symbol	Test Condition	Min	Max	Unit
Long-term Accuracy	L_{ACC}	Measured at VDD/2 differential	—	250	ppm
Clock Input					
CLKIN Duty Cycle	T_{DC}	Measured at VDD/2	47	53	%
CLKIN Rise and Fall Times	T_R/T_F	Measured between 0.2 V_{DD} and 0.8 V_{DD}	0.5	4.0	V/ns
CLKIN Cycle to Cycle Jitter	T_{CCJ}	Measured at VDD/2	—	250	ps
CLKIN Long Term Jitter	T_{LTJ}	Measured at VDD/2		350	ps
Input High Voltage	V_{IH}	XIN / CLKIN pin	2	VDD+0.3	V
Input Low Voltage	V_{IL}	XIN / CLKIN pin	—	0.8	V
Input High Current	I_{IH}	XIN / CLKIN pin, VIN = VDD		35	µA
Input Low Current	I_{IL}	XIN / CLKIN pin, 0 < VIN <0.8	–35	—	µA
CPU at 0.7 V					
CPU Duty Cycle	T_{DC}	Measured at 0 V differential	45	55	%
83.33 MHz CPU Period	T_{PERIOD}	Measured at 0 V differential at 0.1s	11.99880	12.00120	ns
83.33 MHz CPU Period, SSC	$T_{PERIODSS}$	Measured at 0 V differential at 0.1s	12.028872	12.03128	ns
83.33 MHz CPU Absolute Period	$T_{PERIODAbs}$	Measured at 0 V differential at 1clock	11.18969	12.16344	ns
83.33 MHz CPU Absolute Period, SSC	$T_{PERIODSSAbs}$	Measured at 0 V differential at 1 clock	11.89687	12.16344	ns
100 MHz CPU Period	T_{PERIOD}	Measured at 0 V differential at 0.1s	9.99900	10.0010	ns
100 MHz CPU Period, SSC	$T_{PERIODSS}$	Measured at 0 V differential at 0.1s	10.02406	10.02607	ns
100 MHz CPU Absolute Period	$T_{PERIODAbs}$	Measured at 0 V differential at 1clock	9.87400	10.1260	ns
100 MHz CPU Absolute Period, SSC	$T_{PERIODSSAbs}$	Measured at 0 V differential at 1 clock	9.87406	10.1762	ns
133 MHz CPU Period	T_{PERIOD}	Measured at 0 V differential at 0.1s	7.49925	7.50075	ns
133 MHz CPU Period, SSC	$T_{PERIODSS}$	Measured at 0 V differential at 0.1s	7.51804	7.51955	ns
133 MHz CPU Absolute Period	$T_{PERIODAbs}$	Measured at 0 V differential at 1 clock	7.41425	7.58575	ns
133 MHz CPU Absolute period, SSC	$T_{PERIODSSAbs}$	Measured at 0 V differential at 1 clock	7.41430	7.62340	ns

Table 3. AC Electrical Specifications (Continued)

Parameter	Symbol	Test Condition	Min	Max	Unit
166 MHz CPU Period	T_{PERIOD}	Measured at 0 V differential at 0.1s	5.99940	6.00060	ns
166 MHz CPU Period, SSC	$T_{PERIODSS}$	Measured at 0 V differential at 0.1s	6.01444	6.01564	ns
166 MHz CPU Absolute period	$T_{PERIODAbs}$	Measured at 0 V differential at 1 clock	5.91440	6.08560	ns
166 MHz CPU Absolute period, SSC	$T_{PERIODSSAbs}$	Measured at 0 V differential at 1 clock	5.91444	6.11572	ns
CPU Cycle to Cycle Jitter	T_{CCJ}	Measured at 0 V differential	—	85	ps
CPU Cycle to Cycle Jitter for CPU 2	$T_{CCJ\ (CPU2)}$	Measured at 0 V differential	—	125	ps
CPU0 to CPU1 skew	Skew	Measured at 0 V differential	—	100	ps
Long-term Accuracy	L_{ACC}	Measured at 0 V differential	—	100	ppm
CPU Rising/Falling Slew rate	T_R / T_F	Measured differentially from ±150 mV	2.5	8	V/ns
Rise/Fall Matching	T_{RFM}	Measured single-endedly from ±75 mV	—	20	%
Voltage High	V_{HIGH}			1.15	V
Voltage Low	V_{LOW}		–0.3	—	V
Crossing Point Voltage at 0.7 V Swing	V_{OX}		300	550	mV
SRC at 0.7 V					
SRC Duty Cycle	T_{DC}	Measured at 0 V differential	45	55	%
100 MHz SRC Period	T_{PERIOD}	Measured at 0 V differential at 0.1s	9.99900	10.0010	ns
100 MHz SRC Period, SSC	$T_{PERIODSS}$	Measured at 0 V differential at 0.1s	10.02406	10.02607	ns
100 MHz SRC Absolute Period	$T_{PERIODAbs}$	Measured at 0 V differential at 1 clock	9.87400	10.1260	ns
100 MHz SRC Absolute Period, SSC	$T_{PERIODSSAbs}$	Measured at 0 V differential at 1 clock	9.87406	10.1762	ns
Any SRC Clock Skew from the earliest bank to the latest bank	$T_{SKEW(window)}$	Measured at 0 V differential	—	3.0	ns
SRC Cycle to Cycle Jitter	T_{CCJ}	Measured at 0 V differential	—	85	ps
SRC Long Term Accuracy	L_{ACC}	Measured at 0 V differential	—	100	ppm
SRC Rising/Falling Slew Rate	T_R / T_F	Measured differentially from ±150 mV	2.5	8	V/ns

Table 3. AC Electrical Specifications (Continued)

Parameter	Symbol	Test Condition	Min	Max	Unit
Rise/Fall M-atching	T_{RFM}	Measured single-endedly from ±75 mV	—	20	%
Voltage High	V_{HIGH}			1.15	V
Voltage Low	V_{LOW}		–0.3	—	V
Crossing Point Voltage at 0.7 V Swing	V_{OX}		300	550	mV
DOT96 at 0.7 V					
DOT96 Duty Cycle	T_{DC}	Measured at 0 V differential	45	55	%
DOT96 Period	T_{PERIOD}	Measured at 0 V differential at 0.1s	10.4156	10.4177	ns
DOT96 Absolute Period	$T_{PERIODAbs}$	Measured at 0 V differential at 0.1s	10.1656	10.6677	ns
DOT96 Cycle to Cycle Jitter	T_{CCJ}	Measured at 0 V differential at 1 clock	—	250	ps
DOT96 Long Term Accuracy	L_{ACC}	Measured at 0V differential at 1 clock	—	100	ppm
DOT96 Rising/Falling Slew Rate	T_R / T_F	Measured differentially from ±150 mV	2.5	8	V/ns
Rise/Fall Matching	T_{RFM}	Measured single-endedly from ±75 mV	—	20	%
Voltage High	V_{HIGH}			1.15	V
Voltage Low	V_{LOW}		–0.3	—	V
Crossing Point Voltage at 0.7 V Swing	V_{OX}		300	550	mV
SATA at 0.7 V					
SATAM Duty Cycle	T_{DC}	Measured at 0V differential	45	55	%
SATA Cycle to Cycle Jitter	T_{CCJ}	Measured at 0V differential at 1 clock	—	125	ps
SATA Long Term Accuracy	L_{ACC}	Measured at 0V differential at 1 clock	—	100	ppm
SATA Rising/Falling Slew Rate	T_R / T_F	Measured differentially from ±150 mV	2.5	8	V/ns
Rise/Fall Matching	T_{RFM}	Measured single-endedly from ±75 mV	—	20	%
Voltage High	V_{HIGH}			1.15	V
Voltage Low	V_{LOW}		–0.3	—	V

Table 3. AC Electrical Specifications (Continued)

Parameter	Symbol	Test Condition	Min	Max	Unit
Crossing Point Voltage at 0.7 V Swing	V_{OX}		300	550	mV
PCI/PCIF at 3.3 V					
PCI Duty Cycle	T_{DC}	Measurement at 1.5 V	45	55	%
Spread Disabled PCIF/PCI Period	T_{PERIOD}	Measurement at 1.5 V	29.99700	30.00300	ns
Spread Enabled PCIF/PCI Period	$T_{PERIODSS}$	Measurement at 1.5 V	30.08421	30.23459	ns
Spread Disabled PCIF/PCI Period	$T_{PERIODAbs}$	Measurement at 1.5 V	29.49700	30.50300	ns
Spread Enabled PCIF/PCI Period	$T_{PERIODSSAbs}$	Measurement at 1.5 V	29.56617	30.58421	ns
Spread Enabled PCIF and PCI High Time	T_{HIGH}	Measurement at 2 V	12.27095	16.27995	ns
Spread Enabled PCIF and PCI Low Time	T_{LOW}	Measurement at 0.8 V	11.87095	16.07995	ns
Spread Disabled PCIF and PCI High Time	T_{HIGH}	Measurement at 2.0 V	12.27365	16.27665	ns
Spread Disabled PCIF and PCI Low Time	T_{LOW}	Measurement at 0.8 V	11.87365	16.07665	ns
PCIF/PCI Rising/Falling Slew Rate	T_R / T_F	Measured between 0.8 V and 2.0 V	1.0	4.0	V/ns
Any PCI clock to Any PCI clock Skew	T_{SKEW}	Measurement at 1.5 V	—	1000	ps
PCIF and PCI Cycle to Cycle Jitter	T_{CCJ}	Measurement at 1.5 V	—	300	ps
PCIF/PCI Long Term Accuracy	L_{ACC}	Measurement at 1.5 V	—	100	ppm
48M, 12_48M at 3.3 V					
Duty Cycle	T_{DC}	Measurement at 1.5 V	45	55	%
48 MHz Period	T_{PERIOD}	Measurement at 1.5 V	20.83125	20.83542	ns
48 MHz Absolute Period	$T_{PERIODAbs}$	Measurement at 1.5 V	20.48125	21.18542	ns
48 MHz High Time	T_{HIGH}	Measurement at 2 V	8.216563	11.15198	ns
48 MHz Low Time	T_{LOW}	Measurement at 0.8 V	7.816563	10.95198	ns
Rising and Falling Edge Rate	T_R / T_F (48M)	Measured between 0.8 V and 2.0 V	1.0	2.0	V/ns
Rising and Falling Edge Rate	T_R / T_F (12_48M)	Measured between 0.8 V and 2.0 V	1.0	2.0	V/ns
Cycle to Cycle Jitter	T_{CCJ}	Measurement at 1.5 V	—	300	ps

Table 3. AC Electrical Specifications (Continued)

Parameter	Symbol	Test Condition	Min	Max	Unit
48M Long Term Accuracy	L_{ACC}	Measurement at 1.5 V	—	100	ppm
25M at 3.3 V					
Duty Cycle	T_{DC}	Measurement at 1.5 V	45	55	%
Period	T_{PERIOD}	Measurement at 1.5 V	39.996	40.004	ns
Absolute Period	$T_{PERIODAbs}$	Measurement at 1.5 V	39.32360	40.67640	ns
Rising and Falling Edge Rate	T_R / T_F	Measured between 0.8 V and 2.0 V	1.0	4.0	V/ns
Cycle to Cycle Jitter	T_{CCJ}	Measurement at 1.5 V	—	300	ps
25M Long Term Accuracy	L_{ACC}	Measured at 1.5 V	—	100	ppm
14.318M, at 3.3 V					
Duty Cycle	T_{DC}	Measurement at 1.5 V	45	55	%
Period	T_{PERIOD}	Measurement at 1.5 V	69.82033	69.86224	ns
Absolute Period	$T_{PERIODAbs}$	Measurement at 1.5 V	68.83429	70.84826	ns
High Time	T_{HIGH}	Measurement at 2 V	29.97543	38.46654	ns
Low Time	T_{LOW}	Measurement at 0.8 V	29.57543	38.26654	ns
Rising and Falling Edge Rate	T_R / T_F	Measured between 0.8 V and 2.0 V	1.0	4.0	V/ns
Cycle to Cycle Jitter	T_{CCJ}	Measurement at 1.5 V	—	500	ps
Long Term Accuracy	L_{ACC}	Measurement at 1.5 V	—	100	ppm
ENABLE/DISABLE and SET-UP					
Clock Stabilization from Powerup	T_{STABLE}		—	1.8	ms
Stop clock Set-up Time	T_{SS}		10.0	—	ns

Table 4. Thermal Conditions

Parameter	Symbol	Condition	Min	Max	Unit
Temperature, Storage	T_S	Non-functional	–65	150	°C
Temperature, Operating Ambient, Extended	T_A	Functional	–40	85	°C
Temperature, Operating Ambient, Commercial	T_A	Functional	0	70	°C
Temperature, Junction	T_J	Functional	—	150	°C
Dissipation, Junction to Case	$Ø_{JC}$	JEDEC (JESD 51)	—	20	°C/W
Dissipation, Junction to Ambient	$Ø_{JA}$	JEDEC (JESD 51)	—	60	°C/W
Note: For multiple supplies, the voltage on any input or I/O pin cannot exceed the power pin during powerup. Power supply sequencing is not required.					

Table 5. Absolute Maximum Conditions

Parameter	Symbol	Test Condition	Min	Max	Unit
Main Supply Voltage	$V_{DD\_3.3\ V}$	Functional	—	4.6	V
Input Voltage	V_{IN}	Relative to V_{SS}	–0.5	4.6	V_{DC}
Temperature, Storage	T_S	Non-functional	–65	150	°C
Temperature, Operating Ambient	T_A	Functional	–40	85	°C
Temperature, Junction	T_J	Functional	—	150	°C
Dissipation, Junction to Case	$Ø_{JC}$	JEDEC (JESD 51)	—	20	°C/W
Dissipation, Junction to Ambient	$Ø_{JA}$	JEDEC (JESD 51)	—	60	°C/W
ESD Protection (Human Body Model)	ESD_{HBM}	JEDEC (JESD 22 - A114)	2000	—	V
Flammability Rating	UL-94	UL (Class)	V–0		
Moisture Sensitivity Level	MSL	JEDEC (J-STD-020)	1		
Multiple Supplies: The Voltage on any input or I/O pin cannot exceed the power pin during power-up. Power supply sequencing is NOT required.					

2. Functional Description

2.1. Powerdown (PD#) Clarification

The CKPWRGD/PD# pin is a dual-function pin. During initial powerup, the pin functions as CKPWRGD. Once CKPWRGD has been sampled high by the clock chip, the pin assumes PD# functionality. The PD# pin is an asynchronous active low input used to shut off all clocks cleanly before shutting off power to the device. This signal is synchronized internally to the device before powering down the clock synthesizer. PD# is also an asynchronous input for powering up the system. When PD# is asserted low, clocks are driven to a low value and held before turning off the VCOs and the crystal oscillator.

2.2. Powerdown (PD#) Assertion

When PD# is sampled low by two consecutive rising edges of CPUC, all single-ended outputs clocks will be held low on their next high-to-low transition and differential clocks will be held low. When powerdown mode is desired as the initial power on state, PD# must be asserted low in less than 10 µs after asserting CKPWRGD.

.

Table 6. Output Driver Status during CPU_STP and PCIS_STP#

		CPU_STP# Asserted	PCI_STP# Asserted	CLKREQ# Asserted	SMBus OE Disabled
Single-ended Clocks	Stoppable	Running	Driven low	Running	Driven low
	Non-stoppable	Running	Running	Running	
Differential Clocks	Stoppable	Clock driven high	Clock driven high	Clock driven low	Clock driven low
		Clock driven low	Clock driven low	Clock driven low	
	Non-stoppable	Running	Running	Running	

Table 7. Output Driver Status

	All Single-ended Clocks		All Differential Clocks	
	w/o Strap	w/ Strap	Clock	Clock#
PD# = 0 (Powerdown)	Low	Hi-z	Low	Low

2.3. Powerdown (PD#) Deassertion

The powerup latency is less than 1.8 ms. This is the time from the deassertion of the PD# pin or the ramping of the power supply until the time that stable clocks are generated from the clock chip. All differential outputs stopped in a three-state condition resulting from powerdown are driven high in less than 300 µs of PD# deassertion to a voltage greater than 200 mV. After the clock chip's internal PLL is powered up and locked, all outputs are enabled within a few clock cycles. Figure 2 is an example showing the relationship of clocks coming up.

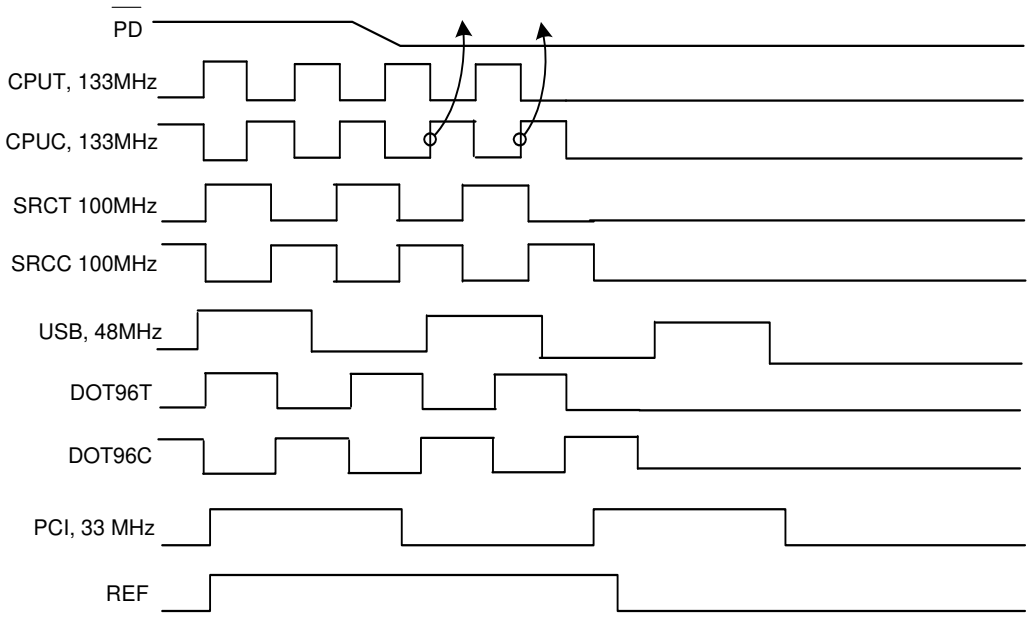

Figure 1. Powerdown Assertion Timing Waveform

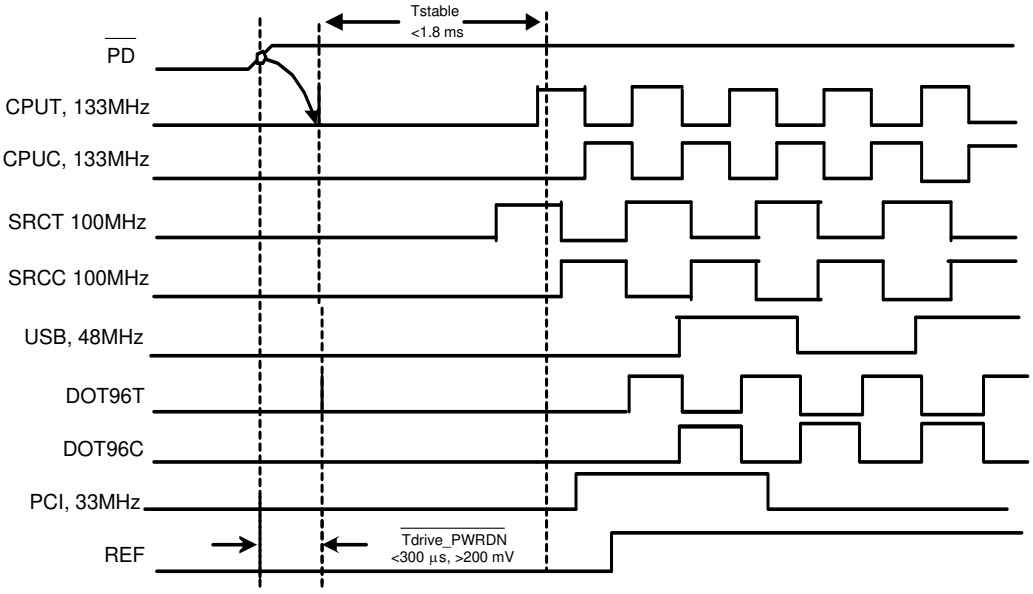

Figure 2. Powerdown Deassertion Timing Waveform

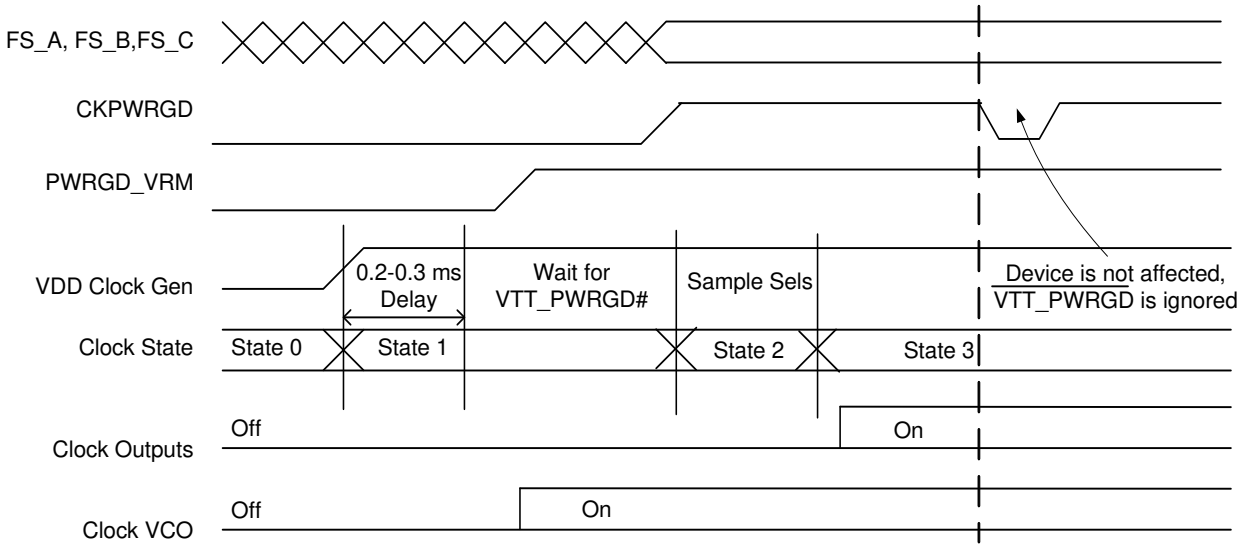

Figure 3. CKPWRGD Timing Diagram

2.4. CPU_STP# Assertion

The CPU_STP# signal is an active LOW input used for synchronous stopping and starting the CPU output clocks while the rest of the clock generator continues to function. When the CPU_STP# pin is asserted, all CPU outputs that are set with the I^2C configuration to be stoppable are stopped within two to six CPU clock periods after being sampled by two rising edges of the internal CPUC clock. The final states of the stopped CPU signals are CPUT = High and CPUC = Low.

2.5. CPU_STP# Deassertion

The deassertion of the CPU_STP# signal causes all stopped CPU outputs to resume normal operation in a synchronous manner. No short or stretched clock pulses are produced when the clock resumes. The maximum latency from the deassertion to active outputs is no more than two CPU clock cycles.

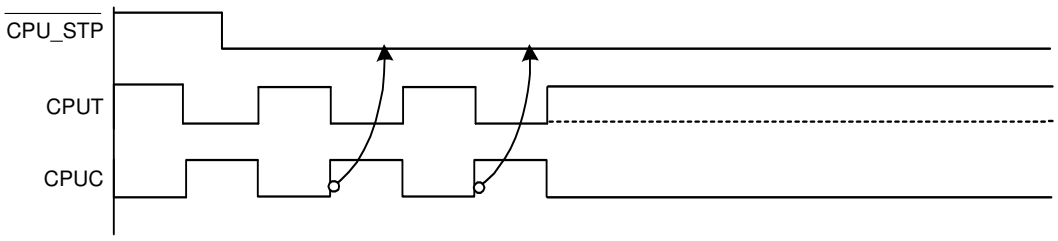

Figure 4. CPU_STP# Assertion Waveform

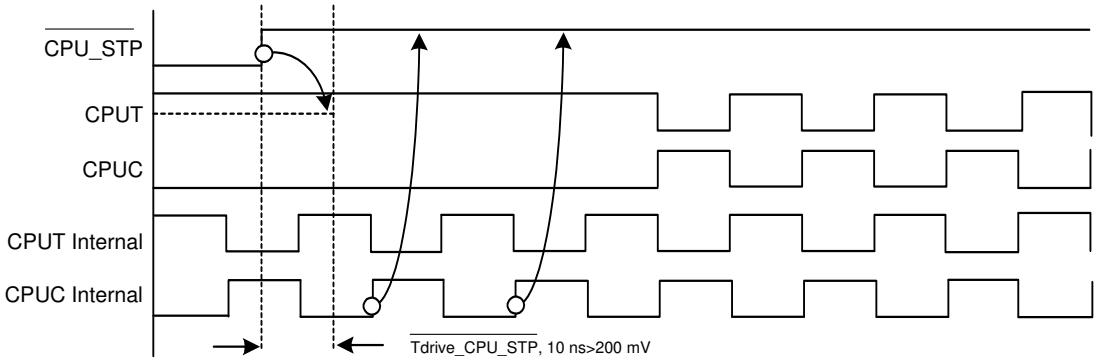

Figure 5. CPU_STP# Deassertion Waveform

2.6. PCI/SRC_STP# Assertion

The PCI/SRC_STP# signal is an active low input used for synchronously stopping and starting the PCI outputs while the rest of the clock generator continues to function. The set-up time for capturing PCI/SRC_STP# going low is 10 ns (t_{SU}) (refer to Figure 6). The PCIF and SRC clocks are affected by the PCI/SRC pin if their corresponding control bit in the I^2C register is set to allow them to be free running. For SRC clocks assertion description, refer to the CPU_STP# descriptions in Section 2.4 and Section 2.5.

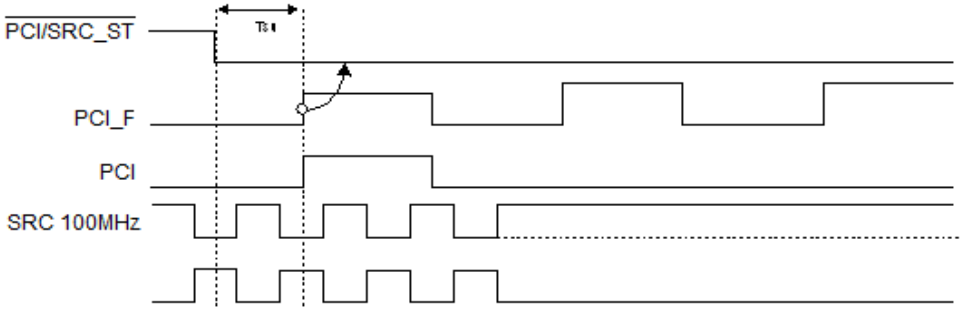

Figure 6. PCI/SRC_STP# Assertion Waveform

2.7. PCI/SRC_STP# Deassertion

The deassertion of the PCI/SRC_STP# signal causes all PCI and stoppable PCIF to resume running in a synchronous manner within two PCI clock periods and after PCI/SRC_STP# transitions to a high level. Similarly, PCI/SRC_STP# deassertion will cause stoppable SRC clocks to resume running. For an SRC clocks deassertion description, refer to the CPU_STP# description Section 2.4 and Section 2.5.

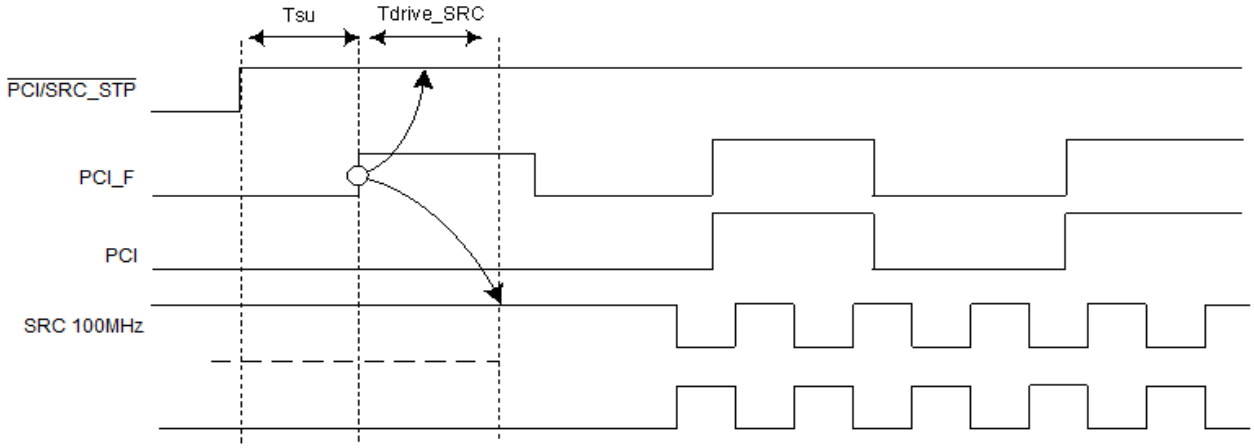

Figure 7. PCI/SRC_STP# Deassertion Waveform

3. Test and Measurement Setup

3.1. Single-ended Clocks

Figure 8 shows the test load configuration for single-ended clock output signals.

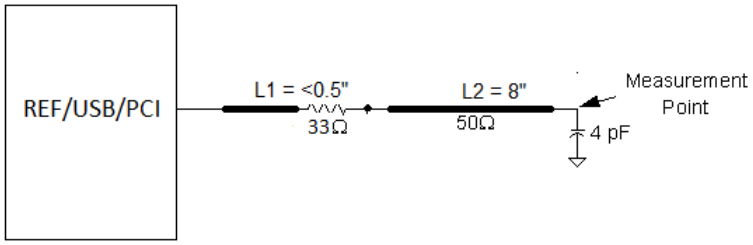

Figure 8. Single-ended Clocks Single Load Configuration

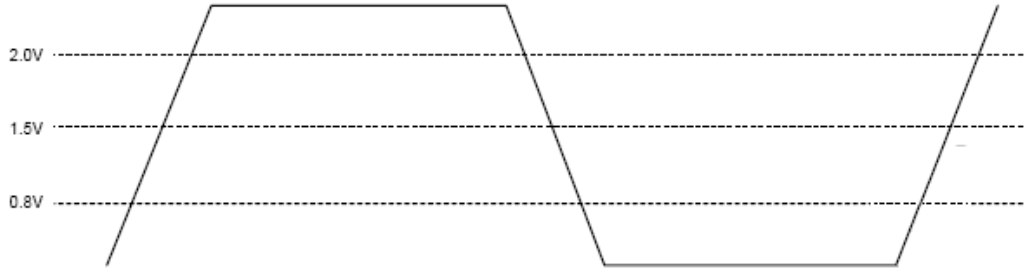

Figure 9. Single-ended Output Signals (for AC Parameters Measurement)

3.2. Differential Clock Signals

Figure 10 shows the test load configuration for differential clock signals.

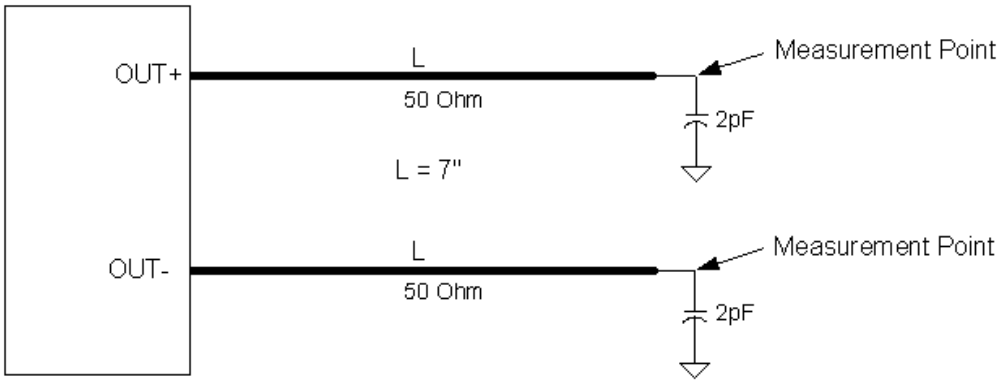

Figure 10. 0.7 V Differential Load Configuration

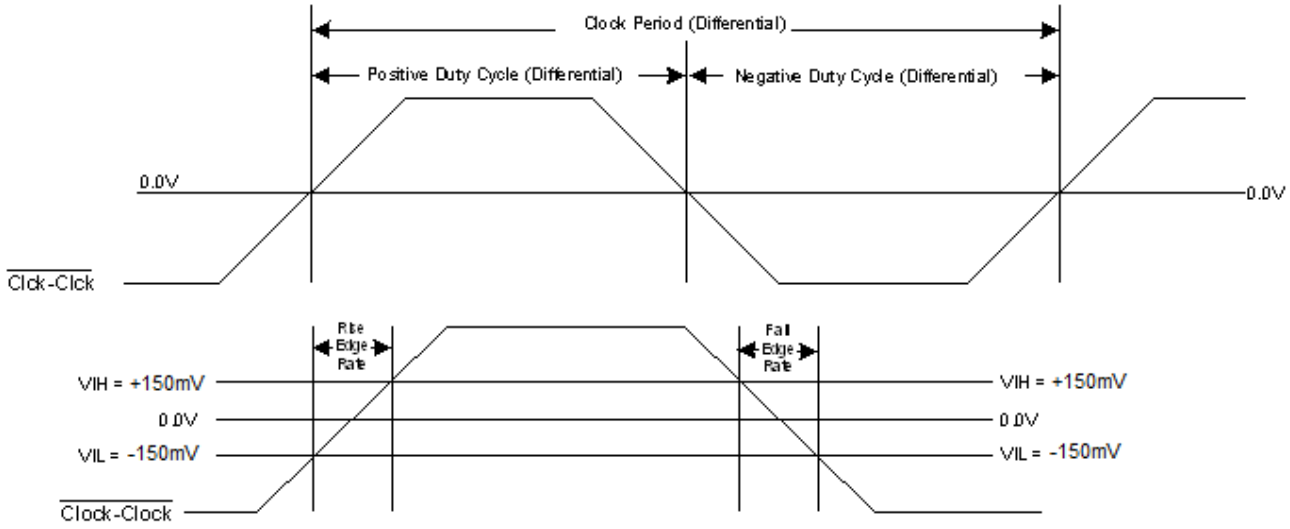

Figure 11. Differential Measurement for Differential Output Signals (for AC Parameters Measurement)

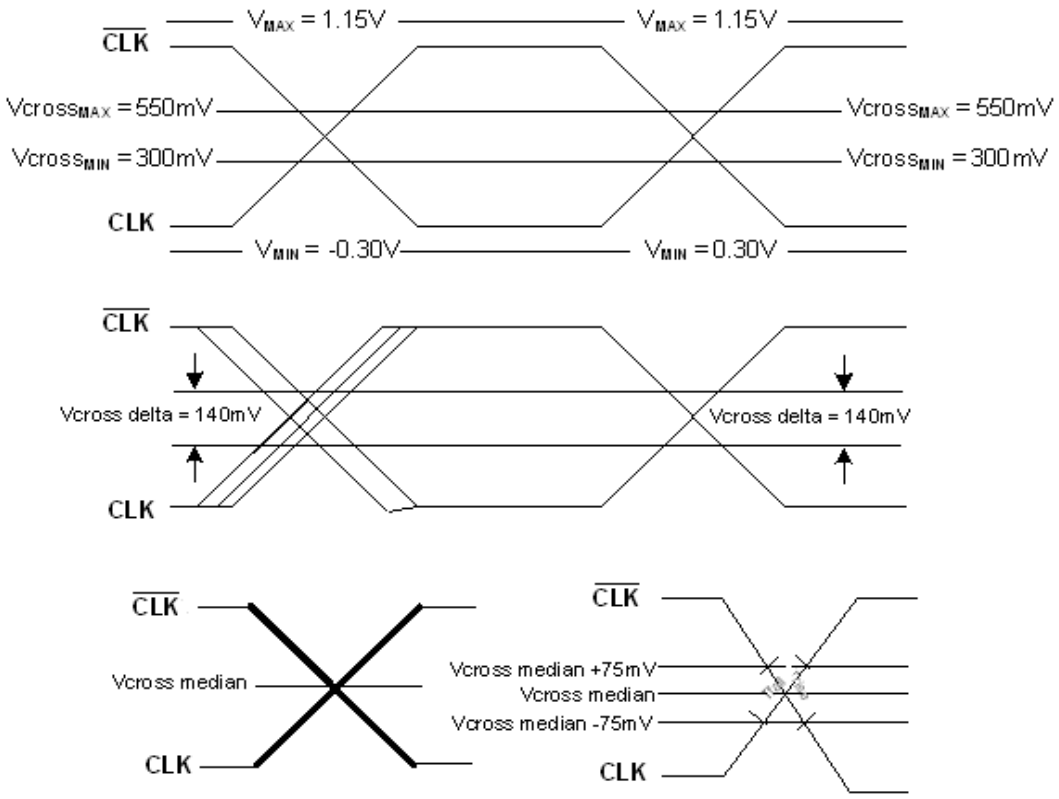

Figure 12. Single-ended Measurement for Differential Output Signals (for AC Parameters Measurement)

4. Control Registers

4.1. Frequency Select Pin FS

Apply the appropriate logic levels to FS inputs before CKPWRGD assertion to achieve host clock frequency selection. When the clock chip sampled HIGH on CKPWRGD and indicates that VTT voltage is stable then FS input values are sampled. This process employs a one-shot functionality and once the CKPWRGD sampled a valid HIGH, all other FS, and CKPWRGD transitions are ignored except in test mode.

Table 8. Frequency Select Pin (FS)

SEL_SATA	FSC	FSB	FSA	CPU	SRC	SATA	PCI
0	0	0	0	100.00	100.00	100.00	33.33
0	0	0	1	100.00	100.00	100.00	33.33
0	0	1	0	83.33	100.00	100.00	33.33
0	0	1	1	83.33	100.00	100.00	33.33
0	1	0	0	133.33	100.00	100.00	33.33
0	1	0	1	133.33	100.00	100.00	33.33
0	1	1	0	166.67	100.00	100.00	33.33
0	1	1	1	166.67	100.00	100.00	33.33
1	0	0	0	100.00	100.00	100.00	33.33
1	0	0	1	100.00	100.00	100.00	33.33
1	0	1	0	83.33	100.00	100.00	33.33
1	0	1	1	83.33	100.00	100.00	33.33
1	1	0	0	133.33	100.00	100.00	33.33
1	1	0	1	133.33	100.00	100.00	33.33
1	1	1	0	166.67	100.00	100.00	33.33
1	1	1	1	166.67	100.00	100.00	33.33

4.2. Serial Data Interface

To enhance the flexibility and function of the clock synthesizer, a two-signal serial interface is provided. Through the Serial Data Interface, various device functions, such as individual clock output buffers are individually enabled or disabled. The registers associated with the Serial Data Interface initialize to their default setting at power-up. The use of this interface is optional. Clock device register changes are normally made at system initialization, if any are required. The interface cannot be used during system operation for power management functions.

4.3. Data Protocol

The clock driver serial protocol accepts byte write, byte read, block write, and block read operations from the controller. For block write/read operation, access the bytes in sequential order from lowest to highest (most significant bit first) with the ability to stop after any complete byte is transferred. For byte write and byte read operations, the system controller can access individually indexed bytes. The offset of the indexed byte is encoded in the command code described in Table 9.

The block write and block read protocol is outlined in Table 10 while Table 11 outlines byte write and byte read protocol. The slave receiver address is 11010010 (D2h).

Table 9. Command Code Definition

Bit	Description
7	0 = Block read or block write operation; 1 = Byte read or byte write operation.
(6:0)	Byte offset for byte read or byte write operation. For block read or block write operations, these bits should be '0000000'.

Table 10. Block Read and Block Write Protocol

Block Write Protocol		Block Read Protocol	
Bit	**Description**	**Bit**	**Description**
1	Start	1	Start
8:2	Slave address–7 bits	8:2	Slave address–7 bits
9	Write	9	Write
10	Acknowledge from slave	10	Acknowledge from slave
18:11	Command Code–8 bits	18:11	Command Code–8 bits
19	Acknowledge from slave	19	Acknowledge from slave
27:20	Byte Count–8 bits	20	Repeat start
28	Acknowledge from slave	27:21	Slave address–7 bits
36:29	Data byte 1–8 bits	28	Read = 1
37	Acknowledge from slave	29	Acknowledge from slave
45:38	Data byte 2–8 bits	37:30	Byte Count from slave–8 bits
46	Acknowledge from slave	38	Acknowledge
....	Data Byte /Slave Acknowledges	46:39	Data byte 1 from slave–8 bits

Table 10. Block Read and Block Write Protocol (Continued)

Block Write Protocol		Block Read Protocol	
Bit	**Description**	**Bit**	**Description**
....	Data Byte N–8 bits	47	Acknowledge
....	Acknowledge from slave	55:48	Data byte 2 from slave–8 bits
....	Stop	56	Acknowledge
		....	Data bytes from slave / Acknowledge
		....	Data Byte N from slave–8 bits
		....	NOT Acknowledge
		....	Stop

Table 11. Byte Read and Byte Write Protocol

Byte Write Protocol		Byte Read Protocol	
Bit	**Description**	**Bit**	**Description**
1	Start	1	Start
8:2	Slave address–7 bits	8:2	Slave address–7 bits
9	Write	9	Write
10	Acknowledge from slave	10	Acknowledge from slave
18:11	Command Code–8 bits	18:11	Command Code–8 bits
19	Acknowledge from slave	19	Acknowledge from slave
27:20	Data byte–8 bits	20	Repeated start
28	Acknowledge from slave	27:21	Slave address–7 bits
29	Stop	28	Read
		29	Acknowledge from slave
		37:30	Data from slave–8 bits
		38	NOT Acknowledge
		39	Stop

Control Register 0. Byte 0

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name			Spread Enable	SEL_SATA		FSC	FSB	FSA
Type	R/W	R/W	R/W	R	R/W	R	R	R

Reset settings = 000x0xxx

Bit	Name	Function
7:6	Reserved	
5	Spread Enable	Enable spread for CPU/SRC/PCI outputs 0 = Disable, 1 = –0.5%
4	SEL_SATA	See Table 9 for SATA/SRC selection.
3	Reserved	
2	FSC	See Table 9 for CPU Frequency Selection Table.
1	FSB	
0	FSA	

Register 1. Byte 1

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	DOT96_ OE	SATA/ SRC0_OE	CPU2/ SRC6_OE	SRC2	SRC1		WOL_EN	
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Reset settings = 1111110

Bit	Name	Function
7	DOT96_OE	**Output enable for DOT96.** 0 = Output Disabled, 1 = Output Enabled
6	SATA/SRC0_OE	**Output enable for SATA/SRC0.** 0 = Output Disabled, 1 = Output Enabled
5	CPU2/SRC6_OE	**Output enable for CPU2/SRC6.** 0 = Output Disabled, 1 = Output Enabled
4	SRC2	**Output enable for SRC2.** 0 = Output Disabled, 1 = Output Enabled
3	SRC1	**Output enable for SRC1.** 0 = Output Disabled, 1 = Output Enabled
2	Reserved	
1	WOL_EN	**Wake-On-LAN Enable bit.** 25 MHz free running during VDD Suspend (S-states). If this bit is set to 0, the XTAL OSC will also be powered down in the Suspend States)
0	Reserved	

Register 2. Byte 2

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	48M_OE		25M_OE	REF_OE	12_48M_OE	PCI0_OE	PCIF_OE	
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Reset settings = 10111110

Bit	Name	Function
7	48M_OE	**Output Enable for 48M.** 0: Output disabled. 1: Output enabled.
6	Reserved	
5	25M_OE	**Output ENABLE for 25M.** 0 = Output Disabled, 1 = Output Enabled
4	REF_OE	**Output Enable for REF.** 0 = Output Disabled, 1 = Output Enabled
3	12_48M_OE	**Output Enable for 12_48M.** 0 = Output Disabled, 1 = Output Enabled
2	PCI0_OE	**Output Enable for PCI0.** 0 = Output Disabled, 1 = Output Enabled
1	PCIF_OE	**Output Enable for PCIF.** 0 = Output Disabled, 1 = Output Enabled
0	Reserved	

Register 3. Byte 3

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	CPU1_OE	CPU0_OE	CLKREQ#_3	CLKREQ#_3	CLKREQ#_2	CLKREQ#_2	CLKREQ#_1	CLKREQ#_1
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Reset settings = 1100000

Bit	Name	Function
7	CPU1_OE	**Output Enable for CPU1.** 0 = Output Disabled, 1 = Output Enabled
6	CPU0_OE	**Output Enable for CPU0.** 0 = Output Disabled, 1 = Output Enabled
5	CLKREQ#_3	**Clock Request for SRC2.** 0 = Not controlled, 1 = Controlled
4	CLKREQ#_3	**Clock Request for SRC6 (does not apply to CPU clock).** 0 = Not controlled, 1 = Controlled
3	CLKREQ#_2	**Clock Request for SRC2.** 0 = Not controlled, 1 = Controlled
2	CLKREQ#_2	**Clock Request for SATA75M/SRC0.** 0 = Not controlled, 1 = Controlled
1	CLKREQ#_1	**Clock Request for SRC1.** 0 = Not controlled, 1 = Controlled
0	CLKREQ#_1	**Clock Request for SATA75M/SRC0.** 0 = Not controlled, 1 = Controlled