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Unipolar 2-Phase Stepper Motor Driver ICs

SLA7070MS Series
Data Sheet

March, 2018 Rev.1.6

Table of Contents

1. General Description

This document describes summary of the SLA7070MS series.

2. Features and Benefits

(1) Main power supply voltages, V_{BB}: 46 V (max.), 10 to 44 V normal operating range
(2) Logic supply voltages, V_{DD}: 3.0 to 5.5 V
(3) Maximum output currents, $I_{O(max)}$: 2.0 A, 3.0 A
(4) Clock-in stepping control (built-in sequencer)
(5) Full-, half-, and microstep products are available
→ Microstepping options are capable of full-, half-, quarter-, eighth-, and sixteenth-stepping
(6) Built-in "sense resistor" detects motor current
(7) All variants are pin-compatible for enhanced design flexibility
(8) ZIP type 23-pin molded package (SLA package)
(9) Self-excitation PWM current control with fixed OFF-time
→ For microstepping variants, OFF-time adjusted automatically by step reference current ratio (3 levels)
(10) Built-in synchronous rectifying circuit reduces power dissipation at PWM-OFF
(11) Synchronous PWM chopping function prevents motor noise in the Hold mode
(12) The Sleep mode to reduce IC input current in stand-by state
(13) Built-in protection circuitry against motor coil opens/shorts and thermal shutdown protection
(14) The following are the product variants and optional features available:

- Blanking Time
  - Full/Half step products: 3.2 µs (standard), 5.2 µs (optional type B)
  - Microstep product: 1.7 µs (standard), 3.2 µs (optional type B)
- Input Clock Edge
  - Standard type: POS (positive) edge
  - Optional type W: POS/NEG (positive and negative) edge

NOTE: The optional types listed above, "type B" and "type W", are abbreviated and referred to "B" and "W" as the letters for product branding codes, respectively. These terms and abbreviations are also used throughout this document. See also Section 6 for more details.

3. Part Numbers and Functional Characteristics

Table 3-1 provides the product variants available in the SLA7070MS series.

Table 3-1. Part Numbers and Functional Characteristics

	Functional Characteristics			
	Sequencer		Rated Current (Maximum Setting Value)	
Part Number	Full/Half Step	Microstep	2.0 A	3.0 A
SLA7072MS	X		X	
SLA7073MS	X			X
SLA7078MS		X		X

In addition, the following functional options are available in the SLA7070MS series:

- Blanking Time
  - Full/Half step products: 3.2 µs (standard), 5.2 µs (optional type B)
  - Microstep product: 1.7 µs (standard), 3.2 µs (optional type B)
- Input Clock Edge
  - Standard type: POS (positive) edge
  - Optional type W: POS/NEG (positive and negative) edge

NOTE: The optional types listed above, "type B" and "type W", are abbreviated and referred to "B" and "W" as the letters for product branding codes, respectively. These terms and abbreviations are also used throughout this document. See also Section 6 for more details.

4. Specifications

Table 4-1. Absolute Maximum Ratings

Unless specifically noted, T_A = 25 °C

Characteristic	Symbol	Rating	Unit	Remarks	
Load (Motor Supply) Voltage	V_M	46	V		
Main Power Supply Voltage	V_{BB}	46	V		
Supply Voltage	V_{DD}	6	V	Power supply to DC	
		7	V	≤1 μs (5% duty)	
Output Current	I_O	2.0	A	SLA7072MS	Control current value
		3.0	A	SLA7073MS SLA7078MS	
Logic Input Voltage	V_{IN}	−0.3 to V_{DD} + 0.3	V		
REF Input Voltage	V_{REF}	−0.3 to V_{DD} + 0.3	V		
Sense Voltage	V_{RS}	±1	V		
Allowable Power Dissipation	P_D	4.7	W	Without heatsink	
Junction Temperature	T_J	150	°C		
Operating Ambient Temperature	T_A	−20 to 85	°C		
Storage Temperature	T_{stg}	−30 to 150	°C		

NOTE: Output current ratings may be limited by duty cycles, ambient temperatures, and heat sinking conditions. Do not exceed the maximum output currents and the maximum junction temperature (T_J) given above, under any conditions of use.

Table 4-2. Recommended Operating Conditions

Unless specifically noted, T_A = 25 °C

Characteristic	Symbol	Standard Value		Unit	Remarks
		Min.	Max.		
Load (Motor Supply) Voltage	V_M		44	V	
Main Power Supply Voltage	V_{BB}	10	44	V	
Logic Supply Voltage	V_{DD}	3.0	5.5	V	Surge voltage at VDD pin should be less than ±0.5 V to avoid malfunctioning in operation
Case Temperature	T_C		90	°C	Measured at Pin 12 (lead portion), without heatsink

NOTE: As the motor supply voltage, V_M, becomes higher, it also approaches the breakdown voltage of the OUTx pins (100 V min.); and breakdown will be more likely to happen. Even if one of the OUTx pins breaks down (due to surge noise or other factors), the SLA7070MS series will recognize it as abnormality (coil open) and will run appropriate protection functions. Therefore, a thorough evaluation is recommended.

Table 4-3. Electrical Characteristics 1

Unless specifically noted, T_A = 25 °C, V_{BB} = 24 V, and V_{DD} = 5 V

Characteristic	Symbol	Rating			Unit	Conditions
		Min.	Typ.	Max.		
Main Power Supply Current	I_{BB}			15	mA	Normal mode
	I_{BBS}			100	µA	Sleep1, Sleep2
Logic Power Current	I_{DD}			5	mA	
MOSFET Breakdown Voltage	V_{DSS}	100			V	V_{BB} = 44V, I_D = 1 mA
Maximum Response Frequency	f_{clk}	250			kHz	Clock duty cycle = 50%
Logic Input Voltage	V_{IL}			0.25 × V_{DD}	V	
	V_{IH}	0.75 × V_{DD}			V	
Logic Input Current	I_{IL}		±1		µA	
	I_{IH}		±1		µA	
REF Input Voltage	V_{REF}	0.04		→	V	Table 4-5, Figure 4-1
	V_{REFS}	2.0		V_{DD}	V	Output OFF, Sleep1[1]
REF Input Current	I_{REF}		±10		µA	
SENSE Detection Voltage	V_{SENSE}	V_{REF} − 0.03	V_{REF}	V_{REF} + 0.03	V	V_{REF} = 0 to1.5 V, Step reference ratio: 100%
Sleep-Enable Recovery Time	t_{SE}	100			µs	Sleep1, Sleep2
Switching Time	t_{con}		2.0		µs	Clock → Output ON
	t_{coff}		1.5		µs	Clock → Output OFF
Overcurrent Detection Voltage[2]	V_{OCP}	0.65	0.7	0.75	V	Motor coils shorted
Overcurrent Detection Current (V_{OCP} / R_S)	I_{OCP}		2.3		A	1.0 A and 1.5 A devices
			3.5		A	2.0 A devices
			4.6		A	3.0 A devices
Load Disconnection Undetected Time	t_{opp}		2		µs	From PWM-OFF
Overheat Protection Temperature	T_{tsd}		140		°C	Measured at back of device case (after heat has saturated)
FLAG Output Voltage	V_{FlagL}			1.25	V	I_{FlagL} = 1.25 mA
	V_{FlagH}	V_{DD} − 1.25			V	I_{FlagH} = −1.25 mA
FLAG Output Current	I_{FlagL}			1.25	mA	
	I_{FlagH}	−1.25			mA	

NOTE: Unless specifically noted, negative current is defined as output current flow from a specified pin.

[1] In a state of: I_{BBS}, output OFF, and sequencer **enabled**.

[2] Protection circuit operates when $V_{SENSE} \geq V_{OCP}$.

Table 4-4. Electrical Characteristics 2 (Varying with Step Sequence)

(1) Full-/Half-step products: SLA7072MS, SLA7073MS

Unless specifically noted, T_A = 25 °C, V_{BB} = 24 V, and V_{DD} = 5 V

Characteristic	Symbol	Rating			Unit	Conditions
		Min.	Typ.	Max.		
Step Reference Current Ratio	Mode F		100		%	$V_{REF} \approx V_{SENSE}$ = 100%, V_{REF} = 0 to 1.0 V
	Mode 8		70		%	
Minimum PWM ON-Time	$t_{on(min)}$		3.2		µs	Standard type (w/o branding codes)
			5.2		µs	Optional type B (w/ branding codes)
PWM OFF-Time	t_{off}		12		µs	

(2) Microstep product: SLA7078MS

Unless specifically noted, T_A = 25 °C, V_{BB} = 24 V, and VDD = 5 V

Characteristic	Symbol	Rating			Unit	Conditions
		Min.	Typ.	Max.		
Step Reference Current Ratio	Mode F		100		%	$V_{REF} \approx V_{SENSE}$ = 100%, V_{REF} = 0 to 1.0 V
	Mode E		98.1		%	
	Mode D		95.7		%	
	Mode C		92.4		%	
	Mode B		88.2		%	
	Mode A		83.1		%	
	Mode 9		77.3		%	
	Mode 8		70.7		%	
	Mode 7		63.4		%	
	Mode 6		55.5		%	
	Mode 5		47.1		%	
	Mode 4		38.2		%	
	Mode 3		29		%	
	Mode 2		19.5		%	
	Mode 1		9.8		%	
MO Output Voltage	V_{MOL}			1.25	V	I_{MOL} = 1.25 mA
	V_{MOH}	V_{DD} − 1.25			V	I_{MOH} = −1.25 mA
MO Output Current	I_{MOL}			1.25	mA	
	I_{MOH}	−1.25			mA	
Minimum PWM ON-Time	$t_{on(min)}$		1.7		µs	Standard type (w/o branding codes)
			3.2		µs	Optional type B (w/ branding codes)
PWM OFF-time	$t_{off\ 1}$		12		µs	Mode 8 to Mode F
	$t_{off\ 2}$		9		µs	Mode 4 to Mode 7
	$t_{off\ 3}$		7		µs	Mode 1 to Mode 3

Table 4-5. Electrical Characteristics 3 (Varying with Output Current Range)

(1) I_O = 2.0 A

Unless specifically noted, T_A = 25 °C, V_{BB} = 24 V, and V_{DD} = 5 V

Characteristic	Symbol	Rating			Unit	Conditions
		Min.	Typ.	Max.		
Output MOSFET ON-Voltage	$R_{DS(on)}$		0.25	0.4	Ω	I_D = 2.0 A
Output MOSFET Body Diodes Forward Voltage	V_F		0.95	1.2	V	I_F = 2.0 A
Sense Resistor[1)]	R_S	0.199	0.205	0.211	Ω	Tolerance: ±3%
REF Input Voltage	V_{REF}	0.04		0.4	V	Within specified current limit

[1)] Includes approximately 5 mΩ circuit resistance in addition to the resistance of the built-in resistor itself.

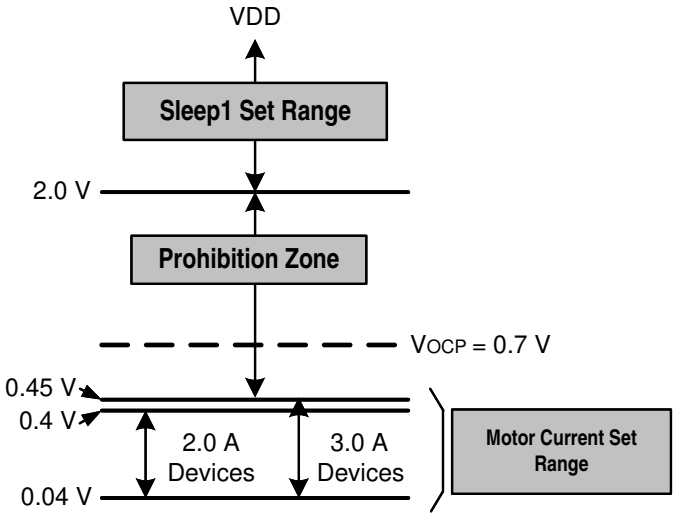
(2) I_O = 3.0 A

Unless specifically noted, T_A = 25 °C, V_{BB} = 24 V, and V_{DD} = 5 V

Characteristic	Symbol	Rating			Unit	Conditions
		Min.	Typ.	Max.		
Output MOSFET ON-Resistance	$R_{DS(on)}$		0.18	0.24	Ω	I_D = 3.0 A
Output MOSFET Body Diodes Forward Voltage	V_F		0.95	2.1	V	I_F = 3.0 A
Sense Resistor[1)]	R_S	0.150	0.155	0.160	Ω	Tolerance: ±3%
REF Input Voltage	V_{REF}	0.04		0.45	V	Within specified current limit

[1)] Includes approximately 5 mΩ circuit resistance in addition to the resistance of the built-in resistor itself.

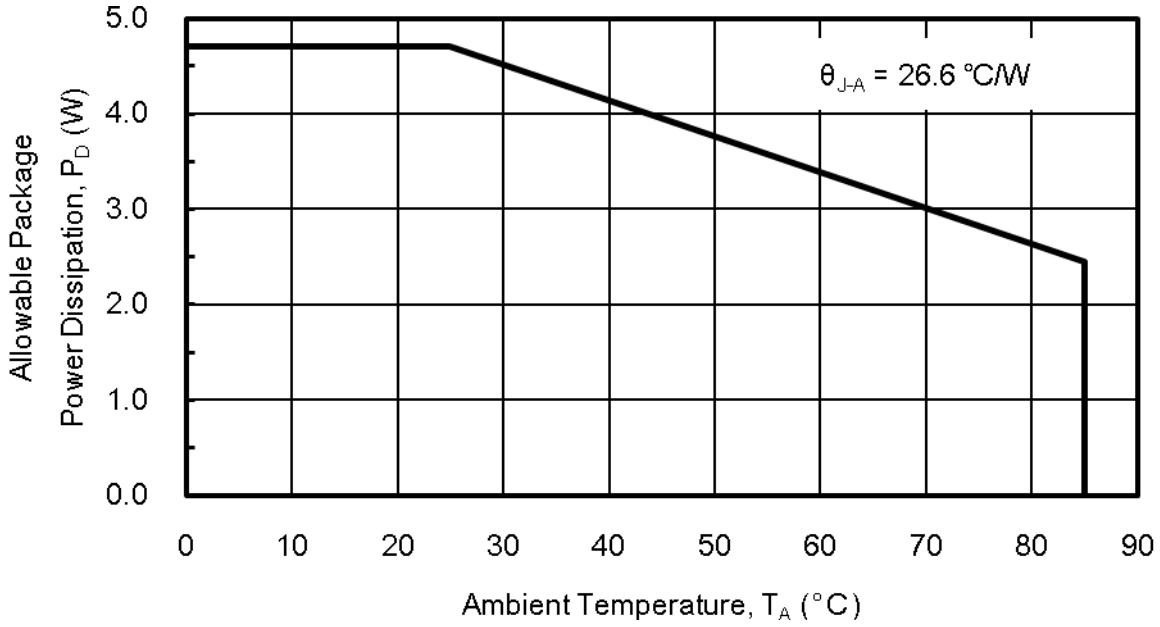
Figure 4-1. Setting Range of Reference Voltage, V_{REF}



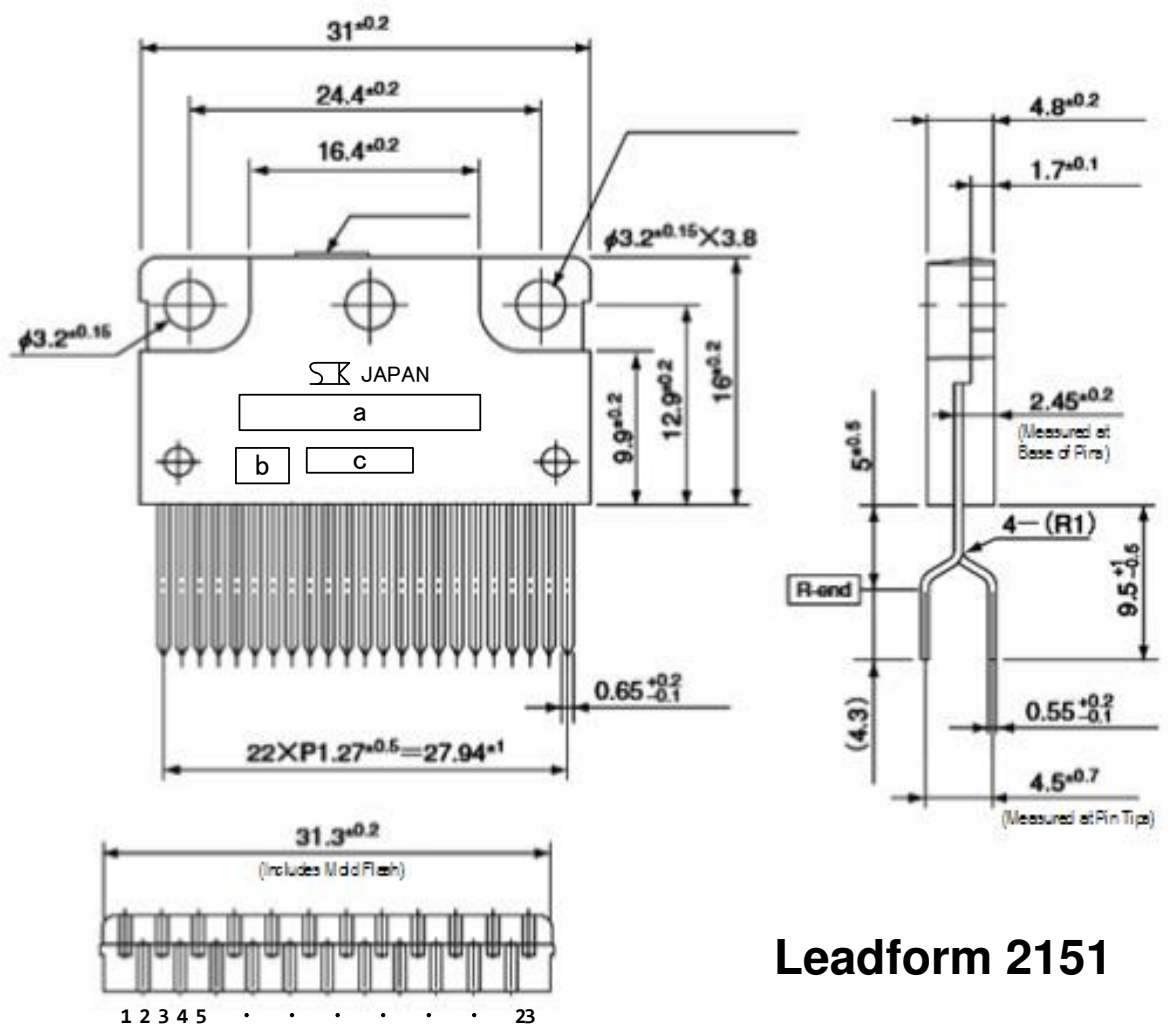
NOTE: Extra attentions should be paid to the changeover between the motor current specification range and the Sleep1 set range. V_{OCP} falls on the "prohibition zone" threshold. If the changeover takes too long, OCP operation will start when $V_{SENSE} > V_{OCP}$.

5. Power Derating Chart

Figure 5-1. Power Derating Chart



6. Package Outline Drawing



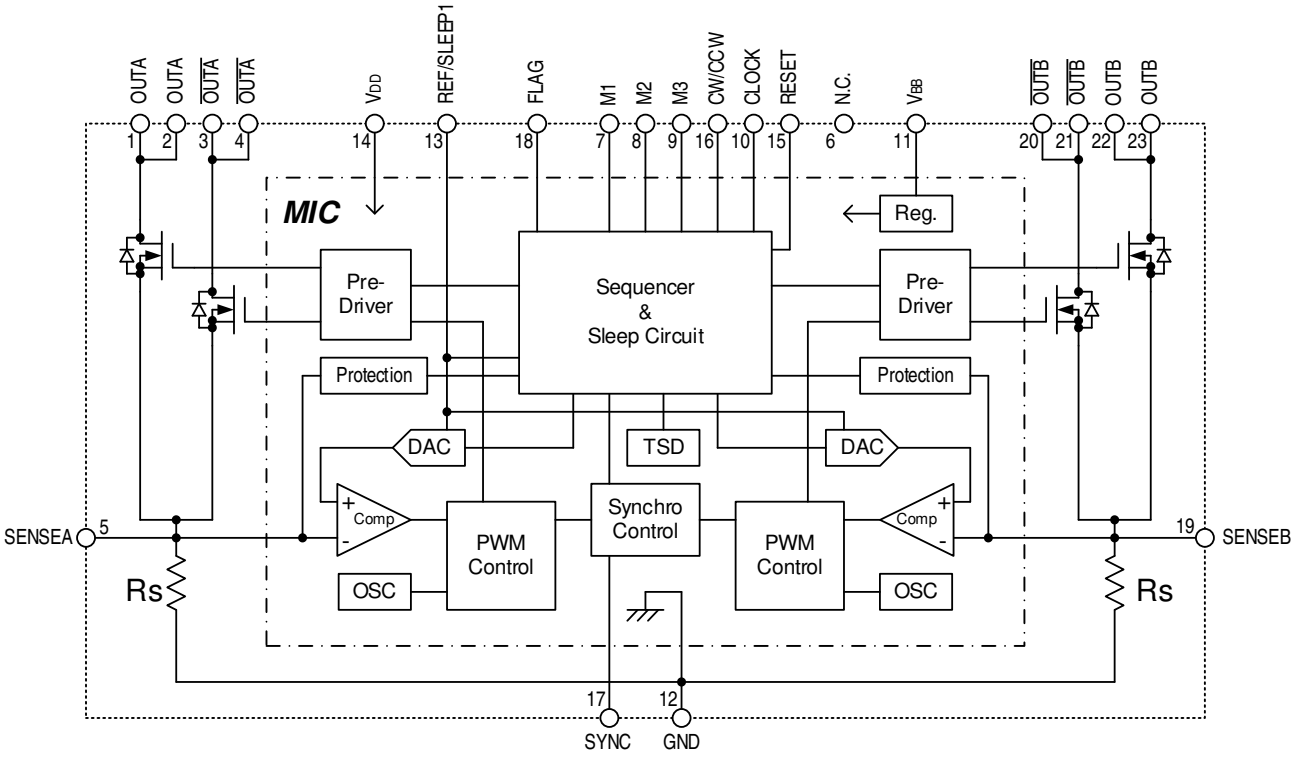
Leadform 2151

NOTES:

- Dimensions in millimeters
- Pin material: Cu
- Pin plating: Solder plating (Pb-free)
- Branding codes:
  - a Part number 1: *SLA707xMS*
    - The lowercase letter *x* represents a number of either of *2*, *3*, *7*, or *8*, according to the combination of rated currents and step sequencers. See also Table 3-1, which lists the part numbers and corresponding features.
  - b Part number 2: *W*, *B*, or *WB*
    - Only optional products have this area labeled with either of the letters listed above. *W*, *B*, and *WB* stand for optional type W (selectable clock inputs), type B (selectable blanking times), and type WB (a combined version of types W and B), respectively.
  - c Lot number: *YMDD*
    - *Y* is the last digit of the year of manufacture
    - *M* is the month of the year (1 to 9, O, N, or D)
    - *DD* is the day of the month (01 to 31)

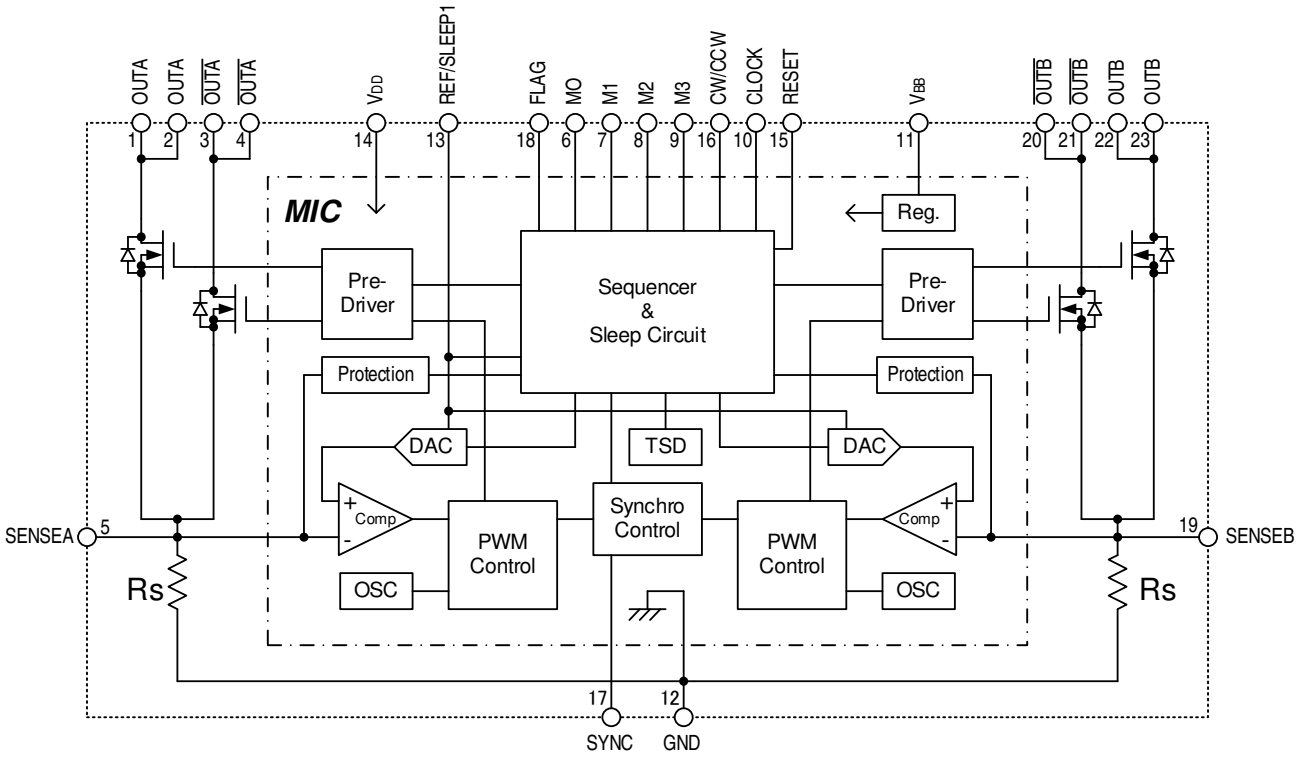
7. Functional Block Diagrams and Pin Assignments

Figure 7-1. Full-/Half-Step Products: SLA7072MS, SLA7073MS



Pin No.	Symbol	Function
1	OUTA	Phase A output
2		
3	$\overline{\text{OUTA}}$	Phase $\overline{\text{A}}$ output
4		
5	SENSEA	Phase A current sensing
6	NC	No connection
7	M1	Input for excitation mode & Sleep2 setting
8	M2	
9	M3	
10	CLOCK	Step clock input
11	V_{BB}	Main power supply voltage (for motor)
12	GND	Ground
13	REF/SLEEP1	Input for control current / Sleep1 setting
14	V_{DD}	Power supply to logic
15	RESET	Reset input for internal logic
16	CW/CCW	Forward / reverse input
17	SYNC	Synchronous PMW control switch input
18	FLAG	Output from protection circuit monitor
19	SENSEB	Phase B current sensing
20	$\overline{\text{OUTB}}$	Phase $\overline{\text{B}}$ output
21		
22	OUTB	Phase B output
23		

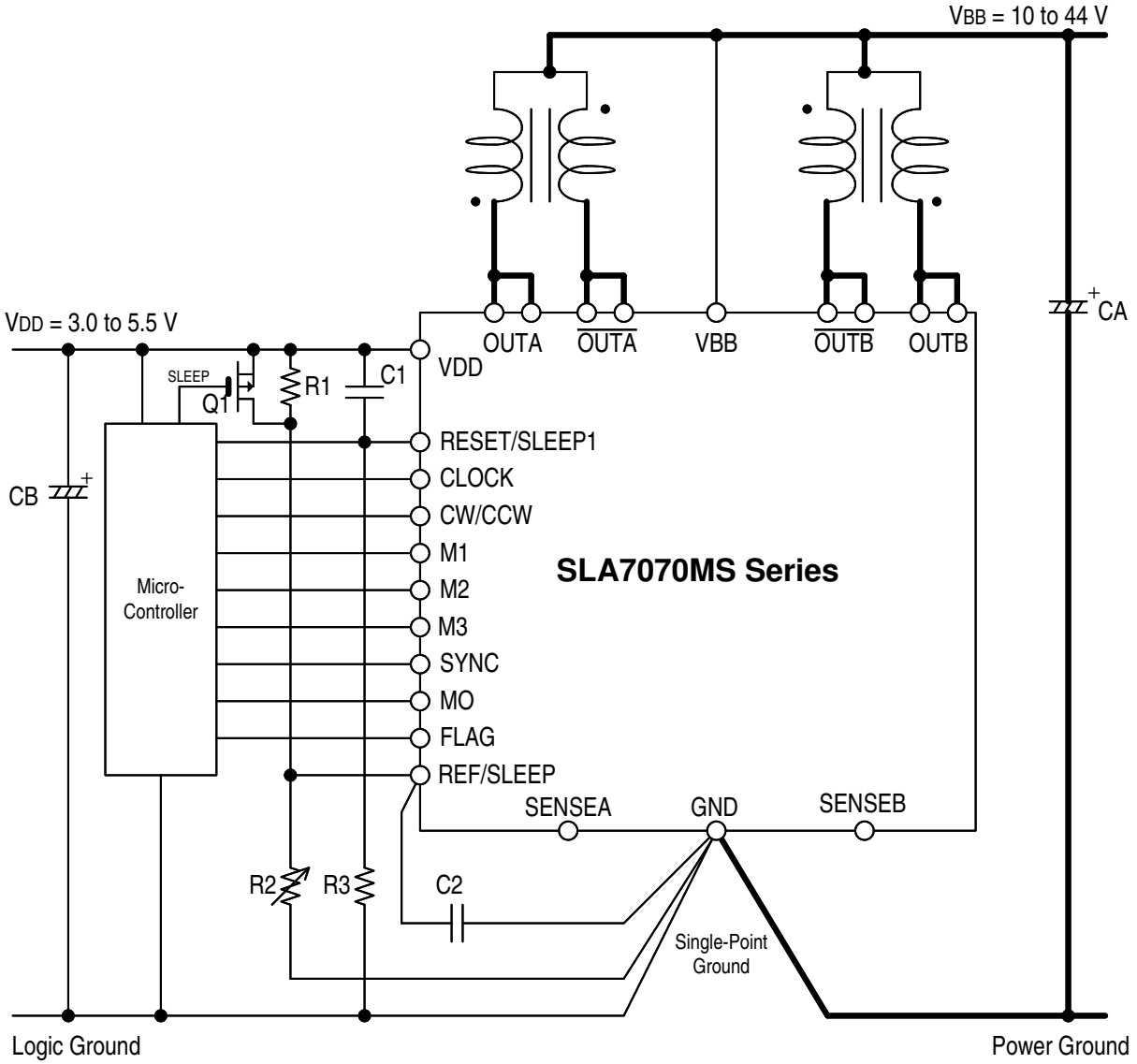
Figure 7-2. Microstep Product: SLA7078MS



Pin No.	Symbol	Function
1	OUTA	Phase A output
2		
3	$\overline{\text{OUTA}}$	Phase $\overline{\text{A}}$ output
4		
5	SENSEA	Phase A current sensing
6	MO	Output from 2-phase excitation status monitor
7	M1	Input for excitation mode & Sleep2 setting
8	M2	
9	M3	
10	CLOCK	Step clock input
11	V_{BB}	Main power supply voltage (for motor)
12	GND	Ground
13	REF/SLEEP1	Input for control current / Sleep1 setting
14	V_{DD}	Power supply to logic
15	RESET	Reset input for internal logic
16	CW/CCW	Forward / reverse input
17	SYNC	Synchronous PMW control switch input
18	FLAG	Output from protection circuit monitor for detecting coil opens/shorts
19	SENSEB	Phase B current sensing
20	$\overline{\text{OUTB}}$	Phase $\overline{\text{B}}$ output
21		
22	OUTB	Phase B output
23		

8. Application Example

Figure 8-1. Application Example for Microstep Product



Constants, for reference use only:

R1 = 10 kΩ	CA = 100 µF / 50 V
R2 = 1 kΩ (VR)	CB = 10 µF / 10 V
R3 = 10 kΩ	C1 = 0.1 µF
	C2 = 0.1 µF

NOTES:

- Take precautions to avoid noise on the V_{DD} line; noise levels greater than 0.5 V on the V_{DD} line may cause device malfunction. Noise can be reduced by separating the logic ground and the power ground on a PCB from the GND pin (Pin 12).
- Unused logic input pins (CW/CCW, M1, M2, M3, RESET, and SYNC) **must be pulled up or down to VDD or ground.** If those unused pins are left open, the device may malfunction.
- Unused logic output pins (MO, FLAG) **must be kept open**.

9. Truth Tables

(1) Common Input Pins

Table 9-1 shows the truth table for the input pins common to both full-/half-stepping and microstepping products available in the SLA7070MS series.

Table 9-1.Truth Table for Common Input Pins

Pin Name	Low Level	High Level	Clock	
			POS Edge (Standard)	POS/NEG Edge (Optional Type W)
RESET	Normal operation	Logic reset	—	
CW/CCW	Forward (CW)	Reverse (CCW)		
M1	Commutation (Sleep2 is not included)			
M2				
M3				
REF/SLEEP1	Normal operation	Sleep1 function	—	
SYNC	Non-sync PWM control	Sync PWM control	—	

The Reset function is asynchronous. If an input on the RESET pin is high, the internal logic circuit is reset. At this point, if the REF/SLEEP1 pin stays low, outputs turn on at the starting point of excitation. Note that a signal on the RESET pin cannot control an output disable command.

Voltage across the REF/SLEEP1 pin controls PWM currents and the Sleep1 function.

- When $V_{REF} \leq 1.5$ V (low level), the REF/SLEEP1 pin functions as the reference voltage input for normal operation.
- When $V_{REF} \geq 2.0$ V (high level), the REF/SLEEP1 pin disables all outputs. This is the Sleep1 mode that disables the internal linear circuitry and minimizes the main power supply current, I_{BB}. Although much of the internal circuitry is disabled, the logic circuit is still active. If an input signal on the CLOCK pin is asserted, the internal sequencer/translator circuit reacts and sets a step starting point for the next operation.

The Sleep2 function operates in the same way as the Sleep1 function does, except that the internal logic circuit enters the Hold mode. Therefore, in the Sleep2 mode, the internal sequencer/translator circuit is not activated even if a step command signal occurs on the CLOCK input pin.

The Sync function runs only at “2-phase excitation timing." If this function is used at other than the 2-phase excitation timing, an overall balance might collapse because PWM OFF-times and setting currents are different in each of phase A and phase B control scenario. (If this function is used at a point of 1-phase excitation, it does not react as the Sync function does. But there is no problem.) The 2-phase excitation timing is a point where the step reference current ratio of both phases A and B is either of Mode 8 or F.

(2) Commutation/Sleep2 Function Setting

Table 9-2 provides the logic for the pins (M1, M2, and M3) which set commutation.

Table 9-2. Truth Table for Commutation/Sleep2 Functions

Function (Pin Name)			Full/Half Step	Microstep
M1	M2	M3		
L	L	L	Full step (Mode 8 fixed)	Full step (Mode 8 fixed)
H	L	L	Full step (Mode F fixed)	Full step (Mode F fixed)
L	H	L	Half step (1-2 Phase)	Half step (1-2 Phase)
H	H	L	Half step (Mode F fixed)	Half step (Mode F fixed)
L	L	H	Sleep2 function	Quarter step (W1-2 Phase)
H	L	H		Eighth step (2W1-2 Phase)
L	H	H		Sixteenth step (4W1-2 Phase)
H	H	H		Sleep2 function

NOTE: The Sleep2 function disables outputs and reduces the driver supply current (I_{BB}) in the same way as the Sleep1 function does. However, unlike the Sleep1 function, the logic circuitry is put into a "standby" state in the Sleep2 function. Therefore, the sequencer/translator is not activated even if a step command signal occurs on the CLOCK input pin. When awaking from the Sleep2 mode, a delay of 100 μs or longer before sending a clock pulse is recommended.

(3) Monitor Output Pins

The SLA7070MS series provides two device status monitor outputs:

- MO pin (microstepping product only) – Step sequence
- FLAG pin – Protection feature operation

Table 9-3 shows the logic for the monitor output pins.

Table 9-3. Truth Table for Monitor Output Pins

Pin Name	Low Level	High Level
MO	Other than 2-phase excitation timing	2-phase excitation timing
FLAG	Normal operation	Protection circuit operation

NOTE: The outputs turn off at the point where the protection circuit starts operating. To release the protection state, cycle the logic supply voltage, V_{DD}.

10. Logic Input Pins

The low pass filter (LPF) incorporated with the logic input pins (CLOCK, RESET, CW/CCW, M1, M2, M3, and SYNC) improves noise rejection.

The logic inputs are CMOS input compatible; therefore, they are in a high impedance state. **Note that the IC should be used at a fixed input level, either low or high.**

If there is a possibility that signals from the microcontroller are in high impedance, add a pull-up/-down resistor. Since outputs from the logic input pins, which function as output ON/OFF controllers, may result in abnormal oscillation, leading to MOSFET breakdown as the worst-case scenario.

11. Logic Input Timing

(1) Clock Signal

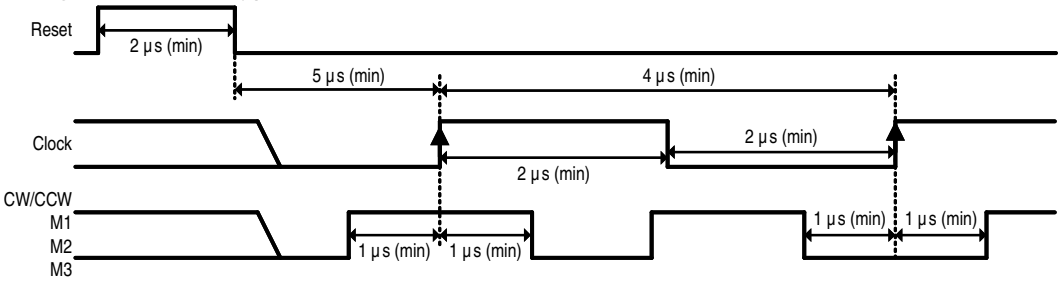
a. A low-to-high transition (rising, or POS edge) or a low-to-high then high-to-low transition (rising and falling, or POS/NEG edge) on the CLOCK input signal advances the sequencer/translator. Clock pulse width should be set at 2 µs or longer in both positive and negative polarities. Therefore, clock response frequency is set to 250 kHz.

b. Clock Edge Timing

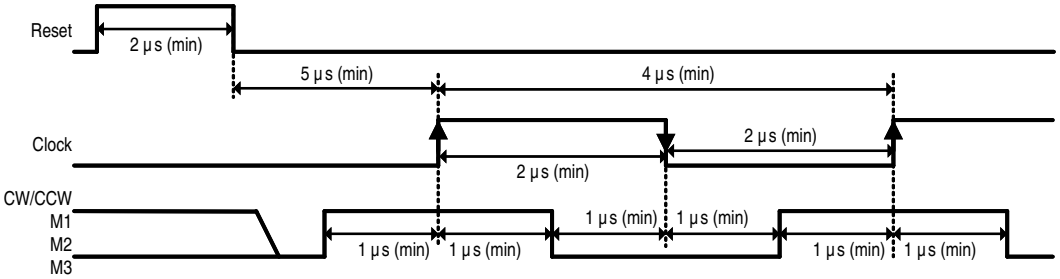
With regard to the input logic of the CW/CCW, M1, M2, and M3 pins, a 1 µs delay should occur both before and after a pulse edge, as setup and hold times (see Figure 11-1). The sequencer logic circuitry might malfunction if the logic polarity is changed during these setup and hold times.

Figure 11-1. Input Signal Timing

POS Edge (Standard Type)



POS/NEG Edge (Optional Type W)



NOTE: When awaking from the Sleep1 or Sleep2 mode, a delay of *100 µs or longer* before sending a clock pulse is recommended.

(2) Reset Signal

a. Reset Signal Pulse Width

Reset pulse width is equivalent to the hold time of a high level input. It should be 2 µs or longer, same as the clock pulse width.

b. Reset Release and Clock Input Timing

When the timing of a reset release (falling edge) and a clock edge is simultaneous, the internal logic might result in an unexpected operation. Therefore, a greater than 5 µs delay is required between the falling edge of the RESET input signal and the next rising edge of the CLOCK input signal (see Figure 11-1).

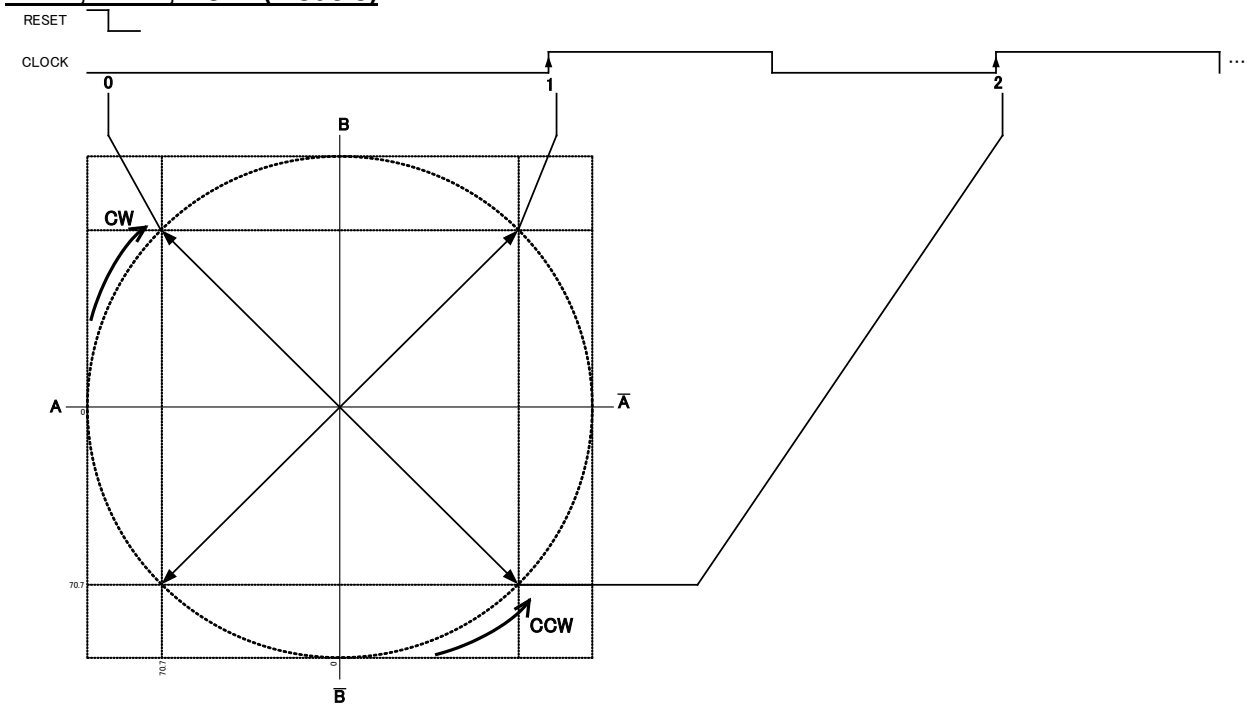
(3) Logic Level Change

Logic level inputs on CW/CCW, M1, M2, and M3 set the translator step direction (CW/CCW) and step mode (M1, M2, and M3; see also Table 9-2, the commutation truth table). Changes to those inputs do not take effect until the rising edge of an input signal on the CLOCK pin. However, depending on the type and state of a motor, there may be errors in motor operation such as step-out. A thorough evaluation on the changes of sequence should be carried out.

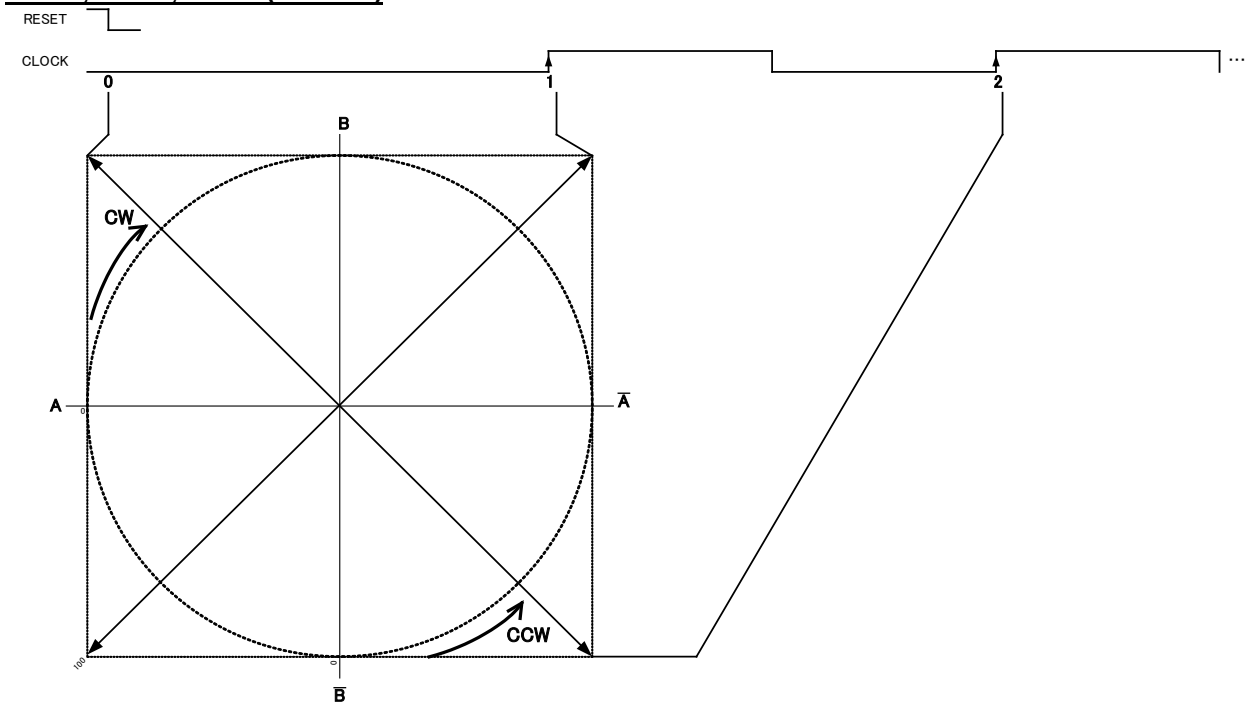
12. Step Sequence Diagrams

Figure 12-1. Full Step (2 Phase Excitation)

M1: L, M2: L, M3: L (Mode 8)



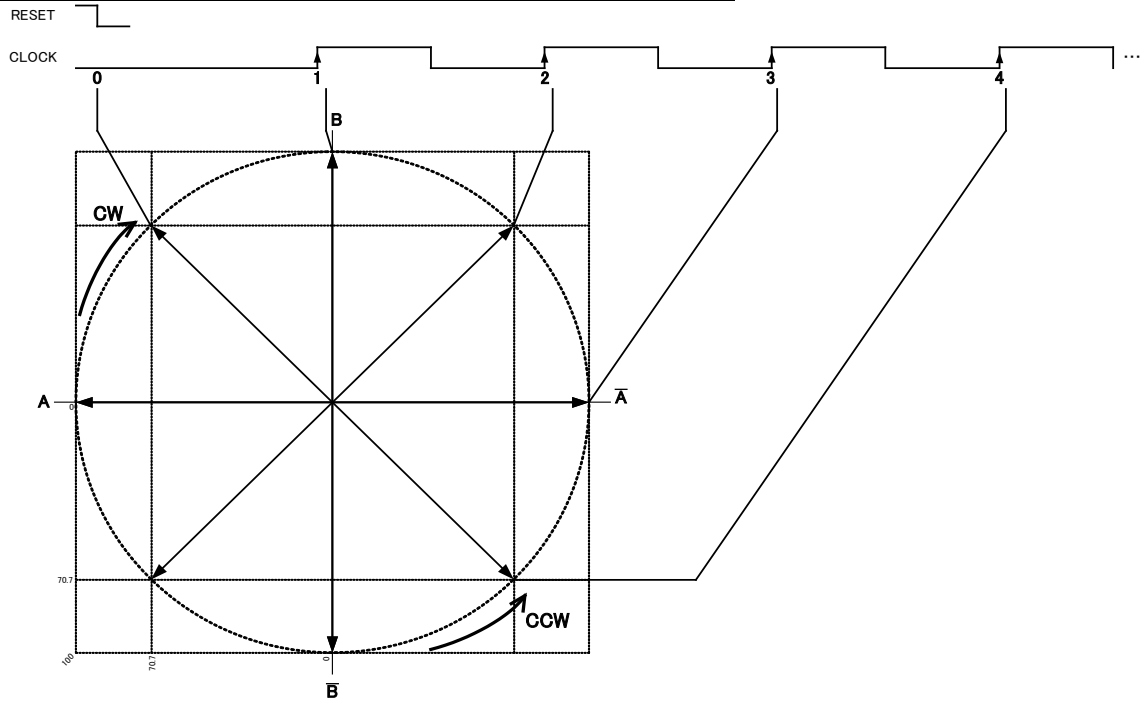
M1: H, M2: L, M3: L (Mode F)



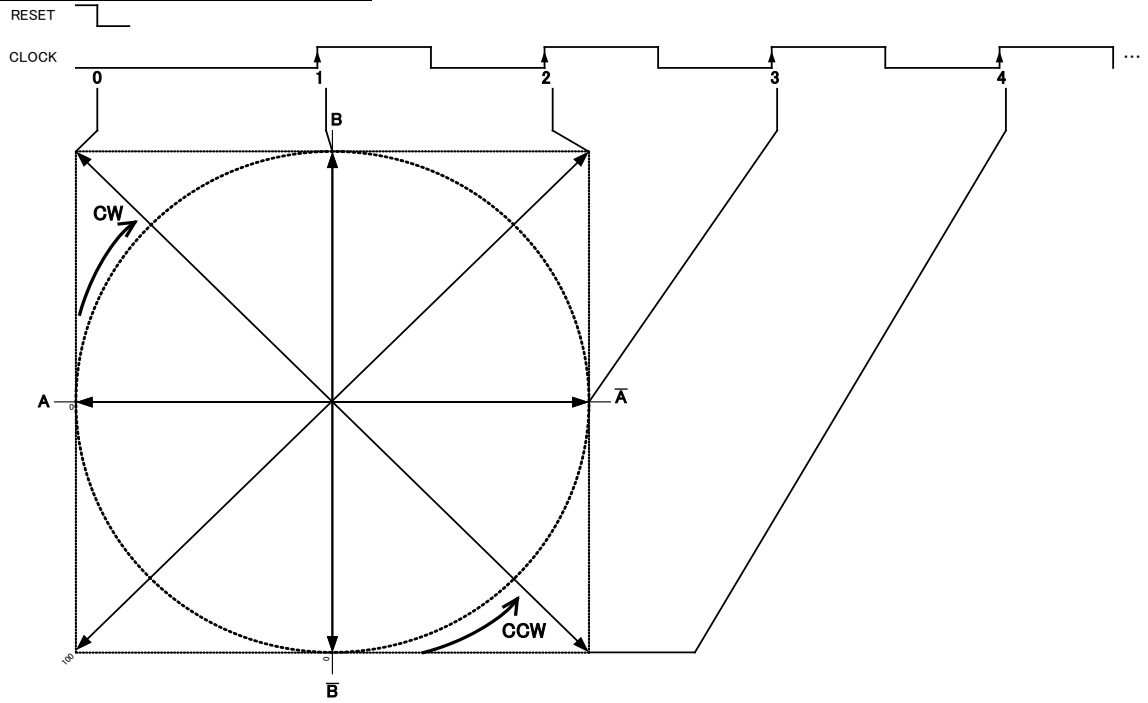
NOTE: All illustrations in this section are based on step sequencing at the POS edge (standard type). For POS/NEG edge (optional type W) products, both of the rising and falling edges of a clock input signal activate the step sequencer.

Figure 12-2. Half Step (1-2 Phase Excitation)

M1: L, M2: H, M3: L (1 Phase: Mode F / 2 Phase: Mode 8)

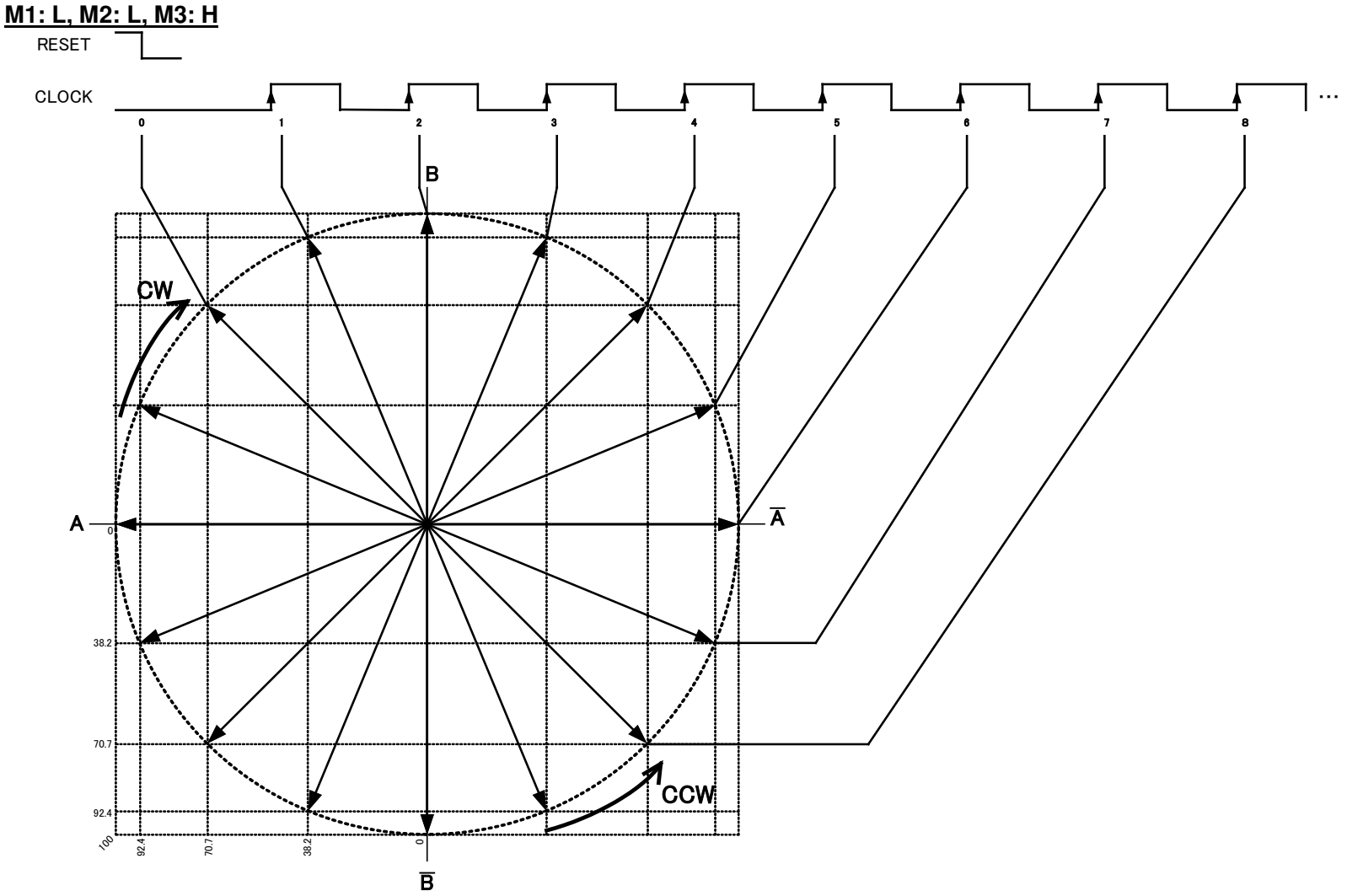


M1: H, M2: H, M3: L (Mode F)



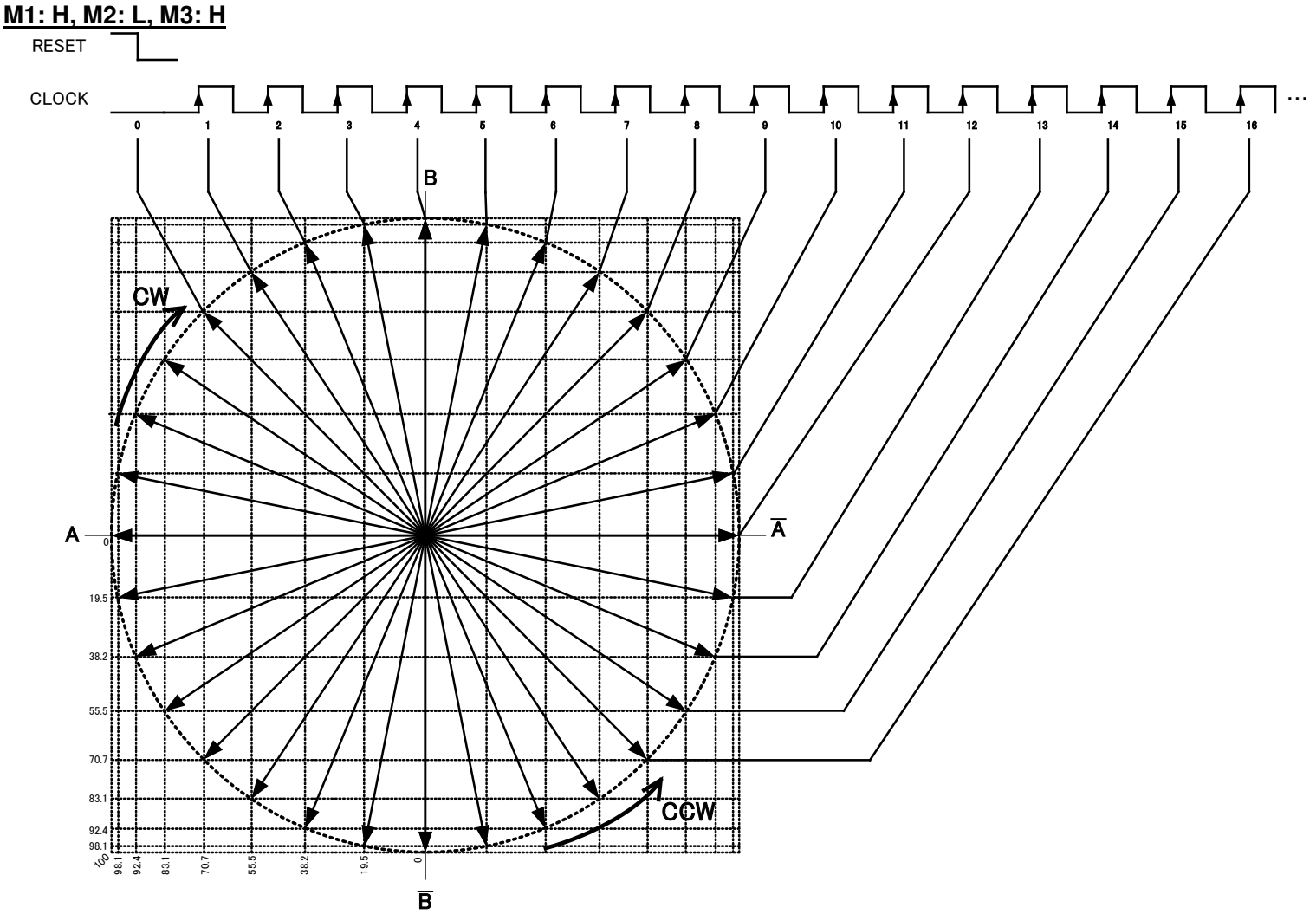
NOTE: All illustrations in this section are based on step sequencing at the POS edge (standard type). For POS/NEG edge (optional type W) products, both of the rising and falling edges of a clock input signal activate the step sequencer.

Figure 12-3. Quarter Step (W1-2 Phase Excitation); for microstep product only



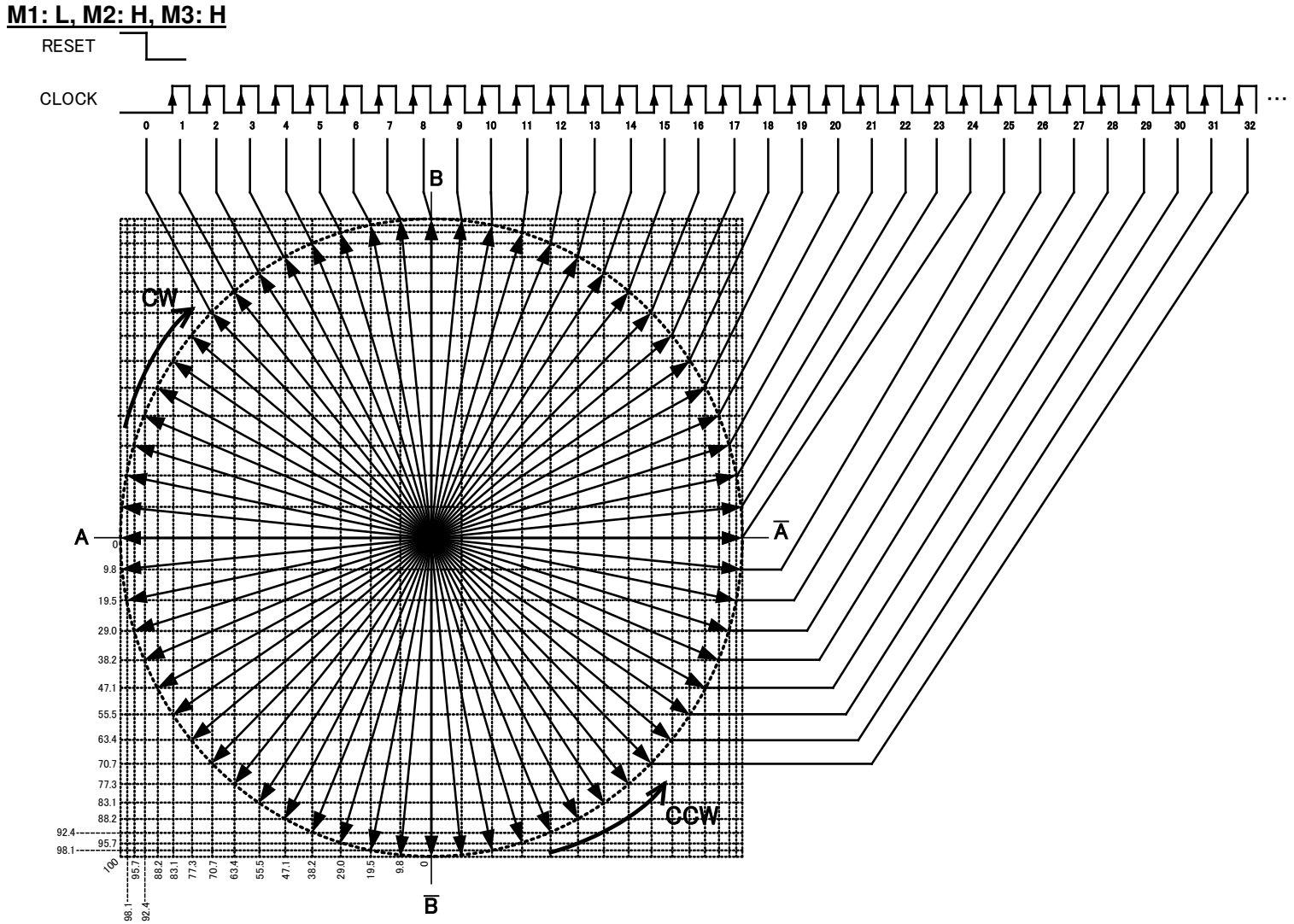
NOTE: All illustrations in this section are based on step sequencing at the POS edge (standard type). For POS/NEG edge (optional type W) products, both of the rising and falling edges of a clock input signal activate the step sequencer.

Figure 12-4. Eighth Step (2W1-2 Phase Excitation); for microstep product only



NOTE: All illustrations in this section are based on step sequencing at the POS edge (standard type). For POS/NEG edge (optional type W) products, both of the rising and falling edges of a clock input signal activate the step sequencer.

Figure 12-5. Sixteenth Step (4W1-2 Phase Excitation); for microstep product only



NOTE: All illustrations in this section are based on step sequencing at the POS edge (standard type). For POS/NEG edge (optional type W) products, both of the rising and falling edges of a clock input signal activate the step sequencer.

Excitation Change Sequence

The change of excitation modes is determined by the settings of the excitation pins (M1, M2, and M3) before and after a step signal. Table 12-1 shows each excitation mode state setting.

Table 12-1. Excitation Mode States

Direction	Internal Sequence State[1]				Step Sequencing[2]						
	Phase A		Phase B		2 Phase (Full Step)		1-2 Phase (Half Step)		W1-2 Phase (1/4 Step)	2W1-2 Phase (1/8 Step)	4W1-2 Phase (1/16 Step)
	PWM	Mode	PWM	Mode	Mode 8	Mode F	Mode 8/F	Mode F			
CCW	A	8	B	8	X	XX	X	XX	X	X	X
	A	7	B	9							X
	A	6	B	A						X	X
	A	5	B	B							X
	A	4	B	C					X	X	X
	A	3	B	D							X
	A	2	B	E						X	X
	A	1	B	F							X
	-	-	B	F			X	X	X	X	X
	/A	1	B	F							X
	/A	2	B	E						X	X
	/A	3	B	D							X
	/A	4	B	C					X	X	X
	/A	5	B	B							X
	/A	6	B	A						X	X
	/A	7	B	9							X
	/A	8	B	8	X	XX	X	XX	X	X	X
	/A	9	B	7							X
	/A	A	B	6						X	X
	/A	B	B	5							X
	/A	C	B	4					X	X	X
	/A	D	B	3							X
	/A	E	B	2						X	X
	/A	F	B	1							X
	/A	F	-	-			X	X	X	X	X
	/A	F	/B	1							X
	/A	E	/B	2						X	X
	/A	D	/B	3							X
	/A	C	/B	4					X	X	X
	/A	B	/B	5							X
	/A	A	/B	6						X	X
	/A	9	/B	7							X
	/A	8	/B	8	X	XX	X	XX	X	X	X
	/A	7	/B	9							X
	/A	6	/B	A						X	X
	/A	5	/B	B							X
	/A	4	/B	C					X	X	X
	/A	3	/B	D							X
	/A	2	/B	E						X	X
	/A	1	/B	F							X
	-	-	/B	F			X	X	X	X	X
	A	1	/B	F							X
	A	2	/B	E						X	X
	A	3	/B	D							X
	A	4	/B	C					X	X	X
	A	5	/B	B							X
	A	6	/B	A						X	X
	A	7	/B	9							X
	A	8	/B	8	X	XX	X	XX	X	X	X
	A	9	/B	7							X
	A	A	/B	6						X	X
CW	A	B	/B	5							X
	A	C	/B	4					X	X	X
	A	D	/B	3							X
	A	E	/B	2						X	X
	A	F	/B	1							X
	A	F	-	-			X	X	X	X	X
	A	F	B	1							X
	A	E	B	2						X	X
	A	D	B	3							X
	A	C	B	4					X	X	X
	A	B	B	5							X
	A	A	B	6						X	X
	A	9	B	7							X

[1] Each mode is defined accordingly to the SLA7070M series.

[2] **XX** indicates that sequence state is Mode 8; but step reference current ratio is Mode F. Mode F has a step reference current ratio of 100%, and a PWM OFF-time of 12 µs.

13. Individual Circuit Descriptions

(1) Monolithic IC (MIC)

・Sequencer Logic

A single clock strategy is employed for step timing. An input on the CW/CCW pin determines the direction of motor rotation. Excitation mode is controlled by the combination of the M1, M2, and M3 input logic levels. See Section 9 for truth tables, and Section 11 for input timings.

・DAC (D-to-A Converter)

DACs that generate the reference voltage for controlling current. In microstep sequencing, the current at each step is set by the values of a sense resistor (R_S), a reference voltage (V_{REF}), the output voltage of the DACs, controlled by the output of the sequencer/translator circuit. For the step reference current ratios, see the electrical characteristics tables given in Section 4.

・PWM Control

Circuits that allow self-excitation PWM current controlling with a fixed OFF-time are used in this series. Each built-in oscillator (OSC) determines an OFF-time and a blanking time for proper PWM operation. The operation mechanism of the PWM control circuitry is identical to that of the SLA7070M family. For more detailed functional descriptions, see Section 14.

・Synchronous Control

A synchronous chopping circuit that prevents occasional motor noise during a hold state which normally results from the asynchronous PWM operation of both motor phases. When the SYNC input pin is set to logic high, the circuit sends a timing signal that simultaneously turns off the chopping of phases A and B.

This function adopts the same operation mechanism applied to the SLA7070M series. Therefore, the use of the synchronous control during normal stepping is not recommended because, it produces less motor torque or may cause motor vibration due to staircase current.

The use of the synchronous control when the motor is not in operation is only allowed in 2-phase excitation timing, because the differences in current control values and PWM OFF-times between phases A and B exist at other excitation timings; otherwise, these two phases may not be synchronized or may be greatly disrupted in their current control values.

・Regulator Circuit

An integrated regulator circuit is used for powering the output MOSFET gate drive circuit (pre-driver) and other internal linear circuits.

・Protection Circuit

Built-in protection circuits against motor coil opens or shorts are provided. This protection is activated by sensing the voltage across internal sense resistors, R_S. Therefore, an overcurrent condition cannot be detected which results from the OUTx pins or SENSEx pins, or both, shorting to GND. The protection against motor coil opens is available only during PWM operation; therefore, it does not work at constant voltage driving, when the motor is rotating at a high speed.

The operation of the protection circuit disables all outputs. To come out of the Protection mode, cycle the logic supply, V_{DD}. For more details, see the next section.

・TSD Circuit

A TSD circuit that protects a driver by shifting an output to the Disable mode is incorporated. When the temperature of the product control IC (MIC) rises and becomes higher than its threshold, the circuit starts operating. To reset the function, perform the same steps as described in the Protection Circuit description.

(2) Output MOSFET Chip

The type of MOSFET chips to be mounted varies according to which of the two different output current ratings has been selected. For specifications, see Table 4-5.

Rated Current (A)	Resistance (ΩTyp.)
2.0	0.25
3.0	0.18

NOTE: Each resistance shown above includes approximately 5 mΩ circuit resistance in addition to the resistance of the built-in resistor itself.

(3) Sense Resistor

Sense resistors are incorporated in this series to detect motor current. The resistance of these varies according to which of the two different output current ratings has been selected. For specifications, see Table 4-5.

Rated Current (A)	Resistance (ΩTyp.)
2.0	0.205
3.0	0.155

NOTE: Each resistance shown above includes approximately 5 mΩ circuit resistance in addition to the resistance of the built-in resistor itself.

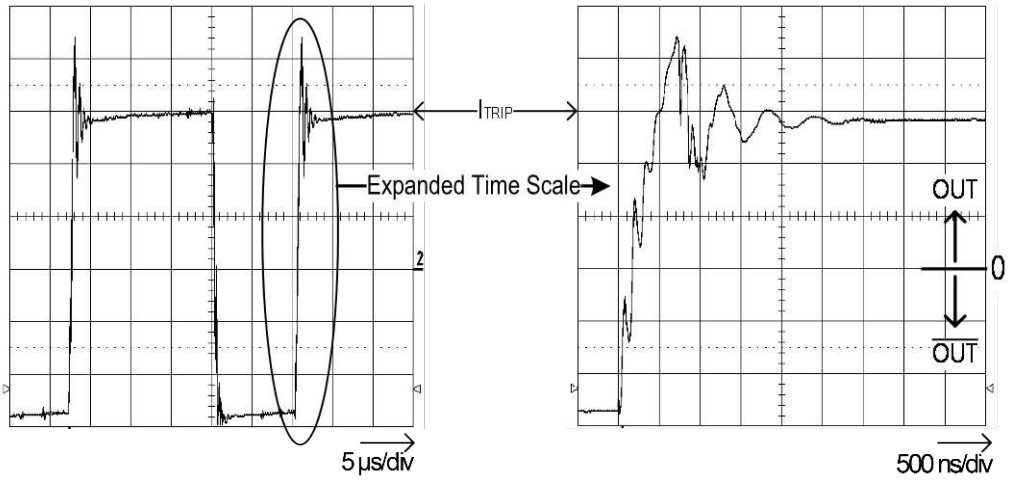
14. Functional Descriptions

(1) PWM Current Control

[1] Blanking Time

An actual operating waveform on the SENSEx pin when driving a motor is shown in Figure 14-1.

Figure 14-1. Operating Waveform on SENSEx Pin during PWM Chopping
(Circled area of the left panel is shown in expanded scale in the right panel)

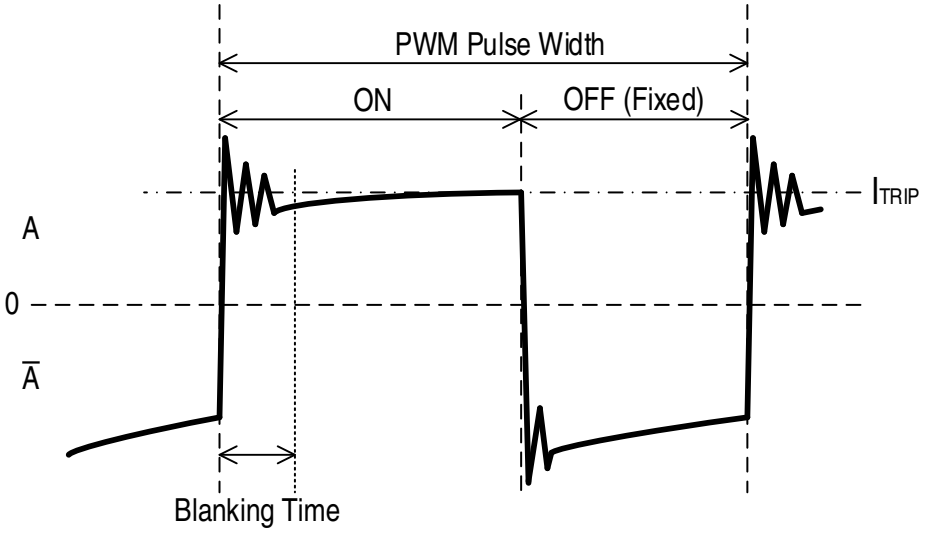


Immediately after a PWM turns off, ringing (or spike) noise on the SENSEx pin is observed for a period of a few microseconds. Ringing noise can be generated by various causes, such as capacitance between motor coils or inappropriate motor wiring.

Each pair of outputs is controlled by a fixed OFF-time PWM current-control circuit that limits the load current to a target value, I_{TRIP}. Initially, an output is enabled and then currents flow through the motor winding and the current sense resistors. When the voltage across the current sense resistors equals the DAC output voltage, V_{TRIP}, the current sense comparator resets a PWM latch. This turns off the driver for the fixed OFF-time, during which the load inductance causes the current to recirculate for the OFF-time period. Therefore, if the ringing noise on the current sense resistor(s) equals and surpasses V_{TRIP}, the PWM turns off (i.e., a hunting phenomenon).

To prevent this phenomenon, a blanking time is set to override signals from the current sense comparator for a certain period immediately after the PWM turns on (Figure 14-2).

Figure 14-2. SENSEx Pin Waveform Pattern during PMW Control

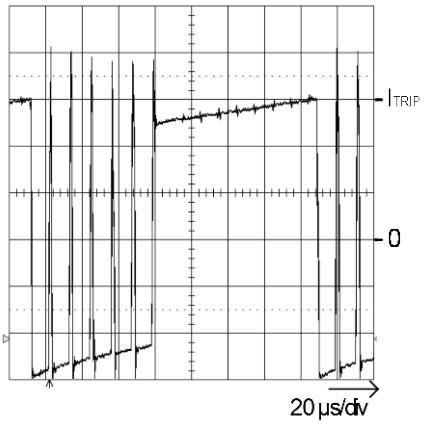


[2] Blanking Time and Hunting Phenomenon

Although current control can be improved by shortening a blanking time, the degree of margin to a ringing noise decreases simultaneously. For this reason, when a motor is driven by the device, a hunting phenomenon may occur. Figure 14-3 shows an example of the waveform pattern when the phenomenon occurs.

In order to overcome this problem, Sanken has released a new option, "type B", which offers a longer blanking time. Having the longer blanking time, the optional type B can improve problems such as torque reduction and huge motor noise that are occasionally found during the hunting phenomenon.

Figure 14-3. Example of SENSEx Pin Waveform during Hunting Phenomenon



[3] Blanking Time Difference

Table 14-1 shows characteristic differences between two blanking times, shorter and longer blanking periods.

This comparison is based on the case where drive conditions, such as a motor, motor power supply voltage, REF input voltage, and circuit constant were kept the same while only the indicated parameters were changed.

Table 14-1. Characteristic Comparison of Difference in Blanking Time

Parameter	Better Performance	
Internal blanking time	Short	Long
Minimum PWM ON-time	Small ←	
Ringing noise suppression		→ Large
Minimum coil current	Small ←	
Coil current waveform distortion at a high rotation (mainly microstep)		→ Large

Brief descriptions for each parameter are as follows:

- Minimum PWM ON-time, $t_{ON(min)}$

  This series has a blanking time that is effectively selected and fixed by the PWM control. Therefore, even if an application attempts to shorten its ON-time for limiting currents, it would not go below the fixed blanking time. Minimum PWM ON-time refers to the time when an output is on during this blanking time period, that is, when an output MOSFET is actually turned on. In other words, a blanking time determines a minimum ON-time ("Small" in Table 14-1).

- Minimum Coil Current

  This refers to the coil current when the PWM control is performed during a minimum PWM ON-time. In other words, the device with a shorter blanking time can reduce more coil current.

- Coil Current Waveform Distortion during High-Velocity Revolution

  While a microstep drive is active, the I_{TRIP} value changes to a predetermined value in accordance with a clock input. The I_{TRIP} value (internal reference voltage splitting ratio) is then set up to be a sine wave. Because the PWM control of motor coil current is set according to the I_{TRIP} value, (the envelope of) the motor coil current will also be controlled to be sine wave-like.