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NON-ISOLATED DC/DC CONVERTERS

4.5 Vdc – 14.4 Vdc Input, 0.45 Vdc – 2.0 Vdc /40 A Outputs



Jul.10, 2015

Bel Power Inc., a subsidiary of Bel Fuse Inc.

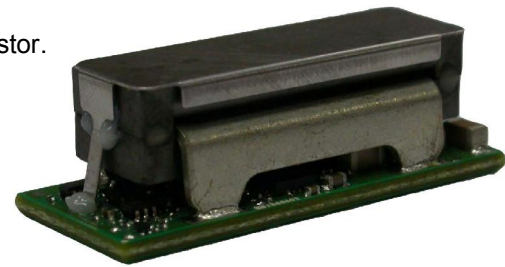
SLDN-40E1Ax

RoHS Compliant

Rev.E

Features

- Non-Isolated
- Power Good signal
- Remote On/Off
- Over temperature protection
- Compliant to IPC-9592 (September 2008), Category 2, Class II
- Compliant to RoHS EU Directive 2002/95/EC
- Compatible in a Pb-free or SnPb reflow environment
- Output voltage programmable from 0.6Vdc to 2.0Vdc via external resistor. Digitally adjustable down to 0.45Vdc.
- Digital interface through the PMBus™ protocol
- Tunable Loop™ optimize to dynamic output voltage response
- Fixed switching frequency with capability of external synchronization
- Output overcurrent protection (non-latching)
- Small size: 33.02mm x 13.46 mm x 10.9mm (1.3 in x 0.53 in x 0.429 in)
- Wide operating temperature range [-40°C to 85°C]
- UL60950-1 2nd Ed. Recognized, CSA C22.2 No. 60950-1-07 Certified
- ISO 9001 and ISO 14001 certified manufacturing facilities
- Wide Input voltage range (4.5Vdc-14.4Vdc)
- Cost efficient open frame design
- Ability to sink and source current



Applications

- Distributed power architectures
- Intermediate bus voltage applications
- Telecommunications equipment
- Servers and storage applications
- Networking equipment
- Industrial equipment



Description

The SLDN-40E1Ax modules are non-isolated dc-dc converters that can deliver up to 40A of output current. These modules operate over a wide range of input voltage ($V_{IN} = 4.5 \text{ Vdc} - 14.4 \text{ Vdc}$) and provide a precisely regulated output voltage from 0.45 Vdc to 2.0 Vdc, programmable via an external resistor and PMBus control. Features include a digital interface using the PMBus protocol, remote On/Off, adjustable output voltage, over current and over temperature protection. The PMBus interface supports a range of commands to both control and monitor the module. The module also includes the Tunable Loop™ feature that allows the user to optimize the dynamic response of the converter to match the load with reduced amount of output capacitance leading to savings on cost and PWB area.

Part Selection

Output Voltage	Input Voltage	Max. Output Current	Max. Output Power	Typical Efficiency	Model Number Active High	Model Number Active Low
0.45 – 2.0 Vdc	4.5 - 14.4 Vdc	40 A	80W	91.5%	SLDN-40E1A0	SLDN-40E1AL

- Notes:** 1. Add "R" suffix at the end of the model number to indicate tape and reel packaging (Standard).
2. Add "G" suffix at the end of the model number to indicate tray packaging (Option).

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Ordering Part Number

S LDN - 40 E 1A x V
 1 2 3 4 5 6 7

1---Surface mount

2---Series code

3---Output current (40A)

4---Wide input voltage range (4.5-14.4V)

5--- With sequencing

6--- Enable, "0" means active high, "L" means active low

7--- Package

Absolute Maximum Ratings

Parameter	Min	Max	Unit	Notes
Continuous Input Voltage	-0.3	15	V	
Voltage on SEQ ,SYNC,VS+	-	7	V	
Voltage on CLK,DATA,SMBALERT terminal	-	3.6	V	
Operating Ambient Temperature	-40	85	°C	see Thermal Considerations section
Storage Temperature	-55	125	°C	
Altitude	-	2000	m	

Note: Stresses in excess of the absolute maximum ratings can cause permanent damage to the device. These are absolute stress ratings only, functional operation of the device is not implied at these or any other conditions in excess of those given in the operations sections of the data sheet. Exposure to absolute maximum ratings for extended periods can adversely affect the device reliability.

Input Specifications

Parameter	Min	Typ	Max	Unit	Notes
Operating Input Voltage	4.5	-	14.4	V	
Input Current (full load)	-	-	24	A	$V_{IN}=4.5V$ to $14V$, $I_O=I_{O,max}$
Input Current (no load)	-	54.7	-	mA	$V_{O,set} = 0.6Vdc$
	-	104	-	mA	$V_{O,set} = 2Vdc$
Input Stand-by Current	-	12.5	-	mA	$V_{IN} = 12V$, module disabled
Input Reflected Ripple Current (pk-pk)	-	90	-	mA	1. 5Hz to 20MHz, $1\mu H$ source impedance; $V_{IN}=0$ to $14V$, $I_O= I_{O,max}$ 2. See Test Configurations
I^2t Inrush Current Transient	-	-	1	A^2s	
Input Ripple Rejection (120Hz)	-	-60	-	dB	

Note: Unless otherwise indicated, specifications apply over all operating input voltage, resistive load, and temperature conditions.

NON-ISOLATED DC/DC CONVERTERS

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Output Specifications

Parameter	Min	Typ	Max	Unit	Notes
Output Voltage Set Point	-1.0	-	+1.0	%V _{o,set}	with 0.1% tolerance for external resistor used to set output voltage
Output Voltage	-3.0	-	+3.0	%V _{o,set}	Over all operating input voltage, resistive load, and temperature conditions until end of life
PMbus Adjustable Output Voltage Range	-25	0	+25	%V _{o,set}	
PMbus Output Voltage Adjustment Step Size	0.4	-	-	%V _{o,set}	
Adjustment Range	0.6	-	2.0	V	1.Selected by an external resistor 2.Some output voltages may not be possible depending on the input voltage – see Feature Descriptions Section
Remote Sense Range	-	-	0.5	V	
Load Regulation			10	mV	I _o =I _{o, min} to I _{o, max}
Line Regulation			6	mV	V _{IN} =V _{IN, min} to V _{IN, max}
Temperature Regulation	-	0.4	-	%V _{o,set}	T _{ref} =T _{A, min} to T _{A, max}
Output Ripple and Noise (pk-pk)	-	50	100	mV	5Hz to 20MHz BW, V _{IN} =V _{IN, nom} and I _o =I _{o, min} to I _{o, max} Co = 0.1µF // 22 µF ceramic capacitors)
Output Ripple and Noise (rms)	-	20	38	mV	
Output Short-Circuit Current	-	2.1	2.83	A _{rms}	V _o ≤250mV, Hiccup Mode
Output Capacitance ² ESR ≥ 1 mΩ	6×47	-	6×47	µF	Without the Tunable Loop™ With the Tunable Loop™ With the Tunable Loop™
ESR ≥ 0.15 mΩ	6×47	-	7000	µF	
ESR ≥ 10 mΩ	6×47	-	8500	µF	
Output Current	0	-	40	A	In either sink or source mode
Output Current Limit Inception	-	150	180	% I _{o,max}	Current limit does not operate in sink mode
Turn-On Delay Times (V _{IN} =V _{IN, nom} , I _o =I _{o, max} , V _O to within ±1% of steady state)	1.0	1.1	1.7	msec	Case 1: On/Off input is enabled and then input power is applied (delay from instant at which V _{IN} = V _{IN, min} until V _o = 10% of V _{o, set})
	600	700	1800	µsec	Case 2: Input power is applied for at least one second and then the On/Off input is enabled (delay from instant at which Von/Off is enabled until V _o = 10% of V _{o, set})
Output voltage Rise time	1.2	1.5	2.2	msec	time for V _o to rise from 10% of V _{o, set} to 90% of V _{o, set}
Output voltage overshoot	0	1.5	3.0	% V _{o, set}	T _A = 25°C, V _{IN} = V _{IN, min} to V _{IN, max} , I _o = I _{o, min} to I _{o, max} With or without maximum external capacitance

Notes: ²External capacitors may require using the new Tunable Loop™ feature to ensure that the module is stable as well as getting the best transient response. See the Tunable Loop™ section for details.

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4.5 Vdc – 14.4 Vdc Input, 0.45 Vdc – 2.0 Vdc /40 A Outputs



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General Specifications

Parameter	Min	Typ	Max	Unit	Notes	
Efficiency						
	Vo=0.6V	78	81.3	-	%	V _{in} = 12Vdc, T _A =25°C I _o =I _{o, max} , Vo= V _{o,set}
	Vo=1.2V	84	88.5	-	%	
	Vo=1.8V	85.25	91.5	-	%	
Switching Frequency	380	400	420		kHz	
Synchronization Frequency Range	350	-	480		kHz	
High-Level Input Voltage	2.0	-	-		V	
Low-Level Input Voltage	-	-	0.4		V	
Input Current, SYNC	-	-	100		nA	
Minimum Pulse Width, SYNC	100				ns	
Maximum SYNC rise time	100				ns	
Over Temperature Protection	123	130	137		°C	
PMBus Over Temperature Warning Threshold	120	130	140		°C	Warning may not activate before alarm and unit may shutdown before warning.
PMBus Adjustable Input Under Voltage Lockout Thresholds	2.5	-	14		V	
Resolution of Adjustable Input Under Voltage Threshold	-	-	500		mV	
Input Undervoltage Lockout						
	Turn-on Threshold	4.144	4.25	4.407		V
	Turn-off Threshold	3.947	3.98	4.163		V
	Hysteresis	0.25	0.3	0.35		V
Tracking Accuracy						
	Power-Up: 0.5V/ms	-	-	100		mV
	Power-Down: 0.5V/ms	-	-	100		mV
PGOOD (Power Good)						
	Overvoltage threshold for PGOOD ON	103	108	113		%V _{o, set}
	Overvoltage threshold for PGOOD OFF	105	110	115		%V _{o, set}
	Undervoltage threshold for PGOOD ON	87	92	97		%V _{o, set}
	Undervoltage threshold for PGOOD OFF	85	90	95		%V _{o, set}
	Pulldown resistance of PGOOD pin	-	-	50		Ω
	Sink current capability into PGOOD pin	-	-	5		mA
Weight	10.53	11.7	12.87		g	
MTBF	6,498,438				hours	Calculated MTBF (I _o =0.8I _{o, max} , T _A =40°C) Telcordia Issue 2 Method 1 Case 3
Dimensions						
	Inches (L × W × H)	1.300 x 0.530 x 0.429				-
	Millimeters (L × W × H)	33.02 x 13.46 x 10.90				

Note: Unless otherwise indicated, specifications apply over all operating input voltage, resistive load, and temperature conditions.

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Digital Interface Specifications

Parameter	Min	Typ	Max	Unit	Notes
PMBus Signal Interface Characteristics					
Input High Voltage (CLK, DATA)	2.1	-	3.6	V	
Input Low Voltage (CLK, DATA)	-	-	0.8	V	
Input high level current (CLK, DATA)	-10	-	10	uA	
Input low level current (CLK, DATA)	-10	-	10	uA	
Output Low Voltage (CLK, DATA, SMBALERT#)	-	-	0.4	V	$I_{out}=2mA$
Output high level open drain leakage current (DATA, SMBALERT#)	0	-	10	uA	$V_{out}=3.6V$
Pin capacitance	-	0.7	-	pF	
PMBus Operating frequency range	10	-	400	KHz	
Data setup time	250	-	-	ns	
Data hold time	$\frac{0}{300}$	-	-	ns	$\frac{\text{Receive Mode}}{\text{Transmit Mode}}$
Measurement System Characteristics					
Read delay time	153	192	231	us	
Output current measurement range	0	-	40	A	
Output current measurement resolution	62.5	-	-	mA	
Output current measurement gain accuracy	-	-	± 5	%	
Output current measurement offset	-	-	0.1	A	
V_{OUT} measurement range	0	-	2.0	V	
V_{OUT} measurement resolution	-	16.25	-	mV	
V_{OUT} measurement gain accuracy	-2	-	2	LSB	
V_{OUT} measurement offset	-3	-	3	%	
V_{OUT} measurement accuracy	-15	-	15	%	
V_{IN} measurement range	0	-	14.4	V	
V_{IN} measurement resolution	-	32.5	-	mV	
V_{IN} measurement gain accuracy	-2	-	2	LSB	
V_{IN} measurement offset	-5.5	-	1.4	%	
V_{IN} measurement accuracy	-	± 3	-	%	

Note: Unless otherwise indicated, specifications apply over all operating input voltage, resistive load, and temperature conditions. See Feature Descriptions for additional information.

NON-ISOLATED DC/DC CONVERTERS

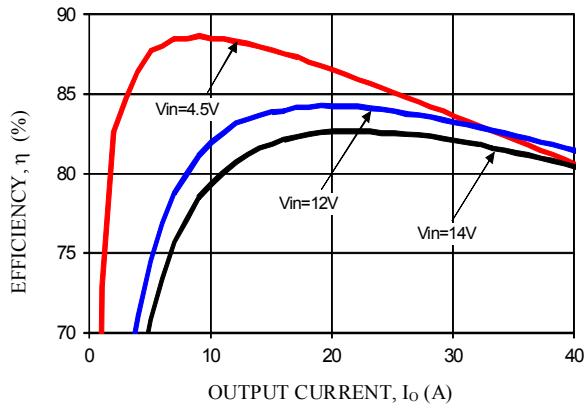
4.5 Vdc – 14.4 Vdc Input, 0.45 Vdc – 2.0 Vdc /40 A Outputs



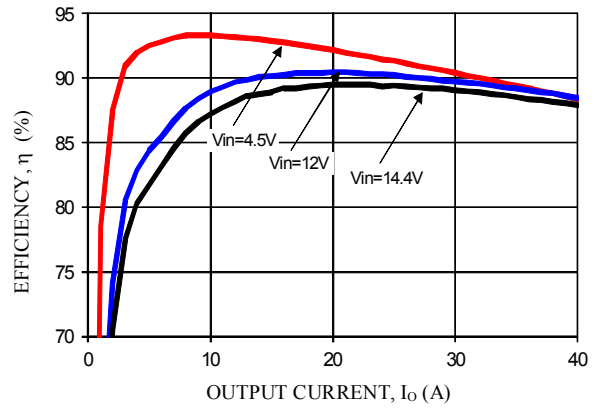
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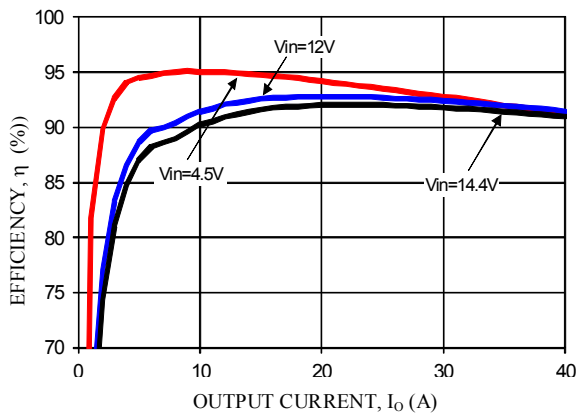
Efficiency Data



$V_o=0.6V$



$V_o=1.2V$



$V_o=1.8V$

NON-ISOLATED DC/DC CONVERTERS

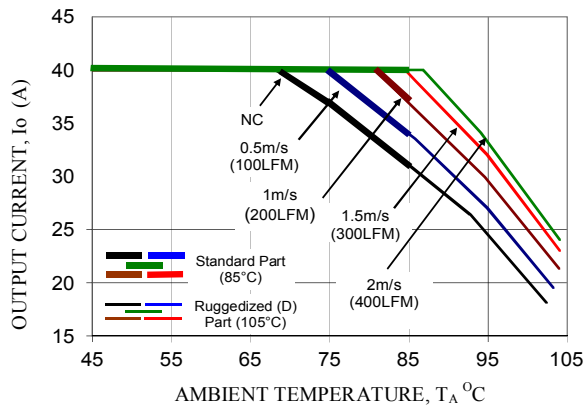
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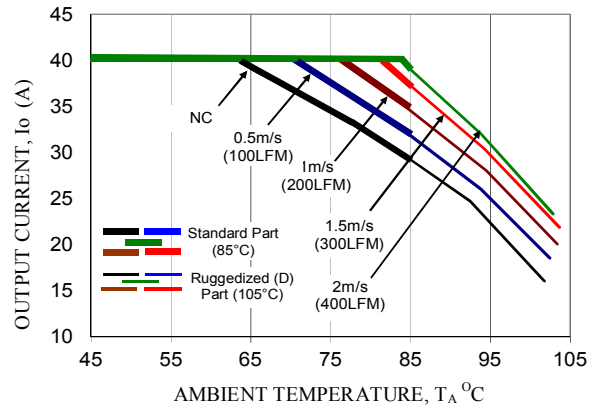
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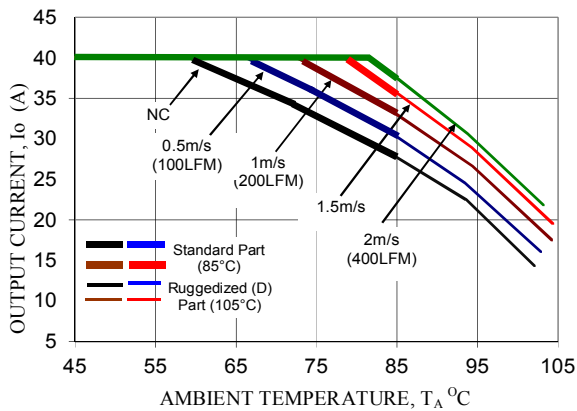
Thermal Derating Curves



$V_o=0.6V$



$V_o=1.2V$



$V_o=1.8V$

NON-ISOLATED DC/DC CONVERTERS

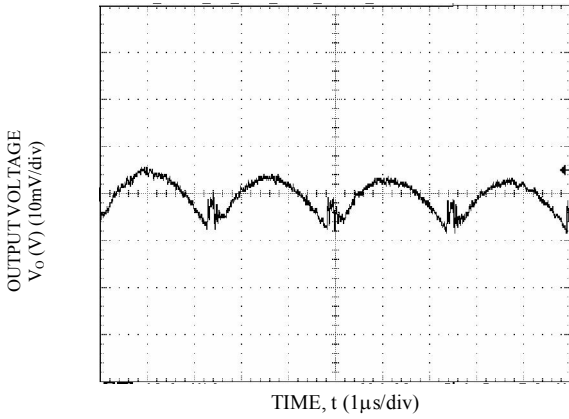
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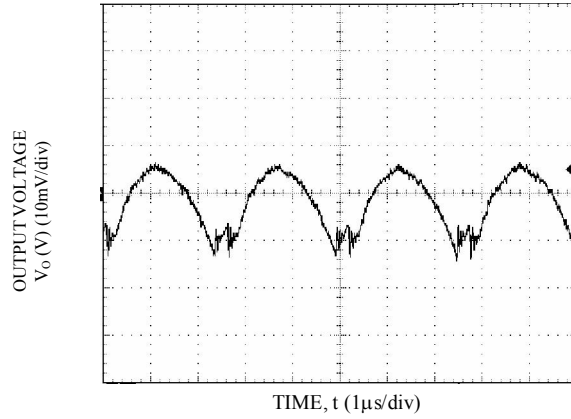
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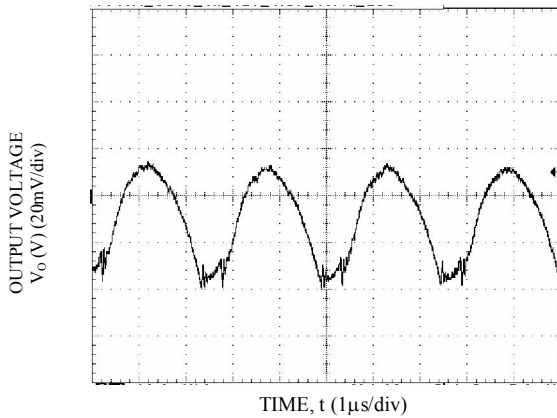
Output ripple and Noise Waveforms



Vo=0.6V, Io = Io,max



Vo=1.2V, Io = Io,max



Vo=1.8V, Io = Io,max

Notes: $C_O=6 \times 47\mu\text{F}$ ceramic, $V_{IN} = 12\text{V}$, $I_O = I_{O,max}$

NON-ISOLATED DC/DC CONVERTERS

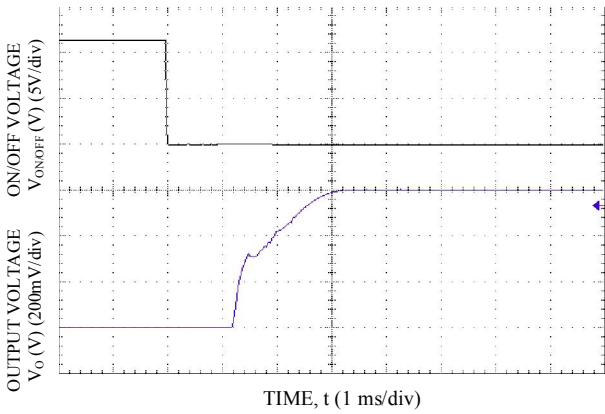
4.5 Vdc – 14.4 Vdc Input, 0.45 Vdc – 2.0 Vdc /40 A Outputs



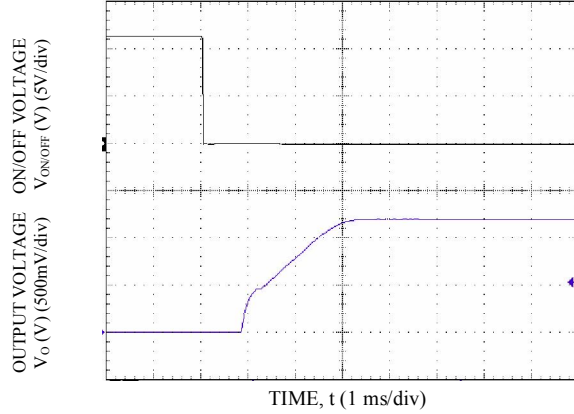
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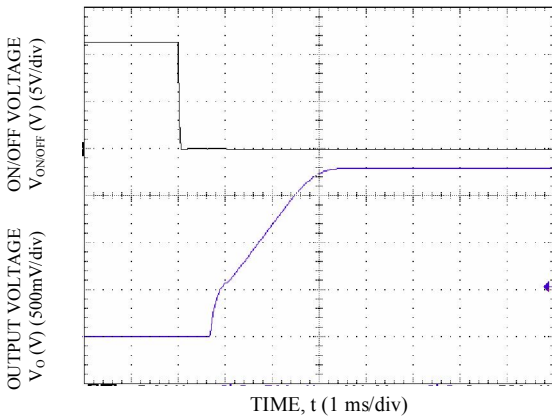
Startup Time



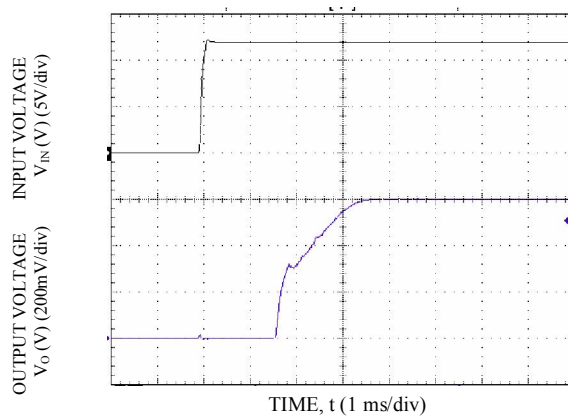
Start-up Using On/Off Voltage ($I_o = I_{o,max}$), $V_o=0.6V$



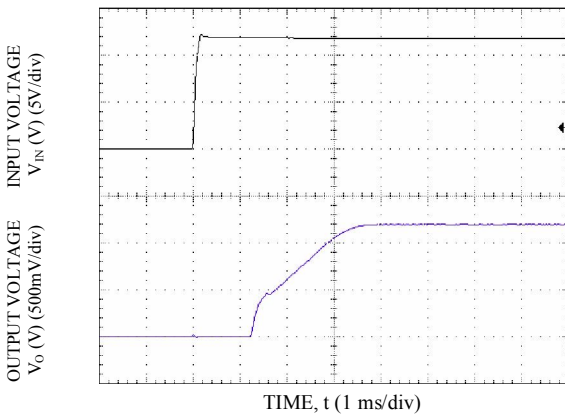
Start-up Using On/Off Voltage ($I_o = I_{o,max}$), $V_o=1.2V$



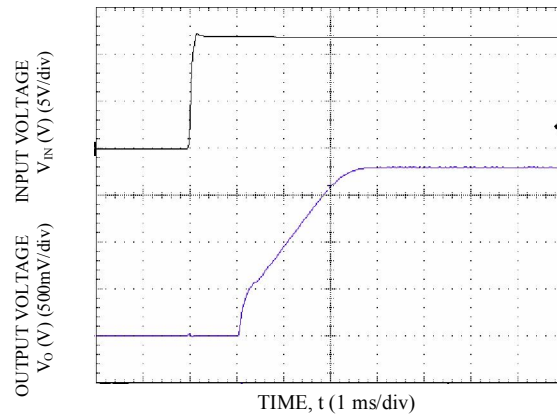
Start-up Using On/Off Voltage ($I_o = I_{o,max}$), $V_o=1.8V$



Start-up Using Input Voltage ($V_{IN} = 12V$, $I_o = I_{o,max}$), $V_o=0.60V$



Start-up Using Input Voltage ($V_{IN} = 12V$, $I_o = I_{o,max}$), $V_o=1.2V$



Start-up Using Input Voltage ($V_{IN} = 12V$, $I_o = I_{o,max}$), $V_o=1.8V$

NON-ISOLATED DC/DC CONVERTERS

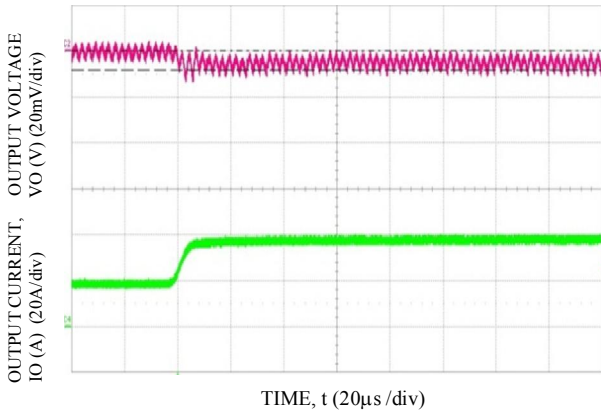
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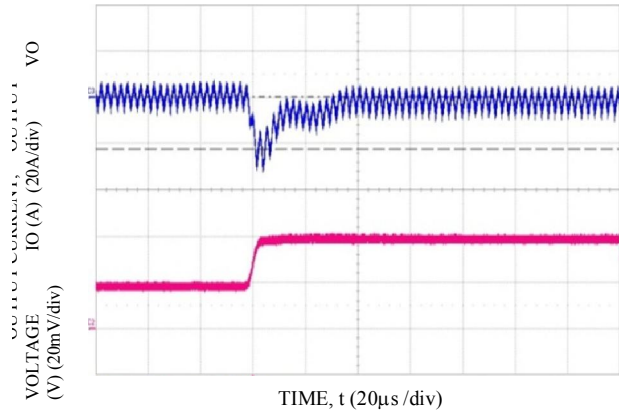
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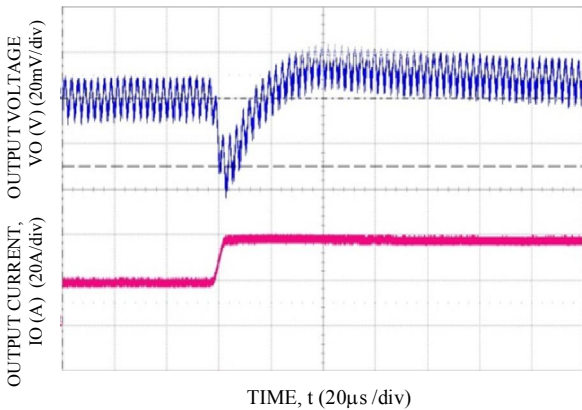
Transient waveforms



Transient Response to Dynamic Load Change from 50% to 100% at 12Vin, Cout= 12x680uF+6x47uF, CTune=47nF, RTune=180 ohms, Vo=0.6V



Transient Response to Dynamic Load Change from 50% to 100% at 12Vin, Cout= 6x330uF, CTune=12nF & RTune=200 ohms, Vo=1.2V



Transient Response to Dynamic Load Change from 50% to 100% at 12Vin, Cout= 6x330uF, CTune=5.6nF & RTune=220 ohms, Vo=1.8V

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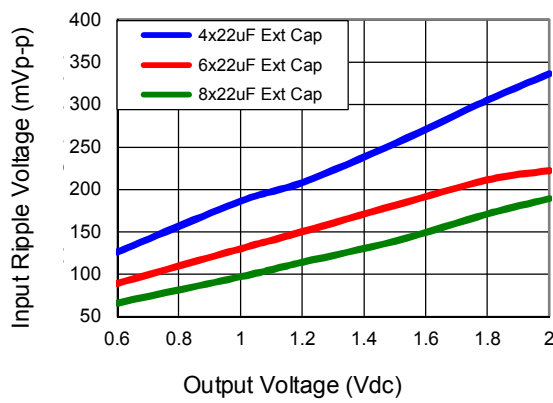
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Design Considerations Input Filtering

The SLDN-40E1Ax module should be connected to a low ac-impedance source. A highly inductive source can affect the stability of the module. An input capacitance must be placed directly adjacent to the input pin of the module, to minimize input ripple voltage and ensure module stability.

To minimize input voltage ripple, ceramic capacitors are recommended at the input of the module. Figure 19 shows the input ripple voltage for various output voltages at 40A of load current with 4x22 μ F, 6x22 μ F or 8x22 μ F ceramic capacitors and an input of 12V.

Figure 19



Note: Input ripple voltage for various output voltages with various external ceramic capacitors at the input (40A load). Input voltage is 12V. Scope Bandwidth limited to 20MHz.

Output Filtering

These modules are designed for low output ripple voltage and will meet the maximum output ripple specification with 0.1 μ F ceramic and 47 μ F ceramic capacitors at the output of the module. However, additional output filtering may be required by the system designer for a number of reasons. First, there may be a need to further reduce the output ripple and noise of the module. Second, the dynamic response characteristics may need to be customized to a particular load step change.

To reduce the output ripple and improve the dynamic response to a step load change, additional capacitance at the output can be used. Low ESR polymer and ceramic capacitors are recommended to improve the dynamic response of the module. Figure 20 provides output ripple information for different external capacitance values at various V_o and a full load current of 40A. For stable operation of the module, limit the capacitance to less than the maximum output capacitance as specified in the electrical specification table. Optimal performance of the module can be achieved by using the Tunable Loop™ feature described later in this data sheet.

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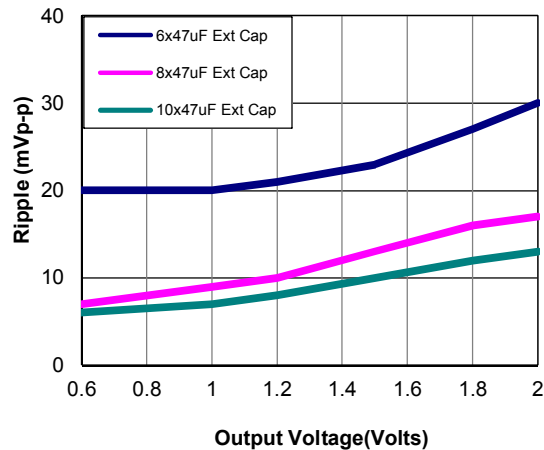


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Output Filtering (continued)

Figure 20



Note: Output ripple voltage for various output voltages with external 6x47 μ F, 8x47 μ F or 10x47 μ F ceramic capacitors at the output (40A load). Input voltage is 12V. Scope Bandwidth limited to 20MHz.

Safety Considerations

For safety agency approval the power module must be installed in compliance with the spacing and separation requirements of the end-use safety agency standards, i.e., UL 60950-1 2nd, CSA C22.2 No. 60950-1-07, DIN EN 60950-1:2006 + A11 (VDE0805 Teil 1 + A11):2009-11; EN 60950-1:2006 + A11:2009-03.

For the converter output to be considered meeting the requirements of safety extra-low voltage (SELV), the input must meet SELV requirements. The power module has extra-low voltage (ELV) outputs when all inputs are ELV.

The input to these units is to be provided with a fast acting fuse with a maximum rating of 30A, 100V (for example, Bel Fuse SMM series) in the positive input lead.

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Analog Feature Descriptions

Remote On/Off

Parameter		Min	Typ	Max	Unit	Notes
Signal Low (Unit On)	Active Low	-0.2	-	0.4	V	The remote on/off pin open, Unit on.
Signal High (Unit Off)		2.0	-	$V_{in,max}$	V	
Signal Low (Unit Off)	Active High	-0.3	-	0.4	V	The remote on/off pin open, Unit on.
Signal High (Unit On)		3.5	-	$V_{in,max}$	V	

The SLDN-40E1Ax module can be turned ON and OFF either by using the ON/OFF pin (Analog interface) or through the PMBus interface (Digital). The module can be configured in a number of ways through the PMBus interface to react to the two ON/OFF inputs:

- Module ON/OFF can be controlled only through the analog interface (digital interface ON/OFF commands are ignored)
- Module ON/OFF can be controlled only through the PMBus interface (analog interface is ignored)
- Module ON/OFF can be controlled by either the analog or digital interface.

The default state of the module (as shipped from the factory) is to be controlled by the analog interface only. If the digital interface is to be enabled, or the module is to be controlled only through the digital interface, this change must be made through the PMBus. These changes can be made and written to non-volatile memory on the module so that it is remembered for subsequent use.

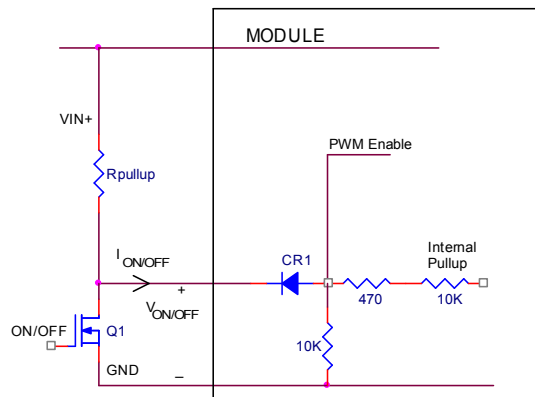
Analog On/Off

The SLDN-40E1Ax modules feature an On/Off pin for remote On/Off operation. Two On/Off logic options are available. In the Positive Logic On/Off option, (device code suffix "0" – see Ordering Information), the module turns ON during a logic High on the On/Off pin and turns OFF during a logic Low. With the Negative Logic On/Off option, (device code suffix "L" – see Ordering Information), the module turns OFF during logic High and ON during logic Low. The On/Off signal should be always referenced to ground. For either On/Off logic option, leaving the On/Off pin disconnected will turn the module ON when input voltage is present.

For positive logic modules, the circuit configuration for using the On/Off pin is shown in Figure 21.

For negative logic On/Off modules, the circuit configuration is shown in Figure 22.

Figure 21



Circuit configuration for using positive On/Off logic.

NON-ISOLATED DC/DC CONVERTERS

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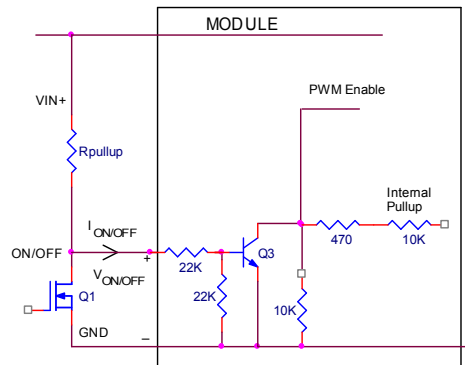


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Analog On/Off (continued)

Figure 22



Circuit configuration for using negative On/Off logic.

Digital On/Off

Please see the Digital Feature Descriptions section.

Monotonic Start-up and Shutdown

The SLDN-40E1Ax module has monotonic start-up and shutdown behavior for any combination of rated input voltage, output current and operating temperature range.

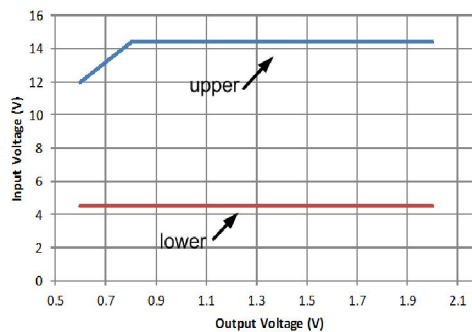
Startup into Pre-biased Output

The SLDN-40E1Ax module can start into a prebiased output as long as the prebias voltage is 0.5V less than the set output voltage.

Analog Output Voltage Programming

The output voltage of the module is programmable to any voltage from 0.6Vdc to 2.0Vdc by connecting a resistor between the Trim and SIG_GND pins of the module. Certain restrictions apply on the output voltage set point depending on the input voltage. These are shown in the Output Voltage vs. Input Voltage Set Point Area plot in Fig. 23. The Upper Limit curve shows that for output voltages lower than 1V, the input voltage must be lower than the maximum of 14.4Vdc. The Lower Limit curve shows that for output voltages higher than 0.6V, the input voltage needs to be larger than the minimum of 4.5Vdc.

Figure 23



Output Voltage vs. Input Voltage Set Point Area plot showing limits where the output voltage can be set for different input voltages.

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4.5 Vdc – 14.4 Vdc Input, 0.45 Vdc – 2.0 Vdc /40 A Outputs

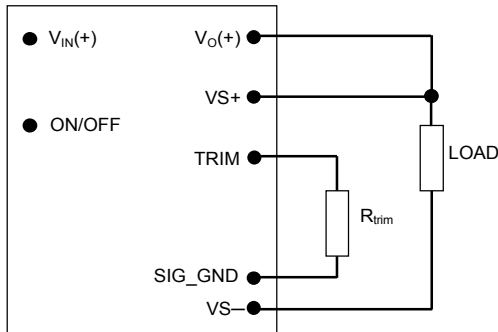


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Output Voltage Programming (continued)

Figure 24



Caution – Do not connect SIG_GND to GND elsewhere in the layout

Circuit configuration for programming output voltage using an external resistor.

Without an external resistor between Trim and SIG_GND pins, the output of the module will be 0.6Vdc. To calculate the value of the trim resistor, R_{trim} for a desired output voltage, should be as per the following equation:

$$R_{trim} = \left[\frac{12}{(V_o - 0.6)} \right] k\Omega$$

R_{trim} is the external resistor in $k\Omega$
 V_o is the desired output voltage.

Table 1 provides R_{trim} values required for some common output voltages.

Table1

$V_{O, set} (V)$	$R_{trim} (K\Omega)$
0.6	Open
0.9	40
1.0	30
1.2	20
1.5	13.33
1.8	10

Digital Output Voltage Adjustment

Please see the Digital Feature Descriptions section.

Remote Sense

The SLDN-40E1Ax power module has a Remote Sense feature to minimize the effects of distribution losses by regulating the voltage between the sense pins (VS+ and VS-). The voltage drop between the sense pins and the VOUT and GND pins of the module should not exceed 0.5V.

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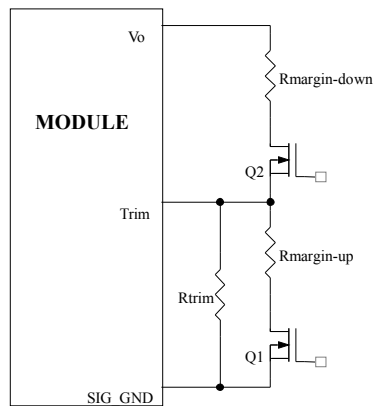
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Analog Voltage Margining

Output voltage margining can be implemented in the module by connecting a resistor, $R_{\text{margin-up}}$, from the Trim pin to the ground pin for margining-up the output voltage and by connecting a resistor, $R_{\text{margin-down}}$, from the Trim pin to output pin for margining-down. Figure 25 shows the circuit configuration for output voltage margining. Please consult your local Bel representative for additional details.

Figure 25



Circuit Configuration for margining Output voltage

Digital Output Voltage Margining

Please see the Digital Feature Descriptions section.

Output Voltage Sequencing

The SLDN-40E1Ax module includes a sequencing feature, EZ-SEQUENCE that enables users to implement various types of output voltage sequencing in their applications. This is accomplished via an additional sequencing pin. When not using the sequencing feature, leave it unconnected.

The voltage applied to the SEQ pin should be scaled down by the same ratio as used to scale the output voltage down to the reference voltage of the module. This is accomplished by an external resistive divider connected across the sequencing voltage before it is fed to the SEQ pin as shown in Fig. 26. In addition, a small capacitor (suggested value 100pF) should be connected across the lower resistor R1.

For SLDN-40E1Ax modules, the minimum recommended delay between the ON/OFF signal and the sequencing signal is 10ms to ensure that the module output is ramped up according to the sequencing signal. This ensures that the module soft-start routine is completed before the sequencing signal is allowed to ramp up.

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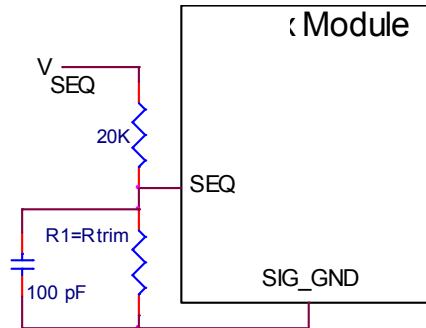


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Output Voltage Sequencing (continued)

Figure 26



Circuit showing connection of the sequencing signal to the SEQ pin

When the scaled down sequencing voltage is applied to the SEQ pin, the output voltage tracks this voltage until the output reaches the set-point voltage. The final value of the sequencing voltage must be set higher than the set-point voltage of the module. The output voltage follows the sequencing voltage on a one-to-one basis. By connecting multiple modules together, multiple modules can track their output voltages to the voltage applied on the SEQ pin.

The module's output can track the SEQ pin signal with slopes of up to 0.5V/msec during power-up or power-down.

To initiate simultaneous shutdown of the modules, the SEQ pin voltage is lowered in a controlled manner. The output voltage of the modules tracks the voltages below their set-point voltages on a one-to-one basis. A valid input voltage must be maintained until the tracking and output voltages reach ground potential.

Note that in all digital Bel series of modules, the PMBus Output Undervoltage Fault will be tripped when sequencing is employed. This will be detected using the STATUS_WORD and STATUS_VOUT PMBus commands. In addition, the SMBALERT signal will be asserted low as occurs for all faults and warnings. To avoid the module shutting down due to the Output Undervoltage Fault, the module must be set to continue operation without interruption as the response to this fault (see the description of the PMBus command VOUT_UV_FAULT_RESPONSE for additional information).

Overcurrent Protection

To provide protection in a fault (output overload) condition, the unit is equipped with internal current-limiting circuitry and can endure current limiting continuously. At the point of current-limit inception, the unit enters hiccup mode. The unit operates normally once the output current is brought back into its specified range.

Load Transient Considerations

The SLDN-40E1Ax module can achieve 100% load transient above 0 °C ambient temperature, the load transient is limited to a maximum of 62.5% of specified full load current.

Digital Adjustable Overcurrent Warning

Please see the Digital Feature Descriptions section.

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Overtemperature Protection

To provide protection in a fault condition, the unit is equipped with a thermal shutdown circuit. The unit will shut down if the overtemperature threshold of 145 °C (typ) is exceeded at the thermal reference point T_{ref} . Once the unit goes into thermal shutdown it will then wait to cool before attempting to restart.

Digital Temperature Status via PMBus

Please see the Digital Feature Descriptions section.

Digitally Adjustable Output Over and Under Voltage Protection

Please see the Digital Feature Descriptions section.

Input Undervoltage Lockout

At input voltages below the input undervoltage lockout limit, the module operation is disabled. The module will begin to operate at an input voltage above the undervoltage lockout turn-on threshold.

Digitally Adjustable Input Undervoltage Lockout

Please see the Digital Feature Descriptions section.

Digitally Adjustable Power Good Thresholds

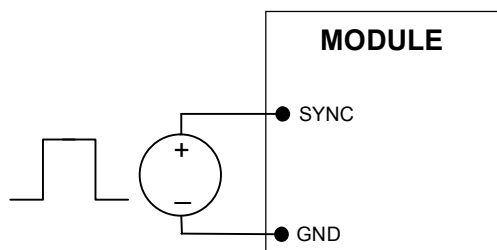
Please see the Digital Feature Descriptions section.

Synchronization

The SLDN-40E1Ax module switching frequency can be synchronized to a signal with an external frequency within a specified range. Synchronization can be done by using the external signal applied to the SYNC pin of the module as shown in Fig. 27, with the converter being synchronized by the rising edge of the external signal. The Electrical Specifications table specifies the requirements of the external SYNC signal. If the SYNC pin is not used, the module should free run at the default switching frequency.

If synchronization is not being used, connect the SYNC pin to GND.

Figure 27



External source connections to synchronize switching frequency of the module.

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Paralleling with Active Load Sharing

For additional power requirements, the Bel power module is also equipped with paralleling capability. Up to five modules can be configured in parallel, with active load sharing.

To implement paralleling, the following conditions must be satisfied.

- All modules connected in parallel must be frequency synchronized where they are switching at the same frequency. This is done by using the SYNC function of the module and connecting to an external frequency source. Modules can be interleaved to reduce input ripple/filtering requirements.
- The share pins of all units in parallel must be connected together. The path of these connections should be as direct as possible.
- The remote sense connections to all modules should be made that to same points for the output, i.e. all VS+ and VS- terminals for all modules are connected to the power bus at the same points.
- For converters operating in parallel, tunable loop components “RTUNE” and “CTUNE” must be selected to meet the required transient specification. For providing better noise immunity, we recommend that RTUNE value to be greater than 300Ω.

Some special considerations apply for design of converters in parallel operation:

- When sizing the number of modules required for parallel operation, take note of the fact that current sharing has some tolerance. In addition, under transient conditions such as a dynamic load change and during startup, all converter output currents will not be equal. To allow for such variation and avoid the likelihood of a converter shutting off due to a current overload, the total capacity of the paralleled system should be no more than 90% of the sum of the individual converters. As an example, for a system of three converters in parallel, the total current drawn should be less than 90% of (3 x 40A), i.e. less than 108 A.
- All modules should be turned ON and OFF together. This is so that all modules come up at the same time avoiding the problem of one converter sourcing current into the other leading to an overcurrent trip condition. To ensure that all modules come up simultaneously, the on/off pins of all paralleled converters should be tied together and the converters enabled and disabled using the on/off pin. Note that this means that converters in parallel cannot be digitally turned ON as that does not ensure that all modules being paralleled turn on at the same time.
- If digital trimming is used to adjust the overall output voltage, the adjustments need to be made in a series of small steps to avoid shutting down the output. Each step should be no more than 20mV for each module. For example, to adjust the overall output voltage in a setup with two modules (A and B) in parallel from 1V to 1.1V, module A would be adjusted from 1.0 to 1.02V followed by module B from 1.0 to 1.02V, then each module in sequence from 1.02 to 1.04V and so on until the final output voltage of 1.1V is reached.
- If the Sequencing function is being used to start-up and shut down modules and the module is being held to 0V by the tracking signal then there may be small deviations on the module output. This is due to controller duty cycle limitations encountered in trying to hold the voltage down near 0V.
- The share bus is not designed for redundant operation and the system will be non-functional upon failure of one of the units when multiple units are in parallel. In particular, if one of the converters shuts down during operation, the other converters may also shut down due to their outputs hitting current limit. In such a situation, unless a coordinated restart is ensured, the system may never properly restart since different converters will try to restart at different times causing an overload condition and subsequent shutdown. This situation can be avoided by having an external output voltage monitor circuit that detects a shutdown condition and forces all converters to shut down and restart together.

When not using the active load share feature, share pins should be left unconnected.

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Measuring Output Current, Output Voltage and Input Voltage

Please see the Digital Feature Descriptions section.

Dual Layout

Identical dimensions and pin layout of Analog and Digital modules permit migration from one to the other without needing to change the layout. In both cases the trim resistor is connected between trim and signal ground.

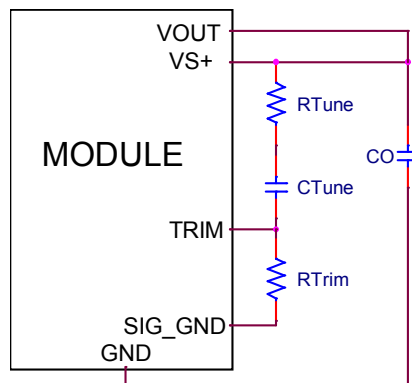
Tunable Loop™

The SLDN-40E1Ax module has a feature that optimizes transient response of the module called Tunable Loop™.

External capacitors are usually added to the output of the module for two reasons: to reduce output ripple and noise (see Figure 20) and to reduce output voltage deviations from the steady-state value in the presence of dynamic load current changes. Adding external capacitance however affects the voltage control loop of the module, typically causing the loop to slow down with sluggish response. Larger values of external capacitance could also cause the module to become unstable.

The Tunable Loop™ allows the user to externally adjust the voltage control loop to match the filter network connected to the output of the module. The Tunable Loop™ is implemented by connecting a series R-C between the VS+ and TRIM pins of the module, as shown in Fig. 28. This R-C allows the user to externally adjust the voltage loop feedback compensation of the module.

Figure 28



Circuit diagram showing connection of R_{TUNE} and C_{TUNE} to tune the control loop of the module.

Recommended values of R_{TUNE} and C_{TUNE} for different output capacitor combinations are given in Table 2. Table 2 shows the recommended values of R_{TUNE} and C_{TUNE} for different values of ceramic output capacitors up to 1000uF that might be needed for an application to meet output ripple and noise requirements. Selecting R_{TUNE} and C_{TUNE} according to Table 2 will ensure stable operation of the module.

In applications with tight output voltage limits in the presence of dynamic current loading, additional output capacitance will be required. Table 3 lists recommended values of R_{TUNE} and C_{TUNE} in order to meet 2% output voltage deviation limits for some common output voltages in the presence of a 20A to 40A step change (50% of full load), with an input voltage of 12V.

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Tunable Loop™ (continued)

Please contact your Bel representative to obtain more details of this feature as well as for guidelines on how to select the right value of external R-C to tune the module for best transient performance and stable operation for other output capacitance values.

Table 2

Co	6x47 μ F	8x47 μ F	10x47 μ F	12x47 μ F	20x47 μ F
R _{TUNE}	330 Ω	330 Ω	330 Ω	330 Ω	200 Ω
C _{TUNE}	330pF	820pF	1200pF	1500pF	3300pF

General recommended values of R_{TUNE} and C_{TUNE} for Vin=12V and various external ceramic capacitor combination.

Table 3

Vo	1.8V	1.2V	0.6V
Co	4x47uF + 6x330 μ F polymer	4x47uF + 11x330 μ F polymer	4x47uF + 12x680 μ F polymer
R _{TUNE}	220 Ω	200 Ω	180 Ω
C _{TUNE}	5600pF	12nF	47nF
Δ V	34mV	22mV	12mV

Recommended values of R_{TUNE} and C_{TUNE} to obtain transient deviation of 2% of Vout for a 20A step load with Vin=12V..

Note: The capacitors used in the Tunable Loop tables are 47 μ F/3 m Ω ESR ceramic, 330 μ F/12 m Ω ESR polymer capacitor and 680 μ F/12 m Ω polymer capacitor.

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Digital Feature Descriptions

PMBus Interface Capability

The SLDN-40E1Ax modules have a PMBus interface that supports both communication and control. The PMBus Power Management Protocol Specification can be obtained from www.pmbus.org. The modules support a subset of version 1.1 of the specification (see Table 6 for a list of the specific commands supported). Most module parameters can be programmed using PMBus and stored as defaults for later use.

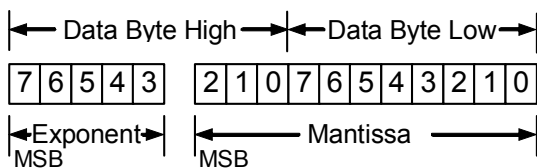
All communication over the module PMBus interface must support the Packet Error Checking (PEC) scheme. The PMBus master must generate the correct PEC byte for all transactions, and check the PEC byte returned by the module.

The module also supports the SMBALERT# response protocol whereby the module can alert the bus master if it wants to talk. For more information on the SMBus alert response protocol, see the System Management Bus (SMBus) specification.

The module has non-volatile memory that is used to store configuration settings. Not all settings programmed into the device are automatically saved into this non-volatile memory, only those specifically identified as capable of being stored can be saved (see Table 6 for which command parameters can be saved to non-volatile storage).

PMBus Data Format

For commands that set thresholds, voltages or report such quantities, the module supports the “Linear” data format among the three data formats supported by PMBus. The Linear Data Format is a two byte value with an 11-bit, two’s complement mantissa and a 5-bit, two’s complement exponent. The format of the two data bytes is shown below:



The value of the number is then given by
$$\text{Value} = \text{Mantissa} \times 2^{\text{Exponent}}$$

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PMBus Addressing

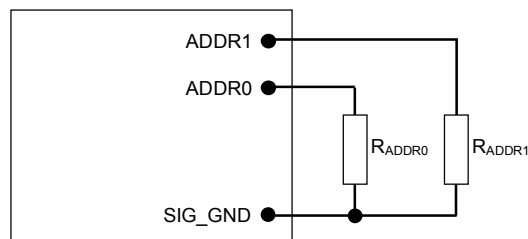
The SLDN-40E1Ax module can be addressed through the PMBus using a device address. The module has 64 possible addresses (0 to 63 in decimal) which can be set using resistors connected from the ADDR0 and ADDR1 pins to SIG_GND. Note that some of these addresses (0, 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 40, 44, 45, 55 in decimal) are reserved according to the SMBus specifications and may not be useable. The address is set in the form of two octal (0 to 7) digits, with each pin setting one digit. The ADDR1 pin sets the high order digit and ADDR0 sets the low order digit. The resistor values suggested for each digit are shown in Table 4 (1% tolerance resistors are recommended). Note that if either address resistor value is outside the range specified in Table 4, the module will respond to address 127.

Table 4

Digit	Resistor Value (K Ω)
0	10
1	15.4
2	23.7
3	36.5
4	54.9
5	84.5
6	130
7	200

The user must know which I2C addresses are reserved in a system for special functions and set the address of the module to avoid interfering with other system operations. Both 100kHz and 400kHz bus speeds are supported by the module. Connection for the PMBus interface should follow the High Power DC specifications given in section 3.1.3 in the SMBus specification V2.0 for the 400kHz bus speed or the Low Power DC specifications in section 3.1.2. The complete SMBus specification is available from the SMBus web site, smbus.org.

Figure 29



Circuit showing connection of resistors used to set the PMBus address of the module.

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PMBus Enabled On/Off

The module can also be turned on and off via the PMBus interface. The OPERATION command is used to actually turn the module on and off via the PMBus, while the ON_OFF_CONFIG command configures the combination of analog ON/OFF pin input and PMBus commands needed to turn the module on and off. Bit [7] in the OPERATION command data byte enables the module, with the following functions:

- 0 : Output is disabled
- 1 : Output is enabled

This module uses the lower five bits of the ON_OFF_CONFIG data byte to set various ON/OFF options as follows:

Bit Position	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r
Function	PU	CMD	CPR	POL	CPA
Default Value	1	0	1	1	1

PU: Sets the default to either operate any time input power is present or for the ON/OFF to be controlled by the analog ON/OFF input and the PMBus OPERATION command. This bit is used together with the CP, CMD and ON bits to determine startup.

Bit Value	Action
0	Module powers up any time power is present regardless of state of the analog ON/OFF pin
1	Module does not power up until commanded by the analog ON/OFF pin and the OPERATION command as programmed in bits [2:0] of the ON_OFF_CONFIG register.

CMD: The CMD bit controls how the device responds to the OPERATION command.

Bit Value	Action
0	Module ignores the ON bit in the OPERATION command
1	Module responds to the ON bit in the OPERATION command

CPR: Sets the response of the analog ON/OFF pin. This bit is used together with the CMD, PU and ON bits to determine startup.

Bit Value	Action
0	Module ignores the analog ON/OFF pin, i.e. ON/OFF is only controlled through the PMBUS via the OPERATION command
1	Module requires the analog ON/OFF pin to be asserted to start the unit

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PMBus Adjustable Soft Start Rise Time

The soft start rise time can be adjusted in the module via PMBus. When setting this parameter, make sure that the charging current for output capacitors can be delivered by the module in addition to any load current to avoid nuisance tripping of the overcurrent protection circuitry during startup. The TON_RISE command sets the rise time in ms, and allows choosing soft start times between 600µs and 9ms, with possible values listed in Table 5. Note that the exponent is fixed at -4 (decimal) and the upper two bits of the mantissa are also fixed at 0.

Table 5

Rise Time	Exponent	Mantissa
600µs	11100	00000001010
900µs	11100	00000001110
1.2ms	11100	00000010011
1.8ms	11100	00000011101
2.7ms	11100	00000101011
4.2ms	11100	00001000011
6.0ms	11100	00001100000
9.0ms	11100	00010010000

Output Voltage Adjustment Using the PMBus

The VOUT_SCALE_LOOP parameter is important for a number of PMBus commands related to output voltage trimming, margining, over/under voltage protection and the PGOOD thresholds. The output voltage of the module is set as the combination of the voltage divider formed by RTrim and a 20kΩ upper divider resistor inside the module, and the internal reference voltage of the module. The reference voltage VREF is nominally set at 600mV, and the output regulation voltage is then given by

$$V_{OUT} = \left[\frac{20000 + RTrim}{RTrim} \right] \times V_{REF}$$

Hence the module output voltage is dependent on the value of RTrim which is connected external to the module. The information on the output voltage divider ratio is conveyed to the module through the VOUT_SCALE_LOOP parameter which is calculated as follows:

$$VOUT_SCALE_LOOP = \frac{RTrim}{20000 + RTrim}$$

The VOUT_SCALE_LOOP parameter is specified using the “Linear” format and two bytes. The upper five bits [7:3] of the high byte are used to set the exponent which is fixed at -9 (decimal). The remaining three bits of the high byte [2:0] and the eight bits of the lower byte are used for the mantissa. The default value of the mantissa is 00100000000 corresponding to 256 (decimal), corresponding to a divider ratio of 0.5. The maximum value of the mantissa is 512 corresponding to a divider ratio of 1. Note that the resolution of the VOUT_SCALE_LOOP command is 0.2%.

When PMBus commands are used to trim or margin the output voltage, the value of VREF is what is changed inside the module, which in turn changes the regulated output voltage of the module.