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my-d™ move
my-d™ move NFC

SLE 66R01P
SLE 66R01PN

Intelligent 1216 bit EEPROM with
Contactless Interface compliant to
ISO/IEC 14443-3 Type A and support of
NFC Forum™ Type 2 Tag Operation

Data Book

2011-11-24

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my-d™ move / my-d™ move NFC - SLE 66R01P / SLE 66R01PN Data Book
The information in this document is subject to change without notice.

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Page	**Subjects (major changes since last revision)**
All	Editorial changes; removed “Preliminary” status; update of figures (memory organization)

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Features

Intelligent 1216 bit EEPROM with Contactless Interface compliant to ISO/IEC 14443-3 Type A and support of NFC Forum™ Type 2 Tag Operation

Contactless Interface

- Physical Interface and Anticollision compliant to ISO/IEC 14443-3 Type A
  - Operation frequency 13.56 MHz
  - Data rate 106 kbit/s in both direction
  - Contactless transmission of data and supply energy
  - Anticollision logic: several cards may be operated in the field simultaneously
- Unique IDentification number (7-byte double-size UID) according to ISO/IEC 14443-3 Type A
- Read and Write Distance up to 10 cm and more (influenced by external circuitry i.e. reader and inlay design)

152 byte EEPROM

- Organized in 38 blocks of 4 bytes each
- 128 bytes freely programmable User Memory
- 24 bytes of Service Area reserved for UID, Configuration, LOCK Bytes, OTP Block and Manufacturer Data
- Read and Write of 128 bytes of User Memory in less than 100 ms
- Programming time per block < 4 ms
- Endurance minimum 10,000 erase/write cycles[1)]
- Data Retention minimum 5 years[1)]

Privacy Features

- 32 bit of One Time Programmable (OTP) memory area
- Locking mechanism for each block
- Block Lock mechanism
- Optional 32 bit Password for Read/Write or Write access
- Optional Password Retry Counter
- Optional 16 bit Value Counter

Data Protection

- Data Integrity supported by 16 bit CRC, parity bit, command length check
- Anti-tearing mechanism for OTP, Password Retry Counter and Value Counter

NFC Forum™ Operation

- Compliant to NFC Forum™ Type 2 Tag Operation
- Support of Static and Dynamic Memory Structure according to NFC Forum™ Type 2 Tag Operation
- SLE 66R01PN: pre-configured NFC memory with empty NDEF message (INITIALIZED state, non-reversible)
- SLE 66R01P: UNINITIALIZED state, may be configured to INITIALIZED state

Electrical Characteristics

- On-Chip capacitance 17 pF ± 5%
- ESD protection minimum 2 kV
- Ambient Temperature -25°C … +70°C (for the chip)

1) Values are temperature dependent

1 Ordering and packaging information

Table 1 Ordering information

Type	Package	Total Memory / User Memory[1)]	Ordering code
SLE 66R01P C	wafer sawn / unsawn	152 / 128 bytes	on request
SLE 66R01P NB	NiAu Bumped (sawn wafer)		SP000911428
SLE 66R01PN C	wafer sawn / unsawn		on request
SLE 66R01PN NB	NiAu Bumped (sawn wafer)		SP000953914

1) Total memory size includes the service area whereas user memory size is freely programmable for user data.

For more ordering information about the form of delivery please contact your local Infineon sales office.

1.1 Pin description

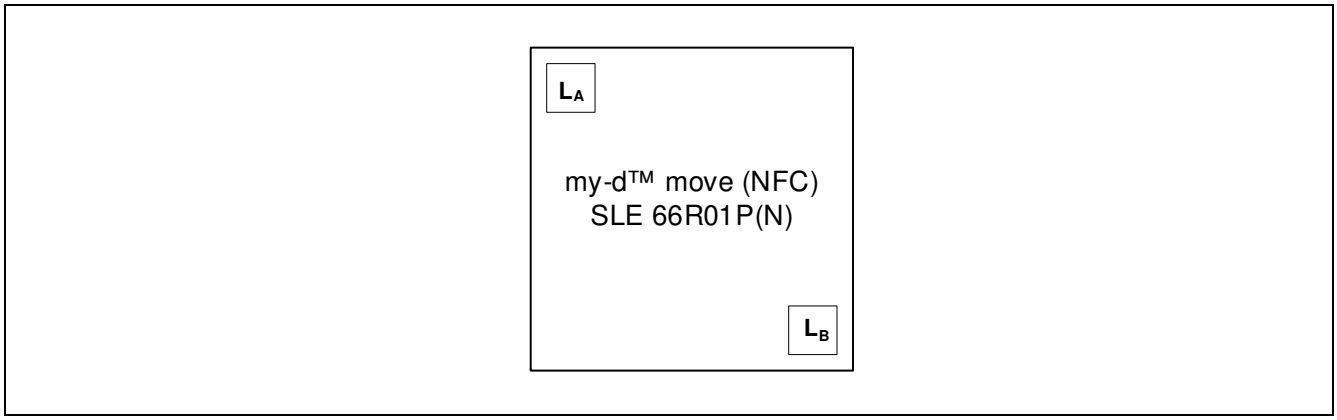

Figure 1 Pin configuration die

Table 2 Pin description and function

Symbol	Function
L_A	Antenna Connection
L_B	Antenna Connection

2 my-d™ Product Family

my-d™ products are available both in plain mode with open memory access and in secure mode with memory access controlled by authentication procedures. The my-d™ product family provides users with different memory sizes, features NFC Forum™ Type 2 Tag functionality and incorporates security features to enable considerable flexibility in the application design.

Flexible controls within the my-d™ devices start with plain mode operation featuring individual page locking; for more complex applications various settings in secure mode can be set for multi user / multi application configurations.

In plain mode access to the memory is supported by both 4-byte block as well as 8-byte page structure.

In secure mode a cryptographic algorithm based on a 64-bit key is available. Mutual authentication, message authentication codes (MAC) and customized access conditions protect the memory against unauthorized access.

The functional architecture, meaning the memory organization and authentication of my-d™ products is the same for both my-d™ proximity (ISO/IEC 14443) and my-d™ vicinity (ISO/IEC 18000-3 mode 1 or ISO/IEC 15693). This eases the system design and allows simple adaptation between applications.

Configurable Value Counters featuring anti-tearing functionality are suitable for value token applications, such as limited use transportation tickets.

Architectural interoperability of my-d™ products enables an easy migration from simple to more demanding applications.

The my-d™ move family is designed for cost optimized applications and its implemented command set eases the usage in existing applications and infrastructures.

In addition, the my-d™ light (ISO/IEC 18000-3 mode 1 or ISO/IEC 15693) is part of the my-d™ family. Its optimized command set and memory expands the range of applications to cost sensitive segments.

2.1 my-d™ move and my-d™ move NFC

The my-d™ move and my-d™ move NFC are part of Infineon's my-d™ product family and are designed to meet the requirements of the increasing NFC market demanding smart memories. They are compliant to ISO/IEC 14443-3 Type A, to ISO/IEC 18092 and to NFC Forum™ Type 2 Tag Operation.

128 Bytes of memory can be arranged in static or dynamic memory structures for NFC applications.

my-d™ move and my-d™ move NFC products also feature configurable Value Counters which support anti-tearing protection.

Privacy features like a password protection including password retry counter provide basic security to the applications.

Based on SLE 66R01P the SLE 66R01PN already contains a pre-configuration of the NFC memory indicating the INITIALIZED state according to the definition of the NFC Forum™ Type 2 Tag life cycle. Due to that the my-d™ move NFC is ready to be used in NFC infrastructures.

my-d™ move and my-d™ move NFC products are suited for a broad range of applications like public transport, event ticketing or smart posters.

2.2 Application Segments

my-d™ products are optimized for personal and object identification. Please find in the following table some dedicated examples

Table 3 my-d™ family product overview

Product	Application
my-d™ move - SLE 66R01P	Public Transport, Smart Posters, NFC Device Pairing
my-d™ move NFC - SLE 66R01PN	Public Transport, Smart Posters, NFC Device Pairing, NFC INITIALIZED state
my-d™ move lean - SLE 66R01L	Public Transport, Smart Posters, NFC Device Pairing
my-d™ NFC - SLE 66RxxP	Smart Posters and Maps, NFC Device Pairing, Loyalty Schemes, Consumer Good Information, Healthcare Monitoring
my-d™ proximity 2 - SLE 66RxxS	Access Control, Entertainment, Public Transport, Customer Loyalty Schemes, Micro Payment
my-d™ proximity enhanced - SLE 55RxxE	Access Control, Gaming, Entertainment, Customer Loyalty Schemes
my-d™ light - SRF 55V01P	Libraries, Laundry, Factory Automation, Media Management, Event Ticketing, Leisure Park Access
my-d™ vicinity plain - SRF 55VxxP	Factory Automation, Healthcare, Ticketing, Access Control
my-d™ vicinity plain HC - SRF 55VxxP HC	Ticketing, Brand Protection, Loyalty Schemes, Ski passes
my-d™ vicinity secure - SRF 55VxxS	Ticketing, Brand protection, Loyalty Schemes, Access Control

3 Scope of my-d™ move / my-d™ move NFC

The SLE 66R01P and SLE 66R01PN are part of the Infineon my-d™ product family and support Infineon's transport and ticketing strategy and are designed to meet the requirements of NFC applications.

They are compliant to ISO/IEC 14443-3 Type A, to ISO/IEC 18092 and to NFC Forum™ Type 2 Tag Operation.

3.1 Circuit Description

The SLE 66R01P and SLE 66R01PN are made up of an EEPROM memory unit, an analog interface for contactless operation, a data transmission path and a control unit. The following diagram shows the main blocks of the SLE 66R01P and SLE 66R01PN.

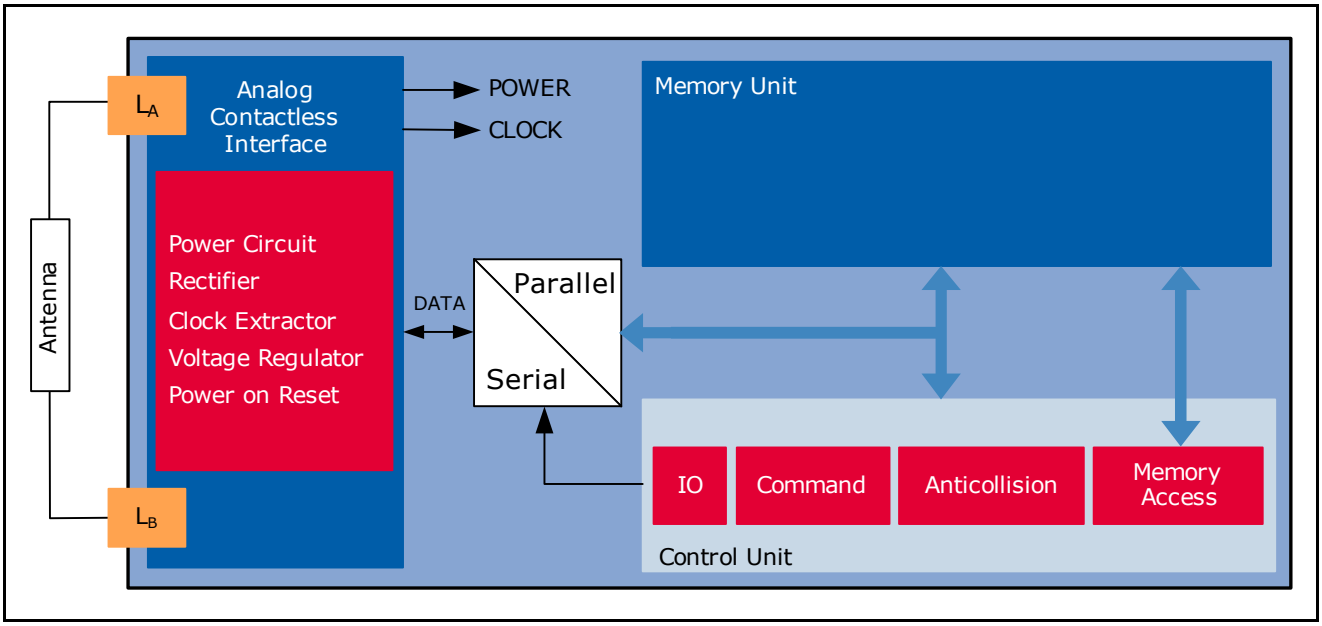

Figure 2 Block Diagram of the SLE 66R01P and SLE 66R01PN

The SLE 66R01P and SLE 66R01PN comprise the following three parts:

- **Analog Contactless Interface**
  - The Analog Contactless Interface contains the voltage rectifier, voltage regulator and system clock to supply the IC with appropriate power. Additionally the data stream is modulated and demodulated.
- **Memory Unit**
  - The Memory Unit consists of 38 blocks of 4 bytes each.
- **Control Unit**
  - The Control Unit decodes and executes all commands. Additionally the control unit is responsible for the correct anticollision flow.

3.2 Memory Principle

The total amount of addressable memory is 152 bytes organized in blocks of 4 bytes each.

The general structure comprises Service Areas as well as User Areas:

- 24 bytes of service and administration data (located in Service Area 1 and 2) reserved for
  - 7-byte double-size UID
  - configuration data
  - LOCKx bytes
  - OTP memory
  - Manufacturing Data
- 128 bytes of User memory (located in User Area 1 and 2) reserved for
  - User Data
  - Value Counter

Additionally the Password and Password Retry Counter are available and accessible via dedicated commands.

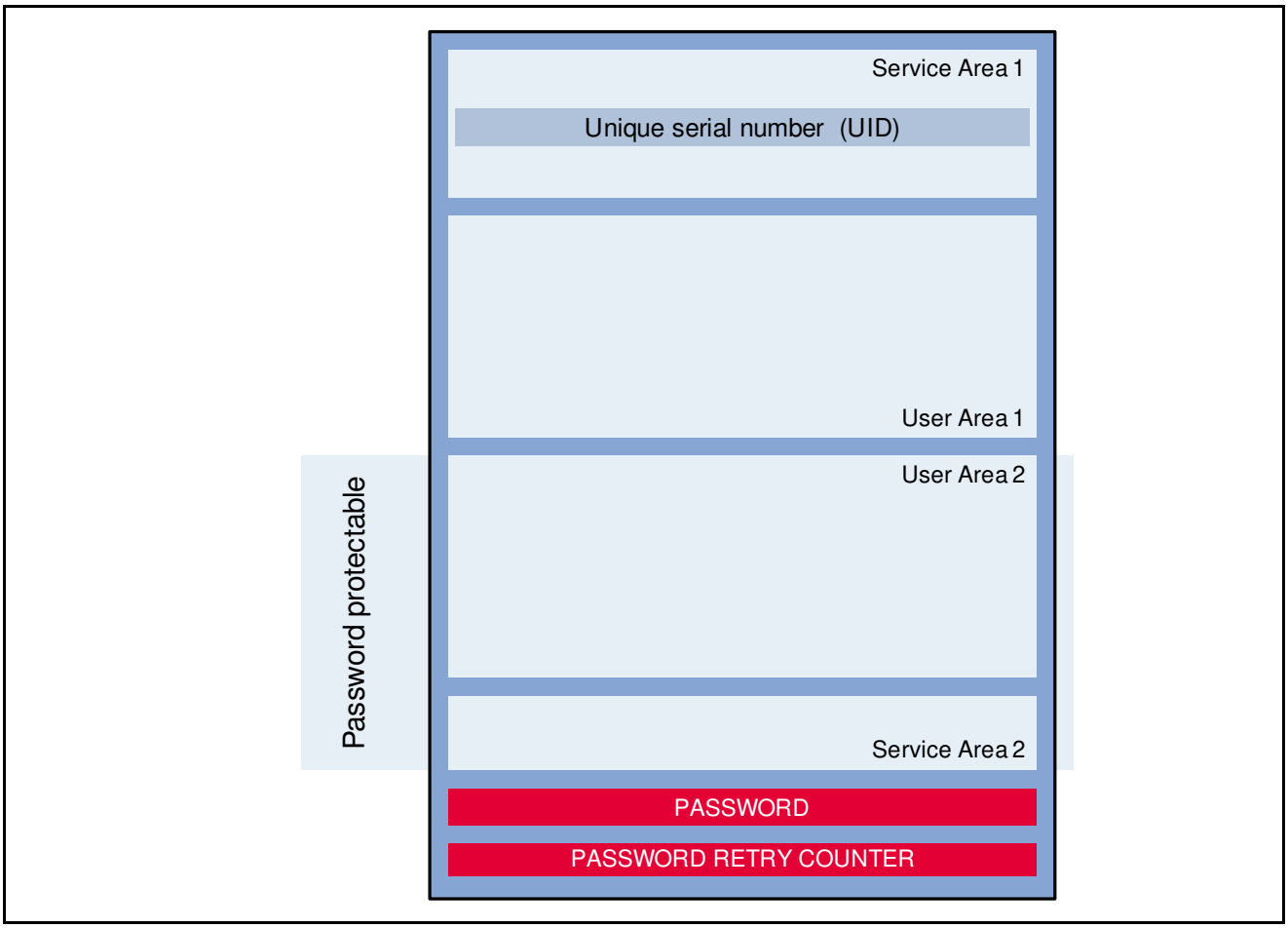

Figure 3 SLE 66R01P and SLE 66R01PN memory principle

3.2.1 Service Area 1

Service Area 1 contains

- the 7-byte UID which is programmed at manufacturing of the chip and cannot be changed
- CONFIG byte to enable the Password (incl. the Password Retry counter) and the Value Counter functionality
- LOCK0, LOCK1 bytes to enable an irreversible write-protection for the blocks located in User Area 1
- 32 bits of the One-Time-Programmable (OTP) memory block can irreversibly be programmed from 0_B to 1_B

3.2.2 User Area 1

48 bytes (12 blocks, 4 bytes each) of memory for user data.

3.2.3 User Area 2

User Area 2 contains

- 80 bytes (20 blocks, 4 bytes each) of user memory for user data. These memory blocks can be used to store user data. This portion of the memory may be protected with a 32 bit password.
- a 16-bit Value Counter may be activated providing a mechanism to store some value (points, trips, ...) on the my-d™ move and my-d™ move NFC chip.

3.2.4 Service Area 2

Service Area 2 contains

- lock bytes LOCK2 to LOCK5 to enable an irreversible write-protection for the blocks loacted in User Area 2
- Manufacturing Data (programmed during manufacturing of the chip) which cannot be changed

3.3 Memory Principle for NFC Forum™ Type 2 Tag

The memory organization is configurable according to the NFC Forum™ Type 2 Tag Operation specification. Static or dynamic memory structures are supported.

Figure 4 illustrates the principle of the SLE 66R01P and SLE 66R01PN as a NFC Forum™ Type 2 Tag compatible chip. The memory can be accessed with NFC Forum™ Type 2 Tag commands.

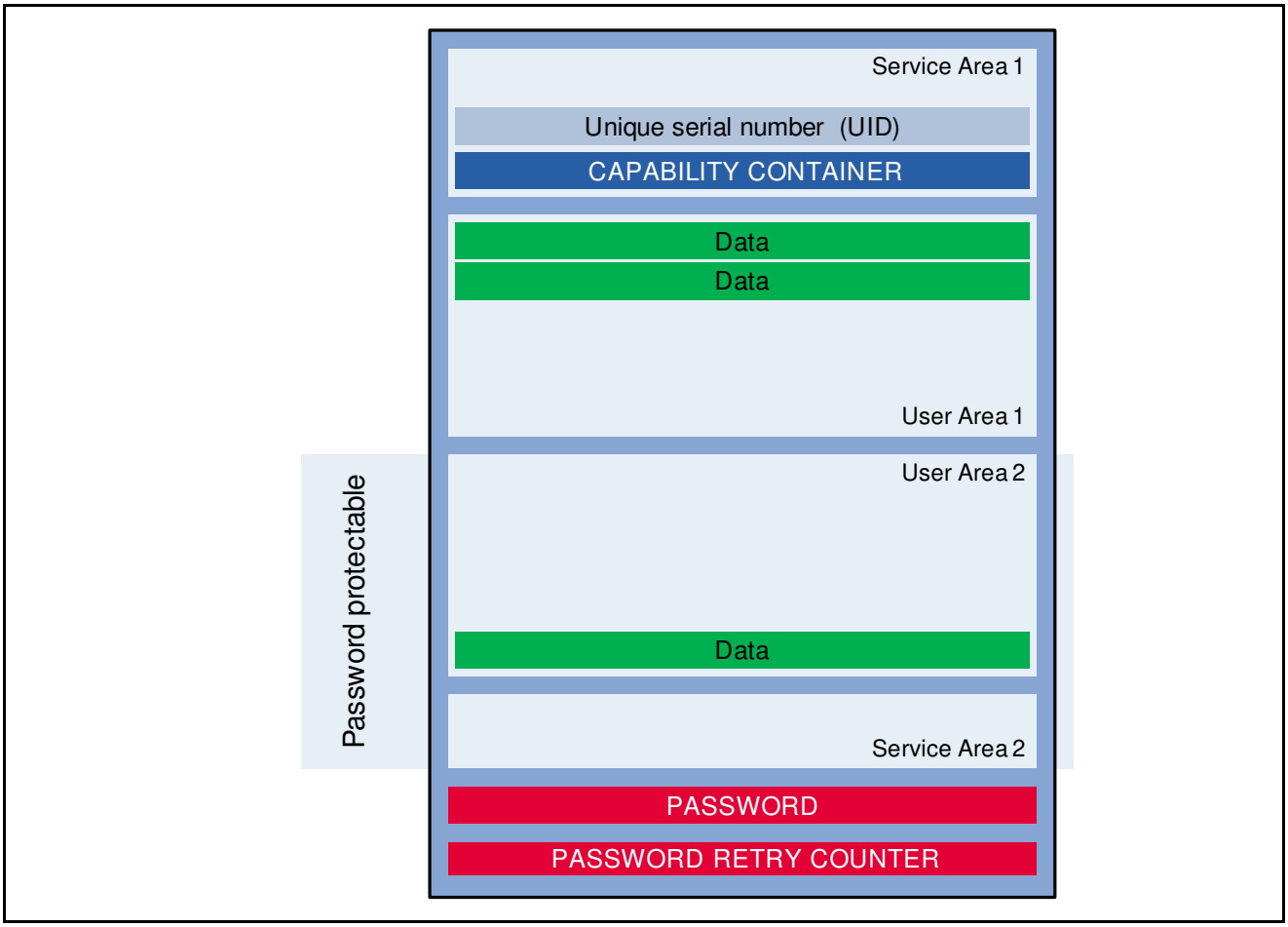

Figure 4 SLE 66R01P and SLE 66R01PN NFC Forum™ Type 2 Tag memory structure

Based on SLE 66R01P the SLE 66R01PN already contains a pre-configuration of the NFC memory indicating the INITIALIZED state according to the definition of the NFC Forum™ Type 2 Tag life cycle. With this pre-configuration the my-d™ move NFC can be immediately used in NFC infrastructures.

For details regarding the NFC initialization of my-d™ move and my-d™ move NFC please refer the the Application Note “How to operate my-d™ move and my-d™ move NFC devices in NFC Forum™ Type 2 Tag infrastructures” available at Chip Card & Security security.chipcard.ics@infineon.com.

Attention: The pre-configuration of SLE 66R01PN is nonreversible and the my-d™ move NFC cannot be overwritten and used as plain, standard my-d™ move anymore.

3.4 System Overview

The system consists of a host system, one or more SLE 66R01P / SLE 66R01PN tags or other ISO/IEC 14443-3 Type A compliant cards and an ISO/IEC 14443-3 Type A compatible contactless reader.

Alternatively, since the SLE 66R01P and SLE 66R01PN can be used in NFC Forum™ Type 2 Tag memory structures, a NFC Forum™ device in card reader/writer mode can be used to operate the chip.

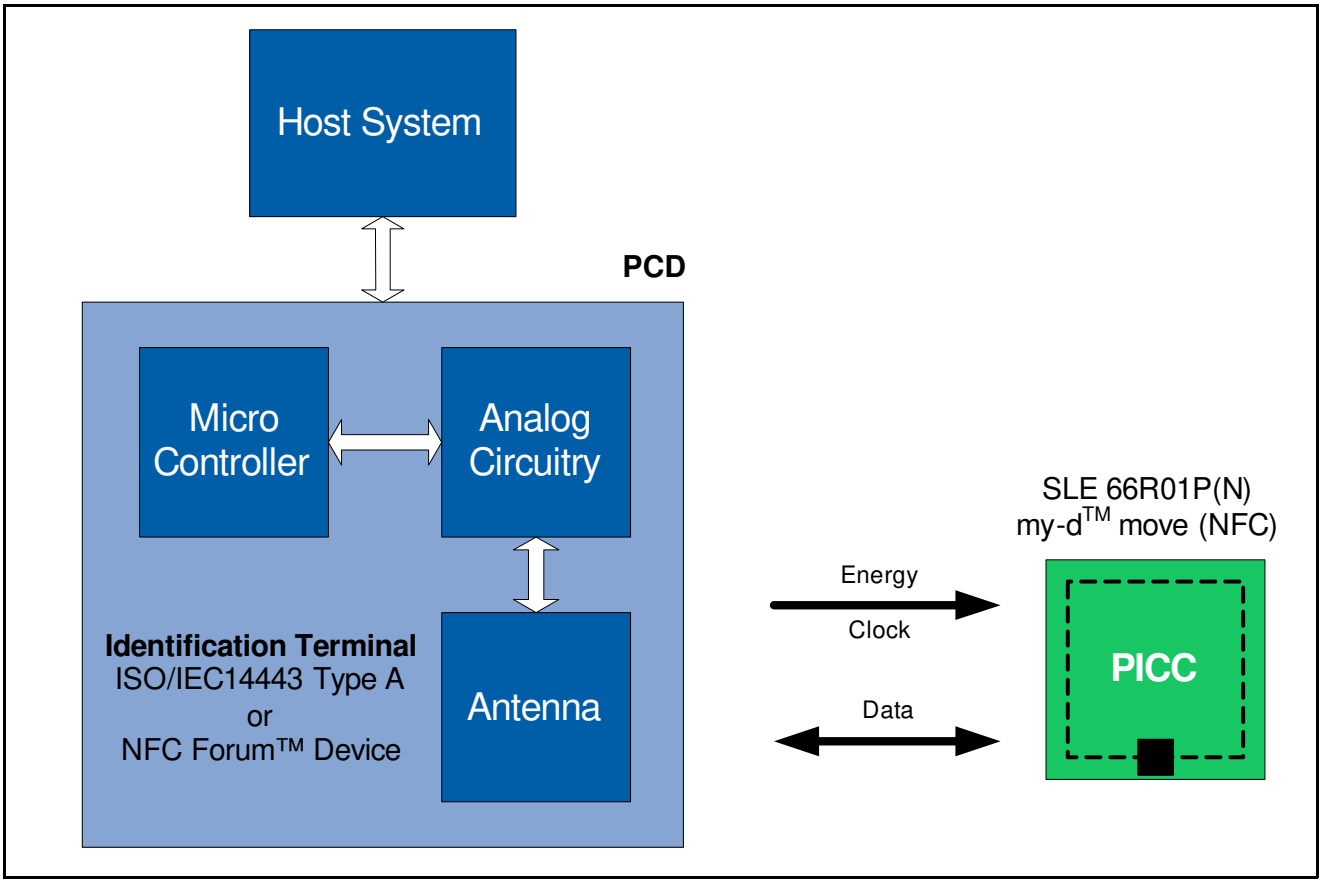

Figure 5 SLE 66R01P and SLE 66R01PN Contactless System Overview

3.5 UID Coding

To identify a SLE 66R01P and SLE 66R01PN chip the manufacturer code and a chip family identifier are coded into the UID as described in the **Table 4**. The chip family identifier can be used to determine the basic command set for the chip.

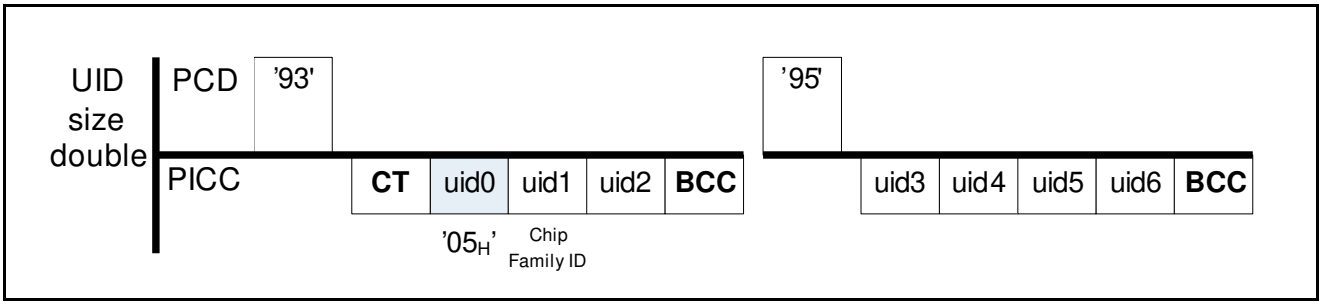

Figure 6 SLE 66R01P and SLE 66R01PN double-size UID

Table 4 UID Coding

UID Field	Value	Description
uid0	05_H	IC Manufacturer Code according to ISO/IEC 7816-6
uid1	$3x_H$	Chip Family Identifier Higher Nibble: 0011_B: my-d™ move and my-d™ move NFC Lower Nibble: part of the UID number

3.6 Supported Standards

the SLE 66R01P and SLE 66R01PN support the following standards:

- ISO/IEC 14443 Type A (Parts 1, 2 and 3)
  tested according to ISO/IEC 10373-6 (PICC Test & Validation)
- ISO/IEC 14443-3 Type A
- NFC Forum™ Type 2 Tag Operation

3.7 Command Set

The SLE 66R01P and SLE 66R01PN is compliant to the ISO/IEC 14443-3 Type A standard.

A set of standard ISO/IEC 14443-3 Type A commands is implemented to operate the chip.

Additionally NFC Forum™ Type 2 Tag commands and a my-d™ move and my-d™ move NFC specific command set is implemented. This facilitates the access to the on-chip integrated memory and supports the execution of password and counter functionality.

4 Memory Organization

The total amount of user memory is 152 byte. It is organized in blocks of 4 bytes each.

It comprises:

- 128 bytes for user data
- 24 bytes for UID, OTP, locking information, IC configuration and manufacturer information.

Additionally the Password and Password Retry Counter are allocated in non-addresable part of the memory and are accessible via dedicated commands only.

Figure 7 shows the memory structure of the SLE 66R01P and SLE 66R01PN chip.

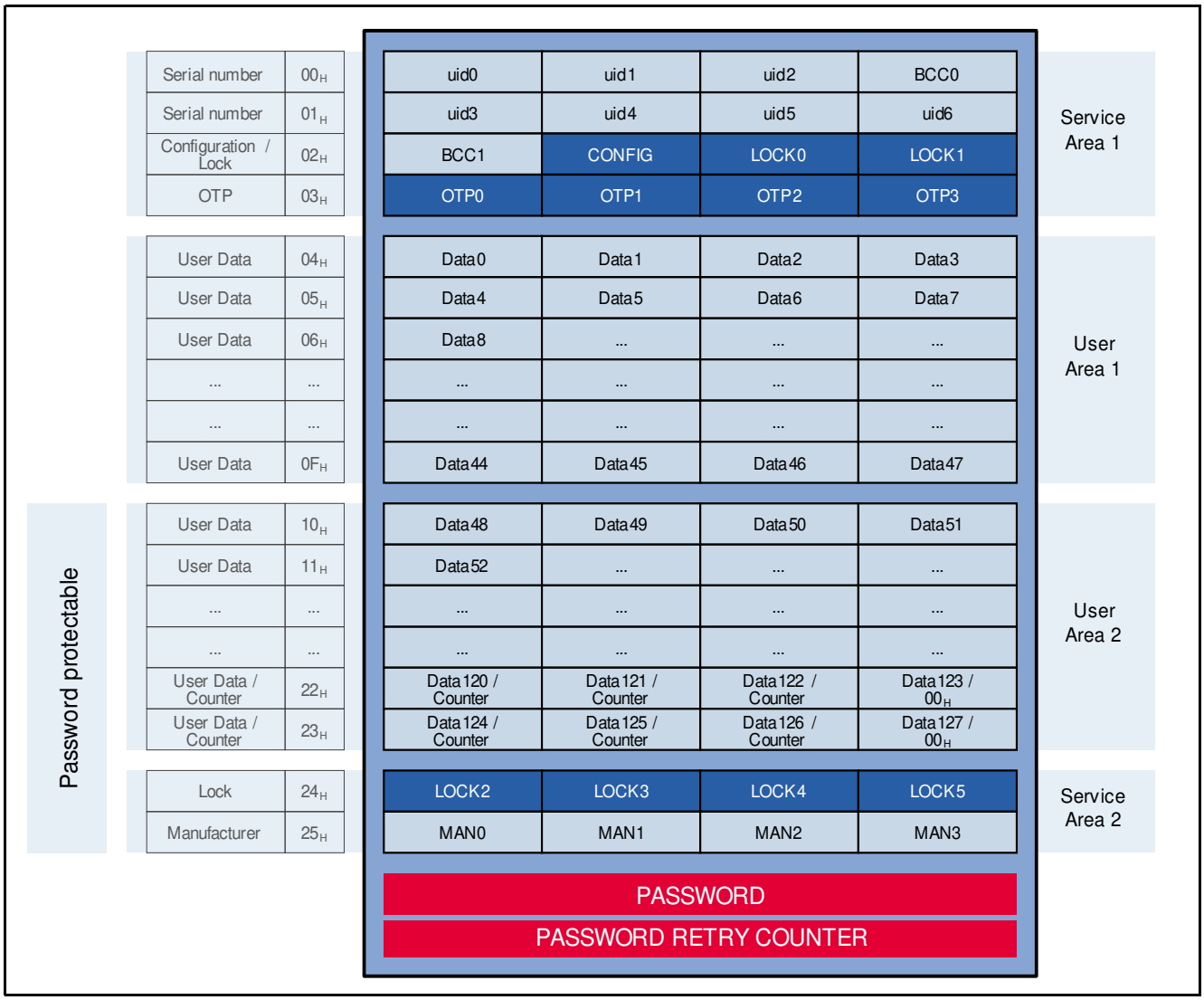

Figure 7 my-d™ move and my-d™ move NFC memory organization

4.1 User Memory Area 1 and 2

Blocks from address 04_H to 23_H belong to the User Memory Area (1 and 2). This part of the memory is readable / writable as well as lockable against unintentional overwriting using a locking mechanism.

Moreover the User Memory Area 2 above the address 10_H can be protected with a Password against unintentional reading or reading/writing.

4.2 Service Area 1 and 2

The Service Area 1 (block address 00_H to 03_H) contains

- 7-byte double-size UID (plus two bytes of UID BCC information)
- Configuration Byte
- LOCK0 and LOCK1 to lock the OTP block and blocks in User Area 1
- 32 bit OTP memory

The Service Area 2 (block address 24_H to 25_H) contains

- LOCK2 - LOCK5 to lock blocks in User Area 2
- Manufacturer Data

4.2.1 Unique Identifier (UID)

The 9 bytes of the UID (7 byte UID + 2 bytes BCC information) are allocated in Block 00_H, Block 01_H and Byte 1 of Block 02_H of the my-d™ move and my-d™ move NFC memory. All bytes are programmed and locked during the manufacturing process. These bytes cannot be changed.

For the content of the UID the following definitions apply:

- SLE 66R01P and SLE 66R01PN support Cascade Level 2 UID according to the ISO/IEC 14443-3 Type A which is a 7 byte unique number

The table below describes the content of the UID including the BCC information.

Table 5 UID Description

Cascade Level 2 - double-size UID										
UID Byte	CT[1]	uid0[2]	uid1[3]	uid2	BCC0[4]	uid3	uid4	uid5	uid6	BCC1[4]

1) CT is the Cascade Tag and designates CL2. It has a value of 88_H. Please note that CT is hardwired and not stored in the memory.
2) uid0 is the Manufacturer Code: 05_H according to ISO/IEC 7816-6
3) uid1 is the Chip Family Identifier.
The higher significant nibble identifies a my-d™ move and my-d™ move NFC chip (0011_B).
The lower significant nibble of uid1 is part of the serial number.
4) BCCx are the UID CLn checkbytes calculated as Exclusive-OR over the four previous bytes (as described in ISO/IEC 14443-3 Type A). BCCx is stored in the memory and read-out during the anti-collision.

4.2.2 Configuration Byte

The Configuration Byte defines the configurable functionality of the my-d™ move and my-d™ move NFC. It is allocated in Byte 1 of Block 02_H. At delivery all bits of the Configuration Byte are set to 0_B. Note that the Configuration Byte is One Time Programmable (OTP) byte. Bits allocated in this byte can only be logically set to 1_B, which is an irreversible process i.e. bits can not be reset to 0_B afterwards.

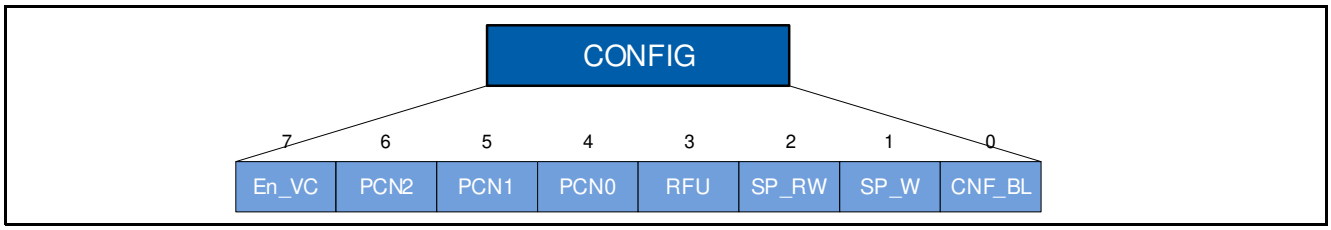

Figure 8 Configuration Byte

Table 6 Configuration Byte Definition

Configuration Bit	Abbreviation	Description
Configuration Byte Lock	CNF_BL	0_B ... Configuration Byte programmable 1_B ... Configuration Byte locked
Set Password for Write access	SP-W	0_B ... The Write Password is not active 1_B ... The Write Password is active for Write Commands which are applied to all blocks starting from the address 10_H
Set Password for Read and Write access	SP_WR	0_B ... The Read and Write Password is not active 1_B ... The Read and Write Password is active for read, write and decrement commands for all blocks above address $0F_H$
RFU	RFU	Reserved for the future use
Initial value of the Password Retry Counter	PCN2 PCN1 PCN0	000_B ... Default setting 111_B ... Maximal initial value (7_D) Password Retry Counter is only active if the initial value is different than 0_D.
16-bit Value Counter	En_VC	0_B ... Value Counter is not configured, blocks 22_H and 23_H are User Data blocks 1_B ... Value Counter is set, blocks 22_H and 23_H are reserved for the 16-bit Value Counter

Note: The CNF_BL bit is active immediately active after writing. To activate the new configuration of SP-W, SP-WR and VCRN16 bits the execution of REQA or WUPA commands is required. The new value of the Password Retry Counter (PCN2, PCN1 and PCN0 bits) is active immediately, i.e. is read each time the information is required (during the execution of the Access command).

4.2.2.1 Locking Mechanism for the Configuration Byte

The my-d™ move and my-d™ move NFC is delivered with all bits of Configuration Byte set to 0_B. The issuer should define the functionality of a chip as required (set e.g. Write and/or Read/Write Password, the Password Retry Counter, the 16-bit Value Counter etc.) and lock the Configuration Byte. Once the Configuration Byte is locked no further changes to the Configuration Byte are possible.

Note: If all three BL Bits in the LOCK0 Byte are set to 1_B, block 02_H is locked. It is then not possible to change the value of this particular block (02_H) any more.

4.2.3 Locking mechanism

Bytes LOCK0, LOCK1 allocated in Block 02_H and LOCK2, LOCK3, LOCK4 and LOCK5 allocated in Block 24_H represent the one time field programmable bits which are used to lock the blocks in the specified address range from block 03_H (OTP Block) to 23_H.

Each block in this range can be individually locked to prevent further write access. A locking mechanism of each block is irreversible, i.e. once the locking information of a particular block (Lx) is set to 1_B it can not be reset back to 0_B any more. **Figure 9** illustrates the locking bytes with the corresponding locking bits.

Furthermore, it is possible to freeze the locking information of some memory areas by setting Block Locking (BL) bits e.g. if the bit BL 15-10 is set to 1_B then the locking information for the corresponding area (L10 to L15) is not changeable any more. See the example in the **Table 7** below.

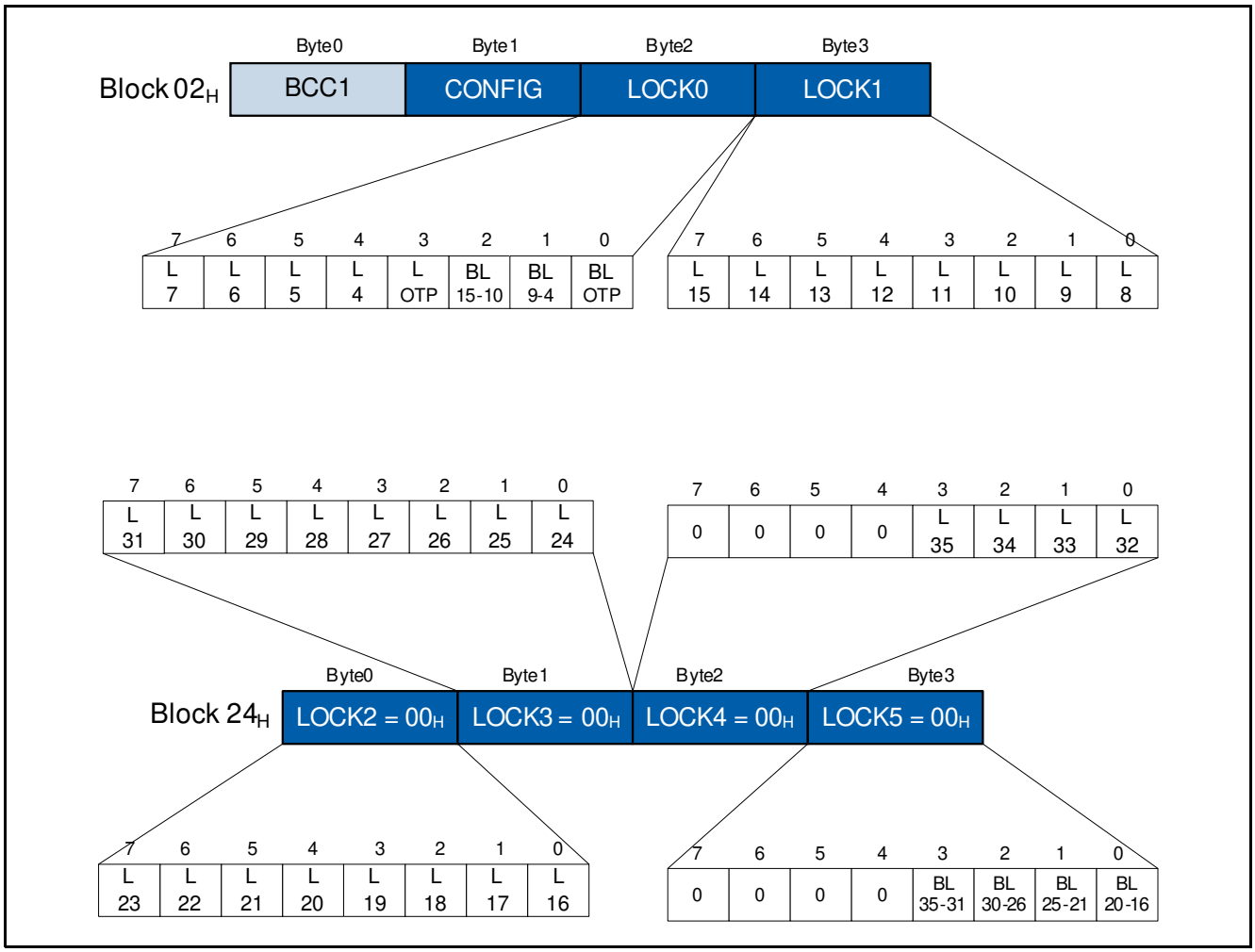

Figure 9 Locking and Block Locking Mechanism

The Write One Block (WR1B) command should be used to set the locking or block locking information of a certain block.

If WR1B is applied to Block 02_H then:

- the Byte 0 (BCC1) will not be changed
- the Byte 1 (Configuration Byte) will be changed only if it is not locked

If WR1B is applied to Block 24_H then:

- the Byte2 [7..4] = Lock4[7..4] and
- the Byte3 [7..4] = Lock5[7..4] will not be changed neither.

The locking and block locking for a certain block is active immediately after writing. That means that it is not necessary to execute the REQA or WUPA command in order to activate the locking.

Note: If all three BL bits in the LOCK0 byte are set to 1_B then Block 02_H is locked. It is not possible to change the locking bits of this block any more. The same applies for block 24_H. If BL bits of the LOCK5 byte are set to 1_B then this block is locked. In this case the SLE 66R01P and SLE 66R01PN responds with NACK to a corresponding Write command.

Table 7 Example for OTP Block Lock and Block Lock

BL OTP	L OTP	OTP BLOCK STATE
0_B	0_B	OTP Block Unlocked
0_B	1_B	OTP Block Locked
1_B	0_B	OTP Block Unlocked and can not be locked ever more
1_B	1_B	OTP Block Locked

An Anti-Tearing mechanism is implemented for Lock bytes on the SLE 66R01P and SLE 66R01PN. This mechanism prevents a stored value to be lost in case of a tearing event. This increases the level of data integrity and it is transparent to the customer.

4.2.4 OTP Block

The Block 03_H is a One Time Programmable (OTP) Block. Bits allocated in this block can only be logically set to 1_B, which is an irreversible process i.e. bits can not be reset to 0_B afterwards.

The Write One Block (WR1B) command should be used to program a specific OTP value. Incoming data of the WR1B command are bit-wise OR-ed with the current content of the OTP Block and the result is written back to the OTP Block.

Table 8 Writing to OTP Block (block 03_H) from the user point of view

OTP Block	Representation bit-wise	Description
Initial value	$0000\ 0000\ 0000\ 0000\ 0000\ 0000\ 0000\ 0000_B$	Production setting
Write $[55550003]_H$	$0101\ 0101\ 0101\ 0101\ 0000\ 0000\ 0000\ 0011_B$	Bit-wise “OR” with previous content of block 03_H
Write $[AA55001C]_H$	$1111\ 1111\ 0101\ 0101\ 0000\ 0000\ 0001\ 1111_B$	Bit-wise “OR” with previous content of block 03_H

An Anti-Tearing mechanism is implemented for the OTP Block on the my-d™ move and my-d™ move NFC. This mechanism prevents the stored value to be lost in case of a tearing event. This increases the level of data integrity and is transparent to the customer.

4.2.5 Manufacturer Block (25_H)

The Manufacturer Block is used to store the my-d™ move and my-d™ move NFC internal on-chip configuration data and the manufacturing data such as Week and Year of production, Lot and Wafer Counter etc. This block is programmed and locked at manufacturing.

4.3 Memory Principle for NFC Forum™ Type 2 Tag

This section desribes how to map the my-d™ move and my-d™ move NFC memory into the memory structures defined in the NFC Forum™ Type 2 Tag technical specification. This enables the usage of the my-d™ move and my-d™ move NFC as a NFC Forum™ Type 2 Tag compatible chip.

4.3.1 NFC Forum™ Static Memory Structure

The Static Memory Structure is applied to a NFC Forum™ Type 2 Tag with a memory size equal to 64 bytes (see **Figure 10**). Blocks 04_H to $0F_H$ are available to store user data.

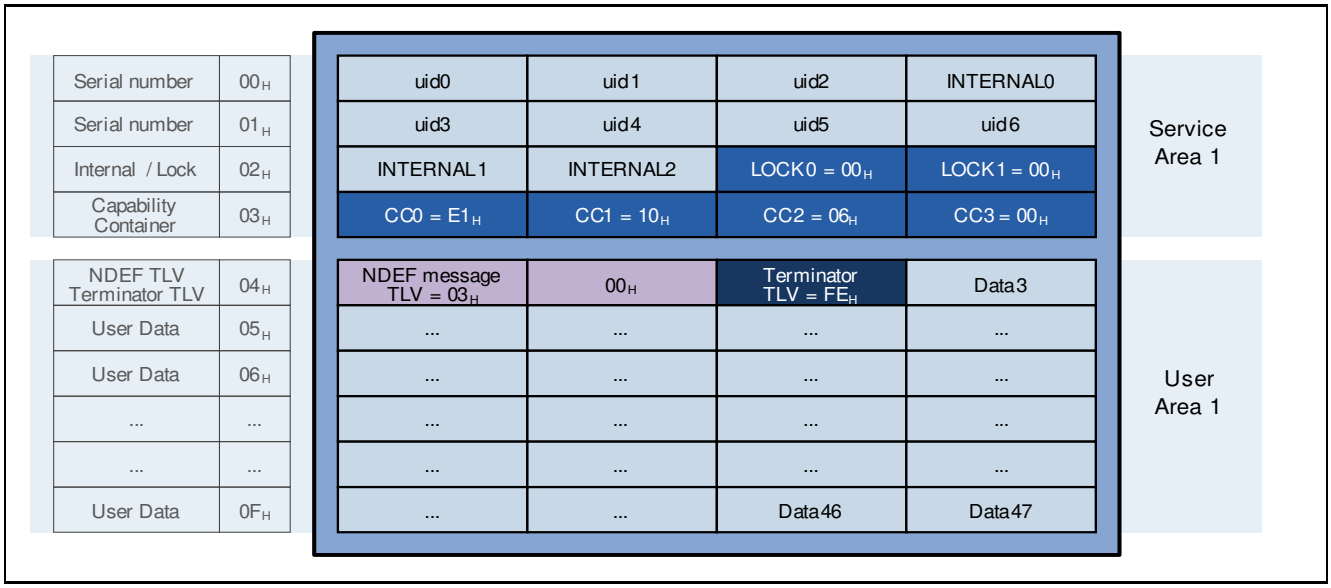

Figure 10 Static Memory Structure

The Static Memory Structure is characterized by the NDEF message TLV (03_H) starting at block address 04_H. The NFC data shown in **Figure 10** is an empty NDEF message (see **Table 10**).

4.3.2 NFC Forum™ Dynamic Memory Structure

The Dynamic Memory Structure can be applied to NFC Forum™ Type 2 Tags with bigger memories than 64 bytes. **Figure 11** shows a generic memory layout with a Dynamic Memory Structure (based on the my-d™ move and my-d™ move NFC chip).

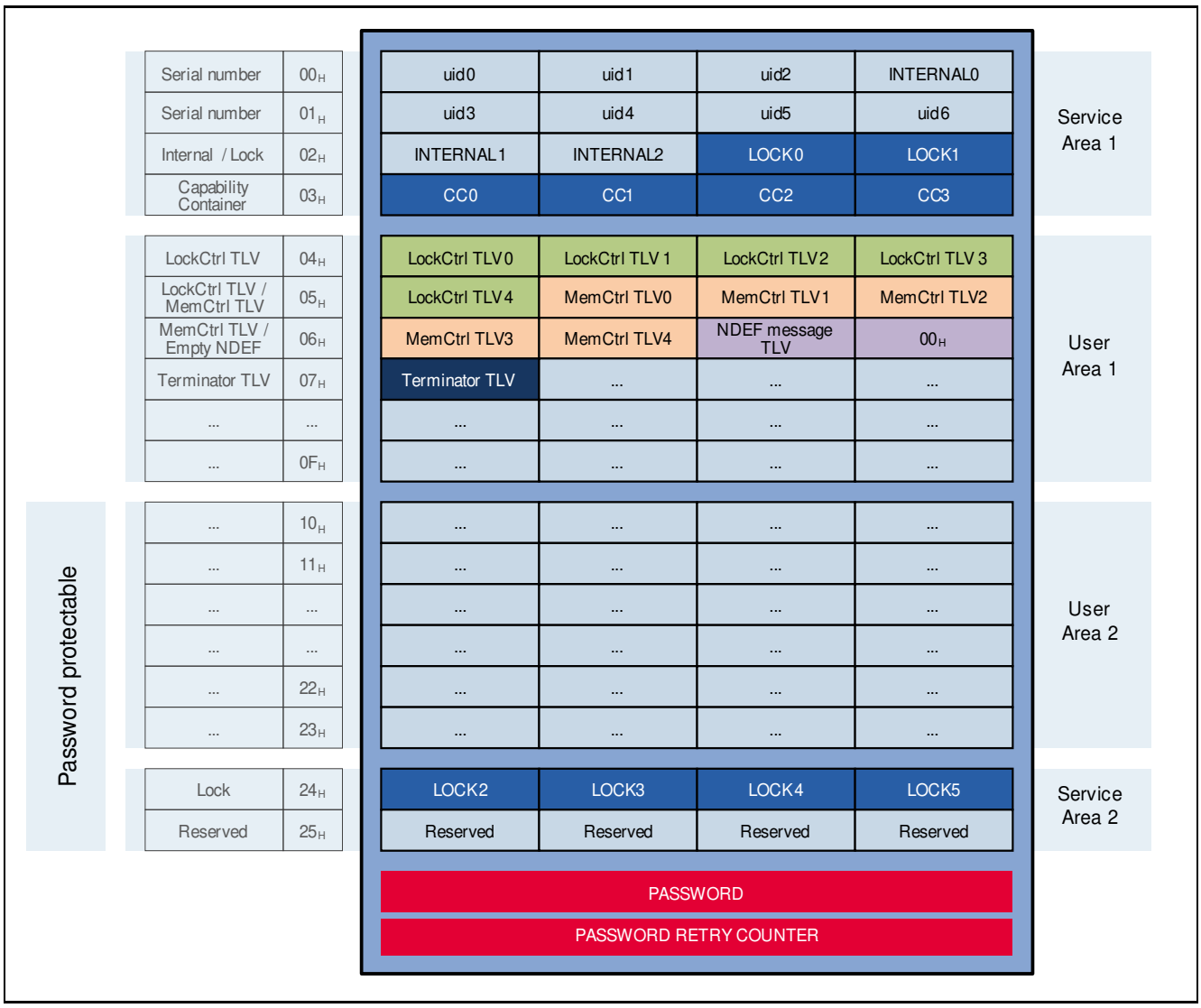

Figure 11 Generic NFC Forum™ Type 2 Tag dynamic memory layout (based on SLE 66R01P(N))

Compared to the Static Memory Structure the Dynamic Memory Structure is characterized by the NDEF message TLV starting after the Lock Control TLV and Memory Control TLV (the Lock Control TLV starts at Block 04_H).

Within a Dynamic Memory Structure dynamic lock bytes and reserved bytes might be located at any address in the data area (see LOCK2 - LOCK5, Reserved shown in **Figure 11**). The location and the number of bytes used for these purposes is defined by the settings of the Lock Control TLV respectively Memory Control TLV.

Following example for a Dynamic Memory Structure (shown in **Figure 12**) focusses on my-d™ move and my-d™ move NFC.

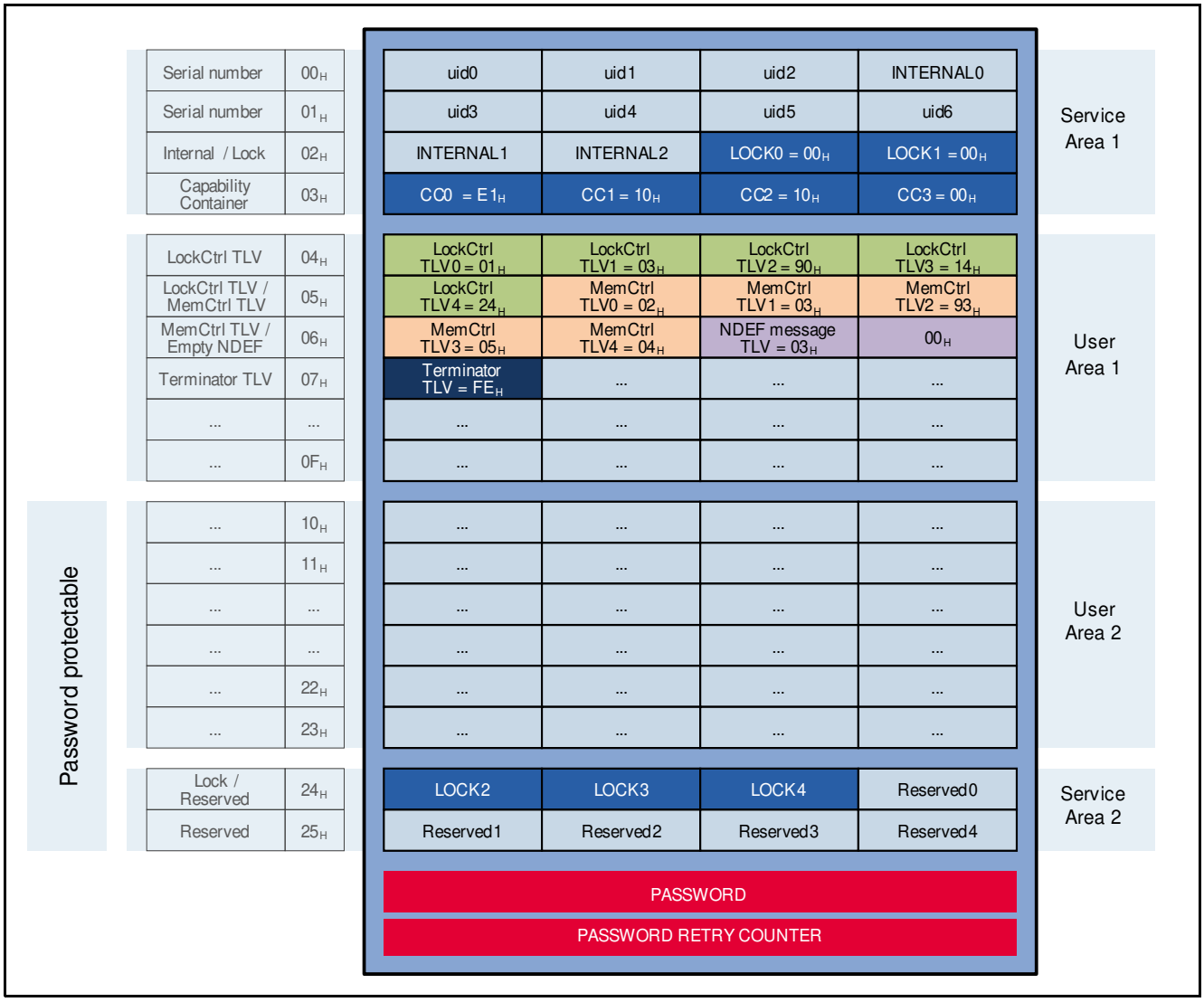

Figure 12 Example of a NFC Forum™ Type 2 Tag dynamic memory layout (based on SLE 66R01P(N))

If a NFC Forum™ Type 2 Tag compliant chip with Lock Control TLV and Memory Control TLV is required, NFC Forum™ Type 2 Tag specific data such as Capability Container, Lock Control TLV, Memory Control TLV, NDEF Message and Terminator TLV should be written to the memory according to the given hardware configuration.

Figure 12 holds valid Lock Control TLV and the Memory Control TLV settings within a Dynamic Memory Structure specially suited for the my-d™ move and my-d™ move NFC devices. For my-d™ move and my-d™ move NFC the position of the static and dynamic lock bytes is hard-wired and it is not possible to change their position in the memory.

- Static lock bytes LOCK0 and LOCK1 are allocated in block 2, bytes 2 and 3. LOCK0 and LOCK1 are used to lock blocks from address 00_H to $0F_H$.
- Dynamic lock bytes LOCK2 to LOCK5 are allocated in block 24_H. These LOCKx bytes are used to lock blocks starting from address 10_H. The position and the number of dynamic lock bits is coded into the Lock Control TLV as shown above. In this example 20 lock bits are required to lock the User Memory blocks 10_H to 23_H. Furthermore the Memory Control TLV defines the location and number of reserved bytes in the memory.