Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!

Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

SLG46108

GreenPAK
Ultra-small Programmable Mixed-signal Matrix

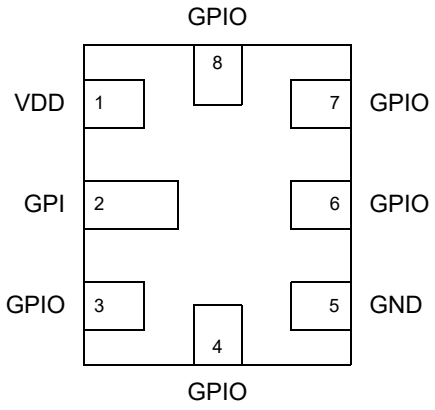
Features

- Logic & Mixed Signal Circuits
- Highly Versatile Macrocells
- 1.8 V (±5%) to 5 V (±10%) Supply
- Operating Temperature Range: -40°C to 85°C
- RoHS Compliant / Halogen-Free
- Pb-Free 8-pin STQFN: 1.0 x 1.2 x 0.55 mm, 0.4 mm pitch

Applications

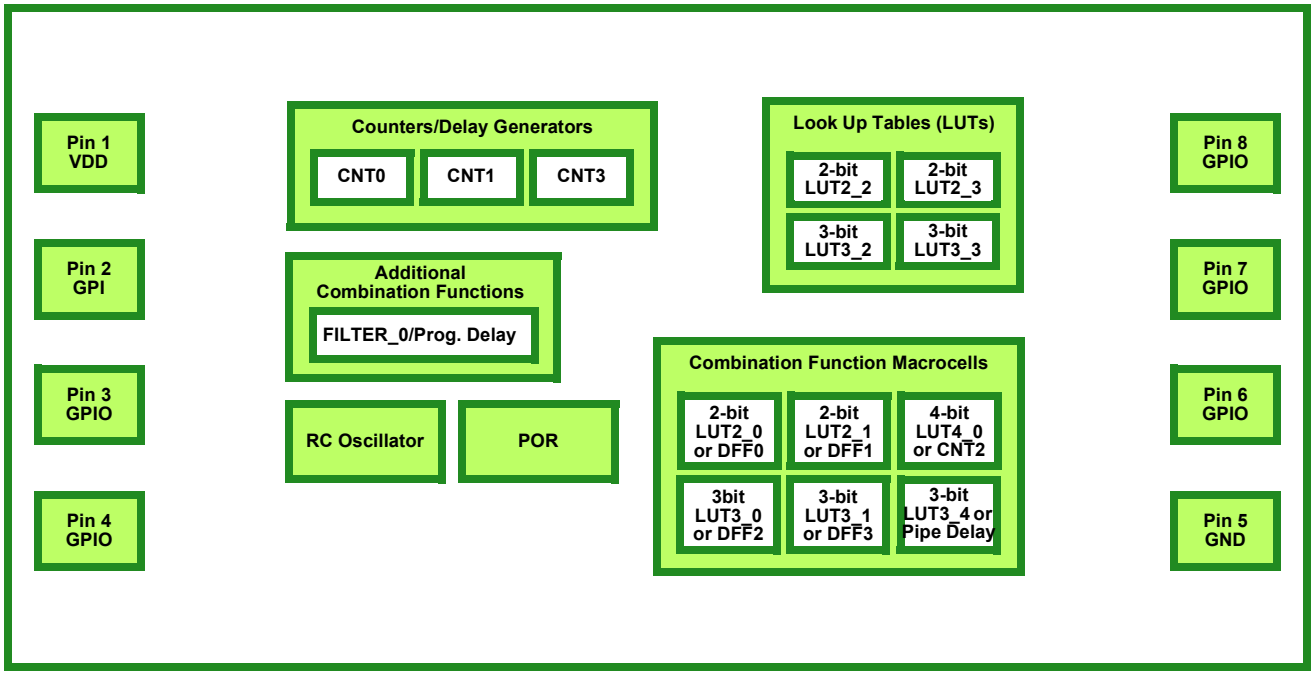
- Personal Computers and Servers
- PC Peripherals
- Consumer Electronics
- Data Communications Equipment
- Handheld and Portable Electronics

Pin Configuration



STQFN-8
(Top View)

Block Diagram



1.0 Overview

The SLG46108 provides a small, low power component for commonly used mixed-signal functions. The user creates their circuit design by programming the one time Non-Volatile Memory (NVM) to configure the interconnect logic, the I/O Pins and the macrocells of the SLG46108. This highly versatile device allows a wide variety of mixed-signal functions to be designed within a very small, low power single integrated circuit. The macrocells in the device include the following:

- Four Combinatorial Look Up Tables (LUTs)
  - Two 2-bit LUTs
  - Two 3-bit LUTs
- Seven Combination Function Macrocell
  - Two Selectable D Flip-Flop / Latches (DFF) or 2-bit LUTs
  - Two Selectable D Flip-Flop / Latches (DFF) or 3-bit LUTs
  - One Selectable Pipe Delay or 3-bit LUT
    - Pipe Delay – 8 stage / 2 output
  - One Selectable Counter/Delay (CNT/DLY) or 4-bit LUT
  - One Programmable Delay / Deglitch Filter
- Three 8-bit Counter / Delay Generators (CNT/DLY) with external clock/reset
- RC Oscillator (RC OSC)
- Power On Reset (POR)

2.0 Pin Description

2.1 Functional Pin Description

Pin #	Pin Name	Function
1	VDD	Power Supply
2	GPI	General Purpose Input
3	GPIO	General Purpose I/O
4	GPIO	General Purpose I/O
5	GND	GND
6	GPIO	General Purpose I/O
7	GPIO	General Purpose I/O
8	GPIO	General Purpose I/O

3.0 User Programmability

Non-volatile memory (NVM) is used to configure the SLG46108's connection matrix routing and macrocells. The NVM is One-Time-Programmable (OTP). However, Silego's GreenPAK development tools can be used to configure the connection matrix and macrocells, without programming the NVM, to allow on-chip emulation. This configuration will remain active on the device as long as it remains powered and can be re-written as needed to facilitate rapid design changes.

When a design is ready for in-circuit testing, the same GreenPAK development tools can be used to program the NVM and create samples for small quantity builds. Once the NVM is programmed, the device will retain this configuration for the duration of its lifetime.

Once the design is finalized, the design file can be forwarded to Silego to integrate into the production process.

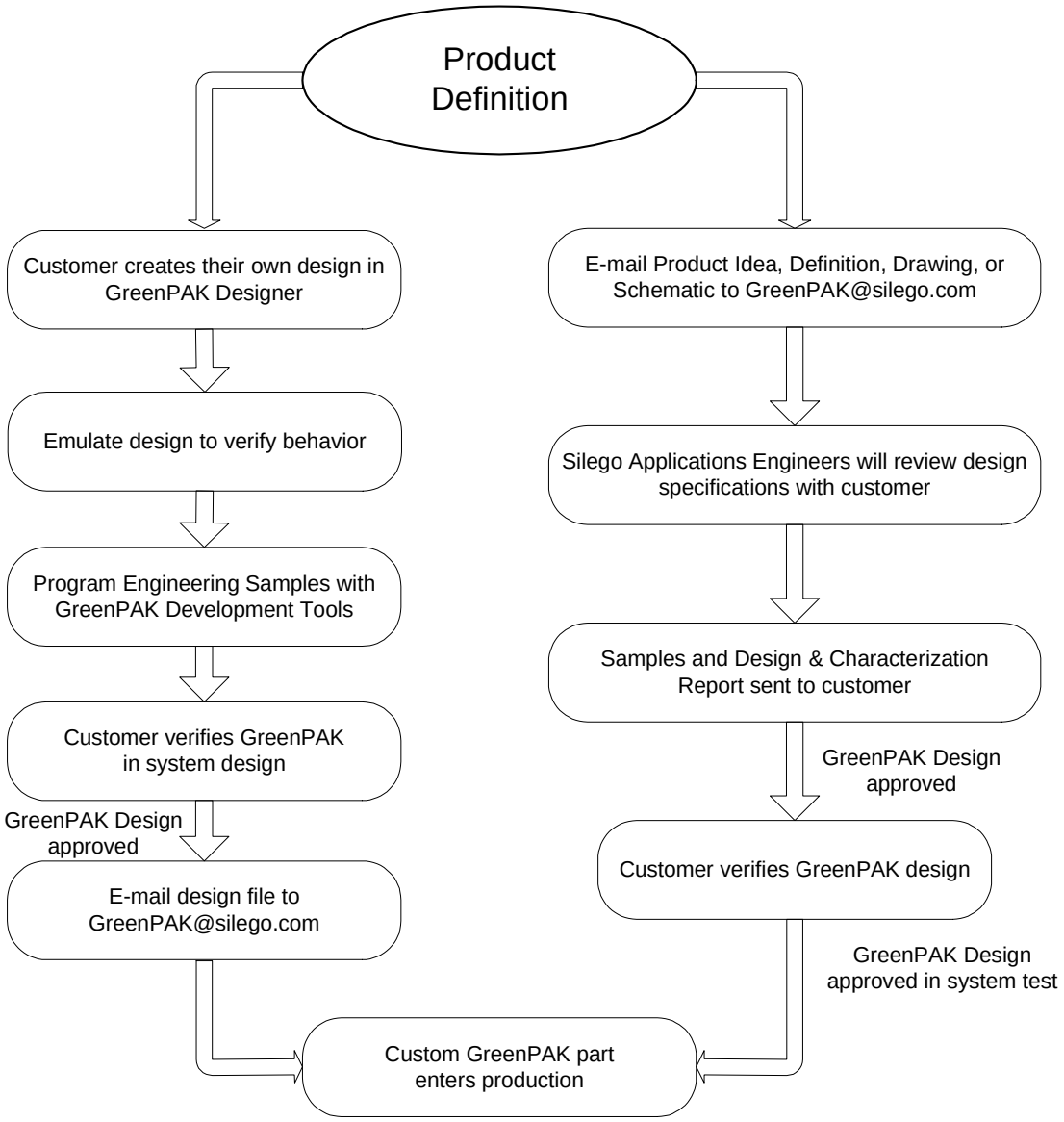


Figure 1. Steps to create a custom Silego GreenPAK device

4.0 Ordering Information

Part Number	Type
SLG46108V	8-pin STQFN
SLG46108VTR	8-pin STQFN - Tape and Reel (3k units)

5.0 Electrical Specifications

5.1 Absolute Maximum Conditions

Parameter		Min.	Max.	Unit
Supply voltage on VDD relative to GND		-0.5	7	V
DC Input voltage		GND - 0.5	VDD + 0.5	V
Maximum Average or DC Current (Through pin)	Push-Pull 1x	--	8	mA
	Push-Pull 2x	--	10	
	OD 1x	--	8	
	OD 2x	--	12	
	OD 4x	--	25	
Current at Input Pin		-1.0	1.0	mA
Storage Temperature Range		-65	150	°C
Junction Temperature		--	150	°C
ESD Protection (Human Body Model)		2000	--	V
ESD Protection (Charged Device Model)		1300	--	V
Moisture Sensitivity Level		1		

5.2 Electrical Characteristics (1.8V ±5% V_{DD})

Symbol	Parameter	Condition/Note	Min.	Typ.	Max.	Unit
V_{DD}	Supply Voltage		1.71	1.80	1.89	V
I_Q	Quiescent Current	Static Inputs and Outputs (when OSC is powered down and non-operational)	--	0.28	--	µA
T_A	Operating Temperature		-40	25	85	°C
V_{PP}	Programming Voltage		7.25	7.50	7.75	V
V_{IH}	HIGH-Level Input Voltage	Logic Input	1.071	--	V_{DD}	V
		Logic Input with Schmitt Trigger	1.276	--	V_{DD}	V
		Low-Level Logic Input	0.936	--	V_{DD}	V
V_{IL}	LOW-Level Input Voltage	Logic Input	--	--	0.730	V
		Logic Input with Schmitt Trigger	--	--	0.475	V
		Low-Level Logic Input	--	--	0.517	V
V_{HYS}	Schmitt Trigger Hysteresis Voltage	Logic Input with Schmitt Trigger	0.26	0.47	0.60	V
I_{LKG}	Input leakage (Absolute Value)		--	0.001	1	µA
V_{OH}	HIGH-Level Output Voltage	Push-Pull 1X, Open Drain PMOS 1X, I_{OH} = 100 µA	1.692	1.788	--	V
		Push-Pull 2X, Open Drain PMOS 2X, I_{OH} = 100 µA	1.700	1.794	--	V

Symbol	Parameter	Condition/Note	Min.	Typ.	Max.	Unit
V_{OL}	LOW-Level Output Voltage	Push-Pull 1X, I_{OL}= 100 µA	--	0.01	0.016	V
		Push-Pull 2X, I_{OL}= 100 µA	--	0.005	0.007	V
		Open Drain NMOS 1X, I_{OL}= 100 µA	--	0.005	0.006	V
		Open Drain NMOS 2X, I_{OL}= 100 µA	--	0.003	0.003	V
I_{OH}	HIGH-Level Output Current (see Note 1)	Push-Pull 1X, Open Drain PMOS 1X, $V_{OH} = V_{DD}$ - 0.2	1.045	1.506	--	mA
		Push-Pull 2X, Open Drain PMOS 2X, $V_{OH} = V_{DD}$ - 0.2	2.097	2.982	--	mA
I_{OL}	LOW-Level Output Current (see Note 1)	Push-Pull 1X, V_{OL} = 0.15 V	0.984	1.363	--	mA
		Push-Pull 2X, V_{OL} = 0.15 V	2.011	2.743	--	mA
		Open Drain NMOS 1X, V_{OL} = 0.15 V	2.029	2.763	--	mA
		Open Drain NMOS 2X, V_{OL} = 0.15 V	4.020	5.471	--	mA
I_{VDD}	Maximum Average or DC Current Through VDD Pin (Per chip side, see Note 2)	T_J = 85°C	--	--	45	mA
		T_J = 110°C	--	--	22	mA
I_{GND}	Maximum Average or DC Current Through GND Pin (Per chip side, see Note 2)	T_J = 85°C	--	--	90	mA
		T_J = 110°C	--	--	44	mA
V_O	Maximal Voltage Applied to any PIN in High-Impedance State		--	--	VDD	V
T_{SU}	Startup Time	From VDD rising past PON_{THR}	--	--	0.54	ms
PON_{THR}	Power On Threshold	V_{DD} Level Required to Start Up the Chip	1.302	1.505	1.707	V
$POFF_{THR}$	Power Off Threshold	V_{DD} Level Required to Switch Off the Chip	0.681	0.902	1.170	V
R_{PUP}	Pull Up Resistance	1 M Pull Up	927	1083	1271	kΩ
		100 k Pull Up	93	110	130	kΩ
		10 k Pull Up	10.9	12.7	14.8	kΩ
R_{PDWN}	Pull Down Resistance	1 M Pull Down	915	1084	1271	kΩ
		100 k Pull Down	93	125	130	kΩ
		10 k Pull Down	10.4	14.0	14.9	kΩ

Note 1: DC or average current through any pin should not exceed value given in Absolute Maximum Conditions.
Note 2: The GreenPAK's power rails are divided in two sides. Pins 2, 3 and 4 are connected to one side, pins 6, 7 and 8 to another.

5.3 Electrical Characteristics (3.3V ±10% V_{DD})

Symbol	Parameter	Condition/Note	Min.	Typ.	Max.	Unit
V_{DD}	Supply Voltage		3.0	3.3	3.6	V
I_Q	Quiescent Current	Static Inputs and Outputs (when OSC is powered down and non-operational)	--	0.52	--	µA
T_A	Operating Temperature		-40	25	85	°C
V_{PP}	Programming Voltage		7.25	7.50	7.75	V
V_{IH}	HIGH-Level Input Voltage	Logic Input	1.840	--	V_{DD}	V
		Logic Input with Schmitt Trigger	2.170	--	V_{DD}	V
		Low-Level Logic Input	1.086	--	V_{DD}	V
V_{IL}	LOW-Level Input Voltage	Logic Input	--	--	1.255	V
		Logic Input with Schmitt Trigger	--	--	0.934	V
		Low-Level Logic Input	--	--	0.669	V
V_{HYS}	Schmitt Trigger Hysteresis Voltage	Logic Input with Schmitt Trigger	0.56	0.71	0.86	V
I_{LKG}	Input leakage (Absolute Value)		--	0.001	1	µA
V_{OH}	HIGH-Level Output Voltage	Push-Pull 1X,Open Drain PMOS 1X, I_{OH} = 3 mA	2.721	3.108	--	V
		Push-Pull 2X, Open Drain PMOS 2X, I_{OH} = 3 mA	2.864	3.204	--	V
V_{OL}	LOW-Level Output Voltage	Push-Pull 1X, I_{OL}= 3 mA	--	0.175	0.257	V
		Push-Pull 2X, I_{OL}= 3 mA	--	0.086	0.122	V
		Open Drain NMOS 1X, I_{OL}= 3 mA	--	0.085	0.121	V
		Open Drain NMOS 2X, I_{OL}= 3 mA	--	0.043	0.061	V
I_{OH}	HIGH-Level Output Current (see Note 1)	Push-Pull 1X, Open Drain PMOS 1X, V_{OH} = 2.4 V	5.774	11.066	--	mA
		Push-Pull 2X, Open Drain PMOS 2X, V_{OH} = 2.4 V	11.351	21.730	--	mA
I_{OL}	LOW-Level Output Current (see Note 1)	Push-Pull 1X, V_{OL} = 0.4 V	4.491	6.438	--	mA
		Push-Pull 2X, V_{OL} = 0.4 V	9.124	12.884	--	mA
		Open Drain NMOS 1X, V_{OL} = 0.4 V	9.227	12.995	--	mA
		Open Drain NMOS 2X, V_{OL} = 0.4 V	17.995	25.459	--	mA
I_{VDD}	Maximum Average or DC Current Through VDD Pin (Per chip side, see Note 2)	T_J = 85°C	--	--	45	mA
		T_J = 110°C	--	--	22	mA
I_{GND}	Maximum Average or DC Current Through GND Pin (Per chip side, see Note 2)	T_J = 85°C	--	--	90	mA
		T_J = 110°C	--	--	44	mA

Symbol	Parameter	Condition/Note	Min.	Typ.	Max.	Unit
V_O	Maximal Voltage Applied to any PIN in High-Impedance State		--	--	VDD	V
T_{SU}	Startup Time	From VDD rising past PON_{THR}	--	--	0.52	ms
PON_{THR}	Power On Threshold	V_{DD} Level Required to Start Up the Chip	1.303	1.506	1.707	V
$POFF_{THR}$	Power Off Threshold	V_{DD} Level Required to Switch Off the Chip	0.718	0.901	1.173	V
R_{PUP}	Pull Up Resistance	1 M Pull Up	922	1082	1272	kΩ
		100 k Pull Up	92	109	129.0	kΩ
		10 k Pull Up	9.6	11.6	14.1	kΩ
R_{PDWN}	Pull Down Resistance	1 M Pull Down	916	1083	1270	kΩ
		100 k Pull Down	96	109	129	kΩ
		10 k Pull Down	9.7	11.4	14.2	kΩ

Note 1: DC or average current through any pin should not exceed value given in Absolute Maximum Conditions.
Note 2: The GreenPAK's power rails are divided in two sides. Pins 2, 3 and 4 are connected to one side, pins 6, 7 and 8 to another.

5.4 Electrical Characteristics (5V ±10% V_{DD})

Symbol	Parameter	Condition/Note	Min.	Typ.	Max.	Unit
V_{DD}	Supply Voltage		4.5	5.0	5.5	V
I_Q	Quiescent Current	Static Inputs and Outputs (when OSC is powered down and non-operational)	--	0.81	--	µA
T_A	Operating Temperature		-40	25	85	°C
V_{PP}	Programming Voltage		7.25	7.50	7.75	V
V_{IH}	HIGH-Level Input Voltage	Logic Input	2.744	--	V_{DD}	V
		Logic Input with Schmitt Trigger	3.190	--	V_{DD}	V
		Low-Level Logic Input	1.185	--	V_{DD}	V
V_{IL}	LOW-Level Input Voltage	Logic Input	--	--	1.877	V
		Logic Input with Schmitt Trigger	--	--	1.488	V
		Low-Level Logic Input	--	--	0.765	V
V_{HYS}	Schmitt Trigger Hysteresis Voltage	Logic Input with Schmitt Trigger	0.77	0.94	1.14	V
I_{LKG}	Input leakage (Absolute Value)		--	0.001	1	µA
V_{OH}	HIGH-Level Output Voltage	Push-Pull 1X,Open Drain PMOS 1X, I_{OH} = 5 mA	4.171	4.761	--	V
		Push-Pull 2X, Open Drain PMOS 2X, I_{OH} = 5 mA	4.336	4.879	--	V
V_{OL}	LOW-Level Output Voltage	Push-Pull 1X, I_{OL}= 5 mA	--	0.225	0.325	V
		Push-Pull 2X, I_{OL}= 5 mA	--	0.111	0.156	V
		Open Drain NMOS 1X, I_{OL}= 5 mA	--	0.110	0.155	V
		Open Drain NMOS 2X, I_{OL}= 5 mA	--	0.057	0.080	V
I_{OH}	HIGH-Level Output Current (see Note 1)	Push-Pull 1X, Open Drain PMOS 1X, V_{OH} = 2.4 V	20.656	30.203	--	mA
		Push-Pull 2X, Open Drain PMOS 2X, V_{OH} = 2.4 V	40.170	56.319	--	mA
I_{OL}	LOW-Level Output Current (see Note 1)	Push-Pull 1X, V_{OL} = 0.4 V	6.087	8.611	--	mA
		Push-Pull 2X, V_{OL} = 0.4 V	12.321	17.147	--	mA
		Open Drain NMOS 1X, V_{OL} = 0.4 V	12.444	17.282	--	mA
		Open Drain NMOS 2X, V_{OL} = 0.4 V	24.032	33.581	--	mA
I_{VDD}	Maximum Average or DC Current Through VDD Pin (Per chip side, see Note 2)	T_J = 85°C	--	--	45	mA
		T_J = 110°C	--	--	22	mA
I_{GND}	Maximum Average or DC Current Through GND Pin (Per chip side, see Note 2)	T_J = 85°C	--	--	90	mA
		T_J = 110°C	--	--	44	mA

Symbol	Parameter	Condition/Note	Min.	Typ.	Max.	Unit
V_O	Maximal Voltage Applied to any PIN in High-Impedance State				VDD	V
T_{SU}	Startup Time	From VDD rising past PON_{THR}			0.51	ms
PON_{THR}	Power On Threshold	V_{DD} Level Required to Start Up the Chip	1.303	1.506	1.707	V
$POFF_{THR}$	Power Off Threshold	V_{DD} Level Required to Switch Off the Chip	0.675	0.901	1.174	V
R_{PUP}	Pull Up Resistance	1 M Pull Up	921	1080	1269	kΩ
		100 k Pull Up	92	108	129	kΩ
		10 k Pull Up	8.8	11.0	13.9	kΩ
R_{PDWN}	Pull Down Resistance	1 M Pull Down	916	1082	1277	kΩ
		100 k Pull Down	92	108	129	kΩ
		10 k Pull Down	8.6	10.9	14.0	kΩ

Note 1: DC or average current through any pin should not exceed value given in Absolute Maximum Conditions.
Note 2: The GreenPAK's power rails are divided in two sides. Pins 2, 3 and 4 are connected to one side, pins 6, 7 and 8 to another.

5.5 IDD Estimator

Table 1. Typical Current estimated for each macrocell

Symbol	Parameter	Note	V_{DD} = 1.8 V	V_{DD} = 3.3V	V_{DD} = 5.0V	Unit
I	Current	Chip Quiescent	0.27	0.51	0.79	µA
		OSC 2 MHz, predivide = 1, divide = 1	21.86	32.18	45.29	µA
		OSC 2 MHz, predivide = 1, divide = 8	21.77	31.96	44.88	µA
		OSC 2 MHz, predivide = 1, divide = 64	21.70	31.82	44.70	µA
		OSC 2 MHz, predivide = 2, divide = 1	18.97	26.19	35.69	µA
		OSC 2 MHz, predivide = 2, divide = 8	18.92	26.07	35.49	µA
		OSC 2 MHz, predivide = 2, divide = 64	18.89	26.01	35.40	µA
		OSC 2 MHz, predivide = 4, divide = 1	17.53	23.21	30.93	µA
		OSC 2 MHz, predivide = 4, divide = 8	17.51	23.16	30.83	µA
		OSC 2 MHz, predivide = 4, divide = 64	17.49	23.12	30.78	µA
		OSC 2 MHz, predivide = 8, divide = 1	16.81	21.70	28.51	µA
		OSC 2 MHz, predivide = 8, divide = 8	16.80	21.67	28.46	µA
		OSC 2 MHz, predivide = 8, divide = 64	16.79	21.65	28.43	µA
		OSC 25 kHz, predivide = 1, divide = 1, 8 , 64	5.16	5.71	6.73	µA
		OSC 25 kHz, predivide = 2, divide = 1, 8 , 64	5.13	5.65	6.63	µA
		OSC 25 kHz, predivide = 4, divide = 1, 8 , 64	5.11	5.62	6.57	µA
		OSC 25 kHz, predivide = 8, divide = 1, 8 , 64	5.10	5.60	6.54	µA

5.6 Timing Estimator

Table 2. Typical Delay estimated for each macrocell

Symbol	Parameter	Note	V_{DD} = 1.8 V		V_{DD} = 3.3V		V_{DD} = 5.0V		Unit
			rising	falling	rising	falling	rising	falling	
tpd	Delay	Digital Input to PP 1X	33.4	36.4	13.6	15.0	9.8	10.6	ns
tpd	Delay	Digital Input to PP 2X	31.1	34.1	12.8	14.1	9.3	10.1	ns
tpd	Delay	Digital Input with Schmitt Trigger to PP 1X	33.4	35.7	13.8	15.2	10.0	11.0	ns
tpd	Delay	Low Voltage Digital input - to PP 1X (Vih = min)	214.1	623.0	216.8	184.6	105.0	120.0	ns
tpd	Delay	Digital Input without Schmitt Trigger -- 1x NMOS	--	79.4	--	28.0	--	18.0	ns
tpd	Delay	Digital Input without Schmitt Trigger -- 1x PMOS	33.8	--	13.8	--	10.0	--	ns
tpd	Delay	Digital Input without Schmitt Trigger -- 2x NMOS	--	71.3	--	25.1	--	16.1	ns
tpd	Delay	Digital Input without Schmitt Trigger -- 2x PMOS	31.4	--	12.9	--	9.4	--	ns
tpd	Delay	Output enable from pin, OE Hi-Z to 1	33.5	--	13.7	--	9.9	--	ns
tpd	Delay	Output enable from pin, OE Hi-Z to 0	--	36.3	--	15.0	--	10.9	ns
tpd	Delay	2-bit LUT (Latch shared macrocell inputs)	24.5	22.3	10.8	9.5	8.0	7.0	ns
tpd	Delay	Latch (2-bit LUT shared macrocell inputs)	25.8	24.8	11.3	10.5	8.4	7.6	ns
tpd	Delay	3-bit LUT (LATCH shared macrocell inputs)	29.5	26.0	12.7	10.9	9.3	8.0	ns

Table 2. Typical Delay estimated for each macrocell

Symbol	Parameter	Note	V_{DD} = 1.8 V		V_{DD} = 3.3V		V_{DD} = 5.0V		Unit
			rising	falling	rising	falling	rising	falling	
tpd	Delay	Latch with nRST/nSET (3-bit LUT shared macrocell inputs)	30.1	34.6	13.2	14.7	9.7	10.6	ns
tpd	Delay	4-bit LUT (shared macrocell inputs)	28.3	25.7	12.3	10.6	9.0	7.7	ns
tpd	Delay	2-bit LUT	17.5	19.4	7.8	8.1	5.9	5.9	ns
tpd	Delay	3-bit LUT	21.7	24.2	9.4	9.8	7.1	7.1	ns
tpd	Delay	CNT/DLY Logic	50.6	42.5	22.0	18.6	15.5	13.3	ns
tpd	Delay	CNT/DLY (shared macrocell inputs)	54.2	46.3	23.4	20.1	16.5	14.3	ns
tpd	Delay	CNT3/DLY3 Rising Edge Detect (shared macrocell inputs)	108.9	--	49.2	--	34.0	--	ns
tpd	Delay	CNT3/DLY3 Falling Edge Detect (shared macrocell inputs)	--	108.1	--	48.9	--	33.9	ns
tpd	Delay	CNT3/DLY3 Both Edge Detect (shared macrocell inputs)	108.4	108.2	49.0	48.9	34.0	33.9	ns
tw	Pulse Width	CNT3/DLY3 Rising Edge Detect (shared macrocell inputs)	49.7	--	21.7	--	15.8	--	ns
tw	Pulse Width	CNT3/DLY3 Falling Edge Detect (shared macrocell inputs)	--	49.1	--	21.2	--	15.5	ns
tw	Pulse Width	CNT3/DLY3 Both Edge Detect (shared macrocell inputs)	47.7	47.1	20.8	20.3	15.2	14.9	ns
tpd	Delay	DFF	29.6	22.1	12.9	9.7	9.5	7.3	ns
tpd	Delay	DFF nReset	--	28.9	--	12.3	--	9.0	ns
tpd	Delay	DFF nSet	--	35.1	--	14.8	--	10.7	ns
tpd	Delay	Filter	183.7	196.7	75.4	78.4	49.5	52.2	ns
tpd	Delay	PDLY 1 Cell Both Edge Delay	352.0	346.5	160.6	157.9	119.2	117.3	ns
tpd	Delay	PDLY 1 Cell Both Edge Detect	39.1	37.7	16.9	16.1	12.2	11.7	ns
tpd	Delay	PDLY 1 Cell Rising Edge Detect	39.1	--	16.9	--	12.2	--	ns
tpd	Delay	PDLY 1 Cell Falling Edge Detect	--	37.7	--	16.1	--	11.7	ns
tpd	Delay	PDLY 2 Cells Both Edge Delay	657.4	653.0	313.2	310.8	224.2	222.5	ns
tpd	Delay	PDLY 2 Cells Both Edge Detect	39.1	37.7	16.9	16.1	12.2	11.7	ns
tpd	Delay	PDLY 2 Cells Rising Edge Detect	39.0	--	16.9	--	12.2	--	ns
tpd	Delay	PDLY 2 Cells Falling Edge Detect	--	37.8	--	16.1	--	11.7	ns
tpd	Delay	PDLY 3 Cells Both Edge Delay	965.1	959.0	460.1	457.0	329.5	324.4	ns
tpd	Delay	PDLY 3 Cells Both Edge Detect	39.1	37.7	16.9	16.1	12.2	11.7	ns
tpd	Delay	PDLY 3 Cells Rising Edge Detect	39.0	--	16.9	--	12.2	--	ns
tpd	Delay	PDLY 3 Cells Falling Edge Detect	--	37.8	--	16.1	--	11.7	ns
tpd	Delay	PDLY 4 Cells Both Edge Delay	1271.5	1266.1	606.9	604.0	434.9	432.8	ns
tpd	Delay	PDLY 4 Cells Both Edge Detect	39.1	37.7	16.9	16.1	12.2	11.7	ns
tpd	Delay	PDLY 4 Cells Rising Edge Detect	39.0	--	16.9	--	12.2	--	ns
tpd	Delay	PDLY 4 Cells Falling Edge Detect	--	37.8	--	16.1	--	11.7	ns

5.7 Typical Counter/Delay Offset Measurements

Table 3. Typical Counter/Delay Offset Measurements

Parameter	RC OSC Freq	RC OSC Power	V_{DD} = 1.8 V	V_{DD} = 3.3V	V_{DD} = 5.0V	Unit
offset	25 kHz	auto	19	14	12	µs
offset	2 MHz	auto	7	4	4	µs
frequency settling time	25 kHz	auto	19	14	12	µs
frequency settling time	2 MHz	auto	14	14	14	µs
variable (CLK period)	25 kHz	forced	0-40	0-40	0-40	µs
variable (CLK period)	2 MHz	forced	0-0.5	0-0.5	0-0.5	µs
tpd (non-delayed edge)	25kHz/2MHz	either	35	14	10	ns

5.8 Expected Delays and Widths

Table 4. Expected Delays and Widths (typical)

Symbol	Parameter	Note	V_{DD} = 1.8 V	V_{DD} = 3.3V	V_{DD} = 5.0V	Unit
Width	Width, 1 cell	mode:(any)edge detect, edge detect output	305	140	105	ns
Width	Width, 2 cell	mode:(any)edge detect, edge detect output	611	281	210	ns
Width	Width, 3 cell	mode:(any)edge detect, edge detect output	918	423	315	ns
Width	Width, 4 cell	mode:(any)edge detect, edge detect output	1225	564	420	ns
time1	Delay, 1 cell	mode:(any)edge detect, edge detect output	39	17	12	ns
time1	Delay, 2 cell	mode:(any)edge detect, edge detect output	39	17	12	ns
time1	Delay, 3 cell	mode:(any)edge detect, edge detect output	39	17	12	ns
time1	Delay, 4 cell	mode:(any)edge detect, edge detect output	39	17	12	ns
time2	Delay, 1 cell	mode: both edge delay, edge detect output	344	157	117	ns
time2	Delay, 2 cell	mode: both edge delay, edge detect output	650	298	222	ns
time2	Delay, 3 cell	mode: both edge delay, edge detect output	957	440	327	ns
time2	Delay, 4 cell	mode: both edge delay, edge detect output	1264	581	432	ns

5.9 Typical Pulse Width Performance

Table 5. Typical Pulse Width Performance.

Parameter	V_{DD} = 1.8 V	V_{DD} = 3.3V	V_{DD} = 5.0V	Unit
Filtered Pulse Width	< 150	< 55	< 35	ns

5.10 OSC Specifications

5.10.1 25 kHz RC Oscillator

Table 6. 25 kHz RC OSC frequency limits

Power Supply Range (VDD), V	Temperature Range					
	+25 °C		0 °C ... +85 °C		-40 °C ... +85 °C	
	Min., kHz	Max. kHz	Min., kHz	Max. kHz	Min., kHz	Max. kHz
1.8 V ±5%	24.442	25.552	23.613	26.037	23.190	26.916
3.3 V ±10%	24.453	25.542	23.566	26.044	23.194	26.945
5 V ±10%	24.207	26.109	23.417	26.220	23.086	26.907
2.5 V - 4.5 V	24.320	25.606	23.487	26.093	23.194	26.998
1.71 V….5.5 V	23.855	26.484	23.257	26.484	23.180	27.048

Table 7. 25 kHz RC OSC frequency error (error calculated relative to nominal value)

Power Supply Range (VDD), V	Temperature Range					
	+25 °C		0 °C ... +85 °C		-40 °C ... +85 °C	
	Error (% at Minimum)	Error (% at Maximum)	Error (% at Minimum)	Error (% at Maximum)	Error (% at Minimum)	Error (% at Maximum)
1.8 V ±5%	-2.23%	2.21%	-5.55%	4.15%	-7.24%	7.66%
3.3 V ±10%	-2.19%	2.17%	-5.73%	4.18%	-7.22%	7.78%
5 V ±10%	-3.17%	4.44%	-6.33%	4.88%	-7.66%	7.63%
2.5 V - 4.5 V	-2.72%	2.42%	-6.05%	4.37%	-7.22%	7.99%
1.71 V….5.5 V	-4.58%	5.93%	-6.97%	5.93%	-7.28%	8.19%

5.10.2 2 MHz RC Oscillator

Table 8. 2 MHz RC OSC frequency limits

Power Supply Range (VDD), V	Temperature Range					
	+25 °C		0 °C ... +85 °C		-40 °C ... +85 °C	
	Min., MHz	Max. MHz	Min., MHz	Max. MHz	Min., MHz	Max. MHz
1.8 V ±5%	1.906	2.068	1.826	2.122	1.762	2.212
3.3 V ±10%	1.937	2.065	1.845	2.140	1.747	2.191
5 V ±10%	1.878	2.267	1.815	2.295	1.691	2.295
2.5 V - 4.5 V	1.873	2.114	1.786	2.187	1.741	2.191
1.71 V….5.5 V	1.690	2.377	1.623	2.394	1.623	2.394

Table 9. 2 MHz RC OSC frequency error (error calculated relative to nominal value)

Power Supply Range (VDD), V	Temperature Range					
	+25 °C		0 °C ... +85 °C		-40 °C ... +85 °C	
	Error (% at Minimum)	Error (% at Maximum)	Error (% at Minimum)	Error (% at Maximum)	Error (% at Minimum)	Error (% at Maximum)
1.8 V ±5%	-4.71%	3.38%	-8.67%	6.10%	-11.90%	10.61%
3.3 V ±10%	-3.15%	3.26%	-7.74%	7.02%	-12.66%	9.56%
5 V ±10%	-6.10%	13.35%	-9.23%	14.73%	-15.45%	14.73%
2.5 V - 4.5 V	-6.36%	5.73%	-10.70%	9.37%	-12.95%	9.56%
1.71 V….5.5 V	-15.50%	18.84%	-18.85%	19.72%	-18.85%	19.72%

5.10.3 OSC Power On Delay

Table 10. Oscillators Power On delay at room temperature, RC OSC power setting, "Auto Power On"

Power Supply Range (VDD), V	2 MHz		2 MHz Fast start-up mode		25 kHz		25 kHz Fast start-up mode	
	Typ., ns	Max., ns	Typ., ns	Max., ns	Typ., µs	Max., µs	Typ., µs	Max., µs
1.71	108	376.4	60	306.7	0.14	41.10	0.43	41.33
1.80	95	351.6	53	291.3	0.12	41.31	0.41	41.23
1.89	83	332.0	46	278.5	0.11	41.04	0.40	41.18
2.30	53	279.0	30	244.0	0.07	41.18	0.34	41.28
2.50	44	265.1	24	234.9	0.06	41.12	0.33	40.93
2.70	38	254.3	21	227.9	0.05	41.24	2.78	41.17
3.00	31	243.5	17	220.5	0.04	41.30	8.73	41.06
3.30	26	235.8	14	215.4	0.04	41.31	11.30	41.19
3.60	23	230.5	13	211.8	0.03	41.19	16.55	41.40
4.20	16	224.3	7	207.8	0.02	41.27	19.65	41.31
4.50	14	223.1	5	206.9	0.41	41.27	19.64	41.20
5.00	12	230.1	5	211.3	1.25	41.25	19.60	41.19
5.50	10	228.1	4	212.0	1.32	41.25	19.54	40.99

6.0 Summary of Macrocell Function

6.1 I/O Pins

- Digital Input (low voltage or normal voltage, with or without Schmitt Trigger)
- Open Drain Outputs (NMOS and PMOS, 1X and 2X)
- Push Pull Outputs (1X and 2X)
- 10 kΩ/100 kΩ/1 MΩ pull-up/pull-down resistors
- Pins 4 and 8 can be configured as bidirectional IO

6.2 Connection Matrix

- Digital matrix for circuit connections based on user design

6.3 Combinational Logic Look Up Tables (LUTs – 4 total)

- Two 2-bit Lookup Tables
- Two 3-bit Lookup Tables

6.4 Combination Function Macrocells (7 total)

- Two Selectable DFF/Latch or 2-bit LUTs
- Two Selectable DFF/Latch or 3-bit LUTs
- One Selectable Pipe Delay or 3-bit LUT
- One Selectable CNT/DLY or 4-bit LUT
- One Programmable Delay or Deglitch Filter

6.5 Delays/Counters (3 total)

- Three 8-bit delays/counters with external clock/reset: Range 1-255 clock cycles

6.6 Pipe Delay (Part of Combination Function Macrocell)

- 8 stage / 2 output
- Two 1 to 8 stage selectable outputs

6.7 Programmable Delay

- 140 ns/280 ns/420 ns/560 ns @ VDD = 3.3 V
- Includes Edge Detection function

6.8 Additional Logic Functions (Part of Combination Function Macrocell)

- One Deglitch filter macrocell

6.9 RC Oscillator

- 25 kHz or 2 MHz selectable frequency
- First Stage Clock pre-divider: OSC/1, OSC/2, OSC/4, and OSC/8
- Second stage divider control with two outputs, OUT0 and OUT1: selectable (OSC/1, OSC/2, OSC/3, OSC/4, OSC/8, OSC/12, OSC/24, or OSC/64)

6.10 Power On Reset (POR)

7.0 I/O Pins

The SLG46108 has a total of multi-function I/O pins which can function as either a user defined Input. Refer to Section *2.0 Pin Description* for pin definitions.

Of the 6 user defined I/O pins on the SLG46108, all but one of the pins (Pin 2) can serve as both digital input and digital output. Pin 2 can only serve as a digital input pin.

7.1 Input Modes

Each I/O pin can be configured as a digital input pin with/without buffered Schmitt trigger, or can also be configured as a low voltage digital input.

7.2 Output Modes

Pins 3, 4, 6, 7, and 8 can all be configured as digital output pins.

7.3 Pull Up/Down Resistors

All I/O pins have the option for user selectable resistors connected to the input structure. The selectable values on these resistors are 10 kΩ, 100 kΩ and 1 MΩ. In the case of Pin 2, the resistors are fixed to a pull-down configuration. In the case of all other I/O pins, the internal resistors can be configured as either pull-up or pull-downs.

7.4 I/O Register Settings

7.4.1 PIN 2 Register Settings

Table 11. PIN 2 Register Settings

Signal Function	Register Bit Address	Register Definition
PIN 2 Mode Control	reg <350:349>	00: Digital Input without Schmitt trigger 01: Digital Input with Schmitt trigger 10: Low voltage digital input 11: Reserved
PIN 2 Pull Down Resistor Value Selection	reg <352:351>	00: Floating 01: 10 kΩ Resistor 10: 100 kΩ Resistor 11: 1 MΩ Resistor

7.4.2 PIN 3 Register Settings

Table 12. PIN 3 Register Settings

Signal Function	Register Bit Address	Register Definition
PIN 3 Mode Control	reg <355:353>	000: Digital Input without Schmitt trigger 001: Digital Input with Schmitt trigger 010: Low voltage digital input 011: Reserved 100: Push Pull 101: Open Drain NMOS 110: Open Drain PMOS 111: Reserved
PIN 3 Pull Up/Down Resistor Value Selection	reg <357:356>	00: Floating 01: 10 kΩ Resistor 10: 100 kΩ Resistor 11: 1 MΩ Resistor
PIN 3 Pull Up/Down Resistor Selection	reg <358>	0: Pull Down Resistor 1: Pull Up Resistor
PIN3 Driver Strength Selection	reg <359>	0: 1X 1: 2X

7.4.3 PIN 4 Register Settings

Table 13. PIN 4 Register Settings

Signal Function	Register Bit Address	Register Definition
PIN 4 Mode Control (sig_PIN4_oe=0)	reg <361:360>	00: Digital Input without Schmitt trigger 01: Digital Input with Schmitt trigger 11: Low Voltage Digital Input 10: Reserved
PIN 4 Mode Control (sig_PIN4_oe =1)	reg <363:362>	00: Push Pull 1X 01: Push Pull 2X 10: Open Drain NMOS 1X 11: Open Drain NMOS 2X
PIN 4 Pull Up/Down Resistor Value Selection	reg <365:364>	00: Floating 01: 10 kΩ Resistor 10: 100 kΩ Resistor 11: 1 MΩ Resistor
PIN 4 Pull Up/Down Resistor Selection	reg <366>	0: Pull Down Resistor 1: Pull Up Resistor

7.4.4 PIN 6 Register Settings

Table 14. PIN 6 Register Settings

Signal Function	Register Bit Address	Register Definition
PIN 6 Mode Control	reg <370:368>	000: Digital Input without Schmitt trigger 001: Digital Input with Schmitt trigger 010: Low voltage digital input 011: Reserved 100: Push Pull 101: Open Drain NMOS 110: Open Drain PMOS 111: Reserved
PIN 6 Pull Up/Down Resistor Value Selection	reg <372:371>	00: Floating 01: 10 kΩ Resistor 10: 100 kΩ Resistor 11: 1 MΩ Resistor
PIN 6 Pull Up/Down Resistor Value Selection	reg <373>	0: Pull Down Resistor 1: Pull Up Resistor
PIN 6 Pull Up/Down Resistor Selection	reg <374>	0: 1X 1: 2X

7.4.5 PIN 7 Register Settings

Table 15. PIN 7 Register Settings

Signal Function	Register Bit Address	Register Definition
PIN 7 Mode Control	reg <377:375>	000: Digital Input without Schmitt trigger 001: Digital Input with Schmitt trigger 010: Low voltage digital input 011: Reserved 100: Push Pull 101: Open Drain NMOS 110: Open Drain PMOS 111: Reserved
PIN 7 Pull Up/Down Resistor Value Selection	reg <379:378>	00: Floating 01: 10 kΩ Resistor 10: 100 kΩ Resistor 11: 1 MΩ Resistor
PIN 7 Pull Up/Down Resistor Selection	reg <380>	0: Pull Down Resistor 1: Pull Up Resistor
PIN 7 Driver Strength Selection	reg <381>	0: 1X 1: 2X

7.4.6 PIN 8 Register Settings

Table 16. PIN 8 Register Settings

Signal Function	Register Bit Address	Register Definition
PIN 8 Mode Control (sig_PIN8_oe=0)	reg <383:382>	00: Digital Input without Schmitt trigger 01: Digital Input with Schmitt trigger 11: Low Voltage Digital Input 10: Reserved
PIN 8 Mode Control (sig_PIN8_oe =1)	reg <385:384>	00: Push Pull 1X 01: Push Pull 2X 10: Open Drain NMOS 1X 11: Open Drain NMOS 2X
PIN 8 Pull Up/Down Resistor Value Selection	reg <387:386>	00: Floating 01: 10 kΩ Resistor 10: 100 kΩ Resistor 11: 1 MΩ Resistor
PIN 8 Pull Up/Down Resistor Selection	reg <388>	0: Pull Down Resistor 1: Pull Up Resistor

7.5 GPI IO Structure

7.5.1 GPI IO Structure (for Pin 2)

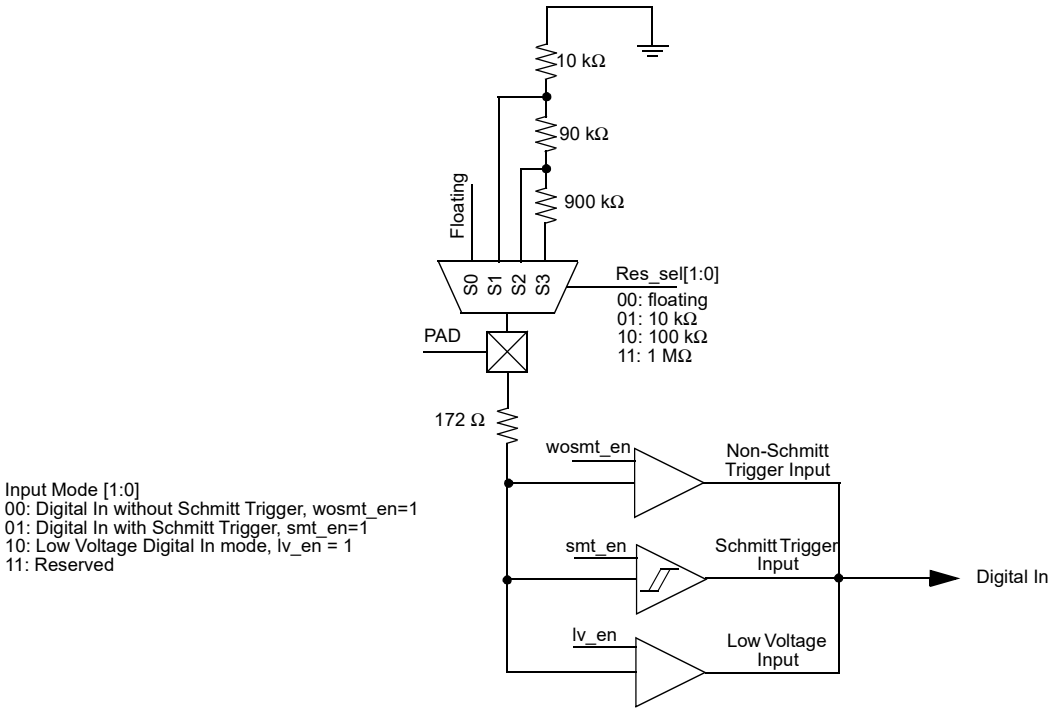


Figure 2. PIN 2 GPI IO Structure Diagram

7.6 Matrix OE IO Structure

7.6.1 Matrix OE IO Structure (for Pin 4, 8)

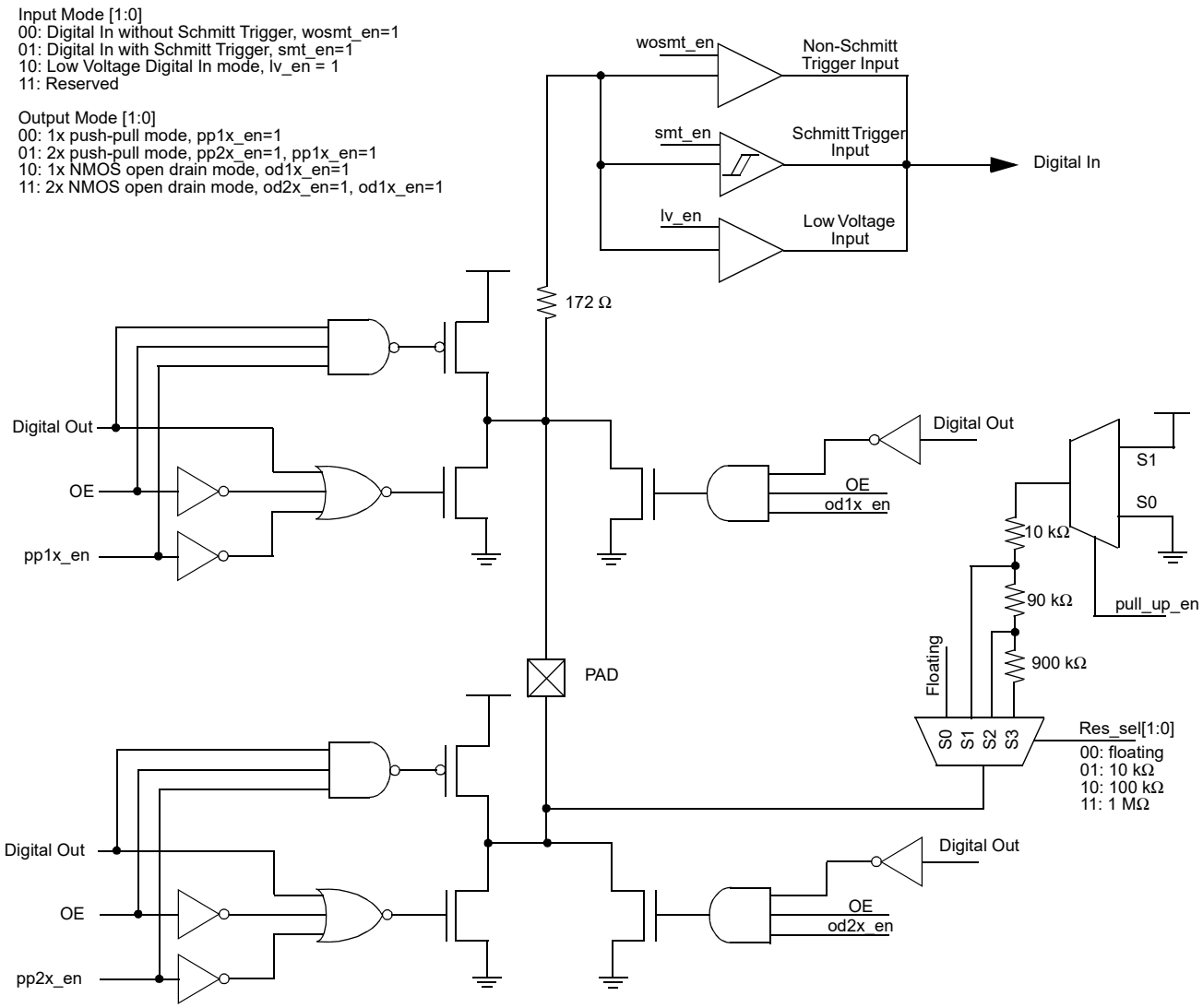


Figure 3. Matrix OE IO Structure Diagram

7.7 Register OE IO Structure

7.7.1 Register OE IO Structure (for Pins 3, 6, 7)

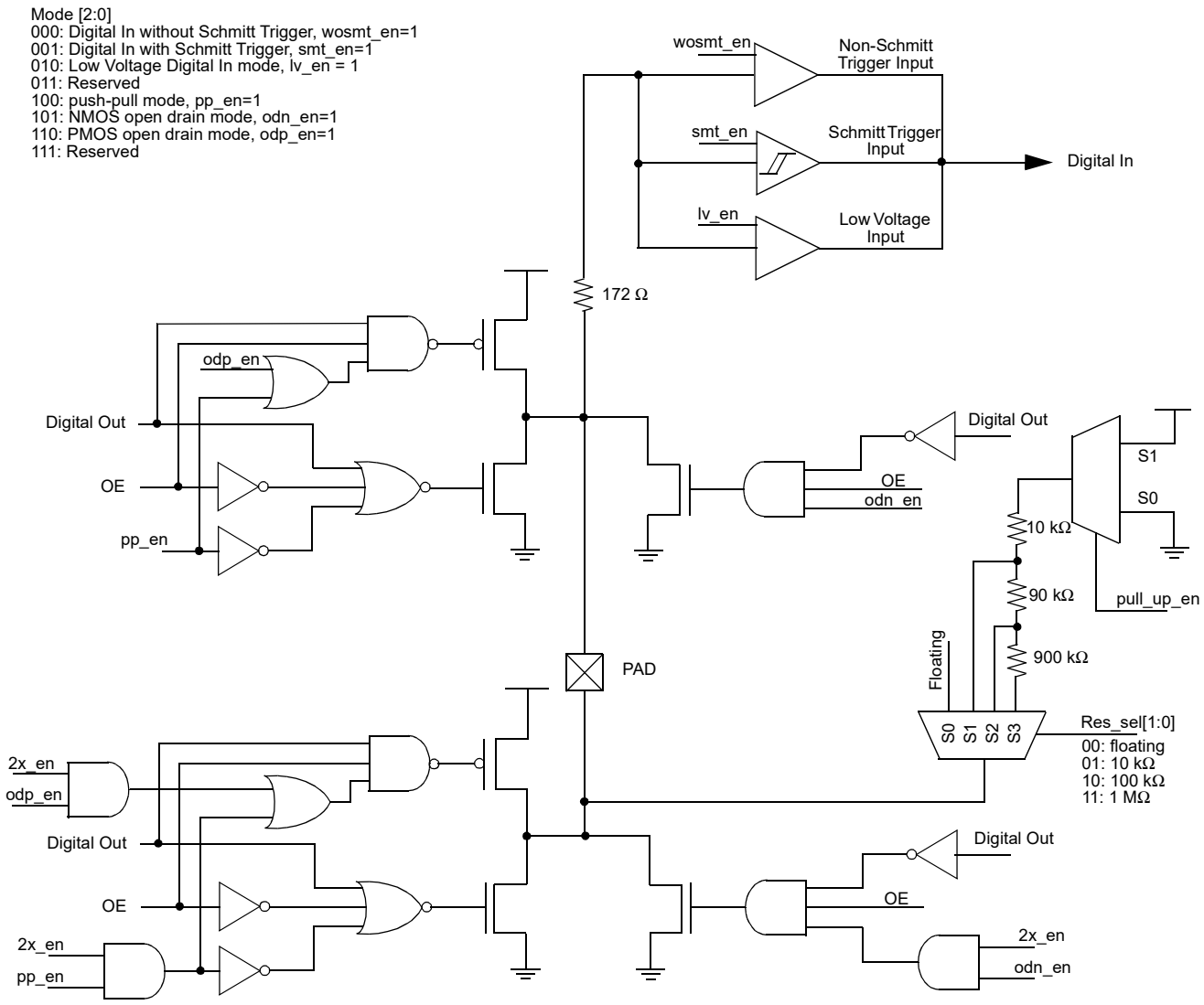


Figure 4. Register OE IO Structure Diagram

8.0 Connection Matrix

The Connection Matrix in the SLG46108 is used to create the internal routing for internal functions of the device once it is programmed. The registers are programmed from the one-time NVM cell during Test Mode Operation. All of the connection point for each logic cell within the SLG46108 has a specific digital bit code assigned to it that is either set to active “High” or inactive “Low” based on the design that is created. Once the 463 register bits within the SLG46108 are programmed a fully custom circuit will be created.

The Connection Matrix has 32 inputs and 40 outputs. Each of the 32 inputs to the Connection Matrix is hard-wired to a particular source macrocell, including I/O pins, LUTs, other digital resources, and V_{DD} and V_{SS}. The input to a digital macrocell uses a 5-bit register to select one of these 32 input lines.

For a complete list of the SLG46108’s register table, see Section *14.0 Appendix A - SLG46108 Register Definition*.

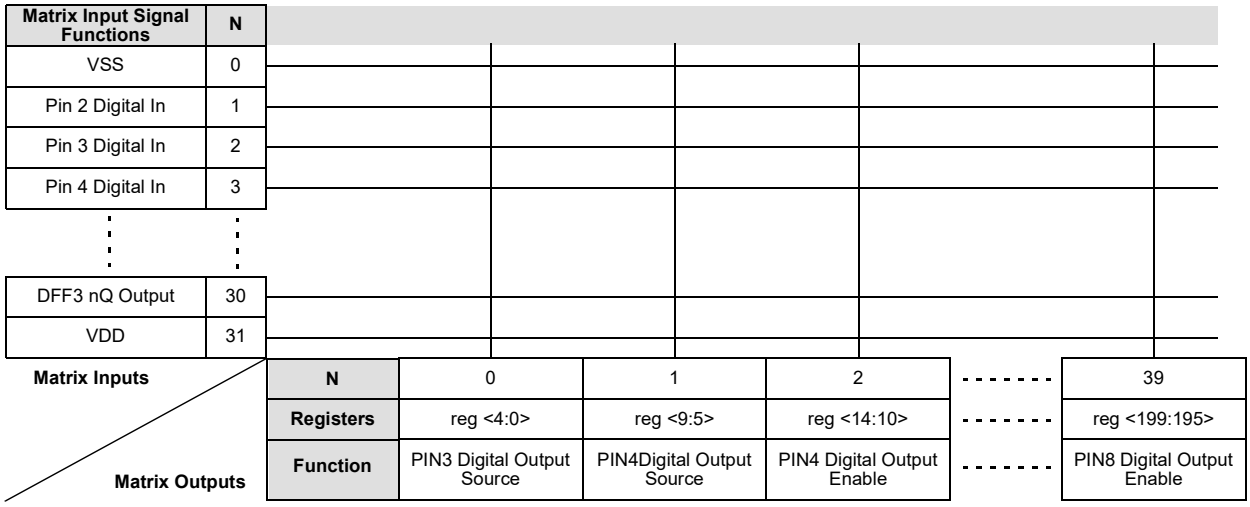


Figure 5. Connection Matrix

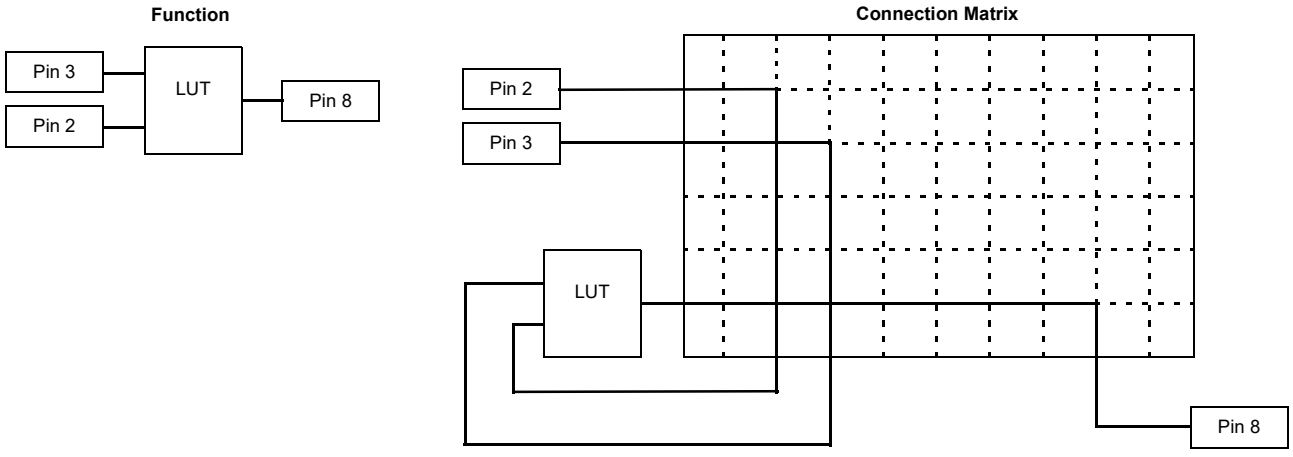


Figure 6. Connection Matrix Example