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SLG46116

GreenPAK Programmable Mixed-signal Matrix with P-FET Power Switch w/o Discharge

General Description

The SLG46116 GreenPAK combines the functionality and versatility of a GreenPAK Programmable Mixed-signal Matrix with the capabilities of Silego's CuFET technology. Capable of integrating a number common discrete ICs and passive components into a single device, the GreenPAK family's SLG46116V enables high power switching with a soft-start 1.25 A P-Ch MOSFET with slew rate control.

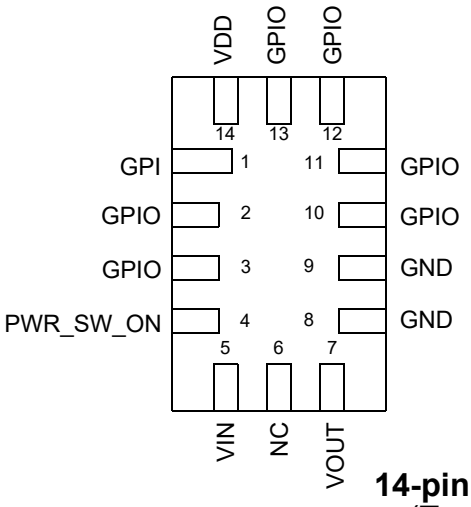
Features

- Logic & Mixed Signal Circuits
- Highly Versatile Macrocells
- Read Back Protection (Read Lock)
- 1.8V (±5%) to 5V (±10%) Supply
- Operating Temperature Range -40 °C to 85 °C
- Soft-Start 1.25 A P-FET Power Switch
- Package
  - 1.6 x 2.5 x 0.55 mm STQFN 14L package
  - Pb-Free / Halogen-Free / RoHS compliant

Applications

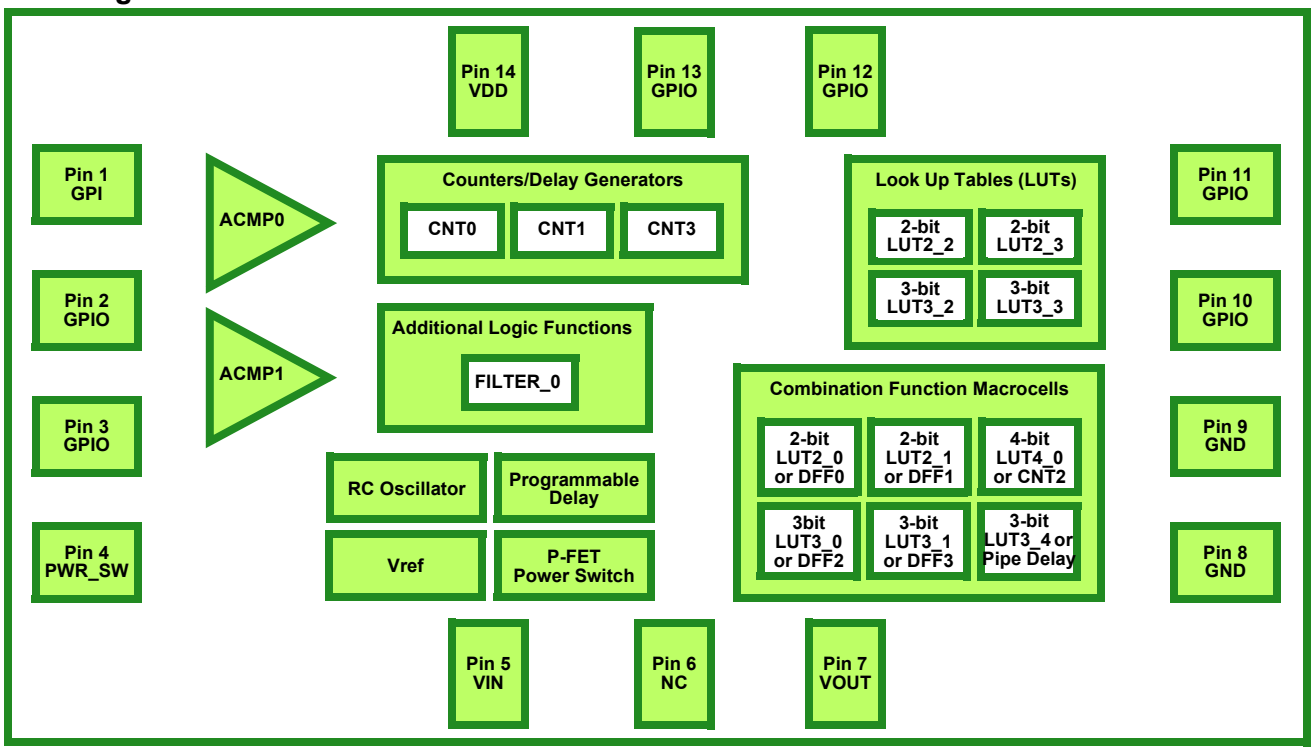
- Power Sequencing with complex analog control
- Power Plane component size reduction project
- LED Driver
- Haptic Motor Driver
- System RESET with Power Switch

Pin Configuration



14-pin STQFN
(Top View)

Block Diagram



1.0 Overview

The SLG46116 provides a small, low power component for commonly used mixed-signal functions. The user creates their circuit design by programming the one time Non-Volatile Memory (NVM) to configure the interconnect logic, the I/O Pins and the macrocells of the SLG46116. This highly versatile device allows a wide variety of mixed-signal functions to be designed within a very small, low power single integrated circuit. The SLG46116 includes the following:

- Two Analog Comparators (ACMP)
- Voltage References (Vref)
- Four Combinatorial Look Up Tables (LUTs)
  - Two 2-bit LUTs
  - Two 3-bit LUTs
- Seven Combination Function Macrocell
  - Two Selectable DFF/Latch or 2-bit LUTs
  - Two Selectable DFF/Latch or 3-bit LUTs
  - One Selectable Pipe Delay or 3-bit LUT
    - Pipe Delay – 8 stage / 2 output
  - One Selectable Counter/Delay or 4-bit LUT
  - One Programmable Delay/ Deglitch Filter
- Three Counter / Delay Generators (CNT/DLY)
  - Three 8-bit counter/delays with external clock/reset
- Four D Flip-Flop / Latches (DFF) (Part of Combination Function Macrocell)
- Pipe Delay – 8 stage/2 output (Part of Combination Function Macrocell)
- Trimmed RC Oscillator (RC OSC)
- Power On Reset (POR)
- One Bandgap
- Soft-Start P-FET Power Switch
  - Power Switch IDS: 1.25 A
  - Slew Rate Control
  - VIN: 1.5 V to 5.5 V
  - Low RDSON
    - 28.5 mΩ @ 5.0 V
    - 36.4 mΩ @ 3.3 V
    - 44.3 mΩ @ 2.5 V
    - 60.8 mΩ @ 1.8 V
    - 77.6 mΩ @ 1.5 V

2.0 Pin Description

2.1 Functional Pin Description

Pin #	Pin Name	Function
1	GPI	General Purpose Input
2	GPIO	General Purpose I/O or Analog Comparator 0 (+)
3	GPIO	General Purpose I/O or Analog Comparator 0 (-)
4	PWR_SW_ON	Input/Output
5	VIN	P-FET Power Switch Input
6	NC	No Connect
7	VOUT	P-FET Power Switch Output
8	GND	Ground
9	GND	Ground
10	GPIO	General Purpose I/O
11	GPIO	General Purpose I/O or POR Output
12	GPIO	General Purpose I/O with OE and Vref output
13	GPIO	General Purpose I/O or External Clock Input
14	VDD	Power Supply

3.0 User Programmability

Non-volatile memory (NVM) is used to configure the SLG46116's connection matrix routing and macrocells. The NVM is One-Time-Programmable (OTP). However, Silego's GreenPAK development tools can be used to configure the connection matrix and macrocells, without programming the NVM, to allow on-chip emulation. This configuration will remain active on the device as long as it remains powered and can be re-written as needed to facilitate rapid design changes.

When a design is ready for in-circuit testing, the same GreenPAK development tools can be used to program the NVM and create samples for small quantity builds. Once the NVM is programmed, the device will retain this configuration for the duration of its lifetime.

Once the design is finalized, the design file can be forwarded to Silego to integrate into the production process.

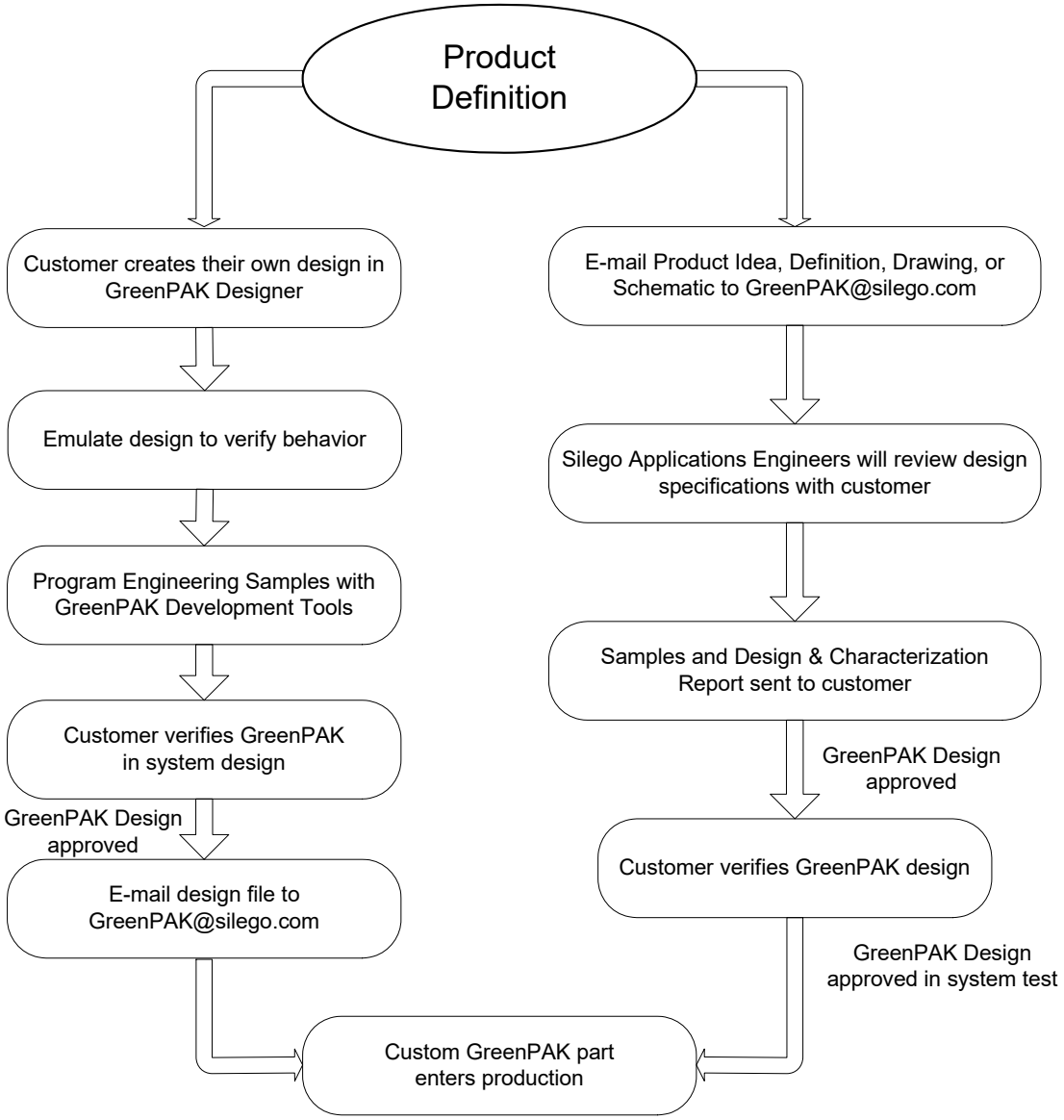


Figure 1. Steps to create a custom Silego GreenPAK device

4.0 Ordering Information

Part Number	Type
SLG46116V	STQFN 14L
SLG46116VTR	STQFN 14L - Tape and Reel (3k units)

5.0 Electrical Specifications

5.1 Absolute Maximum Conditions

Parameter	Condition	Min.	Max.	Unit
Supply voltage on VDD relative to GND		-0.5	7	V
DC Input voltage		GND - 0.5	VDD + 0.5	V
Maximum Average or DC Current (Through pin)	Push-Pull 1x	--	12	mA
	Push-Pull 2x	--	17	
	OD 1x	--	18	
	OD 2x	--	28	
Current at Input Pin		-1.0	1.0	mA
Storage Temperature Range		-65	150	°C
Junction Temperature		--	150	°C
ESD Protection (Human Body Model)		2000	--	V
ESD Protection (Charged Device Model)		1000	--	V
Moisture Sensitivity Level		1		
P-FET Power Switch IDS_{PK}	For no more than 1 ms with 1% duty cycle	--	1.5	A

5.2 Electrical Characteristics (1.8V ±5% V_{DD})

Symbol	Parameter	Condition/Note	Min.	Typ.	Max.	Unit
V_{DD}	Supply Voltage		1.71	1.80	1.89	V
I_Q	Quiescent Current	Static Inputs and Outputs	--	0.5	--	µA
T_A	Operating Temperature		-40	25	85	°C
V_{PP}	Programming Voltage		7.25	7.50	7.75	V
V_{AIR}	Analog Input Voltage Range	Positive Input	0	--	V_{DD}	V
		Negative Input	0	--	1.1	V
V_{IH}	HIGH-Level Input Voltage	Logic Input	1.100	--	V_{DD}	V
		Logic Input with Schmitt Trigger	1.270	--	V_{DD}	V
		Low-Level Logic Input	0.980	--	V_{DD}	V
V_{IL}	LOW-Level Input Voltage	Logic Input	--	--	0.690	V
		Logic Input with Schmitt Trigger	--	--	0.440	V
		Low-Level Logic Input	--	--	0.520	V
I_{IH}	HIGH-Level Input Current	Logic Input Pins; V_{IN} = 1.8 V	-1.0	--	1.0	µA
I_{IL}	LOW-Level Input Current	Logic Input Pins; V_{IN} = 0 V	-1.0	--	1.0	µA
V_{OH}	HIGH-Level Output Voltage	Push-Pull 1X, Open Drain PMOS 1X, I_{OH} = 100 µA	1.680	1.790	--	V
		Push-Pull 2X, Open Drain PMOS 2X, I_{OH} = 100 µA	1.702	1.800	--	V

Symbol	Parameter	Condition/Note	Min.	Typ.	Max.	Unit
V_{OL}	LOW-Level Output Voltage	Push-Pull 1X, I_{OL}= 100 µA	--	0.020	0.030	V
		Push-Pull 2X, I_{OL}= 100 µA	--	0.010	0.020	V
		Open Drain NMOS 1X, I_{OL}= 100 µA	--	0.010	0.020	V
		Open Drain NMOS 2X, I_{OL}= 100 µA	--	0.010	0.010	V
I_{OH}	HIGH-Level Output Current (see Note 1)	Push-Pull 1X, Open Drain PMOS 1X, $V_{OH} = V_{DD}$ - 0.2	1.040	1.400	--	mA
		Push-Pull 2X, Open Drain PMOS 2X, $V_{OH} = V_{DD}$ - 0.2	2.150	2.710	--	mA
I_{OL}	LOW-Level Output Current (see Note 1)	Push-Pull 1X, V_{OL} = 0.15 V	0.760	1.340	--	mA
		Push-Pull 2X, V_{OL} = 0.15 V	1.520	2.660	--	mA
		Open Drain NMOS 1X, V_{OL} = 0.15 V	1.530	2.670	--	mA
		Open Drain NMOS 2X, V_{OL} = 0.15 V	3.060	5.130	--	mA
I_{VDD}	Maximum Average or DC Current Through VDD Pin (Per chip side, see Note 2)	T_J = 85°C	--	--	73	mA
		T_J = 110°C	--	--	35	mA
I_{GND}	Maximum Average or DC Current Through GND Pin (Per chip side, see Note 2)	T_J = 85°C	--	--	92	mA
		T_J = 110°C	--	--	44	mA
T_{SU}	Startup Time	from VDD rising past 1.35 V	--	0.27	--	ms
PON_{THR}	Power On Threshold	V_{DD} Level Required to Start Up the Chip	1.182	1.346	1.505	V
$POFF_{THR}$	Power Off Threshold	V_{DD} Level Required to Switch Off the Chip	0.752	0.918	1.110	V
V_{IN}	Power Switch Input Voltage	-40 °C to 85 °C	1.5	--	5.0	V
I_{IN}	Power Switch Current (PIN 5)	when Off, V_{IN} = 5.0 V	--	0.02	0.1	µA
		when PWR_SW_ON = V_{IN}, No load	--	0.05	0.5	µA
I_{DS_LKG}	Leakage Measured from PIN 5 to PIN 7	when Off, V_{IN} = 5.0 V	--	0.05	1	µA
I_{ON_LKG}	PWR_SW_ON Pin Input Leakage		--	--	0.1	µA
RDS_{ON}	Static Drain to Source ON Resistance @ T_A 25°C	@ V_{IN} = 5.5 V	--	28.5	32.0	mΩ
		@ V_{IN} = 3.3 V	--	36.4	40.0	mΩ
		@ V_{IN} = 2.5 V	--	44.3	49.0	mΩ
		@ V_{IN} = 1.8 V	--	60.8	65.0	mΩ
		@ V_{IN} = 1.5 V	--	77.6	82.0	mΩ

Symbol	Parameter	Condition/Note	Min.	Typ.	Max.	Unit
RDS_{ON}	Static Drain to Source ON Resistance @ T_A 85°C	@ V_{IN} = 5.5 V	--	34.0	36.0	mΩ
		@ V_{IN} = 3.3 V	--	43.8	46.0	mΩ
		@ V_{IN} = 2.5 V	--	53.3	56.0	mΩ
		@ V_{IN} = 1.8 V	--	72.2	76.0	mΩ
		@ V_{IN} = 1.5 V	--	90.7	94.0	mΩ
IDS	Operating Current	V_{IN} = 1.5 V to 5.0 V	--	--	1.25	A
T_{On_Delay}	PWR_SW_ON pin Delay Time	50% PWR_SW_ON to Ramp Begin, V_{IN} = 5 V, VOUT_Cap = 0.1 µF, R_L = 10 Ω	12.0	15.0	18.5	µs
		50% PWR_SW_ON to Ramp Begin, V_{IN} = 3.3 V, VOUT_Cap = 0.1 µF, R_L = 10 Ω	17.0	22.0	30.0	µs
		50% PWR_SW_ON to Ramp Begin, V_{IN} = 1.5 V, VOUT_Cap = 0.1 µF, R_L = 10 Ω	44.0	55.0	76.0	µs
T_{Total_On}	Total Turn On Time	50% PWR_SW_ON to 90% VOUT, V_{IN} = 5 V, VOUT_Cap = 0.1 µF, R_L = 10 Ω	114	122	134	µs
		50% PWR_SW_ON to 90% VOUT, V_{IN} = 3.3 V, VOUT_Cap = 0.1 µF, R_L = 10 Ω	146	156	176	µs
		50% PWR_SW_ON to 90% VOUT, V_{IN} = 1.5 V, VOUT_Cap = 0.1 µF, R_L = 10 Ω	292	332	399	µs
T_{RISE}	Rise Time	10% VOUT to 90% VOUT, V_{IN} = 5.0 V, VOUT_Cap = 0.1 µF, R_L = 10 Ω	92	97	107	µs
		10% VOUT to 90% VOUT, V_{IN} = 3.3 V, VOUT_Cap = 0.1 µF, R_L = 10 Ω	116	120	131	µs
		10% VOUT to 90% VOUT, V_{IN} = 1.5 V, VOUT_Cap = 0.1 µF, R_L = 10 Ω	228	253	296	µs
PWR_SW_ON_V_{IH}	Initial Turn On Voltage		0.85	--	V_{IN} or V_{DD}	V
PWR_SW_ON_V_{IL}	Low Input Voltage on PWR_SW_ON pin		-0.3	0	0.3	V
T_{Delay_Off}	Off Delay Time	50% PWR_SW_ON to VOUT Fall, V_{IN} = 5 V, R_L =10 Ω	6.2	6.5	7.0	µs

Note 1: DC or average current through any pin should not exceed value given in Absolute Maximum Conditions.
Note 2: The GreenPAK's power rails are divided in two sides. Pins 1, 2 and 3 are connected to one side, pins 10, 11, 12 and 13 to another.

5.3 Electrical Characteristics (3.3V ±10% V_{DD})

Symbol	Parameter	Condition/Note	Min.	Typ.	Max.	Unit
V_{DD}	Supply Voltage		3.0	3.3	3.6	V
I_Q	Quiescent Current	Static Inputs and Outputs	--	0.75	--	µA
T_A	Operating Temperature		-40	25	85	°C
V_{PP}	Programming Voltage		7.25	7.50	7.75	V
V_{AIR}	Analog Input Voltage Range	Positive Input	0	--	V_{DD}	V
		Negative Input	0	--	1.2	V
V_{IH}	HIGH-Level Input Voltage	Logic Input	1.780	--	V_{DD}	V
		Logic Input with Schmitt Trigger	2.130	--	V_{DD}	V
		Low-Level Logic Input	1.130	--	V_{DD}	V
V_{IL}	LOW-Level Input Voltage	Logic Input	--	--	1.210	V
		Logic Input with Schmitt Trigger	--	--	0.950	V
		Low-Level Logic Input	--	--	0.690	V
I_{IH}	HIGH-Level Input Current	Logic Input Pins; V_{IN} = 3.3 V	-1.0	--	1.0	µA
I_{IL}	LOW-Level Input Current	Logic Input Pins; V_{IN} = 0 V	-1.0	--	1.0	µA
V_{OH}	HIGH-Level Output Voltage	Push-Pull 1X,Open Drain PMOS 1X, I_{OH} = 3 mA	2.710	3.090	--	V
		Push-Pull 2X, Open Drain PMOS 2X, I_{OH} = 3 mA	2.870	3.190	--	V
V_{OL}	LOW-Level Output Voltage	Push-Pull 1X, I_{OL}= 3 mA	--	0.180	0.280	V
		Push-Pull 2X, I_{OL}= 3 mA	--	0.090	0.130	V
		Open Drain NMOS 1X, I_{OL}= 3 mA	--	0.090	0.130	V
		Open Drain NMOS 2X, I_{OL}= 3 mA	--	0.050	0.070	V
I_{OH}	HIGH-Level Output Current (see Note 1)	Push-Pull 1X, Open Drain PMOS 1X, V_{OH} = 2.4 V	5.830	10.180	--	mA
		Push-Pull 2X, Open Drain PMOS 2X, V_{OH} = 2.4 V	11.264	19.660	--	mA
I_{OL}	LOW-Level Output Current (see Note 1)	Push-Pull 1X, V_{OL} = 0.4 V	4.060	6.440	--	mA
		Push-Pull 2X, V_{OL} = 0.4 V	8.130	12.360	--	mA
		Open Drain NMOS 1X, V_{OL} = 0.4 V	8.130	12.410	--	mA
		Open Drain NMOS 2X, V_{OL} = 0.4 V	16.260	22.900	--	mA
I_{VDD}	Maximum Average or DC Current Through VDD Pin (Per chip side, see Note 2)	T_J = 85°C	--	--	73	mA
		T_J = 110°C	--	--	35	mA
I_{GND}	Maximum Average or DC Current Through GND Pin (Per chip side, see Note 2)	T_J = 85°C	--	--	92	mA
		T_J = 110°C	--	--	44	mA
T_{SU}	Startup Time	from VDD rising past 1.35 V	--	0.27	-	ms

Symbol	Parameter	Condition/Note	Min.	Typ.	Max.	Unit
PON_{THR}	Power On Threshold	V_{DD} Level Required to Start Up the Chip	1.182	1.346	1.505	V
$POFF_{THR}$	Power Off Threshold	V_{DD} Level Required to Switch Off the Chip	0.752	0.918	1.110	V
V_{IN}	Power Switch Input Voltage	-40 °C to 85 °C	1.5	--	5.0	V
I_{IN}	Power Switch Current (PIN 5)	when Off, V_{IN} = 5.0 V	--	0.02	0.1	µA
		when PWR_SW_ON = V_{IN}, No load	--	0.05	0.5	µA
I_{DS_LKG}	Leakage Measured from PIN 5 to PIN 7	when Off, V_{IN} = 5.0 V	--	0.05	1	µA
I_{ON_LKG}	PWR_SW_ON Pin Input Leakage		--	--	0.1	µA
RDS_{ON}	Static Drain to Source ON Resistance @ T_A 25°C	@ V_{IN} = 5.5 V	--	28.5	32.0	mΩ
		@ V_{IN} = 3.3 V	--	36.4	40.0	mΩ
		@ V_{IN} = 2.5 V	--	44.3	49.0	mΩ
		@ V_{IN} = 1.8 V	--	60.8	65.0	mΩ
		@ V_{IN} = 1.5 V	--	77.6	82.0	mΩ
RDS_{ON}	Static Drain to Source ON Resistance @ T_A 85°C	@ V_{IN} = 5.5 V	--	34.0	36.0	mΩ
		@ V_{IN} = 3.3 V	--	43.8	46.0	mΩ
		@ V_{IN} = 2.5 V	--	53.3	56.0	mΩ
		@ V_{IN} = 1.8 V	--	72.2	76.0	mΩ
		@ V_{IN} = 1.5 V	--	90.7	94.0	mΩ
IDS	Operating Current	V_{IN} = 1.5 V to 5.0 V	--	--	1.25	A
T_{On_Delay}	PWR_SW_ON pin Delay Time	50% PWR_SW_ON to Ramp Begin, V_{IN} = 5 V, VOUT_Cap = 0.1 µF, R_L = 10 Ω	12.0	15.0	18.5	µs
		50% PWR_SW_ON to Ramp Begin, V_{IN} = 3.3 V, VOUT_Cap = 0.1 µF, R_L = 10 Ω	17.0	22.0	30.0	µs
		50% PWR_SW_ON to Ramp Begin, V_{IN} = 1.5 V, VOUT_Cap = 0.1 µF, R_L = 10 Ω	44.0	55.0	76.0	µs
T_{Total_On}	Total Turn On Time	50% PWR_SW_ON to 90% VOUT, V_{IN} = 5 V, VOUT_Cap = 0.1 µF, R_L = 10 Ω	114	122	134	µs
		50% PWR_SW_ON to 90% VOUT, V_{IN} = 3.3 V, VOUT_Cap = 0.1 µF, R_L = 10 Ω	146	156	176	µs
		50% PWR_SW_ON to 90% VOUT, V_{IN} = 1.5 V, VOUT_Cap = 0.1 µF, R_L = 10 Ω	292	332	399	µs
T_{RISE}	Rise Time	10% VOUT to 90% VOUT V_{IN} = 5.0 V, VOUT_Cap = 0.1 µF, R_L = 10 Ω	92	97	107	µs
		10% VOUT to 90% VOUT V_{IN} = 3.3 V, VOUT_Cap = 0.1 µF, R_L = 10 Ω	116	120	131	µs
		10% VOUT to 90% VOUT V_{IN} = 1.5 V, VOUT_Cap = 0.1 µF, R_L = 10 Ω	228	253	296	µs

Symbol	Parameter	Condition/Note	Min.	Typ.	Max.	Unit
PWR_SW_ON_V_{IH}	Initial Turn On Voltage		0.85	--	V_{IN} or V_{DD}	V
PWR_SW_ON_V_{IL}	Low Input Voltage on PWR_SW_ON pin		-0.3	0	0.3	V
T_{Delay_Off}	Off Delay Time	50% PWR_SW_ON to VOUT Fall, V_{IN} = 5 V, R_L =10 Ω	6.2	6.5	7.0	µs

Note 1: DC or average current through any pin should not exceed value given in Absolute Maximum Conditions.
Note 2: The GreenPAK's power rails are divided in two sides. Pins 1, 2 and 3 are connected to one side, pins 10, 11, 12 and 13 to another.

5.4 Electrical Characteristics (5V ±10% V_{DD})

Symbol	Parameter	Condition/Note	Min.	Typ.	Max.	Unit
V_{DD}	Supply Voltage		4.5	5.0	5.5	V
I_Q	Quiescent Current	Static Inputs and Outputs	--	1.0	--	µA
T_A	Operating Temperature		-40	25	85	°C
V_{PP}	Programming Voltage		7.25	7.50	7.75	V
V_{AIR}	Analog Input Voltage Range	Positive Input	0	--	V_{DD}	V
		Negative Input	0	--	1.2	V
V_{IH}	HIGH-Level Input Voltage	Logic Input	2.640	--	V_{DD}	V
		Logic Input with Schmitt Trigger	3.160	--	V_{DD}	V
		Low-Level Logic Input	1.230	--	V_{DD}	V
V_{IL}	LOW-Level Input Voltage	Logic Input	--	--	1.840	V
		Logic Input with Schmitt Trigger	--	--	1.510	V
		Low-Level Logic Input	--	--	0.780	V
I_{IH}	HIGH-Level Input Current	Logic Input Pins; V_{IN} = 5 V	-1.0	--	1.0	µA
I_{IL}	LOW-Level Input Current	Logic Input Pins; V_{IN} = 0 V	-1.0	--	1.0	µA
V_{OH}	HIGH-Level Output Voltage	Push-Pull 1X,Open Drain PMOS 1X, I_{OH} = 5 mA	4.150	4.730	--	V
		Push-Pull 2X, Open Drain PMOS 2X, I_{OH} = 5 mA	4.300	4.860	--	V
V_{OL}	LOW-Level Output Voltage	Push-Pull 1X, I_{OL}= 5 mA	--	0.230	0.330	V
		Push-Pull 2X, I_{OL}= 5 mA	--	0.120	0.160	V
		Open Drain NMOS 1X, I_{OL}= 5 mA	--	0.120	0.160	V
		Open Drain NMOS 2X, I_{OL}= 5 mA	--	0.070	0.090	V
I_{OH}	HIGH-Level Output Current (see Note 1)	Push-Pull 1X, Open Drain PMOS 1X, V_{OH} = 2.4 V	21.808	29.100	--	mA
		Push-Pull 2X, Open Drain PMOS 2X, V_{OH} = 2.4 V	40.598	56.080	--	mA
I_{OL}	LOW-Level Output Current (see Note 1)	Push-Pull 1X, V_{OL} = 0.4 V	6.010	9.730	--	mA
		Push-Pull 2X, V_{OL} = 0.4 V	11.590	19.460	--	mA
		Open Drain NMOS 1X, V_{OL} = 0.4 V	11.760	19.460	--	mA
		Open Drain NMOS 2X, V_{OL} = 0.4 V	19.120	35.621	--	mA
I_{VDD}	Maximum Average or DC Current Through VDD Pin (Per chip side, see Note 2)	T_J = 85°C	--	--	73	mA
		T_J = 110°C	--	--	35	mA
I_{GND}	Maximum Average or DC Current Through GND Pin (Per chip side, see Note 2)	T_J = 85°C	--	--	92	mA
		T_J = 110°C	--	--	44	mA
T_{SU}	Startup Time	from VDD rising past 1.35 V	--	0.27	-	ms

Symbol	Parameter	Condition/Note	Min.	Typ.	Max.	Unit
PON_{THR}	Power On Threshold	V_{DD} Level Required to Start Up the Chip	1.182	1.346	1.505	V
$POFF_{THR}$	Power Off Threshold	V_{DD} Level Required to Switch Off the Chip	0.752	0.918	1.110	V
V_{IN}	Power Switch Input Voltage	-40 °C to 85 °C	1.5	--	5.0	V
I_{IN}	Power Switch Current (PIN 5)	when Off, V_{IN} = 5.0 V	--	0.02	0.1	µA
		when PWR_SW_ON = V_{IN}, No load	--	0.05	0.5	µA
I_{DS_LKG}	Leakage Measured from PIN 5 to PIN 7	when Off, V_{IN} = 5.0 V	--	0.05	1	µA
I_{ON_LKG}	PWR_SW_ON Pin Input Leakage		--	--	0.1	µA
RDS_{ON}	Static Drain to Source ON Resistance @ T_A 25°C	@ V_{IN} = 5.5 V	--	28.5	32.0	mΩ
		@ V_{IN} = 3.3 V	--	36.4	40.0	mΩ
		@ V_{IN} = 2.5 V	--	44.3	49.0	mΩ
		@ V_{IN} = 1.8 V	--	60.8	65.0	mΩ
		@ V_{IN} = 1.5 V	--	77.6	82.0	mΩ
RDS_{ON}	Static Drain to Source ON Resistance @ T_A 85°C	@ V_{IN} = 5.5 V	--	34.0	36.0	mΩ
		@ V_{IN} = 3.3 V	--	43.8	46.0	mΩ
		@ V_{IN} = 2.5 V	--	53.3	56.0	mΩ
		@ V_{IN} = 1.8 V	--	72.2	76.0	mΩ
		@ V_{IN} = 1.5 V	--	90.7	94.0	mΩ
IDS	Operating Current	V_{IN} = 1.5 V to 5.0 V	--	--	1.25	A
T_{On_Delay}	PWR_SW_ON pin Delay Time	50% PWR_SW_ON to Ramp Begin V_{IN} = 5 V, VOUT_Cap = 0.1 µF, R_L = 10 Ω	12.0	15.0	18.5	µs
		50% PWR_SW_ON to Ramp Begin V_{IN} = 3.3 V, VOUT_Cap = 0.1 µF, R_L = 10 Ω	17.0	22.0	30.0	µs
		50% PWR_SW_ON to Ramp Begin V_{IN} = 1.5 V, VOUT_Cap = 0.1 µF, R_L = 10 Ω	44.0	55.0	76.0	µs
T_{Total_On}	Total Turn On Time	50% PWR_SW_ON to 90% VOUT V_{IN} = 5 V, VOUT_Cap = 0.1 µF, R_L = 10 Ω	114	122	134	µs
		50% PWR_SW_ON to 90% VOUT V_{IN} = 3.3 V, VOUT_Cap = 0.1 µF, R_L = 10 Ω	146	156	176	µs
		50% PWR_SW_ON to 90% VOUT V_{IN} = 1.5 V, VOUT_Cap = 0.1 µF, R_L = 10 Ω	292	332	399	µs
T_{RISE}	Rise Time	10% VOUT to 90% VOUT V_{IN} = 5.0 V, VOUT_Cap = 0.1 µF, R_L = 10 Ω	92	97	107	µs
		10% VOUT to 90% VOUT V_{IN} = 3.3 V, VOUT_Cap = 0.1 µF, R_L = 10 Ω	116	120	131	µs
		10% VOUT to 90% VOUT V_{IN} = 1.5 V, VOUT_Cap = 0.1 µF, R_L = 10 Ω	228	253	296	µs

Symbol	Parameter	Condition/Note	Min.	Typ.	Max.	Unit
PWR_SW_ON_V_{IH}	Initial Turn On Voltage		0.85	--	V_{IN} or V_{DD}	V
PWR_SW_ON_V_{IL}	Low Input Voltage on PWR_SW_ON pin		-0.3	0	0.3	V
T_{Delay_Off}	Off Delay Time	50% PWR_SW_ON to VOUT Fall, V_{IN} = 5 V, R_L =10 Ω	6.2	6.5	7.0	µs

Note 1: DC or average current through any pin should not exceed value given in Absolute Maximum Conditions.
Note 2: The GreenPAK's power rails are divided in two sides. Pins 1, 2 and 3 are connected to one side, pins 10, 11, 12 and 13 to another.

5.5 IDD Estimator

Table 1. Typical Current estimated for each macrocell.

Symbol	Parameter	Note	V_{DD} = 1.8 V	V_{DD} = 3.3V	V_{DD} = 5.0V	Unit
I	Current	Chip Quiescent	0.5	0.8	1.0	µA
		Vref	56.9	56.9	63.3	µA
		Vref Buffer (each)	2.7	13.0	13.7	µA
		OSC 25 kHz, predivide = 1	3.1	4.8	6.4	µA
		OSC 25 kHz, predivide = 8	3.0	4.5	6.0	µA
		OSC 2 MHz, predivide = 1	27.4	45.4	67.4	µA
		OSC 2 MHz, predivide = 8	17.5	23.7	29.5	µA
		1st ACMP used (includes Vref)	60.6	62.0	68.4	µA
		Each additional ACMP add	3.7	4.9	5.1	µA

5.6 Timing Estimator

Table 2. Typical Delay estimated for each macrocell.

Symbol	Parameter	Note	V_{DD} = 1.8 V		V_{DD} = 3.3V		V_{DD} = 5.0V		Unit
			rising	falling	rising	falling	rising	falling	
tpd	Delay	Digital Input without Schmitt Trigger - Push Pull	35.3	34.4	14.5	14.3	10.3	10.5	ns
tpd	Delay	Digital Input with Schmitt Trigger - Push Pull	34.8	32.9	14.2	13.8	10.0	10.1	ns
tpd	Delay	Low Voltage Digital input - Push Pull	37.8	450.0	15.0	208.2	10.5	142.3	ns
tpd	Delay	Digital Input without Schmitt Trigger -- NMOS	—	73.5	—	26.0	—	16.3	ns
tpd	Delay	Output enable from pin, OE Hi-Z to 1	44.6	—	17.9	—	12.4	—	ns
tpd	Delay	Output enable from pin, OE Hi-Z to 0	—	43.0	—	17.6	—	12.5	ns
tpd	Delay	2-bit LUT (Latch shared macrocell inputs)	29.6	24.8	11.5	10.1	8.2	6.9	ns
tpd	Delay	Latch (2-bit LUT shared macrocell inputs)	29.2	31.5	11.8	12.5	8.4	8.4	ns
tpd	Delay	3-bit LUT (LATCH shared macrocell inputs)	33.0	27.4	12.8	11.1	9.1	7.5	ns
tpd	Delay	Latch with nRST/nSET (3-bit LUT shared macrocell inputs)	29.9	32.4	12.1	13.0	8.7	8.7	ns
tpd	Delay	4-bit LUT (shared macrocell inputs)	29.2	27.2	11.2	10.8	8.0	7.3	ns
tpd	Delay	2-bit LUT	19.4	18.8	7.2	7.4	5.1	5.0	ns
tpd	Delay	3-bit LUT	22.3	22.7	8.3	8.9	6.0	5.9	ns
tpd	Delay	CNT/DLY	38.4	36.0	15.2	15.1	10.8	10.4	ns
tpd	Delay	CNT/DLY (shared macrocell inputs)	41.0	36.2	16.3	15.6	11.5	10.9	ns
tpd	Delay	CNT3/DLY3 Rising Edge Detect (shared macrocell inputs)	39.7	—	15.7	—	11.1	—	ns
tpd	Delay	CNT3/DLY3 Falling Edge Detect (shared macrocell inputs)	—	41.5	—	16.9	—	11.6	ns
tpd	Delay	CNT3/DLY3 Both Edge Detect (shared macrocell inputs)	39.7	41.5	15.7	16.9	11.1	11.6	ns
tpd	Delay	Filter	183.1	186.2	73.5	75.7	47.9	50.2	ns

5.7 Typical Counter/Delay Offset Measurements

Table 3. Typical Counter/Delay Offset Measurements.

Parameter	RC OSC Freq	RC OSC Power	V_{DD} = 1.8 V	V_{DD} = 3.3V	V_{DD} = 5.0V	Unit
offset	25kHz	auto	19	14	12	µs
offset	2MHz	auto	7	4	4	µs
frequency settling time	25kHz	auto	19	14	12	µs
frequency settling time	2MHz	auto	14	14	14	µs
variable (CLK period)	25kHz	forced	0-40	0-40	0-40	µs
variable (CLK period)	2MHz	forced	0-0.5	0-0.5	0-0.5	µs
tpd (non-delayed edge)	25kHz/2MHz	either	35	14	10	ns

5.8 Expected Delays and Widths

Table 4. Expected Delays and Widths for Programmable Delay(typical).

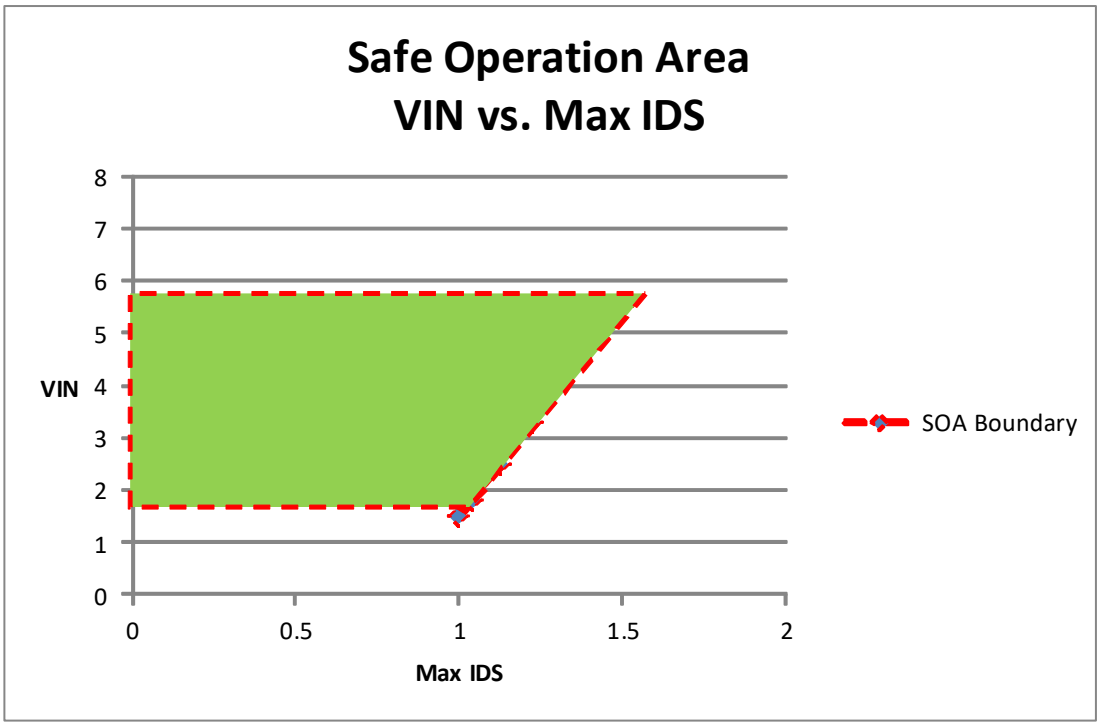
Symbol	Parameter	Note	V_{DD} = 1.8 V	V_{DD} = 3.3V	V_{DD} = 5.0V	Unit
time1	Width, 1 cell	PDLY mode:(any)edge detect, edge detect output	272.4	128.8	97.5	ns
time1	Width, 2 cell	PDLY mode:(any)edge detect, edge detect output	582.7	272.6	205.1	ns
time1	Width, 3 cell	PDLY mode:(any)edge detect, edge detect output	893.4	416.6	312.9	ns
time1	Width, 4 cell	PDLY mode:(any)edge detect, edge detect output	1203.4	560.6	420.9	ns
time2	Delay, 1 cell	PDLY mode:(any)edge detect, edge detect output	39.3	15.7	10.9	ns
time2	Delay, 2 cell	PDLY mode:(any)edge detect, edge detect output	39.3	15.7	10.9	ns
time2	Delay, 3 cell	PDLY mode:(any)edge detect, edge detect output	39.3	15.7	10.9	ns
time2	Delay, 4 cell	PDLY mode:(any)edge detect, edge detect output	39.3	15.7	10.9	ns
time1	Delay, 1 cell	PDLY mode: both edge delay (shared macrocell inputs)	354	161.5	120.1	ns
time1	Delay, 2 cell	PDLY mode: both edge delay (shared macrocell inputs)	664.2	305.2	227.8	ns
time1	Delay, 3 cell	PDLY mode: both edge delay (shared macrocell inputs)	974.9	449.1	335.7	ns
time1	Delay, 4 cell	PDLY mode: both edge delay (shared macrocell inputs)	1284.8	593.1	443.6	ns
time1	Width	CNT3/DLY3 Rising Edge Detect (shared macrocell inputs)	63.6	32.4	22.9	ns
time1	Width	CNT3/DLY3 Falling Edge Detect (shared macrocell inputs)	61.3	31.1	22.5	ns
time1	Width	CNT3/DLY3 Both Edge Detect (shared macrocell inputs)	62.2	31.6	22.7	ns

5.9 Typical Pulse Width Performance

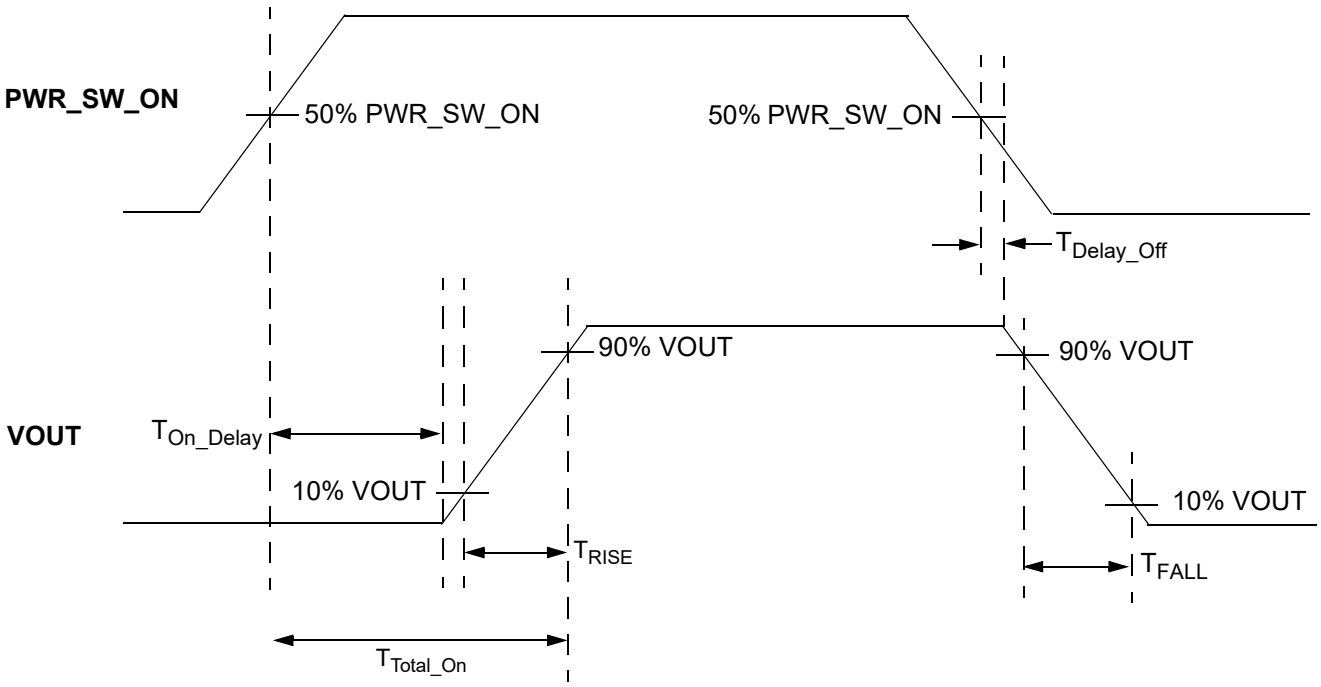
Table 5. Typical Pulse Width Performance.

Parameter	V_{DD} = 1.8 V	V_{DD} = 3.3V	V_{DD} = 5.0V	Unit
Filtered Pulse Width	< 150	< 55	< 35	ns

5.10 VIN vs. Max IDS, Safe Operation Area



5.11 T_{Total_On}, T_{On_Delay} and Slew Rate Measurement



6.0 Summary of Macrocell Function

6.1 I/O Pins

- Digital Input (low voltage or normal voltage, with or without Schmitt Trigger)
- Open Drain Outputs
- Push Pull Outputs
- Analog I/O
- 10 kΩ/100 kΩ/1 MΩ pull-up/pull-down resistors

6.2 Connection Matrix

- Digital matrix for circuit connections based on user design

6.3 Analog Comparators (2 total)

- Selectable hysteresis 0 mV/25 mV/50 mV/200 mV

6.4 Voltage Reference

- Used for references on Analog Comparators
- Can also be driven to external pins

6.5 Combinational Logic Look Up Tables (LUTs – 4 total)

- Two 2-bit Lookup Tables
- Two 3-bit Lookup Tables

6.6 Combination Function Macrocells (7 total)

- Two Selectable DFF/Latch or 2-bit LUTs
- Two Selectable DFF/Latch or 3-bit LUTs
- One Selectable Pipe Delay or 3-bit LUT
- One Selectable CNT/DLY or 4-bit LUT
- One Programmable Delay/ Deglitch Filter

6.7 Delays/Counters (3 total)

- Three 8-bit delays/counters with external clock/reset: Range 1-255 clock cycles

6.8 Pipe Delay (Part of Combination Function Macrocell)

- 8 stage / 2 output
- Two 1-8 stage selectable outputs.

6.9 Programmable Delay

- 125 ns/250 ns/375 ns/500 ns @ 3.3 V
- Includes Edge Detection function

6.10 RC Oscillator

- 25 kHz and 2 MHz selectable frequency
- First stage divider (4): OSC/1, OSC/2, OSC/4, and OSC/8
- Second stage divider (8): selectable (OSC/1, OSC/2, OSC/3, OSC/4, OSC/8, OSC/12, OSC/24, or OSC/64)

6.11 Power On Reset (POR)

7.0 I/O Pins

The SLG46116 has a total of 7 multi-function I/O pins which can function as either a user defined Input or Output, as well as serving as a special function (such as outputting the voltage reference). Refer to Section 2.0 Pin Description for pin definitions.

Of the 7 user defined I/O pins on the SLG46116, all but one of the pins (Pin 1) can serve as both digital input and digital output. Pin 1 can only serve as a digital input pin.

7.1 Input Modes

Each I/O pin can be configured as a digital input pin with/without buffered Schmitt trigger, or can also be configured as a low voltage digital input. Pins 2 and 3 can also be configured to serve as analog inputs to the on-chip comparators.

7.2 Output Modes

Pins 2, 3, 10, 11, 12, and 13 can all be configured as digital output pins.

7.3 Pull Up/Down Resistors

All I/O pins have the option for user selectable resistors connected to the input structure. The selectable values on these resistors are 10 kΩ, 100 kΩ and 1 MΩ. In the case of Pin 1, the resistors are fixed to a pull-down configuration. In the case of all other I/O pins, the internal resistors can be configured as either pull-up or pull-downs.

7.4 I/O Register Settings

7.4.1 PIN 1 Register Settings

Table 6. PIN 1 Register Settings

Signal Function	Register Bit Address	Register Definition
PIN 1 Mode Control	reg <380:379>	00: Digital Input without Schmitt trigger 01: Digital Input with Schmitt trigger 10: Low voltage digital input 11: Reserved
PIN 1 Pull Down Resistor Value Selection	reg <382:381>	00: Floating 01: 10 kΩ Resistor 10: 100 kΩ Resistor 11: 1 MΩ Resistor

7.4.2 PIN 2 Register Settings

Table 7. PIN 2 Register Settings

Signal Function	Register Bit Address	Register Definition
PIN 2 Mode Control	reg <385:383>	000: Digital Input without Schmitt trigger 001: Digital Input with Schmitt trigger 010: Low voltage digital input 011: Analog Input / Output 100: Push Pull 101: Open Drain NMOS 110: Open Drain PMOS 111: Analog Input / Output & Open drain
PIN 2 Pull Up/Down Resistor Value Selection	reg <387:386>	00: Floating 01: 10 kΩ Resistor 10: 100 kΩ Resistor 11: 1 MΩ Resistor
PIN 2 Pull Up/Down Resistor Selection	reg <388>	0: Pull Down Resistor 1: Pull Up Resistor
PIN2 Driver Strength Selection	reg <389>	0: 1X 1: 2X

7.4.3 PIN 3 Register Settings

Table 8. PIN 3 Register Settings

Signal Function	Register Bit Address	Register Definition
PIN 3 Mode Control	reg <392:390>	000: Digital Input without Schmitt trigger 001: Digital Input with Schmitt trigger 010: Low voltage digital input 011: Analog Input / Output 100: Push Pull 101: Open Drain NMOS 110: Open Drain PMOS 111: Analog Input / Output & Open drain
PIN 3 Pull Up/Down Resistor Value Selection	reg <394:393>	00: Floating 01: 10 kΩ Resistor 10: 100 kΩ Resistor 11: 1 MΩ Resistor
PIN 3 Pull Up/Down Resistor Selection	reg <395>	0: Pull Down Resistor 1: Pull Up Resistor
PIN 3 Driver Strength Selection	reg <396>	0: 1X 1: 2X

7.4.4 PIN 10 Register Settings

Table 9. PIN 10 Register Settings

Signal Function	Register Bit Address	Register Definition
PIN 10 Mode Control	reg <406:404>	000: Digital Input without Schmitt trigger 001: Digital Input with Schmitt trigger 010: Low voltage digital input 011: Analog Input / Output 100: Push Pull 101: Open Drain NMOS 110: Open Drain PMOS 111: Analog Input / Output & Open drain
PIN 10 Pull Up/Down Resistor Value Selection	reg <408:407>	00: Floating 01: 10 kΩ Resistor 10: 100 kΩ Resistor 11: 1 MΩ Resistor
PIN 10 Pull Up/Down Resistor Selection	reg <409>	0: Pull Down Resistor 1: Pull Up Resistor
PIN 10 Driver Strength Selection	reg <410>	0: 1X 1: 2X

7.4.5 PIN 11 Register Settings

Table 10. PIN 11 Register Settings

Signal Function	Register Bit Address	Register Definition
PIN 11 Mode Control	reg <413:411>	000: Digital Input without Schmitt trigger 001: Digital Input with Schmitt trigger 010: Low voltage digital input 011: Analog Input / Output 100: Push Pull 101: Open Drain NMOS 110: Open Drain PMOS 111: Analog Input / Output & Open drain
PIN 11 Pull Up/Down Resistor Value Selection	reg <415:414>	00: Floating 01: 10 kΩ Resistor 10: 100 kΩ Resistor 11: 1 MΩ Resistor
PIN 11 Pull Up/Down Resistor Selection	reg <416>	0: Pull Down Resistor 1: Pull Up Resistor
PIN 11 Driver Strength Selection	reg <417>	0: 1X 1: 2X

7.4.6 PIN 12 Register Settings

Table 11. PIN 12 Register Settings

Signal Function	Register Bit Address	Register Definition
PIN 12 Mode Control (sig_PIN12_oe =0)	reg <419:418>	00: Digital Input without Schmitt trigger 01: Digital Input with Schmitt trigger 11: Low Voltage Digital Input 10: Analog Input / Output
PIN 12 Mode Control (sig_PIN12_oe =1)	reg <421:420>	00: Push Pull 1X 01: Push Pull 2X 10: Open Drain NMOS 1X 11: Open Drain NMOS 2X
PIN 12 Pull Up/Down Resistor Value Selection	reg <423:422>	00: Floating 01: 10 kΩ Resistor 10: 100 kΩ Resistor 11: 1 MΩ Resistor
PIN 12 Pull Up/Down Resistor Selection	reg <424>	0: Pull Down Resistor 1: Pull Up Resistor

7.4.7 PIN 13 Register Settings

Table 12. PIN 13 Register Settings

Signal Function	Register Bit Address	Register Definition
PIN 13 Mode Control	reg <427:425>	000: Digital Input without Schmitt trigger 001: Digital Input with Schmitt trigger 010: Low voltage digital input 011: Analog Input / Output 100: Push Pull 101: Open Drain NMOS 110: Open Drain PMOS 111: Analog Input / Output & Open drain
PIN 13 Pull Up/Down Resistor Value Selection	reg <429:428>	00: Floating 01: 10 kΩ Resistor 10: 100 kΩ Resistor 11: 1 MΩ Resistor
PIN 13 Pull Up/Down Resistor Selection	reg <430>	0: Pull Down Resistor 1: Pull Up Resistor
PIN 13 Driver Strength Selection	reg <431>	0: 1X 1: 2X