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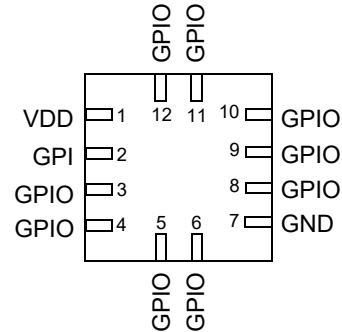
Features

- Logic & Mixed Signal Circuits
- Highly Versatile Macrocells
- 1.8V ($\pm 5\%$) to 5V ($\pm 10\%$) Supply
- Operating Temperature Range: -40°C to 85°C
- RoHS Compliant / Halogen-Free
- Pb-Free 12-pin STQFN: 1.6 x 1.6 x 0.55 mm, 0.4 mm pitch

Applications

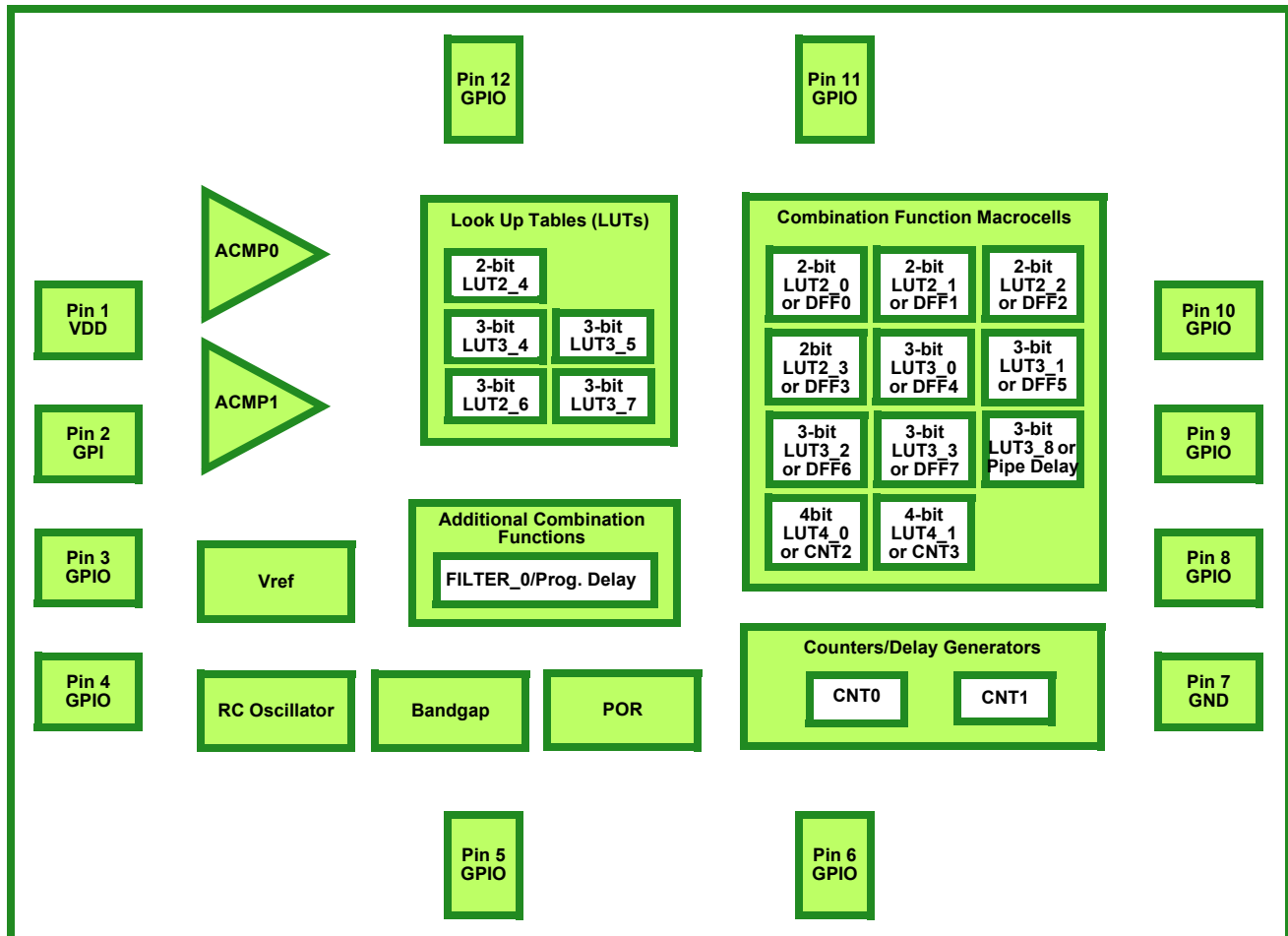
- Personal Computers and Servers
- PC Peripherals
- Consumer Electronics
- Data Communications Equipment
- Handheld and Portable Electronics

Pin Configuration



**STQFN-12
(Top View)**

Block Diagram





1.0 Overview

The SLG46120 provides a small, low power component for commonly used mixed-signal functions. The user creates their circuit design by programming the one time Non-Volatile Memory (NVM) to configure the interconnect logic, the I/O Pins and the macrocells of the SLG46120. This highly versatile device allows a wide variety of mixed-signal functions to be designed within a very small, low power single integrated circuit. The macrocells in the device include the following:

- Two Analog Comparators (ACMP)
- Voltage References (Vref)
- Five Combinatorial Look Up Tables (LUTs)
 - One 2-bit LUTs
 - Four 3-bit LUTs
- Twelve Combination Function Macrocell
 - Four Selectable DFF/Latch or 2-bit LUTs
 - Four Selectable DFF/Latch or 3-bit LUTs
 - One Selectable Pipe Delay or 3-bit LUT
 - Pipe Delay – 8 stage / 2 output, one 1 stage fixed output
 - Two Selectable Counter/Delay or 4-bit LUT
 - One Programmable Delay / Deglitch Filter
- Two Counter / Delay Generators (CNT/DLY)
 - One 8-bit counter/delay
 - One 14-bit counter/delay with external clock/reset
- Eight D Flip-Flop / Latches (DFF) (Part of Combination Function Macrocell)
- Pipe Delay – 8 stage/2 output (Part of Combination Function Macrocell)
- One Bandgap
- RC Oscillator (RC OSC)
- Power On Reset (POR)



2.0 Pin Description

2.1 Functional and Programming Pin Description

Pin #	Pin Name	Function	Programming Function
1	VDD	Power Supply	Power Supply
2	GPI	General Purpose Input	V _{PP} (Programming Voltage)
3	GPIO	General Purpose I/O or Analog Comparator 0 (+)	Programming ID Pin
4	GPIO	General Purpose I/O or Analog Comparator 0 (-)	N/A
5	GPIO	General Purpose I/O	N/A
6	GPIO	General Purpose I/O or Analog Comparator 1 (+) with OE	N/A
7	GND	Ground	N/A
8	GPIO	General Purpose I/O	Programming Mode Control
9	GPIO	General Purpose I/O	Programming SDIO Pin
10	GPIO	General Purpose I/O with OE and Vref output	Programming SRDWB Pin
11	GPIO	General Purpose I/O	N/A
12	GPIO	General Purpose I/O or External Clock Input	Programming SCL Pin



3.0 User Programmability

Non-volatile memory (NVM) is used to configure the SLG46120's connection matrix routing and macrocells. The NVM is One-Time-Programmable (OTP). However, Silego's GreenPAK development tools can be used to configure the connection matrix and macrocells, without programming the NVM, to allow on-chip emulation. This configuration will remain active on the device as long as it remains powered and can be re-written as needed to facilitate rapid design changes.

When a design is ready for in-circuit testing, the same GreenPAK development tools can be used to program the NVM and create samples for small quantity builds. Once the NVM is programmed, the device will retain this configuration for the duration of its lifetime.

Once the design is finalized, the design file can be forwarded to Silego to integrate into the production process.

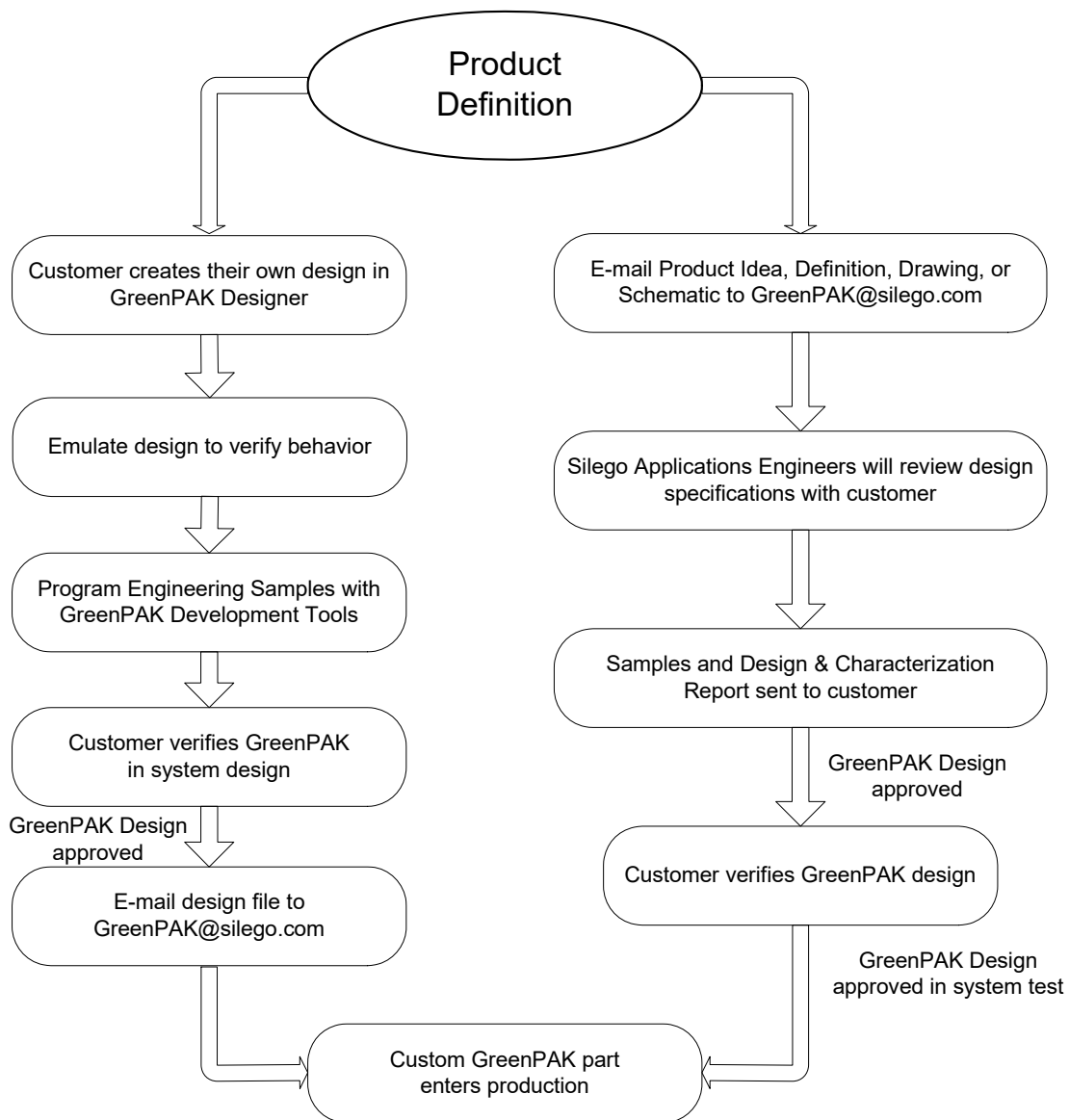


Figure 1. Steps to create a custom Silego GreenPAK device



4.0 Ordering Information

Part Number	Type
SLG46120V	12-pin STQFN
SLG46120VTR	12-pin STQFN - Tape and Reel (3k units)



5.0 Electrical Specifications

5.1 Absolute Maximum Conditions

Parameter		Min.	Max.	Unit
Supply voltage on VDD relative to GND		-0.5	7	V
DC Input voltage		GND - 0.5	VDD + 0.5	V
Maximum Average or DC Current (Through pin)	Push-Pull 1x	--	12	mA
	Push-Pull 2x	--	17	
	OD 1x	--	18	
	OD 2x	--	28	
Current at Input Pin		-1.0	1.0	mA
Storage Temperature Range		-65	150	°C
Junction Temperature		--	150	°C
ESD Protection (Human Body Model)		2000	--	V
ESD Protection (Charged Device Model)		1000	--	V
Moisture Sensitivity Level		1		

5.2 Electrical Characteristics (1.8V ±5% V_{DD})

Symbol	Parameter	Condition/Note	Min.	Typ.	Max.	Unit
V _{DD}	Supply Voltage		1.71	1.80	1.89	V
I _Q	Quiescent Current	Static Inputs and Outputs (when ACMP, Vref and RC OSC are powered down and non-operational)	--	0.5	--	μA
T _A	Operating Temperature		-40	25	85	°C
V _{PP}	Programming Voltage		7.25	7.50	7.75	V
V _{AIR}	Analog Input Voltage Range	Positive Input	0	--	V _{DD}	V
		Negative Input	0	--	1.1	V
V _{IH}	HIGH-Level Input Voltage	Logic Input	1.100	--	V _{DD}	V
		Logic Input with Schmitt Trigger	1.270	--	V _{DD}	V
		Low-Level Logic Input	0.980	--	V _{DD}	V
V _{IL}	LOW-Level Input Voltage	Logic Input	--	--	0.690	V
		Logic Input with Schmitt Trigger	--	--	0.440	V
		Low-Level Logic Input	--	--	0.520	V
I _{IH}	HIGH-Level Input Current	Logic Input Pins; V _{IN} = 1.8 V	-1.0	--	1.0	μA
I _{IL}	LOW-Level Input Current	Logic Input Pins; V _{IN} = 0 V	-1.0	--	1.0	μA
V _{OH}	HIGH-Level Output Voltage	Push-Pull 1X, Open Drain PMOS 1X, I _{OH} = 100 μA	1.680	1.790	--	V
		Push-Pull 2X, Open Drain PMOS 2X, I _{OH} = 100 μA	1.700	1.800	--	V



Symbol	Parameter	Condition/Note	Min.	Typ.	Max.	Unit
V_{OL}	LOW-Level Output Voltage	Push-Pull 1X, $I_{OL} = 100 \mu A$	--	0.020	0.030	V
		Push-Pull 2X, $I_{OL} = 100 \mu A$	--	0.010	0.020	V
		Open Drain NMOS 1X, $I_{OL} = 100 \mu A$	--	0.010	0.020	V
		Open Drain NMOS 2X, $I_{OL} = 100 \mu A$	--	0.010	0.010	V
I_{OH}	HIGH-Level Output Current (see Note 1)	Push-Pull 1X, Open Drain PMOS 1X, $V_{OH} = V_{DD} - 0.2$	1.000	1.390	--	mA
		Push-Pull 2X, Open Drain PMOS 2X, $V_{OH} = V_{DD} - 0.2$	2.100	2.680	--	mA
I_{OL}	LOW-Level Output Current (see Note 1)	Push-Pull 1X, $V_{OL} = 0.15 V$	0.760	1.340	--	mA
		Push-Pull 2X, $V_{OL} = 0.15 V$	1.520	2.660	--	mA
		Open Drain NMOS 1X, $V_{OL} = 0.15 V$	1.530	2.670	--	mA
		Open Drain NMOS 2X, $V_{OL} = 0.15 V$	3.060	5.136	--	mA
I_{VDD}	Maximum Average or DC Current Through VDD Pin (Per chip side, see Note 2)	$T_J = 85^\circ C$	--	--	73	mA
		$T_J = 110^\circ C$	--	--	35	mA
I_{GND}	Maximum Average or DC Current Through GND Pin (Per chip side, see Note 2)	$T_J = 85^\circ C$	--	--	92	mA
		$T_J = 110^\circ C$	--	--	44	mA
T_{SU}	Startup Time	from VDD rising past 1.35 V	--	0.31	--	ms
PON_{THR}	Power On Threshold	V_{DD} Level Required to Start Up the Chip	1.180	1.353	1.516	V
$POFF_{THR}$	Power Off Threshold	V_{DD} Level Required to Switch Off the Chip	0.730	0.914	1.103	V

Note 1: DC or average current through any pin should not exceed value given in Absolute Maximum Conditions.
Note 2: The GreenPAK's power rails are divided in two sides. Pins 2, 3, 4, 5 and 6 are connected to one side, pins 8, 9, 10, 11 and 12 to another.



5.3 Electrical Characteristics (3.3V ±10% V_{DD})

Symbol	Parameter	Condition/Note	Min.	Typ.	Max.	Unit
V _{DD}	Supply Voltage		3.0	3.3	3.6	V
I _Q	Quiescent Current	Static Inputs and Outputs (when ACMP, Vref and RC OSC are powered down and non-operational)	--	0.75	--	μA
T _A	Operating Temperature		-40	25	85	°C
V _{PP}	Programming Voltage		7.25	7.50	7.75	V
V _{AIR}	Analog Input Voltage Range	Positive Input	0	--	V _{DD}	V
		Negative Input	0	--	1.2	V
V _{IH}	HIGH-Level Input Voltage	Logic Input	1.780	--	V _{DD}	V
		Logic Input with Schmitt Trigger	2.130	--	V _{DD}	V
		Low-Level Logic Input	1.130	--	V _{DD}	V
V _{IL}	LOW-Level Input Voltage	Logic Input	--	--	1.210	V
		Logic Input with Schmitt Trigger	--	--	0.950	V
		Low-Level Logic Input	--	--	0.690	V
I _{IH}	HIGH-Level Input Current	Logic Input Pins; V _{IN} = 3.3 V	-1.0	--	1.0	μA
I _{IL}	LOW-Level Input Current	Logic Input Pins; V _{IN} = 0 V	-1.0	--	1.0	μA
V _{OH}	HIGH-Level Output Voltage	Push-Pull 1X, Open Drain PMOS 1X, I _{OH} = 3 mA	2.720	3.090	--	V
		Push-Pull 2X, Open Drain PMOS 2X, I _{OH} = 3 mA	2.850	3.190	--	V
V _{OL}	LOW-Level Output Voltage	Push-Pull 1X, I _{OL} = 3 mA	--	0.180	0.280	V
		Push-Pull 2X, I _{OL} = 3 mA	--	0.090	0.130	V
		Open Drain NMOS 1X, I _{OL} = 3 mA	--	0.090	0.130	V
		Open Drain NMOS 2X, I _{OL} = 3 mA	--	0.050	0.070	V
I _{OH}	HIGH-Level Output Current (see Note 1)	Push-Pull 1X, Open Drain PMOS 1X, V _{OH} = 2.4 V	6.010	10.150	--	mA
		Push-Pull 2X, Open Drain PMOS 2X, V _{OH} = 2.4 V	11.460	19.610	--	mA
I _{OL}	LOW-Level Output Current (see Note 1)	Push-Pull 1X, V _{OL} = 0.4 V	4.060	6.440	--	mA
		Push-Pull 2X, V _{OL} = 0.4 V	8.130	12.360	--	mA
		Open Drain NMOS 1X, V _{OL} = 0.4 V	8.130	12.410	--	mA
		Open Drain NMOS 2X, V _{OL} = 0.4 V	16.260	22.900	--	mA
I _{VDD}	Maximum Average or DC Current Through VDD Pin (Per chip side, see Note 2)	T _J = 85°C	--	--	73	mA
		T _J = 110°C	--	--	35	mA
I _{GND}	Maximum Average or DC Current Through GND Pin (Per chip side, see Note 2)	T _J = 85°C	--	--	92	mA
		T _J = 110°C	--	--	44	mA



Symbol	Parameter	Condition/Note	Min.	Typ.	Max.	Unit
T _{SU}	Startup Time	from VDD rising past 1.35 V	--	0.31	--	ms
PON _{THR}	Power On Threshold	V _{DD} Level Required to Start Up the Chip	1.180	1.353	1.516	V
POFF _{THR}	Power Off Threshold	V _{DD} Level Required to Switch Off the Chip	0.730	0.914	1.103	V

Note 1: DC or average current through any pin should not exceed value given in Absolute Maximum Conditions.

Note 2: The GreenPAK's power rails are divided in two sides. Pins 2, 3, 4, 5 and 6 are connected to one side, pins 8, 9, 10, 11 and 12 to another.

5.4 Electrical Characteristics (5V ±10% V_{DD})

Symbol	Parameter	Condition/Note	Min.	Typ.	Max.	Unit
V _{DD}	Supply Voltage		4.5	5.0	5.5	V
I _Q	Quiescent Current	Static Inputs and Outputs (when ACMP, Vref and RC OSC are powered down and non-operational)	--	1.0	--	μA
T _A	Operating Temperature		-40	25	85	°C
V _{PP}	Programming Voltage		7.25	7.50	7.75	V
V _{AIR}	Analog Input Voltage Range	Positive Input	0	--	V _{DD}	V
		Negative Input	0	--	1.2	V
V _{IH}	HIGH-Level Input Voltage	Logic Input	2.640	--	V _{DD}	V
		Logic Input with Schmitt Trigger	3.160	--	V _{DD}	V
		Low-Level Logic Input	1.230	--	V _{DD}	V
V _{IL}	LOW-Level Input Voltage	Logic Input	--	--	1.840	V
		Logic Input with Schmitt Trigger	--	--	1.510	V
		Low-Level Logic Input	--	--	0.780	V
I _{IH}	HIGH-Level Input Current	Logic Input Pins; V _{IN} = 5 V	-1.0	--	1.0	μA
I _{IL}	LOW-Level Input Current	Logic Input Pins; V _{IN} = 0 V	-1.0	--	1.0	μA
V _{OH}	HIGH-Level Output Voltage	Push-Pull 1X, Open Drain PMOS 1X, I _{OH} = 5 mA	4.170	4.740	--	V
		Push-Pull 2X, Open Drain PMOS 2X, I _{OH} = 5 mA	4.320	4.860	--	V
V _{OL}	LOW-Level Output Voltage	Push-Pull 1X, I _{OL} = 5 mA	--	0.230	0.330	V
		Push-Pull 2X, I _{OL} = 5 mA	--	0.120	0.160	V
		Open Drain NMOS 1X, I _{OL} = 5 mA	--	0.120	0.160	V
		Open Drain NMOS 2X, I _{OL} = 5 mA	--	0.700	0.090	V
I _{OH}	HIGH-Level Output Current (see Note 1)	Push-Pull 1X, Open Drain PMOS 1X, V _{OH} = 2.4 V	21.980	29.0010	--	mA
		Push-Pull 2X, Open Drain PMOS 2X, V _{OH} = 2.4 V	41.886	55.990	--	mA



Symbol	Parameter	Condition/Note	Min.	Typ.	Max.	Unit
I_{OL}	LOW-Level Output Current (see Note 1)	Push-Pull 1X, $V_{OL} = 0.4\text{ V}$	6.010	9.730	--	mA
		Push-Pull 2X, $V_{OL} = 0.4\text{ V}$	11.590	19.460	--	mA
		Open Drain NMOS 1X, $V_{OL} = 0.4\text{ V}$	11.760	19.460	--	mA
		Open Drain NMOS 2X, $V_{OL} = 0.4\text{ V}$	19.120	35.952	--	mA
I_{VDD}	Maximum Average or DC Current Through VDD Pin (Per chip side, see Note 2)	$T_J = 85^\circ\text{C}$	--	--	73	mA
		$T_J = 110^\circ\text{C}$	--	--	35	mA
I_{GND}	Maximum Average or DC Current Through GND Pin (Per chip side, see Note 2)	$T_J = 85^\circ\text{C}$	--	--	92	mA
		$T_J = 110^\circ\text{C}$	--	--	44	mA
T_{SU}	Startup Time	from VDD rising past 1.35 V	--	0.31	--	ms
PON_{THR}	Power On Threshold	V_{DD} Level Required to Start Up the Chip	1.180	1.353	1.516	V
$POFF_{THR}$	Power Off Threshold	V_{DD} Level Required to Switch Off the Chip	0.730	0.914	1.103	V

Note 1: DC or average current through any pin should not exceed value given in Absolute Maximum Conditions.

Note 2: The GreenPAK's power rails are divided in two sides. Pins 2, 3, 4, 5 and 6 are connected to one side, pins 8, 9, 10, 11 and 12 to another.



5.5 IDD Estimator

Table 1. Typical Current estimated for each macrocell.

Symbol	Parameter	Note	V _{DD} = 1.8 V	V _{DD} = 3.3V	V _{DD} = 5.0V	Unit
I	Current	Chip Quiescent	0.5	0.8	1.0	μA
		Vref	55.7	56.0	62.5	μA
		Vref Buffer (each)	0.6	14.1	14.6	μA
		OSC 25 kHz, predivide = 1	3.1	4.7	6.4	μA
		OSC 25 kHz, predivide = 8	3.0	4.3	5.8	μA
		OSC 2 MHz, predivide = 1	29.3	51.0	79.8	μA
		OSC 2 MHz, predivide = 8	17.4	23.2	29.0	μA
		1st ACMP used (includes Vref)	59.6	60.0	66.5	μA
		Each additional ACMP add	3.9	4.0	4.0	μA

5.6 Timing Estimator

Table 2. Typical Delay estimated for each macrocell.

Symbol	Parameter	Note	V _{DD} = 1.8 V		V _{DD} = 3.3V		V _{DD} = 5.0V		Unit
			rising	falling	rising	falling	rising	falling	
tpd	Delay	Digital Input without Schmitt Trigger -- Push Pull	44.2	43.5	17.8	18.2	12.7	13.0	ns
tpd	Delay	Digital Input with Schmitt Trigger -- Push Pull	43.3	42.5	17.7	18.0	12.6	13.0	ns
tpd	Delay	Low Voltage Digital input -- Push Pull	45.6	517.0	18.1	215.3	12.7	144.9	ns
tpd	Delay	Digital Input without Schmitt Trigger -- NMOS	—	83.8	—	29.9	—	19.5	ns
tpd	Delay	Output enable from pin, OE Hi-Z to 1	44.8	—	17.9	—	12.6	—	ns
tpd	Delay	Output enable from pin, OE Hi-Z to 0	—	43.4	—	17.7	—	12.8	ns
tpd	Delay	2-bit LUT	18.7	22.1	8.0	8.7	5.8	6.0	ns
tpd	Delay	Latch (2-bit LUT shared macrocell inputs)	26.5	30.8	11.3	12.3	8.1	8.5	ns
tpd	Delay	3-bit LUT	21.3	24.4	9.1	9.6	6.5	6.6	ns
tpd	Delay	3-bit LUT (LATCH shared macrocell inputs)	26.8	25.4	11.2	10.2	8.0	7.1	ns
tpd	Delay	Latch with nRST/nSET (3-bit LUT shared macrocell inputs)	29.7	34.7	12.6	13.9	9.1	9.6	ns
tpd	Delay	4-bit LUT (shared macrocell inputs)	34.0	32.6	14.4	13.0	10.3	9.1	ns
tpd	Delay	2-bit LUT (Latch shared macrocell inputs)	26.8	25.4	11.2	10.2	8.0	7.1	ns
tpd	Delay	CNT/DLY	44.2	38.8	18.7	16.4	13.3	11.8	ns
tpd	Delay	CNT/DLY (shared macrocell inputs)	43.2	39.7	18.4	16.8	13.0	12.1	ns
tpd	Delay	CNT3/DLY3 Rising Edge Detect (shared macrocell inputs)	38.2	—	16.0	—	11.4	—	ns
tpd	Delay	CNT3/DLY3 Falling Edge Detect (shared macrocell inputs)	—	40.4	—	16.4	—	11.6	ns
tpd	Delay	CNT3/DLY3 Both Edge Detect (shared macrocell inputs)	38.2	40.5	15.9	16.5	11.3	11.5	ns
tpd	Delay	Filter	191.6	193	77.4	77.8	50.7	52.1	ns



5.7 Typical Counter/Delay Offset Measurements

Table 3. Typical Counter/Delay Offset Measurements.

Parameter	RC OSC Freq	RC OSC Power	V _{DD} = 1.8 V	V _{DD} = 3.3V	V _{DD} = 5.0V	Unit
offset	25kHz	auto	19	14	12	μs
offset	2MHz	auto	7	4	4	μs
frequency settling time	25kHz	auto	19	14	12	μs
frequency settling time	2MHz	auto	14	14	14	μs
variable (CLK period)	25kHz	forced	0-40	0-40	0-40	μs
variable (CLK period)	2MHz	forced	0-0.5	0-0.5	0-0.5	μs
tpd (non-delayed edge)	25kHz/2MHz	either	35	14	10	ns

5.8 Expected Delays and Widths

Table 4. Expected Delays and Widths for Programmable Delay (typical).

Symbol	Parameter	Note	V _{DD} = 1.8 V	V _{DD} = 3.3V	V _{DD} = 5.0V	Unit
time1	Width, 1 cell	PDLY mode:(any)edge detect, edge detect output	256.7	120.8	110	ns
time1	Width, 2 cell	PDLY mode:(any)edge detect, edge detect output	564.4	262.7	225	ns
time1	Width, 3 cell	PDLY mode:(any)edge detect, edge detect output	873.5	405	340	ns
time1	Width, 4 cell	PDLY mode:(any)edge detect, edge detect output	1182.3	547.5	450	ns
time2	Delay, 1 cell	PDLY mode:(any)edge detect, edge detect output	48.2	20	14	ns
time2	Delay, 2 cell	PDLY mode:(any)edge detect, edge detect output	48.2	20.1	14	ns
time2	Delay, 3 cell	PDLY mode:(any)edge detect, edge detect output	48.2	20.1	14	ns
time2	Delay, 4 cell	PDLY mode:(any)edge detect, edge detect output	48.3	20.1	14	ns
time1	Delay, 1 cell	PDLY mode: both edge delay (shared macrocell inputs)	357.9	162.2	110	ns
time1	Delay, 2 cell	PDLY mode: both edge delay (shared macrocell inputs)	666.1	304.3	220	ns
time1	Delay, 3 cell	PDLY mode: both edge delay (shared macrocell inputs)	974.7	446.3	335	ns
time1	Delay, 4 cell	PDLY mode: both edge delay (shared macrocell inputs)	1283.8	588.8	450	ns
time1	Width	CNT3/DLY3 Rising Edge Detect (shared macrocell inputs)	136.6	73.4	140	ns
time1	Width	CNT3/DLY3 Falling Edge Detect (shared macrocell inputs)	130.6	71	140	ns
time1	Width	CNT3/DLY3 Both Edge Detect (shared macrocell inputs)	133.05	72	140	ns



5.9 Typical Pulse Width Performance

Table 5. Typical Pulse Width Performance.

Parameter	V_{DD} = 1.8 V	V_{DD} = 3.3V	V_{DD} = 5.0V	Unit
Filtered Pulse Width	< 150	< 55	< 35	ns



6.0 Summary of Macrocell Function

6.1 I/O Pins

- Digital Input (low voltage or normal voltage, with or without Schmitt Trigger)
- Open Drain NMOS and Open Drain PMOS Outputs
- Push Pull Outputs
- Analog I/O
- 10 k Ω /100 k Ω /1 M Ω pull-up/pull-down resistors

6.2 Connection Matrix

- Digital matrix for circuit connections based on user design

6.3 Analog Comparators (2 total)

- Selectable hysteresis 0 mV/25 mV/50 mV/200 mV and selectable gain 1x/0.5x/0.33x/0.25x

6.4 Voltage Reference

- Used for references on Analog Comparators
- Can also be driven to external pins

6.5 Combinational Logic Look Up Tables (LUTs – 5 total)

- One 2-bit Lookup Tables
- Four 3-bit Lookup Tables

6.6 Combination Function Macrocells (12 total)

- Four Selectable DFF/Latches or 2-bit LUTs
- Four Selectable DFF/Latches or 3-bit LUTs
- One Selectable Pipe Delay or 3-bit LUT
- Two Selectable CNT/DLYs or 4-bit LUTs
- One Programmable Delay or Deglitch Filter

6.7 Delays/Counters (2 total)

- One 8-bit delay/counter with external clock/reset: Range 1-255 clock cycles
- One 14-bit delay/counter with external clock/reset: Range 1-16383 clock cycles

6.8 Pipe Delay (Part of Combination Function Macrocell)

- 8 stage / 2 output
- Two 1-8 stage selectable outputs
- One 1 stage fixed output

6.9 Additional Logic Functions (Part of Combination Function Macrocell)

- One Deglitch filter macrocell
- One Programmable Delay
 - 163 ns / 305 ns / 446 ns / 588 ns @ 3.3 V
 - Includes Edge Detection function



6.10 RC Oscillator

- 25 kHz and 2 MHz selectable frequency
- First Stage Clock pre=divider (4): OSC/1, OSC/2, OSC/4, and OSC/8
- Second stage divider control with two outputs, OUT0 and OUT1 (8): selectable (OSC/1, OSC/2, OSC/3, OSC/4, OSC/8, OSC/12, OSC/24, or OSC/64)

6.11 Power On Reset (POR)



7.0 I/O Pins

The SLG46120 has a total of 10 multi-function I/O pins which can function as either a user defined Input or Output, as well as serving as a special function (such as outputting the voltage reference), or serving as a signal for programming of the on-chip Non Volatile Memory (NVM).

Normal Mode pin definitions are as follows:

- Pin 1: V_{DD} Power Supply
- Pin 2: General Purpose Input
- Pin 3: General Purpose I/O or Analog Comparator 0 (+)
- Pin 4: General Purpose I/O or Analog Comparator 0 (-)
- Pin 5: General Purpose I/O
- Pin 6: General Purpose I/O or Analog Comparator 1 (+) with OE
- Pin 7: Ground
- Pin 8: General Purpose I/O
- Pin 9: General Purpose I/O
- Pin 10: General Purpose I/O with OE and Vref Output
- Pin 11: General Purpose I/O
- Pin 12: General Purpose I/O or External Clock Input

Programming Mode pin definitions are as follows:

- Pin 1: V_{DD} Power Supply
- Pin 2: V_{PP} Programming Voltage
- Pin 3: Programming ID Pin
- Pin 7: Ground
- Pin 8: Programming Mode Control
- Pin 9: Programming SDIO Pin
- Pin 10: Programming SRDWB Pin
- Pin 12: Programming SCL Pin

Of the 10 user defined I/O pins on the SLG46120, all but one of the pins (Pin 2) can serve as both digital input and digital output. Pin 2 can only serve as a digital input pin.

7.1 Input Modes

Each I/O pin can be configured as a digital input pin with/without buffered Schmitt Trigger, or can also be configured as a low voltage digital input. Pins 3, 4, and 6 can also be configured to serve as analog inputs to the on-chip comparators.

7.2 Output Modes

Pins 3, 4, 5, 6, 8, 9, 10, 11, and 12 can all be configured as digital output pins.

7.3 Pull Up/Down Resistors

All I/O pins have the option for user selectable resistors connected to the input structure. The selectable values on these resistors are 10 k Ω , 100 k Ω and 1 M Ω . In the case of Pin 2, the resistors are fixed to a pull-down configuration. In the case of all other I/O pins, the internal resistors can be configured as either pull-up or pull-downs.



7.4 I/O Register Settings

7.4.1 PIN 2 Register Settings

Table 6. PIN 2 Register Settings

Signal Function	Register Bit Address	Register Definition
PIN 2 Mode Control	reg <624:623>	00: Digital Input without Schmitt Trigger 01: Digital Input with Schmitt Trigger 10: Low Voltage Digital Input 11: Reserved
PIN 2 Pull Down Resistor Value Selection	reg <626:625>	00: Floating 01: 10 kΩ Resistor 10: 100 kΩ Resistor 11: 1 MΩ Resistor

7.4.2 PIN 3 Register Settings

Table 7. PIN 3 Register Settings

Signal Function	Register Bit Address	Register Definition
PIN 3 Mode Control	reg <629:627>	000: Digital Input without Schmitt Trigger 001: Digital Input with Schmitt Trigger 010: Low Voltage Digital Input 011: Analog Input 100: Push Pull 101: Open Drain NMOS 110: Open Drain PMOS 111: Analog Input & Open Drain NMOS
PIN 3 Pull Up/Down Resistor Value Selection	reg <631:630>	00: Floating 01: 10 kΩ Resistor 10: 100 kΩ Resistor 11: 1 MΩ Resistor
PIN 3 Pull Up/Down Resistor Selection	reg <632>	0: Pull Down Resistor 1: Pull Up Resistor
PIN3 Driver Strength Selection	reg <633>	0: 1X 1: 2X



7.4.3 PIN 4 Register Settings

Table 8. PIN 4 Register Settings

Signal Function	Register Bit Address	Register Definition
PIN 4 Mode Control	reg <636:634>	000: Digital Input without Schmitt Trigger 001: Digital Input with Schmitt Trigger 010: Low Voltage Digital Input 011: Analog Input 100: Push Pull 101: Open Drain NMOS 110: Open Drain PMOS 111: Analog Input & Open Drain NMOS
PIN 4 Pull Up/Down Resistor Value Selection	reg <638:637>	00: Floating 01: 10 kΩ Resistor 10: 100 kΩ Resistor 11: 1 MΩ Resistor
PIN 4 Pull Up/Down Resistor Selection	reg <639>	0: Pull Down Resistor 1: Pull Up Resistor
PIN 4 Driver Strength Selection	reg <640>	0: 1X 1: 2X

7.4.4 PIN 5 Register Settings

Table 9. PIN 5 Register Settings

Signal Function	Register Bit Address	Register Definition
PIN 5 Mode Control	reg <643:641>	000: Digital Input without Schmitt Trigger 001: Digital Input with Schmitt Trigger 010: Low Voltage Digital Input 011: Analog Input 100: Push Pull 101: Open Drain NMOS 110: Open Drain PMOS 111: Analog Input & Open Drain NMOS
PIN 5 Pull Up/Down Resistor Value Selection	reg <645:644>	00: Floating 01: 10 kΩ Resistor 10: 100 kΩ Resistor 11: 1 MΩ Resistor
PIN 5 Pull Up/Down Resistor Selection	reg <646>	0: Pull Down Resistor 1: Pull Up Resistor
PIN 5 Driver Strength Selection	reg <647>	0: 1X 1: 2X



7.4.5 PIN 6 Register Settings

Table 10. PIN 6 Register Settings

Signal Function	Register Bit Address	Register Definition
PIN 6 Mode Control (sig_PIN6_oe =0)	reg <649:648>	00: Digital Input without Schmitt Trigger 01: Digital Input with Schmitt Trigger 11: Low Voltage Digital Input 10: Analog Input / Output
PIN 6 Mode Control (sig_PIN6_oe =1)	reg <651:650>	00: Push Pull 1X 01: Push Pull 2X 10: Open Drain NMOS 1X 11: Open Drain NMOS 2X
PIN 6 Pull Up/Down Resistor Value Selection	reg <653:652>	00: Floating 01: 10 kΩ Resistor 10: 100 kΩ Resistor 11: 1 MΩ Resistor
PIN 6 Pull Up/Down Resistor Selection	reg <654>	0: Pull Down Resistor 1: Pull Up Resistor

7.5 PIN 8 Register Settings

Table 11. PIN 8 Register Settings

Signal Function	Register Bit Address	Register Definition
PIN 8 Mode Control	reg <657:655>	000: Digital Input without Schmitt Trigger 001: Digital Input with Schmitt Trigger 010: Low Voltage Digital Input 011: Analog Input / Output 100: Push Pull 101: Open Drain NMOS 110: Open Drain PMOS 111: Reserved
PIN 8 Pull Up/Down Resistor Value Selection	reg <659:658>	00: Floating 01: 10 kΩ Resistor 10: 100 kΩ Resistor 11: 1 MΩ Resistor
PIN 8 Pull Up/Down Resistor Selection	reg <660>	0: Pull Down Resistor 1: Pull Up Resistor
PIN 8 Driver Strength Selection	reg <661>	0: 1X 1: 2X



7.5.1 PIN 9 Register Settings

Table 12. PIN 9 Register Settings

Signal Function	Register Bit Address	Register Definition
PIN 9 Mode Control	reg <664:662>	000: Digital Input without Schmitt Trigger 001: Digital Input with Schmitt Trigger 010: Low Voltage Digital Input 011: Reserved 100: Push Pull 101: Open Drain NMOS 110: Open Drain PMOS 111: Open drain
PIN 9 Pull Up/Down Resistor Value Selection	reg <666:665>	00: Floating 01: 10 kΩ Resistor 10: 100 kΩ Resistor 11: 1 MΩ Resistor
PIN 9 Pull Up/Down Resistor Selection	reg <667>	0: Pull Down Resistor 1: Pull Up Resistor
PIN 8 Driver Strength Selection	reg <668>	0: 1X 1: 2X

7.6 PIN 10 Register Settings

Table 13. PIN 10 Register Settings

Signal Function	Register Bit Address	Register Definition
PIN 10 Mode Control (sig_PIN10_oe =0)	reg <670:669>	00: Digital Input without Schmitt Trigger 01: Digital Input with Schmitt Trigger 11: Low Voltage Digital Input 10: Analog Input
PIN 10 Mode Control (sig_PIN10_oe =1)	reg <672:671>	00: Push Pull 1X 01: Push Pull 2X 10: Open Drain NMOS 1X 11: Open Drain NMOS 2X
PIN 10 Pull Up/Down Resistor Value Selection	reg <674:673>	00: Floating 01: 10 kΩ Resistor 10: 100 kΩ Resistor 11: 1 MΩ Resistor
PIN 10 Pull Up/Down Resistor Selection	reg <675>	0: Pull Down Resistor 1: Pull Up Resistor

7.7 PIN 11 Register Settings

Table 14. PIN 11 Register Settings

Signal Function	Register Bit Address	Register Definition
PIN 11 Mode Control	reg <678:676>	000: Digital Input without Schmitt Trigger 001: Digital Input with Schmitt Trigger 010: Low Voltage Digital Input 011: Reserved 100: Push Pull 101: Open Drain NMOS 110: Open Drain PMOS 111: Open drain



Table 14. PIN 11 Register Settings

Signal Function	Register Bit Address	Register Definition
PIN 11 Pull Up/Down Resistor Value Selection	reg <680:679>	00: Floating 01: 10 k Ω Resistor 10: 100 k Ω Resistor 11: 1 M Ω Resistor
PIN 11 Pull Up/Down Resistor Selection	reg <681>	0: Pull Down Resistor 1: Pull Up Resistor
PIN 11 Driver Strength Selection	reg <682>	0: 1X 1: 2X



7.8 PIN 12 Register Settings

Table 15. PIN 12 Register Settings

Signal Function	Register Bit Address	Register Definition
PIN 12 Mode Control	reg <685:683>	000: Digital Input without Schmitt Trigger 001: Digital Input with Schmitt Trigger 010: Low Voltage Digital Input 011: Reserved 100: Push Pull 101: Open Drain NMOS 110: Open Drain PMOS 111: Open drain
PIN 12 Pull Up/Down Resistor Value Selection	reg <687:686>	00: Floating 01: 10 k Ω Resistor 10: 100 k Ω Resistor 11: 1 M Ω Resistor
PIN 12 Pull Up/Down Resistor Selection	reg <688>	0: Pull Down Resistor 1: Pull Up Resistor
PIN 12 Driver Strength Selection	reg <689>	0: 1X 1: 2X



7.9 GPI IO Structure

7.9.1 GPI IO Structure (for Pin 2)

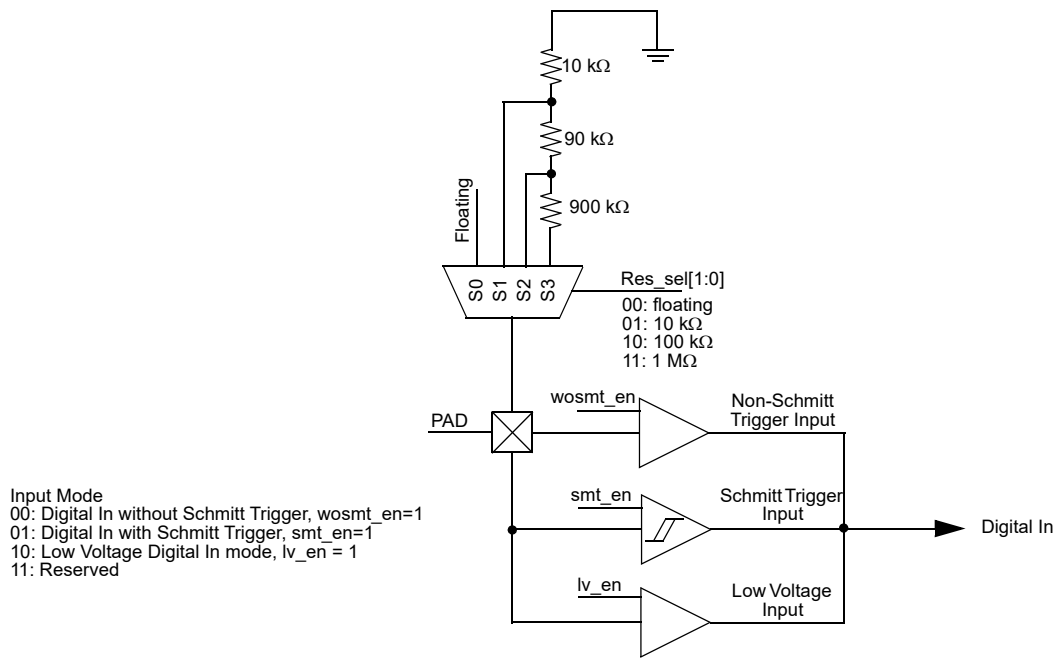


Figure 2. PIN 2 GPI IO Structure Diagram



7.10 Matrix OE IO Structure

7.10.1 Matrix OE IO Structure (for Pin 6, 10)

Input Mode
 00: Digital In without Schmitt Trigger, *wosmt_en*=1
 01: Digital In with Schmitt Trigger, *smt_en*=1
 10: Low Voltage Digital In mode, *lv_en* = 1
 11: analog IO mode

Output Mode
 00: 1x push-pull mode, *pp1x_en*=1
 01: 2x push-pull mode, *pp2x_en*=1, *pp1x_en*=1
 10: 1x NMOS open drain mode, *od1x_en*=1
 11: 2x NMOS open drain mode, *od2x_en*=1, *od1x_en*=1

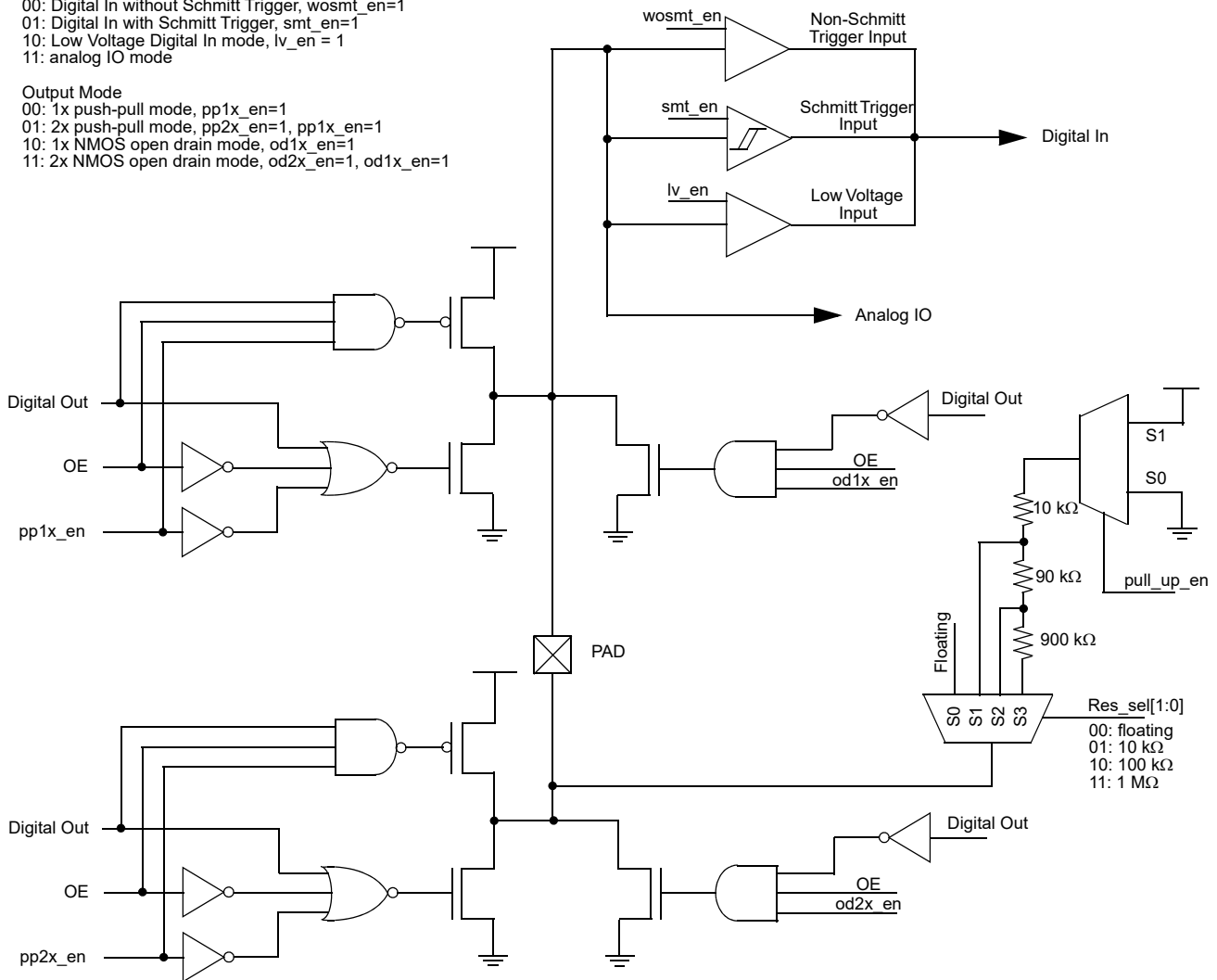


Figure 3. Matrix OE IO Structure Diagram



7.11 Register OE IO Structure

7.11.1 Register OE IO Structure (for Pins 3, 4, 5, 8, 9, 11, 12)

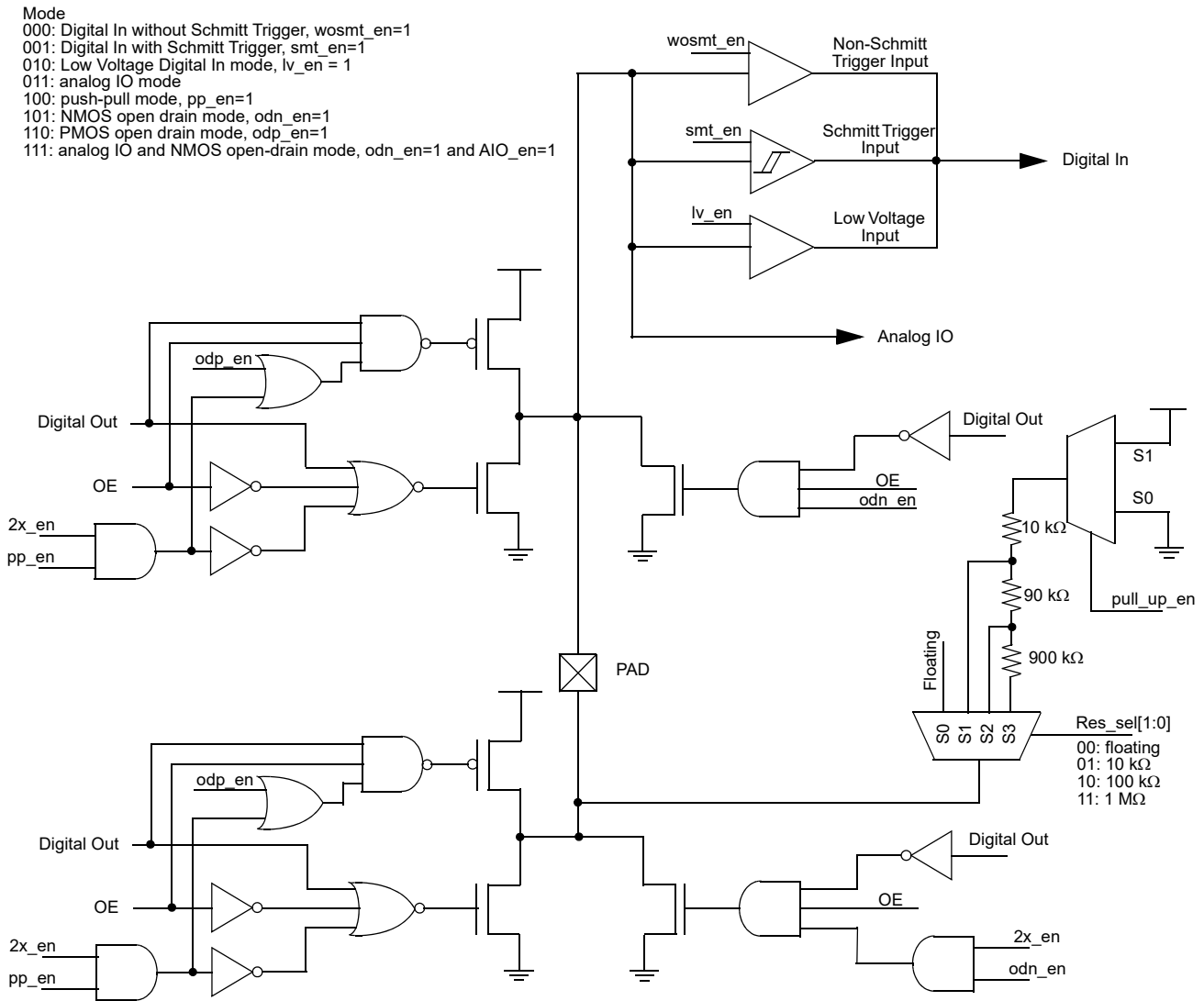


Figure 4. Register OE IO Structure Diagram