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SLG46121

GreenPAK
Dual Supply Programmable Mixed-signal Matrix

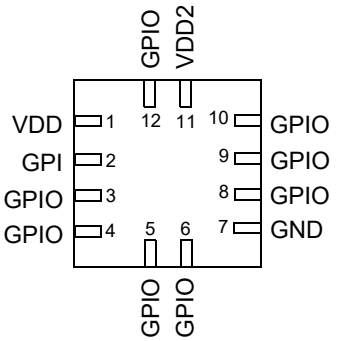
Features

- Logic & Mixed Signal Circuits
- Highly Versatile Macrocells
- 1.8 V (±5%) to 5 V (±10%) VDD
- 1.8 V (±5%) to 5 V (±10%) VDD2 (VDD2 ≤ VDD)
- Operating Temperature Range: -40°C to 85°C
- RoHS Compliant / Halogen-Free
- Pb-Free 12-pin STQFN: 1.6 x 1.6 x 0.55 mm, 0.4 mm pitch

Applications

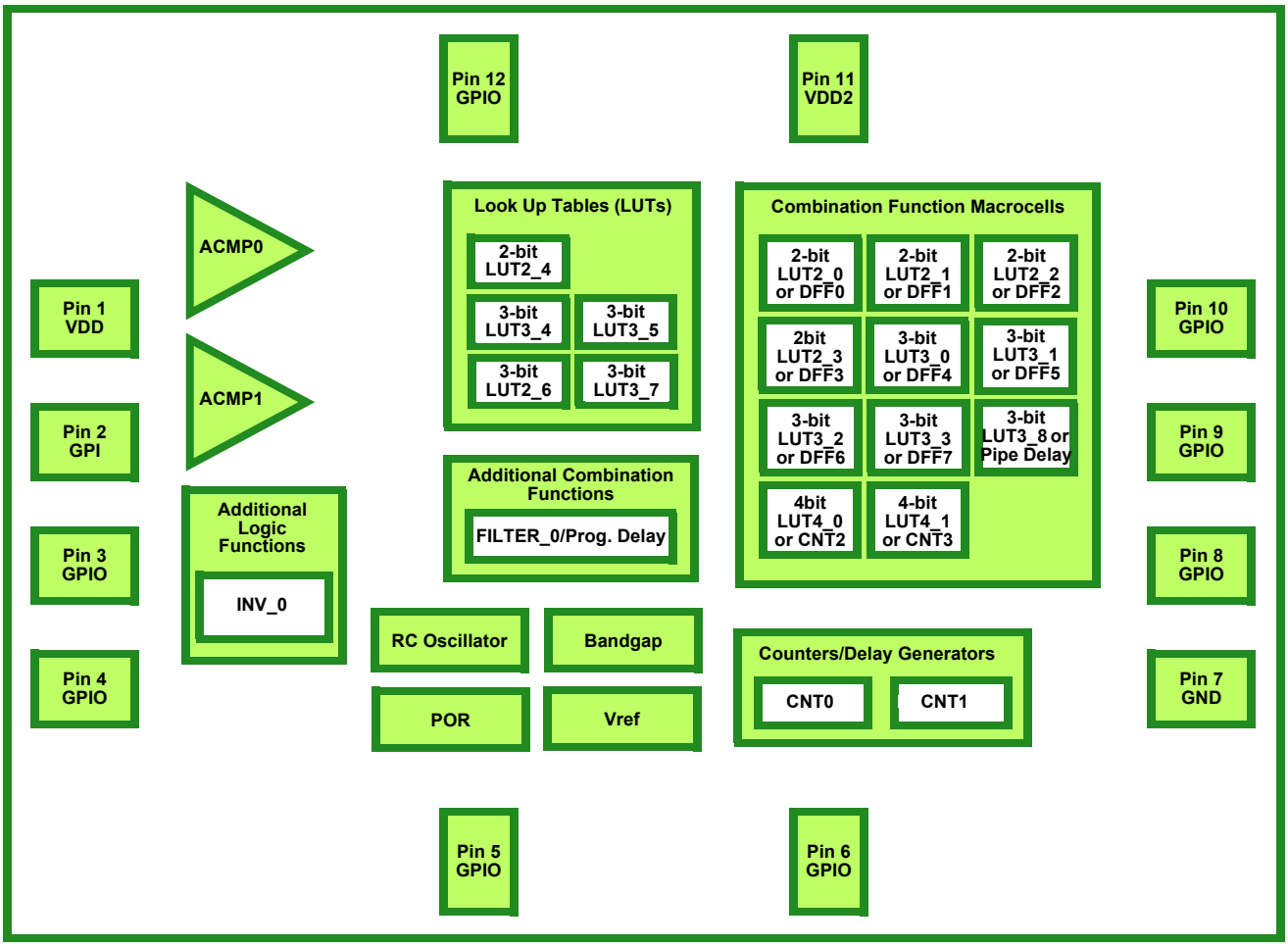
- Personal Computers and Servers
- PC Peripherals
- Consumer Electronics
- Data Communications Equipment
- Handheld and Portable Electronics

Pin Configuration



STQFN-12
(Top View)

Block Diagram



1.0 Overview

The SLG46121 provides a small, low power component for commonly used mixed-signal functions. The user creates their circuit design by programming the one time Non-Volatile Memory (NVM) to configure the interconnect logic, the I/O Pins and the macrocells of the SLG46121. This highly versatile device allows a wide variety of mixed-signal functions to be designed within a very small, low power single integrated circuit.

The additional power supply (VDD2) on the SLG46121 provides the ability to interface two independent voltage domains within the same design. Users can configure pins, dedicated to each power supply, as inputs, outputs, or both (controlled dynamically by internal logic) to both VDD and VDD2 voltage domains. Using the available macrocells designers can implement mixed-signal functions bridging both domains or simply pass through level-translation in both High to Low and Low to High directions.

The macrocells in the device include the following:

- Two Analog Comparators (ACMP)
- Voltage References (Vref)
- Five Combinatorial Look Up Tables (LUTs)
  - One 2-bit LUTs
  - Four 3-bit LUTs
- Twelve Combination Function Macrocell
  - Four Selectable DFF/Latch or 2-bit LUTs
  - Four Selectable DFF/Latch or 3-bit LUTs
  - One Selectable Pipe Delay or 3-bit LUT
    - Pipe Delay – 8 stage / 2 output, one 1 stage fixed output
  - Two Selectable Counter/Delay or 4-bit LUT
  - One Programmable Delay / Deglitch Filter
- Two Counter / Delay Generators (CNT/DLY)
  - One 8-bit counter/delay
  - One 14-bit counter/delay with external clock/reset
- Eight D Flip-Flop / Latches (DFF) (Part of Combination Function Macrocell)
- Additional Logic Function - 1 Inverter
- Pipe Delay – 8 stage/2 output (Part of Combination Function Macrocell)
- One Bandgap
- RC Oscillator (RC OSC)
- Power On Reset (POR)

2.0 Pin Description

2.1 Functional Pin Description

Pin #	Pin Name	Function
1	VDD	Power Supply (PIN 2, 3, 4, 5, 6)
2	GPI	General Purpose Input
3	GPIO	General Purpose I/O or Analog Comparator 0 (+)
4	GPIO	General Purpose I/O or Analog Comparator 0 (-)
5	GPIO	General Purpose I/O
6	GPIO	General Purpose I/O or Analog Comparator 1 (+) with OE
7	GND	Ground
8	GPIO	General Purpose I/O
9	GPIO	General Purpose I/O
10	GPIO	General Purpose I/O with OE and Vref output
11	VDD2	Power Supply (PIN 8, 9, 10, 12)
12	GPIO	General Purpose I/O or External Clock Input

3.0 User Programmability

Non-volatile memory (NVM) is used to configure the SLG46121's connection matrix routing and macrocells. The NVM is One-Time-Programmable (OTP). However, Silego's GreenPAK development tools can be used to configure the connection matrix and macrocells, without programming the NVM, to allow on-chip emulation. This configuration will remain active on the device as long as it remains powered and can be re-written as needed to facilitate rapid design changes.

When a design is ready for in-circuit testing, the same GreenPAK development tools can be used to program the NVM and create samples for small quantity builds. Once the NVM is programmed, the device will retain this configuration for the duration of its lifetime.

Once the design is finalized, the design file can be forwarded to Silego to integrate into the production process.

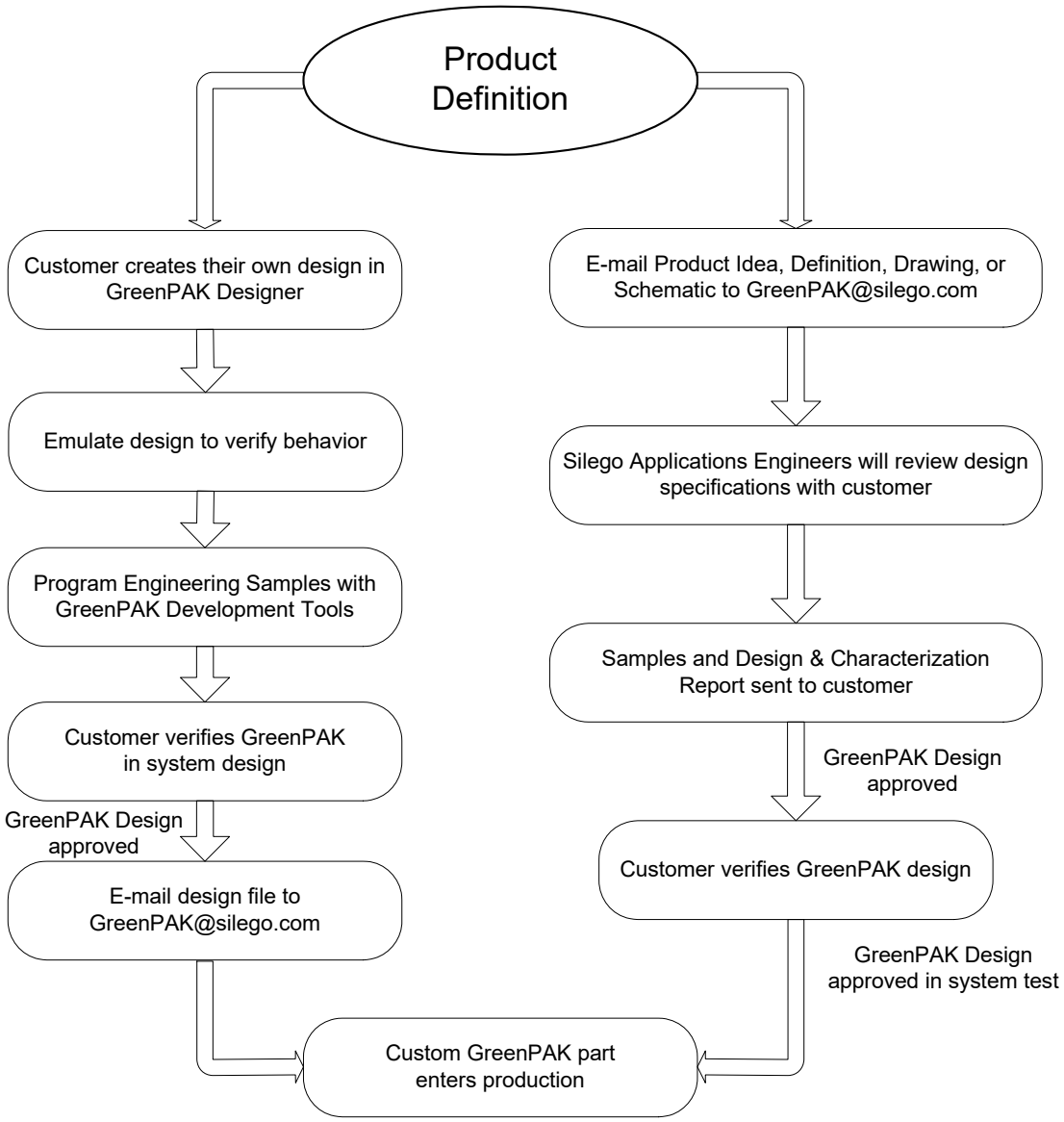


Figure 1. Steps to create a custom Silego GreenPAK device

4.0 Ordering Information

Part Number	Type
SLG46121V	12-pin STQFN
SLG46121VTR	12-pin STQFN - Tape and Reel (3k units)

5.0 Electrical Specifications

5.1 Absolute Maximum Conditions

Parameter		Min.	Max.	Unit
Supply voltage on VDD relative to GND		-0.5	7	V
Supply voltage on VDD2 relative to GND		-0.5	VDD + 0.5	V
DC Input voltage	Pins 2,3,4,5,6	GND - 0.5	VDD + 0.5	V
	Pins 8,9,10,12		VDD2 + 0.5	
Maximum Average or DC Current (Through pin)	Push-Pull 1x	--	12	mA
	Push-Pull 2x	--	17	
	OD 1x	--	18	
	OD 2x	--	28	
Current at Input Pin		-1.0	1.0	mA
Storage Temperature Range		-65	150	°C
Junction Temperature		--	150	°C
ESD Protection (Human Body Model)		2000	--	V
ESD Protection (Charged Device Model)		500	--	V
Moisture Sensitivity Level		1		

5.2 Electrical Characteristics (1.8V ±5% V_{DD})

Symbol	Parameter	Condition/Note	Min.	Typ.	Max.	Unit
V_{DD}	Supply Voltage	VDD2 ≤ VDD	1.71	1.80	1.89	V
I_Q	Quiescent Current	Static Inputs and Outputs (when ACMP, Vref and RC OSC are powered down and non-operational)	--	0.5	--	µA
T_A	Operating Temperature		-40	25	85	°C
V_{PP}	Programming Voltage		7.25	7.50	7.75	V
V_{ACMP}	ACMP Input Voltage Range	Positive Input	0	--	V_{DD}	
		Negative Input	0	--	1.1	
V_{IH}	HIGH-Level Input Voltage PIN 2, 3, 4, 5, 6	Logic Input	1.100	--	V_{DD}	V
		Logic Input with Schmitt Trigger	1.270	--	V_{DD}	V
		Low-Level Logic Input	0.980	--	V_{DD}	V
V_{IL}	LOW-Level Input Voltage PIN 2, 3, 4, 5, 6	Logic Input	--	--	0.690	V
		Logic Input with Schmitt Trigger	--	--	0.440	V
		Low-Level Logic Input	--	--	0.520	V
V_{HYS}	Schmitt Trigger Hysteresis Voltage	Logic Input with Schmitt Trigger	0.280	0.445	0.600	V
I_{LGK}	Input leakage PIN 2, 3, 4, 5, 6 (Absolute Value)		--	1	1000	nA
V_{OH}	HIGH-Level Output Voltage PIN 2, 3, 4, 5, 6	Push-Pull 1X, Open Drain PMOS 1X, I_{OH} = 100 µA	1.680	1.790	--	V
		Push-Pull 2X, Open Drain PMOS 2X, I_{OH} = 100 µA	1.700	1.800	--	V

Symbol	Parameter	Condition/Note	Min.	Typ.	Max.	Unit
V_{OL}	LOW-Level Output Voltage PIN 2, 3, 4, 5, 6	Push-Pull 1X, I_{OL}= 100 µA	--	0.020	0.030	V
		Push-Pull 2X, I_{OL}= 100 µA	--	0.010	0.020	V
		Open Drain NMOS 1X, I_{OL}= 100 µA	--	0.010	0.020	V
		Open Drain NMOS 2X, I_{OL}= 100 µA	--	0.010	0.010	V
I_{OH}	HIGH-Level Output Current (see Note 1) PIN 2, 3, 4, 5, 6	Push-Pull 1X, Open Drain PMOS 1X, $V_{OH} = V_{DD}$ - 0.2	1.000	1.390	--	mA
		Push-Pull 2X, Open Drain PMOS 2X, $V_{OH} = V_{DD}$ - 0.2	2.100	2.680	--	mA
I_{OL}	LOW-Level Output Current (see Note 1) PIN 2, 3, 4, 5, 6	Push-Pull 1X, V_{OL} = 0.15 V	0.760	1.340	--	mA
		Push-Pull 2X, V_{OL} = 0.15 V	1.520	2.660	--	mA
		Open Drain NMOS 1X, V_{OL} = 0.15 V	1.530	2.670	--	mA
		Open Drain NMOS 2X, V_{OL} = 0.15 V	3.060	5.136	--	mA
I_{VDD}	Maximum Average or DC Current Through VDD Pin (Per chip side, see Note 2)	T_J = 85°C	--	--	73	mA
		T_J = 110°C	--	--	35	mA
I_{GND}	Maximum Average or DC Current Through GND Pin (Per chip side, see Note 2)	T_J = 85°C	--	--	92	mA
		T_J = 110°C	--	--	44	mA
T_{SU}	Startup Time	from VDD rising past 1.35 V	--	0.31	--	ms
PON_{THR}	Power On Threshold	V_{DD} Level Required to Start Up the Chip	1.180	1.353	1.516	V
$POFF_{THR}$	Power Off Threshold	V_{DD} Level Required to Switch Off the Chip	0.730	0.914	1.103	V
R_{PUP}	Pull Up Resistance	1 M Pull Up	975.92	1061.05	1132.72	kΩ
		100 k Pull Up	99.56	107.15	114.11	kΩ
		10 k Pull Up	11.51	12.86	14.36	kΩ
R_{PDWN}	Pull Down Resistance	1 M Pull Down	975.32	1061.05	1133.17	kΩ
		100 k Pull Down	100.43	107.26	114.05	kΩ
		10 k Pull Down	11.17	12.48	13.86	kΩ

Note 1: DC or average current through any pin should not exceed value given in Absolute Maximum Conditions.
Note 2: The GreenPAK's power rails are divided in two sides. Pins 2, 3, 4, 5 and 6 are connected to one side, pins 8, 9, 10 and 12 to another.

5.3 Electrical Characteristics (3.3V ±10% V_{DD})

Symbol	Parameter	Condition/Note	Min.	Typ.	Max.	Unit
V_{DD}	Supply Voltage		3.0	3.3	3.6	V
I_Q	Quiescent Current	Static Inputs and Outputs (when ACMP, Vref and RC OSC are powered down and non-operational)	--	0.75	--	µA
T_A	Operating Temperature		-40	25	85	°C
V_{PP}	Programming Voltage		7.25	7.50	7.75	V
V_{ACMP}	ACMP Input Voltage Range	Positive Input	0	--	V_{DD}	V
		Negative Input	0	--	1.2	V
V_{IH}	HIGH-Level Input Voltage PIN 2, 3, 4, 5, 6	Logic Input	1.780	--	V_{DD}	V
		Logic Input with Schmitt Trigger	2.130	--	V_{DD}	V
		Low-Level Logic Input	1.130	--	V_{DD}	V
V_{IL}	LOW-Level Input Voltage PIN 2, 3, 4, 5, 6	Logic Input	--	--	1.210	V
		Logic Input with Schmitt Trigger	--	--	0.950	V
		Low-Level Logic Input	--	--	0.690	V
V_{HYS}	Schmitt Trigger Hysteresis Voltage	Logic Input with Schmitt Trigger	0.498	0.685	0.866	V
I_{LGK}	Input leakage PIN 2, 3, 4, 5, 6 (Absolute Value)		--	1	1000	nA
V_{OH}	HIGH-Level Output Voltage PIN 2, 3, 4, 5, 6	Push-Pull 1X,Open Drain PMOS 1X, I_{OH} = 3 mA	2.720	3.090	--	V
		Push-Pull 2X, Open Drain PMOS 2X, I_{OH} = 3 mA	2.850	3.190	--	V
V_{OL}	LOW-Level Output Voltage PIN 2, 3, 4, 5, 6	Push-Pull 1X, I_{OL}= 3 mA	--	0.180	0.280	V
		Push-Pull 2X, I_{OL}= 3 mA	--	0.090	0.130	V
		Open Drain NMOS 1X, I_{OL}= 3 mA	--	0.090	0.130	V
		Open Drain NMOS 2X, I_{OL}= 3 mA	--	0.050	0.070	V
I_{OH}	HIGH-Level Output Current (see Note 1) PIN 2, 3, 4, 5, 6	Push-Pull 1X, Open Drain PMOS 1X, V_{OH} = 2.4 V	6.010	10.150	--	mA
		Push-Pull 2X, Open Drain PMOS 2X, V_{OH} = 2.4 V	11.460	19.610	--	mA
I_{OL}	LOW-Level Output Current (see Note 1) PIN 2, 3, 4, 5, 6	Push-Pull 1X, V_{OL} = 0.4 V	4.060	6.440	--	mA
		Push-Pull 2X, V_{OL} = 0.4 V	8.130	12.360	--	mA
		Open Drain NMOS 1X, V_{OL} = 0.4 V	8.130	12.410	--	mA
		Open Drain NMOS 2X, V_{OL} = 0.4 V	16.260	22.900	--	mA
I_{VDD}	Maximum Average or DC Current Through VDD Pin (Per chip side, see Note 2)	T_J = 85°C	--	--	73	mA
		T_J = 110°C	--	--	35	mA

Symbol	Parameter	Condition/Note	Min.	Typ.	Max.	Unit
I_{GND}	Maximum Average or DC Current Through GND Pin (Per chip side, see Note 2)	T_J = 85°C	--	--	92	mA
		T_J = 110°C	--	--	44	mA
T_{SU}	Startup Time	from VDD rising past 1.35 V	--	0.31	--	ms
PON_{THR}	Power On Threshold	V_{DD} Level Required to Start Up the Chip	1.180	1.353	1.516	V
$POFF_{THR}$	Power Off Threshold	V_{DD} Level Required to Switch Off the Chip	0.730	0.914	1.103	V
R_{PUP}	Pull Up Resistance	1 M Pull Up	976.93	1060.60	1140.64	kΩ
		100 k Pull Up	98.50	106.38	113.21	kΩ
		10 k Pull Up	10.22	11.66	12.95	kΩ
R_{PDWN}	Pull Down Resistance	1 M Pull Down	974.63	1060.65	1132.96	kΩ
		100 k Pull Down	99.69	106.50	113.26	kΩ
		10 k Pull Down	9.94	11.46	12.85	kΩ

Note 1: DC or average current through any pin should not exceed value given in Absolute Maximum Conditions.
Note 2: The GreenPAK's power rails are divided in two sides. Pins 2, 3, 4, 5 and 6 are connected to one side, pins 8, 9, 10 and 12 to another.

5.4 Electrical Characteristics (5V ±10% V_{DD})

Symbol	Parameter	Condition/Note	Min.	Typ.	Max.	Unit
V_{DD}	Supply Voltage		4.5	5.0	5.5	V
I_Q	Quiescent Current	Static Inputs and Outputs (when ACMP, Vref and RC OSC are powered down and non-operational)	--	1.0	--	µA
T_A	Operating Temperature		-40	25	85	°C
V_{PP}	Programming Voltage		7.25	7.50	7.75	V
V_{ACMP}	ACMP Input Voltage Range	Positive Input	0	--	V_{DD}	V
		Negative Input	0	--	1.2	V
V_{IH}	HIGH-Level Input Voltage PIN 2, 3, 4, 5, 6	Logic Input	2.640	--	V_{DD}	V
		Logic Input with Schmitt Trigger	3.160	--	V_{DD}	V
		Low-Level Logic Input	1.230	--	V_{DD}	V
V_{IL}	LOW-Level Input Voltage PIN 2, 3, 4, 5, 6	Logic Input	--	--	1.840	V
		Logic Input with Schmitt Trigger	--	--	1.510	V
		Low-Level Logic Input	--	--	0.780	V
V_{HYS}	Schmitt Trigger Hysteresis Voltage	Logic Input with Schmitt Trigger	0.694	0.923	1.182	V
I_{LGK}	Input leakage PIN 2, 3, 4, 5, 6 (Absolute Value)		--	1	1000	nA
V_{OH}	HIGH-Level Output Voltage PIN 2, 3, 4, 5, 6	Push-Pull 1X,Open Drain PMOS 1X, I_{OH} = 5 mA	4.170	4.740	--	V
		Push-Pull 2X, Open Drain PMOS 2X, I_{OH} = 5 mA	4.320	4.860	--	V

Symbol	Parameter	Condition/Note	Min.	Typ.	Max.	Unit
V_{OL}	LOW-Level Output Voltage PIN 2, 3, 4, 5, 6	Push-Pull 1X, I_{OL}= 5 mA	--	0.230	0.330	V
		Push-Pull 2X, I_{OL}= 5 mA	--	0.120	0.160	V
		Open Drain NMOS 1X, I_{OL}= 5 mA	--	0.120	0.160	V
		Open Drain NMOS 2X, I_{OL}= 5 mA	--	0.700	0.090	V
I_{OH}	HIGH-Level Output Current (see Note 1) PIN 2, 3, 4, 5, 6	Push-Pull 1X, Open Drain PMOS 1X, V_{OH} = 2.4 V	21.980	29.0010	--	mA
		Push-Pull 2X, Open Drain PMOS 2X, V_{OH} = 2.4 V	41.886	55.990	--	mA
I_{OL}	LOW-Level Output Current (see Note 1) PIN 2, 3, 4, 5, 6	Push-Pull 1X, V_{OL} = 0.4 V	6.010	9.730	--	mA
		Push-Pull 2X, V_{OL} = 0.4 V	11.590	19.460	--	mA
		Open Drain NMOS 1X, V_{OL} = 0.4 V	11.760	19.460	--	mA
		Open Drain NMOS 2X, V_{OL} = 0.4 V	19.120	35.952	--	mA
I_{VDD}	Maximum Average or DC Current Through VDD Pin (Per chip side, see Note 2)	T_J = 85°C	--	--	73	mA
		T_J = 110°C	--	--	35	mA
I_{GND}	Maximum Average or DC Current Through GND Pin (Per chip side, see Note 2)	T_J = 85°C	--	--	92	mA
		T_J = 110°C	--	--	44	mA
T_{SU}	Startup Time	from VDD rising past 1.35 V	--	0.31	--	ms
PON_{THR}	Power On Threshold	V_{DD} Level Required to Start Up the Chip	1.180	1.353	1.516	V
$POFF_{THR}$	Power Off Threshold	V_{DD} Level Required to Switch Off the Chip	0.730	0.914	1.103	V
R_{PUP}	Pull Up Resistance	1 M Pull Up	972.75	1060.76	1134.23	kΩ
		100 k Pull Up	98.89	106.16	112.84	kΩ
		10 k Pull Up	9.27	11.11	12.62	kΩ
R_{PDWN}	Pull Down Resistance	1 M Pull Down	968.47	1060.59	1138.02	kΩ
		100 k Pull Down	99.49	106.23	113.02	kΩ
		10 k Pull Down	9.06	10.97	12.57	kΩ

Note 1: DC or average current through any pin should not exceed value given in Absolute Maximum Conditions.
Note 2: The GreenPAK's power rails are divided in two sides. Pins 2, 3, 4, 5 and 6 are connected to one side, pins 8, 9, 10 and 12 to another.

5.5 Electrical Characteristics (1.8V ±5% V_{DD2})

Symbol	Parameter	Condition/Note	Min.	Typ.	Max.	Unit
V_{DD2}	Supply Voltage	VDD2 ≤ VDD	1.71	1.80	1.89	V
I_{LGK}	Input leakage PIN 8, 9, 10, 12 (Absolute Value)		--	1	1000	nA
V_{IH2}	HIGH-Level Input Voltage PIN 8, 9, 10, 12	Logic Input	1.100	--	V_{DD2}	V
		Logic Input with Schmitt Trigger	1.270	--	V_{DD2}	V
		Low-Level Logic Input	0.980	--	V_{DD2}	V
V_{IL2}	LOW-Level Input Voltage PIN 8, 9, 10, 12	Logic Input	--	--	0.690	V
		Logic Input with Schmitt Trigger	--	--	0.440	V
		Low-Level Logic Input	--	--	0.520	V
V_{OH2}	HIGH-Level Output Voltage PIN 8, 9, 10, 12	Push-Pull 1X, Open Drain PMOS 1X, I_{OH} = 100 µA	1.680	1.790	--	V
		Push-Pull 2X, Open Drain PMOS 2X, I_{OH} = 100 µA	1.700	1.800	--	V
V_{OL2}	LOW-Level Output Voltage PIN 8, 9, 10, 12	Push-Pull 1X, I_{OL}= 100 µA	--	0.020	0.030	V
		Push-Pull 2X, I_{OL}= 100 µA	--	0.010	0.020	V
		Open Drain NMOS 1X, I_{OL}= 100 µA	--	0.010	0.020	V
		Open Drain NMOS 2X, I_{OL}= 100 µA	--	0.010	0.010	V
I_{OH2}	HIGH-Level Output Current (see Note 1) PIN 8, 9, 10, 12	Push-Pull 1X, Open Drain PMOS 1X, $V_{OH} = V_{DD}$ - 0.2	1.000	1.390	--	mA
		Push-Pull 2X, Open Drain PMOS 2X, $V_{OH} = V_{DD}$ - 0.2	2.100	2.680	--	mA
I_{OL2}	LOW-Level Output Current (see Note 1) PIN 8, 9, 10, 12	Push-Pull 1X, V_{OL} = 0.15 V	0.760	1.340	--	mA
		Push-Pull 2X, V_{OL} = 0.15 V	1.520	2.660	--	mA
		Open Drain NMOS 1X, V_{OL} = 0.15 V	1.530	2.670	--	mA
		Open Drain NMOS 2X, V_{OL} = 0.15 V	3.060	5.136	--	mA
I_{VDD2}	Maximum Average or DC Current Through VDD2 Pin (Per chip side, see Note 2)	T_J = 85°C	--	--	73	mA
		T_J = 110°C	--	--	35	mA
I_{GND}	Maximum Average or DC Current Through GND Pin (Per chip side, see Note 2)	T_J = 85°C	--	--	92	mA
		T_J = 110°C	--	--	44	mA

Note 1: DC or average current through any pin should not exceed value given in Absolute Maximum Conditions.
Note 2: The GreenPAK's power rails are divided in two sides. Pins 2, 3, 4, 5 and 6 are connected to one side, pins 8, 9, 10 and 12 to another.

5.6 Electrical Characteristics (3.3V ±10% V_{DD2})

Symbol	Parameter	Condition/Note	Min.	Typ.	Max.	Unit
V_{DD2}	Supply Voltage	VDD2 ≤ VDD	1.71	--	V_{DD2}	V
I_{LGK}	Input leakage PIN 8, 9, 10, 12 (Absolute Value)		--	1	1000	nA
V_{IH2}	HIGH-Level Input Voltage PIN 8, 9, 10, 12	Logic Input, V_{DD2} = 1.8 V	1.100	--	V_{DD2}	V
		Logic Input with Schmitt Trigger, V_{DD2} = 1.8 V	1.270	--	V_{DD2}	V
		Low-Level Logic Input, V_{DD2} = 1.8 V	0.980	--	V_{DD2}	V
V_{IL2}	LOW-Level Input Voltage PIN 8, 9, 10, 12	Logic Input, V_{DD2} = 1.8 V	--	--	0.690	V
		Logic Input with Schmitt Trigger, V_{DD2} = 1.8 V	--	--	0.440	V
		Low-Level Logic Input, V_{DD2} = 1.8 V	--	--	0.520	V
V_{OH2}	HIGH-Level Output Voltage PIN 8, 9, 10, 12	Push-Pull 1X, Open Drain PMOS 1X, I_{OH} = 100 µA, V_{DD2} = 1.8 V	1.680	1.790	--	V
		Push-Pull 2X, Open Drain PMOS 2X, I_{OH} = 100 µA, V_{DD2} = 1.8 V	1.700	1.800	--	V
V_{OL2}	LOW-Level Output Voltage PIN 8, 9, 10, 12	Push-Pull 1X, I_{OL}= 100 µA, V_{DD2} = 1.8 V	--	0.020	0.030	V
		Push-Pull 2X, I_{OL}= 100 µA, V_{DD2} = 1.8 V	--	0.010	0.020	V
		Open Drain NMOS 1X, I_{OL}= 100 µA, V_{DD2} = 1.8 V	--	0.010	0.020	V
		Open Drain NMOS 2X, I_{OL}= 100 µA, V_{DD2} = 1.8 V	--	0.010	0.010	V
I_{OH2}	HIGH-Level Output Current (see Note 1) PIN 8, 9, 10, 12	Push-Pull 1X, Open Drain PMOS 1X, V_{OH} = V_{DD} - 0.2, V_{DD2} = 1.8 V	1.000	1.390	--	mA
		Push-Pull 2X, Open Drain PMOS 2X, V_{OH} = V_{DD} - 0.2, V_{DD2} = 1.8 V	2.100	2.680	--	mA
I_{OL2}	LOW-Level Output Current (see Note 1) PIN 8, 9, 10, 12	Push-Pull 1X, V_{OL} = 0.15 V, V_{DD2} = 1.8 V	0.760	1.340	--	mA
		Push-Pull 2X, V_{OL} = 0.15 V, V_{DD2} = 1.8 V	1.520	2.660	--	mA
		Open Drain NMOS 1X, V_{OL} = 0.15 V, V_{DD2} = 1.8 V	1.530	2.670	--	mA
		Open Drain NMOS 2X, V_{OL} = 0.15 V, V_{DD2} = 1.8 V	3.060	5.136	--	mA
I_{VDD2}	Maximum Average or DC Current Through VDD2 Pin (Per chip side, see Note 2)	T_J = 85°C	--	--	73	mA
		T_J = 110°C	--	--	35	mA
I_{GND}	Maximum Average or DC Current Through GND Pin (Per chip side, see Note 2)	T_J = 85°C	--	--	92	mA
		T_J = 110°C	--	--	44	mA

Note 1: DC or average current through any pin should not exceed value given in Absolute Maximum Conditions.
Note 2: The GreenPAK's power rails are divided in two sides. Pins 2, 3, 4, 5 and 6 are connected to one side, pins 8, 9, 10 and 12 to another.

5.7 Electrical Characteristics (5V ±10% V_{DD2})

Symbol	Parameter	Condition/Note	Min.	Typ.	Max.	Unit
V_{DD2}	Supply Voltage	VDD2 ≤ VDD	1.71	--	V_{DD2}	V
I_{LGK}	Input leakage PIN 8, 9, 10, 12 (Absolute Value)		--	1	1000	nA
V_{IH2}	HIGH-Level Input Voltage PIN 8, 9, 10, 12	Logic Input, V_{DD2} = 3.3 V	1.780	--	V_{DD2}	V
		Logic Input with Schmitt Trigger, V_{DD2} = 3.3 V	2.130	--	V_{DD2}	V
		Low-Level Logic Input, V_{DD2} = 3.3 V	1.130	--	V_{DD2}	V
V_{IL2}	LOW-Level Input Voltage PIN 8, 9, 10, 12	Logic Input, V_{DD2} = 3.3 V	--	--	1.210	V
		Logic Input with Schmitt Trigger, V_{DD2} = 3.3 V	--	--	0.950	V
		Low-Level Logic Input, V_{DD2} = 3.3 V	--	--	0.690	V
V_{OH2}	HIGH-Level Output Voltage PIN 8, 9, 10, 12	Push-Pull 1X,Open Drain PMOS 1X, I_{OH} = 3 mA, V_{DD2} = 3.3 V	2.720	3.090	--	V
		Push-Pull 2X, Open Drain PMOS 2X, I_{OH} = 3 mA, V_{DD2} = 3.3 V	2.850	3.190	--	V
V_{OL2}	LOW-Level Output Voltage PIN 8, 9, 10, 12	Push-Pull 1X, I_{OL}= 3 mA, V_{DD2} = 3.3 V	--	0.180	0.280	V
		Push-Pull 2X, I_{OL}= 3 mA, V_{DD2} = 3.3 V	--	0.090	0.130	V
		Open Drain NMOS 1X, I_{OL}= 3 mA, V_{DD2} = 3.3 V	--	0.090	0.130	V
		Open Drain NMOS 2X, I_{OL}= 3 mA, V_{DD2} = 3.3 V	--	0.050	0.070	V
I_{OH2}	HIGH-Level Output Current (see Note 1) PIN 8, 9, 10, 12	Push-Pull 1X, Open Drain PMOS 1X, V_{OH} = 2.4 V, V_{DD2} = 3.3 V	6.010	10.150	--	mA
		Push-Pull 2X, Open Drain PMOS 2X, V_{OH} = 2.4 V, V_{DD2} = 3.3 V	11.460	19.610	--	mA
I_{OL2}	LOW-Level Output Current (see Note 1) PIN 8, 9, 10, 12	Push-Pull 1X, V_{OL} = 0.4 V, V_{DD2} = 3.3 V	4.060	6.440	--	mA
		Push-Pull 2X, V_{OL} = 0.4 V, V_{DD2} = 3.3 V	8.130	12.360	--	mA
		Open Drain NMOS 1X, V_{OL} = 0.4 V, V_{DD2} = 3.3 V	8.130	12.410	--	mA
		Open Drain NMOS 2X, V_{OL} = 0.4 V, V_{DD2} = 3.3 V	16.260	22.900	--	mA
V_{IH2}	HIGH-Level Input Voltage PIN 8, 9, 10, 12	Logic Input, V_{DD2} = 1.8 V	1.100	--	V_{DD}	V
		Logic Input with Schmitt Trigger, V_{DD2} = 1.8 V	1.270	--	V_{DD}	V
		Low-Level Logic Input, V_{DD2} = 1.8 V	0.980	--	V_{DD}	V
V_{IL2}	LOW-Level Input Voltage PIN 8, 9, 10, 12	Logic Input, V_{DD2} = 1.8 V	--	--	0.690	V
		Logic Input with Schmitt Trigger, V_{DD2} = 1.8 V	--	--	0.440	V
		Low-Level Logic Input, V_{DD2} = 1.8 V	--	--	0.520	V
I_{IH2}	HIGH-Level Input Current PIN 8, 9, 10, 12	Logic Input Pins; V_{IN} = 1.8 V, V_{DD2} = 1.8 V	-1.0	--	1.0	µA

Symbol	Parameter	Condition/Note	Min.	Typ.	Max.	Unit
I_{IL2}	LOW-Level Input Current PIN 8, 9, 10, 12	Logic Input Pins; V_{IN} = 0 V, V_{DD2} = 1.8 V	-1.0	--	1.0	µA
V_{OH2}	HIGH-Level Output Voltage PIN 8, 9, 10, 12	Push-Pull 1X, Open Drain PMOS 1X, I_{OH} = 100 µA, V_{DD2} = 1.8 V	1.680	1.790	--	V
		Push-Pull 2X, Open Drain PMOS 2X, I_{OH} = 100 µA, V_{DD2} = 1.8 V	1.700	1.800	--	V
V_{OL2}	LOW-Level Output Voltage PIN 8, 9, 10, 12	Push-Pull 1X, I_{OL}= 100 µA, V_{DD2} = 1.8 V	--	0.020	0.030	V
		Push-Pull 2X, I_{OL}= 100 µA, V_{DD2} = 1.8 V	--	0.010	0.020	V
		Open Drain NMOS 1X, I_{OL}= 100 µA, V_{DD2} = 1.8 V	--	0.010	0.020	V
		Open Drain NMOS 2X, I_{OL}= 100 µA, V_{DD2} = 1.8 V	--	0.010	0.010	V
I_{OH2}	HIGH-Level Output Current (see Note 1) PIN 8, 9, 10, 12	Push-Pull 1X, Open Drain PMOS 1X, V_{OH} = V_{DD} - 0.2, V_{DD2} = 1.8 V	1.000	1.390	--	mA
		Push-Pull 2X, Open Drain PMOS 2X, V_{OH} = V_{DD} - 0.2, V_{DD2} = 1.8 V	2.100	2.680	--	mA
I_{OL2}	LOW-Level Output Current (see Note 1) PIN 8, 9, 10, 12	Push-Pull 1X, V_{OL} = 0.15 V, V_{DD2} = 1.8 V	0.760	1.340	--	mA
		Push-Pull 2X, V_{OL} = 0.15 V, V_{DD2} = 1.8 V	1.520	2.660	--	mA
		Open Drain NMOS 1X, V_{OL} = 0.15 V, V_{DD2} = 1.8 V	1.530	2.670	--	mA
		Open Drain NMOS 2X, V_{OL} = 0.15 V, V_{DD2} = 1.8 V	3.060	5.136	--	mA
I_{VDD2}	Maximum Average or DC Current Through VDD2 Pin (Per chip side, see Note 2)	T_J = 85°C	--	--	73	mA
		T_J = 110°C	--	--	35	mA
I_{GND}	Maximum Average or DC Current Through GND Pin (Per chip side, see Note 2)	T_J = 85°C	--	--	92	mA
		T_J = 110°C	--	--	44	mA

Note 1: DC or average current through any pin should not exceed value given in Absolute Maximum Conditions.
Note 2: The GreenPAK's power rails are divided in two sides. Pins 2, 3, 4, 5 and 6 are connected to one side, pins 8, 9, 10 and 12 to another.

5.8 IDD Estimator

Table 1. Typical Current estimated for each macrocell.

Symbol	Parameter	Note	V_{DD} = 1.8V	V_{DD} = 3.3V	V_{DD} = 5.0V	Unit
I	Current	Chip Quiescent	0.5	0.8	1.0	µA
		Vref	55.7	56.0	62.5	µA
		Vref Buffer (each)	0.6	14.1	14.6	µA
		OSC 25 kHz, predivide = 1	3.1	4.7	6.4	µA
		OSC 25 kHz, predivide = 8	3.0	4.3	5.8	µA
		OSC 2 MHz, predivide = 1	29.3	51.0	79.8	µA
		OSC 2 MHz, predivide = 8	17.4	23.2	29.0	µA
		1st ACMP used (includes Vref)	59.6	60.0	66.5	µA
		Each additional ACMP add	3.9	4.0	4.0	µA

5.9 Timing Estimator

Table 2. Typical Delay estimated for each macrocell.

Symbol	Parameter	Note	V_{DD}/V_{DD2} = 1.8V		V_{DD}/V_{DD2} = 3.3V		V_{DD}/V_{DD2} = 5.0V		Unit
			rising	falling	rising	falling	rising	falling	
tpd	Delay	Digital Input without Schmitt Trigger -- Push Pull	44.2	43.5	17.8	18.2	12.7	13.0	ns
tpd	Delay	Digital Input with Schmitt Trigger -- Push Pull	43.3	42.5	17.7	18.0	12.6	13.0	ns
tpd	Delay	Low Voltage Digital input -- Push Pull	45.6	517.0	18.1	215.3	12.7	144.9	ns
tpd	Delay	Digital Input without Schmitt Trigger -- NMOS	—	83.8	—	29.9	—	19.5	ns
tpd	Delay	Output enable from pin, OE Hi-Z to 1	44.8	—	17.9	—	12.6	—	ns
tpd	Delay	Output enable from pin, OE Hi-Z to 0		43.4		17.7		12.8	ns
tpd	Delay	2-bit LUT	18.7	22.1	8.0	8.7	5.8	6.0	ns
tpd	Delay	Latch (2-bit LUT shared macrocell inputs)	26.5	30.8	11.3	12.3	8.1	8.5	ns
tpd	Delay	3-bit LUT	21.3	24.4	9.1	9.6	6.5	6.6	ns
tpd	Delay	3-bit LUT (LATCH shared macrocell inputs)	26.8	25.4	11.2	10.2	8.0	7.1	ns
tpd	Delay	Latch with nRST/nSET (3-bit LUT shared macrocell inputs)	29.7	34.7	12.6	13.9	9.1	9.6	ns
tpd	Delay	4-bit LUT (shared macrocell inputs)	34.0	32.6	14.4	13.0	10.3	9.1	ns
tpd	Delay	2-bit LUT (Latch shared macrocell inputs)	26.8	25.4	11.2	10.2	8.0	7.1	ns
tpd	Delay	CNT/DLY	44.2	38.8	18.7	16.4	13.3	11.8	ns
tpd	Delay	CNT/DLY (shared macrocell inputs)	43.2	39.7	18.4	16.8	13.0	12.1	ns
tpd	Delay	CNT3/DLY3 Rising Edge Detect (shared macrocell inputs)	38.2	—	16.0	—	11.4	—	ns
tpd	Delay	CNT3/DLY3 Falling Edge Detect (shared macrocell inputs)	—	40.4	—	16.4	—	11.6	ns
tpd	Delay	CNT3/DLY3 Both Edge Detect (shared macrocell inputs)	38.2	40.5	15.9	16.5	11.3	11.5	ns
tpd	Delay	Filter	191.6	193	77.4	77.8	50.7	52.1	ns

5.10 Typical Counter/Delay Offset Measurements

Table 3. Typical Counter/Delay Offset Measurements.

Parameter	RC OSC Freq	RC OSC Power	V_{DD} = 1.8V	V_{DD} = 3.3V	V_{DD} = 5.0V	Unit
offset	25 kHz	auto	19	14	12	µs
offset	2 MHz	auto	7	4	4	µs
frequency settling time	25 kHz	auto	19	14	12	µs
frequency settling time	2 MHz	auto	14	14	14	µs
variable (CLK period)	25 kHz	forced	0-40	0-40	0-40	µs
variable (CLK period)	2 MHz	forced	0-0.5	0-0.5	0-0.5	µs
tpd (non-delayed edge)	25 kHz/ 2 MHz	either	35	14	10	ns

5.11 Expected Delays and Widths

Table 4. Expected Delays and Widths for Programmable Delay (typical).

Symbol	Parameter	Note	V_{DD}/V_{DD2}= 1.8V	V_{DD}/V_{DD2}= 3.3V	V_{DD}/V_{DD2} = 5.0V	Unit
time1	Width, 1 cell	PDLY mode:(any)edge detect, edge detect output	256.7	120.8	110	ns
time1	Width, 2 cell	PDLY mode:(any)edge detect, edge detect output	564.4	262.7	225	ns
time1	Width, 3 cell	PDLY mode:(any)edge detect, edge detect output	873.5	405	340	ns
time1	Width, 4 cell	PDLY mode:(any)edge detect, edge detect output	11.82.3	547.5	450	ns
time2	Delay, 1 cell	PDLY mode:(any)edge detect, edge detect output	48.2	20	14	ns
time2	Delay, 2 cell	PDLY mode:(any)edge detect, edge detect output	48.2	20.1	14	ns
time2	Delay, 3 cell	PDLY mode:(any)edge detect, edge detect output	48.2	20.1	14	ns
time2	Delay, 4 cell	PDLY mode:(any)edge detect, edge detect output	48.3	20.1	14	ns
time1	Delay, 1 cell	PDLY mode: both edge delay (shared macrocell inputs)	357.9	162.2	110	ns
time1	Delay, 2 cell	PDLY mode: both edge delay (shared macrocell inputs)	666.1	304.3	220	ns
time1	Delay, 3 cell	PDLY mode: both edge delay (shared macrocell inputs)	974.7	446.3	335	ns
time1	Delay, 4 cell	PDLY mode: both edge delay (shared macrocell inputs)	1283.8	588.8	450	ns
time1	Width	CNT3/DLY3 Rising Edge Detect (shared macrocell inputs)	136.6	73.4	140	ns
time1	Width	CNT3/DLY3 Falling Edge Detect (shared macrocell inputs)	130.6	71	140	ns
time1	Width	CNT3/DLY3 Both Edge Detect (shared macrocell inputs)	133.05	72	140	ns

5.12 Typical Pulse Width Performance

Table 5. Typical Pulse Width Performance.

Parameter	V_{DD}/V_{DD2}= 1.8V	V_{DD}/V_{DD2}= 3.3V	V_{DD}/V_{DD2}= 5.0V	Unit
Filtered Pulse Width	< 150	< 55	< 35	ns

6.0 Summary of Macrocell Function

6.1 I/O Pins

- Digital Input (low voltage or normal voltage, with or without Schmitt Trigger)
- Open Drain NMOS and Open Drain PMOS Outputs
- Push Pull Outputs
- Analog I/O
- 10 kΩ/100 kΩ/1 MΩ pull-up/pull-down resistors

6.2 Connection Matrix

- Digital matrix for circuit connections based on user design

6.3 Analog Comparators (2 total)

- Selectable hysteresis 0 mV/25 mV/50 mV/200 mV and selectable gain 1x/0.5x/0.33x/0.25x

6.4 Voltage Reference

- Used for references on Analog Comparators
- Can also be driven to external pins

6.5 Combinational Logic Look Up Tables (LUTs – 5 total)

- One 2-bit Lookup Tables
- Four 3-bit Lookup Tables

6.6 Combination Function Macrocells (12 total)

- Four Selectable DFF/Latches or 2-bit LUTs
- Four Selectable DFF/Latches or 3-bit LUTs
- One Selectable Pipe Delay or 3-bit LUT
- Two Selectable CNT/DLYs or 4-bit LUTs
- One Programmable Delay or Deglitch Filter

6.7 Delays/Counters (2 total)

- One 8-bit delay/counter with external clock/reset: Range 1-255 clock cycles
- One 14-bit delay/counter with external clock: Range 1-16383 clock cycles

6.8 Pipe Delay (Part of Combination Function Macrocell)

- 8 stage / 2 output
- Two 1-8 stage selectable outputs
- One 1 stage fixed output

6.9 Additional Logic Functions (Part of Combination Function Macrocell)

- One Deglitch filter macrocell
- One Programmable Delay
  - 163 ns / 305 ns / 446 ns / 588 ns @ 3.3 V
  - Includes Edge Detection function

6.10 Additional Logic Function

- One Inverter

6.11 RC Oscillator

- 25 kHz and 2 MHz selectable frequency
- First Stage Clock pre=divider (4): OSC/1, OSC/2, OSC/4, and OSC/8
- Second stage divider control with two outputs, OUT0 and OUT1 (8): selectable (OSC/1, OSC/2, OSC/3, OSC/4, OSC/8, OSC/12, OSC/24, or OSC/64)

6.12 Power On Reset (POR)

7.0 I/O Pins

The SLG46121 has a total of 9 multi-function I/O pins which can function as either a user defined Input or Output, as well as serving as a special function (such as outputting the voltage reference). Refer to Section 2.0 Pin Description for pin definitions.

All of the 9 user defined I/O pins on the SLG46121, exept Pin 2 can serve as both digital input and digital output. Pin 2 can only serve as a digital input pin.

The high side of the user selectable push-pull or open-drain pin output structures for each GPIO is connected to either VDD or VDD2. This allows for the appropriate voltage level output compatible with each voltage domain. The level shifters are located in lower power IO PADs (pins 8, 9, 10 and 12) powered from VDD2. All configuration registers of the SLG46121 are powered from VDD, so it is possible to maintain the configuration information even after VDD2 was turned off, discharged and turned back on again.

7.1 Input Modes

Each I/O pin can be configured as a digital input pin with/without buffered Schmitt Trigger, or can also be configured as a low voltage digital input. Pins 3, 4, and 6 can also be configured to serve as analog inputs to the on-chip comparators.

7.2 Output Modes

Pins 3, 4, 5, 6, 8, 9, 10, and 12 can all be configured as digital output pins.

7.3 Pull Up/Down Resistors

All I/O pins have the option for user selectable resistors connected to the input structure. The selectable values on these resistors are 10 kΩ, 100 kΩ and 1 MΩ. In the case of Pin 2, the resistors are fixed to a pull-down configuration. In the case of all other I/O pins, the internal resistors can be configured as either pull-up or pull-downs.

7.4 I/O Register Settings

7.4.1 PIN 2 Register Settings

Table 6. PIN 2 Register Settings

Signal Function	Register Bit Address	Register Definition
PIN 2 Mode Control	reg <624:623>	00: Digital Input without Schmitt Trigger 01: Digital Input with Schmitt Trigger 10: Low Voltage Digital Input 11: Reserved
PIN 2 Pull Down Resistor Value Selection	reg <626:625>	00: Floating 01: 10 kΩ Resistor 10: 100 kΩ Resistor 11: 1 MΩ Resistor

7.4.2 PIN 3 Register Settings

Table 7. PIN 3 Register Settings

Signal Function	Register Bit Address	Register Definition
PIN 3 Mode Control	reg <629:627>	000: Digital Input without Schmitt Trigger 001: Digital Input with Schmitt Trigger 010: Low Voltage Digital Input 011: Analog Input 100: Push Pull 101: Open Drain NMOS 110: Open Drain PMOS 111: Analog Input & Open Drain NMOS
PIN 3 Pull Up/Down Resistor Value Selection	reg <631:630>	00: Floating 01: 10 kΩ Resistor 10: 100 kΩ Resistor 11: 1 MΩ Resistor
PIN 3 Pull Up/Down Resistor Selection	reg <632>	0: Pull Down Resistor 1: Pull Up Resistor
PIN3 Driver Strength Selection	reg <633>	0: 1X 1: 2X

7.4.3 PIN 4 Register Settings

Table 8. PIN 4 Register Settings

Signal Function	Register Bit Address	Register Definition
PIN 4 Mode Control	reg <636:634>	000: Digital Input without Schmitt Trigger 001: Digital Input with Schmitt Trigger 010: Low Voltage Digital Input 011: Analog Input 100: Push Pull 101: Open Drain NMOS 110: Open Drain PMOS 111: Analog Input & Open Drain NMOS
PIN 4 Pull Up/Down Resistor Value Selection	reg <638:637>	00: Floating 01: 10 kΩ Resistor 10: 100 kΩ Resistor 11: 1 MΩ Resistor
PIN 4 Pull Up/Down Resistor Selection	reg <639>	0: Pull Down Resistor 1: Pull Up Resistor
PIN 4 Driver Strength Selection	reg <640>	0: 1X 1: 2X

7.4.4 PIN 5 Register Settings

Table 9. PIN 5 Register Settings

Signal Function	Register Bit Address	Register Definition
PIN 5 Mode Control	reg <643:641>	000: Digital Input without Schmitt Trigger 001: Digital Input with Schmitt Trigger 010: Low Voltage Digital Input 011: Analog Input 100: Push Pull 101: Open Drain NMOS 110: Open Drain PMOS 111: Reserved & Open Drain NMOS
PIN 5 Pull Up/Down Resistor Value Selection	reg <645:644>	00: Floating 01: 10 kΩ Resistor 10: 100 kΩ Resistor 11: 1 MΩ Resistor
PIN 5 Pull Up/Down Resistor Selection	reg <646>	0: Pull Down Resistor 1: Pull Up Resistor
PIN 5 Driver Strength Selection	reg <647>	0: 1X 1: 2X

7.4.5 PIN 6 Register Settings

Table 10. PIN 6 Register Settings

Signal Function	Register Bit Address	Register Definition
PIN 6 Mode Control (sig_PIN6_oe =0)	reg <649:648>	00: Digital Input without Schmitt Trigger 01: Digital Input with Schmitt Trigger 10: Low Voltage Digital Input 11: Analog Input / Output
PIN 6 Mode Control (sig_PIN6_oe =1)	reg <651:650>	00: Push Pull 1X 01: Push Pull 2X 10: Open Drain NMOS 1X 11: Open Drain NMOS 2X
PIN 6 Pull Up/Down Resistor Value Selection	reg <653:652>	00: Floating 01: 10 kΩ Resistor 10: 100 kΩ Resistor 11: 1 MΩ Resistor
PIN 6 Pull Up/Down Resistor Selection	reg <654>	0: Pull Down Resistor 1: Pull Up Resistor

7.5 PIN 8 Register Settings

Table 11. PIN 8 Register Settings

Signal Function	Register Bit Address	Register Definition
PIN 8 Mode Control	reg <657:655>	000: Digital Input without Schmitt Trigger 001: Digital Input with Schmitt Trigger 010: Low Voltage Digital Input 011: Reserved 100: Push Pull 101: Open Drain NMOS 110: Open Drain PMOS 111: Open Drain NMOS
PIN 8 Pull Up/Down Resistor Value Selection	reg <659:658>	00: Floating 01: 10 kΩ Resistor 10: 100 kΩ Resistor 11: 1 MΩ Resistor
PIN 8 Pull Up/Down Resistor Selection	reg <660>	0: Pull Down Resistor 1: Pull Up Resistor
PIN 8 Driver Strength Selection	reg <661>	0: 1X 1: 2X

7.5.1 PIN 9 Register Settings

Table 12. PIN 9 Register Settings

Signal Function	Register Bit Address	Register Definition
PIN 9 Mode Control	reg <664:662>	000: Digital Input without Schmitt Trigger 001: Digital Input with Schmitt Trigger 010: Low Voltage Digital Input 011: Reserved 100: Push Pull 101: Open Drain NMOS 110: Open Drain PMOS 111: Open drain NMOS
PIN 9 Pull Up/Down Resistor Value Selection	reg <666:665>	00: Floating 01: 10 kΩ Resistor 10: 100 kΩ Resistor 11: 1 MΩ Resistor
PIN 9 Pull Up/Down Resistor Selection	reg <667>	0: Pull Down Resistor 1: Pull Up Resistor
PIN 8 Driver Strength Selection	reg <668>	0: 1X 1: 2X

7.6 PIN 10 Register Settings

Table 13. PIN 10 Register Settings

Signal Function	Register Bit Address	Register Definition
PIN 10 Mode Control (sig_PIN10_oe =0)	reg <670:669>	00: Digital Input without Schmitt Trigger 01: Digital Input with Schmitt Trigger 10: Low Voltage Digital Input 11: Analog Input
PIN 10 Mode Control (sig_PIN10_oe =1)	reg <672:671>	00: Push Pull 1X 01: Push Pull 2X 10: Open Drain NMOS 1X 11: Open Drain NMOS 2X
PIN 10 Pull Up/Down Resistor Value Selection	reg <674:673>	00: Floating 01: 10 kΩ Resistor 10: 100 kΩ Resistor 11: 1 MΩ Resistor
PIN 10 Pull Up/Down Resistor Selection	reg <675>	0: Pull Down Resistor 1: Pull Up Resistor

7.7 PIN 12 Register Settings

Table 14. PIN 12 Register Settings

Signal Function	Register Bit Address	Register Definition
PIN 12 Mode Control	reg <685:683>	000: Digital Input without Schmitt Trigger 001: Digital Input with Schmitt Trigger 010: Low Voltage Digital Input 011: Reserved 100: Push Pull 101: Open Drain NMOS 110: Open Drain NMOS 111: Open Drain NMOS
PIN 12 Pull Up/Down Resistor Value Selection	reg <687:686>	00: Floating 01: 10 kΩ Resistor 10: 100 kΩ Resistor 11: 1 MΩ Resistor
PIN 12 Pull Up/Down Resistor Selection	reg <688>	0: Pull Down Resistor 1: Pull Up Resistor
PIN 12 Driver Strength Selection	reg <689>	0: 1X 1: 2X