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SLG46140

GreenPAK
Programmable Mixed-signal Matrix

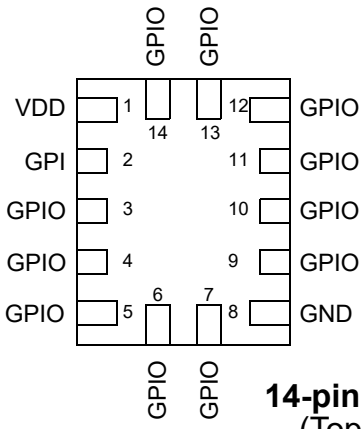
General Description

The SLG46140 GreenPAK is a one-time non-volatile memory (NVM) Programmable Mixed-Signal Matrix designed to implement a wide variety of mixed-signal functions in a single, small, low-power device by integrating a number of common discrete ICs and passive components.

Features

- Logic & Mixed Signal Circuits
- Highly Versatile Macrocells
- 1.8V (±5%) to 5V (±10%) Supply
- Operating Temperature Range: -40°C to 85°C
- RoHS Compliant / Halogen-Free
- Pb-Free: 1.6 x 2.0 x 0.55 mm, 0.4 mm pitch

Pin Configuration



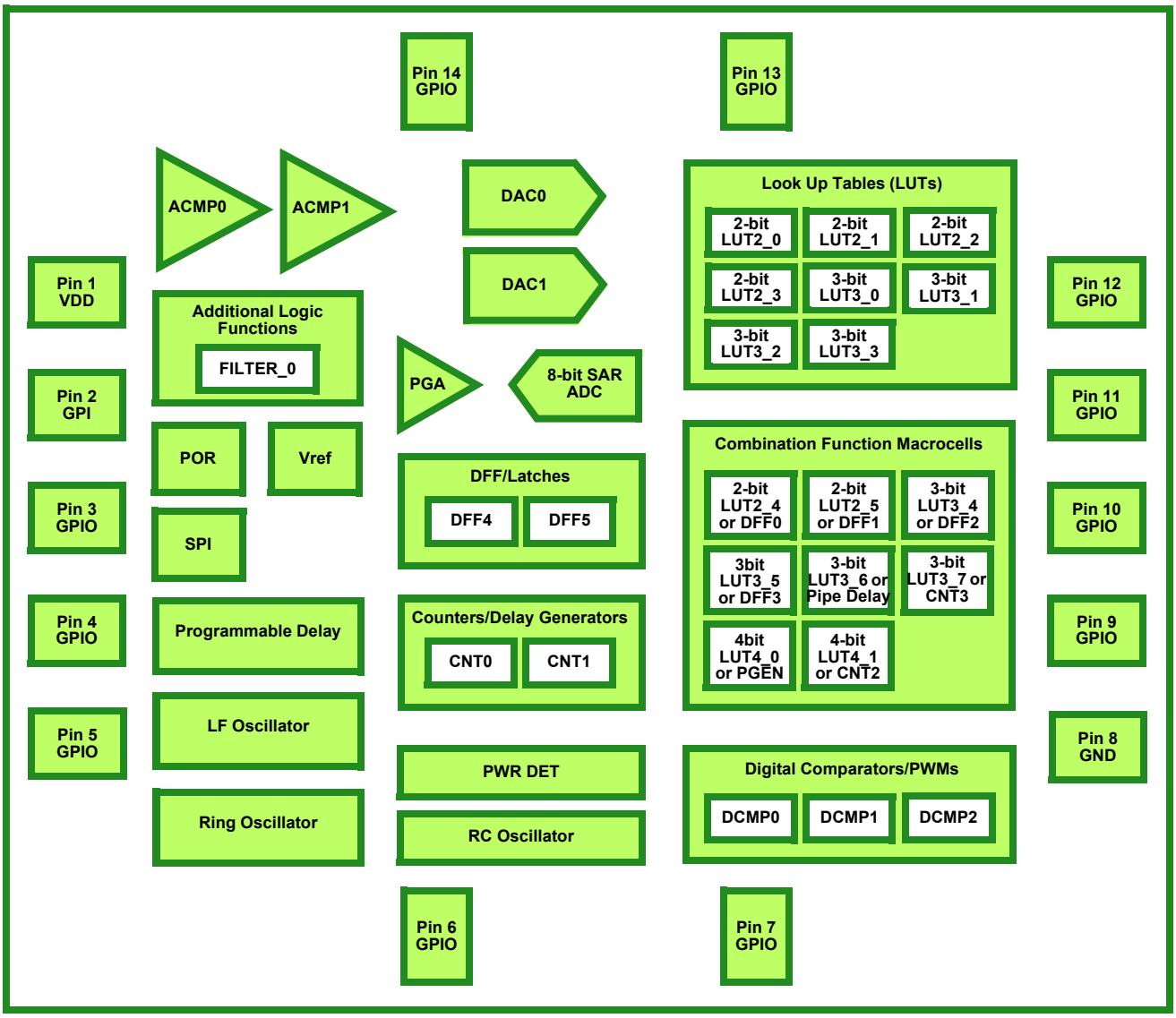
14-pin STQFN
(Top View)

Applications

The extensive list of integrated components included in the SLG46140 can be used to implement these and many other functions, often in combination.

- Ambient Light Detect
- Battery Charge Control
- Fan Control
- Hall Effect Drive
- LED Control
- Level Shift
- One-Shot Detect
- Optical Encode
- Over Voltage Protect
- Port Detection
- Power Sequencing
- Sensor Interface
- Signal De-Glitch
- Signal Delay
- System Reset
- Thermal Management
- Voltage Level Detect

Block Diagram



1.0 Overview

In addition to the integrated analog and digital components, the SLG46140 comprises an internal connection matrix and one-time programmable NVM. By programming the NVM, using the easy-to-use GreenPAK development tools, the designer configures the connection matrix, I/O Pins, and integrated components of the SLG46140. The SLG46140 includes the following analog and digital resources:

- 8-bit Successive Approximation Register Analog-to-Digital Converter (SAR ADC)
- ADC 3-bit Programmable Gain Amplifier (PGA)
- Two Digital-to-Analog Converters (DAC)
- Two Analog Comparators (ACMP)
- Voltage Reference (VREF)
- Eight Combinatorial Lookup Tables (LUTs)
  - Four 2-bit LUTs
  - Four 3-bit LUTs
- Nine Combination Function Macrocells
  - One 14-bit Delay/Counter (Wake-Sleep Control)
  - Two Selectable DFF/Latch or 2-bit LUTs
  - Two Selectable DFF/Latch or 3-bit LUTs
  - One Selectable 16-Stage / 3-Output Pipe Delay or 3-bit LUT
  - One 8-bit Delay/Counter/Finite State Machine
  - One 14-bit Delay/Counter/Finite State Machine
  - One Selectable Pattern Generator or 4-bit LUT
- Three Digital Comparators/Pulse Width Modulators (DCMPs /PWMs) w/ Selectable Deadband
- Three Counters/Delays (CNT/DLY)
  - One 14-bit Delay/Counter/Finite State Machine
  - One 14-bit Delay/Counter
  - One 8-bit Delay/Counter
- Two D Flip-flops/Latches
- Programmable Delay w/ Edge Detection
- Three Internal Oscillators
  - Low-Frequency
  - Ring
  - RC 25 kHz and 2 MHz
- Power-On-Reset (POR)
- Slave SPI
- One Bandgap

2.0 Pin Description

2.1 Functional Pin Description

Pin #	Pin Name	Function
1	VDD	Power Supply
2	GPI	General Purpose Input
3	GPIO	General Purpose I/O or ADC Vref_IO
4	GPIO	General Purpose I/O or Analog Comparator 0 (-) / PGA_OUT
5	GPIO	General Purpose I/O or Analog Comparator 1 (-)
6	GPIO	General Purpose I/O or PGA(+)
7	GPIO	General Purpose I/O or PGA(-)
8	GND	GND
9	GPIO	General Purpose I/O or ACMP1(+)
10	GPIO	General Purpose I/O or ACMP0(+)
11	GPIO	General Purpose I/O or AIN MUX
12	GPIO	General Purpose I/O
13	GPIO	General Purpose I/O
14	GPIO	General Purpose I/O

3.0 User Programmability

The SLG46140 is a user programmable device with One-Time-Programmable (OTP) memory elements that are able to construct combinatorial logic elements. Three of the I/O Pins provide a connection for the bit patterns into the OTP on board memory. A programming development kit allows the user the ability to create initial devices. Once the design is finalized, the programming code (.gpx file) is forwarded to Silego to integrate into a production process.

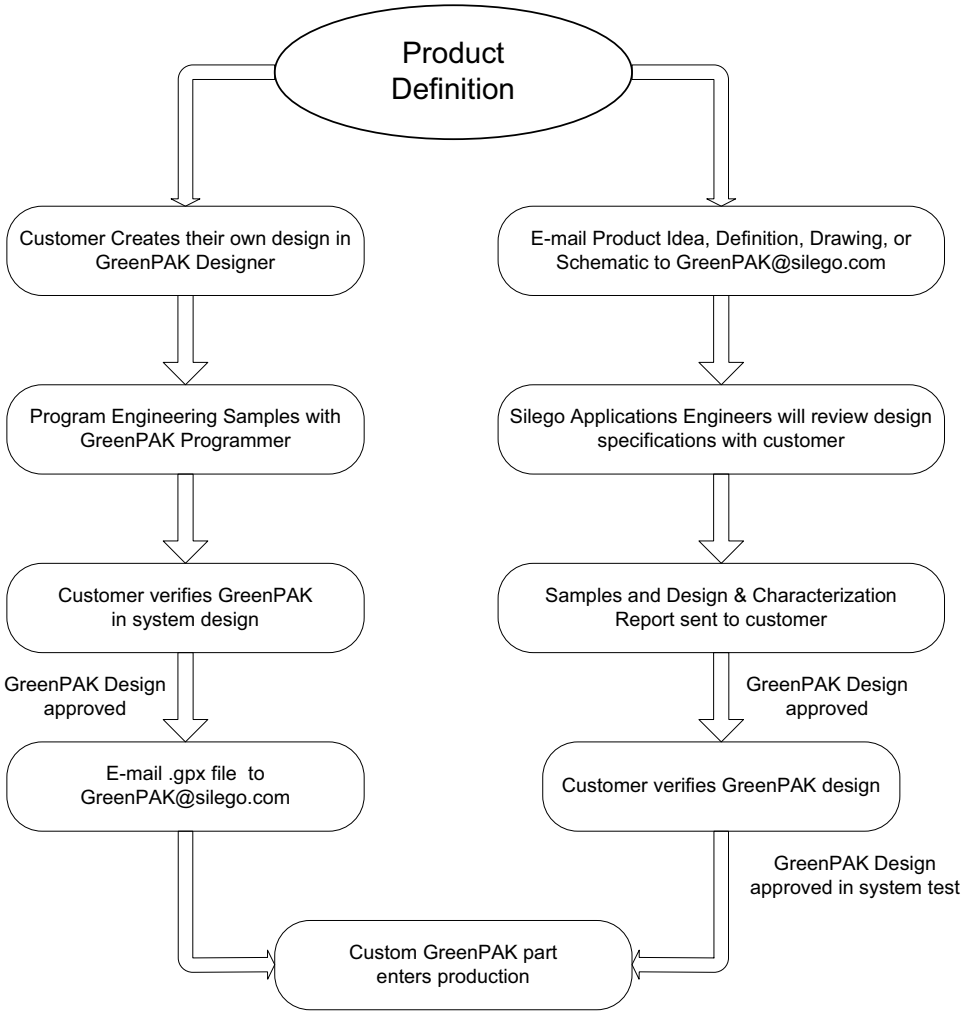


Figure 1. Steps to create a custom Silego GreenPAK device

4.0 Ordering Information

Part Number	Type
SLG46140V	14-pin STQFN
SLG46140VTR	14-pin STQFN - Tape and Reel (3k units)

5.0 Electrical Specifications

5.1 Absolute Maximum Conditions

Parameter		Min.	Max.	Unit
Supply voltage on VDD relative to GND		-0.5	7	V
DC Input voltage		GND - 0.5	VDD + 0.5	V
PGA Input voltage*	Single-ended	--	1.98/G	V
	Differential	--	(1.98 - 0.55)/G	V
	Pseudo-differential	--	(1.98 - 0.18)/G	V
Maximum Average or DC Current (Through pin)	Push-Pull 1x	--	12	mA
	Push-Pull 2x	--	21	
	Push-Pull 4x	--	43	
	OD 1x	--	18	
	OD 2x	--	45	
	OD 4x	--	72	
Current at Input Pin		-1.0	1.0	mA
Storage Temperature Range		-65	150	°C
Junction Temperature		--	150	°C
ESD Protection (Human Body Model)		2000	--	V
ESD Protection (Charged Device Model)		500	--	V
Moisture Sensitivity Level		1		

Note: IN+ relative to GND in Single-ended mode, IN+ and IN- relative to each other in Differential and Pseudo-differential modes.*

5.2 Electrical Characteristics (1.8V ±5% V_{DD})

Symbol	Parameter	Condition/Note	Min.	Typ.	Max.	Unit
V_{DD}	Supply Voltage		1.71	1.80	1.89	V
I_Q	Quiescent Current	Static Inputs and Outputs, all macrocells disabled	--	0.08	--	µA
T_A	Operating Temperature		-40	25	85	°C
V_{PP}	Programming Voltage		7.25	7.50	7.75	V
V_{ACMP}	ACMP Input Voltage Range	Positive Input	0	--	V_{DD}	V
		Negative Input	0	--	1.1	V
V_{IH}	HIGH-Level Input Voltage	Logic Input	1.100	--	V_{DD}	V
		Logic Input with Schmitt Trigger	1.270	--	V_{DD}	V
		Low-Level Logic Input	0.980	--	V_{DD}	V
V_{IL}	LOW-Level Input Voltage	Logic Input	0	--	0.690	V
		Logic Input with Schmitt Trigger	0	--	0.440	V
		Low-Level Logic Input	0	--	0.520	V
V_{HYS}	Schmitt Trigger Hysteresis Voltage	Logic Input with Schmitt Trigger	0.273	0.413	0.553	V

Symbol	Parameter	Condition/Note	Min.	Typ.	Max.	Unit
I_{LKG} (Absolute Value)	ACMP Input Leakage	Vin = 0 V	--	0.39	2.39	nA
		Vin = VDD	--	0.26	1.29	nA
	PGA Input Leakage	Vin = 0 V	--	0.04	0.18	nA
		Vin = VDD	--	0.12	0.65	nA
	Logic Input without Schmitt Trigger (Floating) Leakage	Vin = 0 V	--	0.04	0.34	nA
		Vin = VDD	--	1.55	71.77	nA
	Logic Input with Schmitt Trigger (Floating) Leakage	Vin = 0 V	--	0.04	0.39	nA
		Vin = VDD	--	1.55	72.26	nA
	Low-Level Logic Input (Floating) Leakage	Vin = 0 V	--	0.04	0.33	nA
		Vin = VDD	--	1.55	72.39	nA
V_{OH}	HIGH-Level Output Voltage	Push-Pull 1X, Open Drain PMOS 1X, I_{OH} = 100 µA	1.670	1.788	--	V
		Push-Pull 2X, Open Drain PMOS 2X, I_{OH} = 100 µA	1.679	1.792	--	V
		Push-Pull 4X, Open Drain PMOS 4X, I_{OH} = 100 µA	1.700	1.798	--	V
V_{OL}	LOW-Level Output Voltage	Push-Pull 1X, I_{OL}= 100 µA	--	0.010	0.020	V
		Push-Pull 2X, I_{OL}= 100 µA	--	0.007	0.010	V
		Push-Pull 4X, I_{OL}= 100 µA	--	0.004	0.009	V
		Open Drain NMOS 1X, I_{OL}= 100 µA	--	0.007	0.010	V
		Open Drain NMOS 2X, I_{OL}= 100 µA	--	0.002	0.010	V
		Open Drain NMOS 4X, I_{OL}= 100 µA	--	0.001	0.004	V
I_{OH}	HIGH-Level Output Pulse Current (see Note 1)	Push-Pull 1X, Open Drain PMOS 1X, $V_{OH} = V_{DD}$ - 0.2	1.053	1.690	--	mA
		Push-Pull 2X, Open Drain PMOS 2X, $V_{OH} = V_{DD}$ - 0.2	2.069	3.390	--	mA
		Push-Pull 4X, Open Drain PMOS 4X, $V_{OH} = V_{DD}$ - 0.2	4.007	7.070	--	mA
I_{OL}	LOW-Level Output Pulse Current (see Note 1)	Push-Pull 1X, V_{OL} = 0.15 V	0.760	1.420	--	mA
		Push-Pull 2X, V_{OL} = 0.15 V	1.520	2.840	--	mA
		Push-Pull 4X, V_{OL} = 0.15 V	4.430	6.122	--	mA
		Open Drain NMOS 1X, V_{OL} = 0.15 V	1.530	2.840	--	mA
		Open Drain NMOS 2X, V_{OL} = 0.15 V	3.060	5.680	--	mA
		Open Drain NMOS 4X, V_{OL} = 0.15 V	10.504	14.987	--	mA

Symbol	Parameter	Condition/Note	Min.	Typ.	Max.	Unit
I_{VDD}	Maximum Average or DC Current Through VDD Pin (Per chip side, see Note 2)	T_J = 85°C	--	--	45	mA
		T_J = 110°C	--	--	21	mA
I_{GND}	Maximum Average or DC Current Through GND Pin (Per chip side, see Note 2)	T_J = 85°C	--	--	45	mA
		T_J = 110°C	--	--	21	mA
V_O	Maximal Voltage Applied to any PIN in High-Impedance State				V_{DD}	V
T_{SU}	Startup Time (see Note 3)	from VDD rising past PON_{THR}	0.671	1.179	4.999	ms
PON_{THR}	Power On Threshold	VDD Level Required to Start Up the Chip	0.961	1.310	1.657	V
$POFF_{THR}$	Power Off Threshold	VDD Level Required to Switch Off the Chip	0.875	1.109	1.287	V
R_{PUP}	Pull Up Resistance	1 M Pull Up	896.67	1075.81	1337.85	kΩ
		100 k Pull Up	93.13	111.06	132.78	kΩ
		10 k Pull Up	11.10	12.95	15.30	kΩ
R_{PDWN}	Pull Down Resistance	1 M Pull Down	660.68	1074.06	1287.58	kΩ
		100 k Pull Down	93.29	111.06	132.78	kΩ
		10 k Pull Down	10.90	12.75	15.51	kΩ

Note 1: DC or average current through any pin should not exceed value given in Absolute Maximum Conditions.
Note 2: The GreenPAK's power rails are divided in two sides. Pins 2, 3, 4, 5, 6 and 7 are connected to one side, pins 9,10, 11, 12, 13 and 14 to another.
Note 3: VDD ramp rising speed must be less than 0.6 V/µs after power on. Violating this specification may cause chip to restart.

5.3 Electrical Characteristics (3.3V ±10% V_{DD})

Symbol	Parameter	Condition/Note	Min.	Typ.	Max.	Unit
V_{DD}	Supply Voltage		3.0	3.3	3.6	V
I_Q	Quiescent Current	Static Inputs and Outputs (when all macrocells that require internal RC OSC or bandgap are inactive)	--	0.16	--	µA
T_A	Operating Temperature		-40	25	85	°C
V_{PP}	Programming Voltage		7.25	7.50	7.75	V
V_{ACMP}	ACMP Input Voltage Range	Positive Input	0	--	V_{DD}	V
		Negative Input	0	--	1.2	V
V_{IH}	HIGH-Level Input Voltage	Logic Input	1.780	--	V_{DD}	V
		Logic Input with Schmitt Trigger	2.130	--	V_{DD}	V
		Low-Level Logic Input	1.130	--	V_{DD}	V
V_{IL}	LOW-Level Input Voltage	Logic Input	0	--	1.210	V
		Logic Input with Schmitt Trigger	0	--	0.950	V
		Low-Level Logic Input	0	--	0.690	V
V_{HYS}	Schmitt Trigger Hysteresis Voltage	Logic Input with Schmitt Trigger	0.346	0.486	0.625	V
I_{LKG} (Absolute Value)	ACMP Input Leakage	Vin = 0 V	--	0.42	2.49	nA
		Vin = VDD	--	0.30	1.48	nA
	PGA Input Leakage	Vin = 0 V	--	0.05	0.21	nA
		Vin = VDD	--	0.13	0.73	nA
	Logic Input without Schmitt Trigger (Floating) Leakage	Vin = 0 V	--	0.05	0.39	nA
		Vin = VDD	--	1.47	67.45	nA
	Logic Input with Schmitt Trigger (Floating) Leakage	Vin = 0 V	--	0.05	0.40	nA
		Vin = VDD	--	1.47	67.80	nA
	Low-Level Logic Input (Floating) Leakage	Vin = 0 V	--	0.05	0.39	nA
		Vin = VDD	--	1.47	67.84	nA
V_{OH}	HIGH-Level Output Voltage	Push-Pull 1X, Open Drain PMOS 1X, I_{OH} = 3 mA	2.722	3.102	--	V
		Push-Pull 2X, Open Drain PMOS 2X, I_{OH} = 3 mA	2.861	3.201	--	V
		Push-Pull 4X, Open Drain PMOS 4X, I_{OH} = 3 mA	2.927	3.248	--	V

Symbol	Parameter	Condition/Note	Min.	Typ.	Max.	Unit
V_{OL}	LOW-Level Output Voltage	Push-Pull 1X, I_{OL}= 3 mA	--	0.151	0.280	V
		Push-Pull 2X, I_{OL}= 3 mA	--	0.079	0.130	V
		Push-Pull 4X, I_{OL}= 3 mA	--	0.055	0.104	V
		Open Drain NMOS 1X, I_{OL}= 3 mA	--	0.070	0.130	V
		Open Drain NMOS 2X, I_{OL}= 3 mA	--	0.040	0.070	V
		Open Drain NMOS 4X, I_{OL}= 3 mA	--	0.018	0.023	V
I_{OH}	HIGH-Level Output Pulse Current (see Note 1)	Push-Pull 1X, Open Drain PMOS 1X, V_{OH} = 2.4 V	5.770	11.151	--	mA
		Push-Pull 2X, Open Drain PMOS 2X, V_{OH} = 2.4 V	11.278	21.750	--	mA
		Push-Pull 4X, Open Drain PMOS 4X, V_{OH} = 2.4 V	21.458	40.903	--	mA
I_{OL}	LOW-Level Output Pulse Current (see Note 1)	Push-Pull 1X, V_{OL} = 0.4 V	4.060	6.920	--	mA
		Push-Pull 2X, V_{OL} = 0.4 V	8.130	13.840	--	mA
		Push-Pull 4X, V_{OL} = 0.4 V	19.628	28.240	--	mA
		Open Drain NMOS 1X, V_{OL} = 0.4 V	8.130	13.850	--	mA
		Open Drain NMOS 2X, V_{OL} = 0.4 V	16.260	23.700	--	mA
		Open Drain NMOS 4X, V_{OL} = 0.4 V	45.976	66.769	--	mA
I_{VDD}	Maximum Average or DC Current Through VDD Pin (Per chip side, see Note 2)	T_J = 85°C	--	--	45	mA
		T_J = 110°C	--	--	21	mA
I_{GND}	Maximum Average or DC Current Through GND Pin (Per chip side, see Note 2)	T_J = 85°C	--	--	45	mA
		T_J = 110°C	--	--	21	mA
V_O	Maximal Voltage Applied to any PIN in High-Impedance State				VDD	V
T_{SU}	Startup Time (see Note 3)	from VDD rising past PON_{THR}	0.504	0.927	3.092	ms
PON_{THR}	Power On Threshold	VDD Level Required to Start Up the Chip	0.962	1.312	1.658	V
$POFF_{THR}$	Power Off Threshold	VDD Level Required to Switch Off the Chip	0.876	1.109	1.287	V
R_{PUP}	Pull Up Resistance	1 M Pull Up	888.18	1075.30	1316.50	kΩ
		100 k Pull Up	92.15	110.40	132.16	kΩ
		10 k Pull Up	9.83	11.99	14.49	kΩ

Symbol	Parameter	Condition/Note	Min.	Typ.	Max.	Unit
R_{PDWN}	Pull Down Resistance	1 M Pull Down	662.60	1074.47	1285.21	kΩ
		100 k Pull Down	92.42	110.60	132.48	kΩ
		10 k Pull Down	10.00	11.88	14.25	kΩ

Note 1: DC or average current through any pin should not exceed value given in Absolute Maximum Conditions.
Note 2: The GreenPAK's power rails are divided in two sides. Pins 2, 3, 4, 5, 6 and 7 are connected to one side, pins 9,10, 11, 12, 13 and 14 to another.
Note 3: VDD ramp rising speed must be less than 0.6 V/µs after power on. Violating this specification may cause chip to restart.

5.4 Electrical Characteristics (5V ±10% V_{DD})

Symbol	Parameter	Condition/Note	Min.	Typ.	Max.	Unit
V_{DD}	Supply Voltage		4.5	5.0	5.5	V
I_Q	Quiescent Current	Static Inputs and Outputs (when all macrocells that require internal RC OSC or bandgap are inactive)	--	0.25	--	µA
T_A	Operating Temperature		-40	25	85	°C
V_{PP}	Programming Voltage		7.25	7.50	7.75	V
V_{ACMP}	ACMP Input Voltage Range	Positive Input	0	--	V_{DD}	V
		Negative Input	0	--	1.2	V
V_{IH}	HIGH-Level Input Voltage	Logic Input	2.901	--	V_{DD}	V
		Logic Input with Schmitt Trigger	3.254	--	V_{DD}	V
		Low-Level Logic Input	1.209	--	V_{DD}	V
V_{IL}	LOW-Level Input Voltage	Logic Input	0	--	1.840	V
		Logic Input with Schmitt Trigger	0	--	1.510	V
		Low-Level Logic Input	0	--	0.780	V
V_{HYS}	Schmitt Trigger Hysteresis Voltage	Logic Input with Schmitt Trigger	0.443	0.618	0.792	V
I_{LKG} (Absolute Value)	ACMP Input Leakage	Vin = 0 V	--	0.70	3.30	nA
		Vin = VDD	--	0.38	1.84	nA
	PGA Input Leakage	Vin = 0 V	--	0.25	1.05	nA
		Vin = VDD	--	0.17	0.91	nA
	Logic Input without Schmitt Trigger (Floating) Leakage	Vin = 0 V	--	0.29	1.40	nA
		Vin = VDD	--	1.46	64.99	nA
	Logic Input with Schmitt Trigger (Floating) Leakage	Vin = 0 V	--	0.29	1.40	nA
		Vin = VDD	--	1.45	65.16	nA
	Low-Level Logic Input (Floating) Leakage	Vin = 0 V	--	0.29	1.40	nA
		Vin = VDD	--	1.45	66.16	nA
V_{OH}	HIGH-Level Output Voltage	Push-Pull 1X, Open Drain PMOS 1X, I_{OH} = 5 mA	4.168	4.759	--	V
		Push-Pull 2X, Open Drain PMOS 2X, I_{OH} = 5 mA	4.330	4.878	--	V
		Push-Pull 4X, Open Drain PMOS 4X, I_{OH} = 5 mA	4.405	4.932	--	V

Symbol	Parameter	Condition/Note	Min.	Typ.	Max.	Unit
V_{OL}	LOW-Level Output Voltage	Push-Pull 1X, I_{OL}= 5 mA	--	0.193	0.330	V
		Push-Pull 2X, I_{OL}= 5 mA	--	0.101	0.160	V
		Push-Pull 4X, I_{OL}= 5 mA	--	0.071	0.135	V
		Open Drain NMOS 1X, I_{OL}= 5 mA	--	0.090	0.160	V
		Open Drain NMOS 2X, I_{OL}= 5 mA	--	0.050	0.080	V
		Open Drain NMOS 4X, I_{OL}= 5 mA	--	0.021	0.030	V
I_{OH}	HIGH-Level Output Pulse Current (see Note 1)	Push-Pull 1X, Open Drain PMOS 1X, V_{OH} = 2.4 V	20.716	30.759	--	mA
		Push-Pull 2X, Open Drain PMOS 2X, V_{OH} = 2.4 V	40.059	59.691	--	mA
		Push-Pull 4X, Open Drain PMOS 4X, V_{OH} = 2.4 V	76.137	112.724	--	mA
I_{OL}	LOW-Level Output Pulse Current (see Note 1)	Push-Pull 1X, V_{OL} = 0.4 V	6.010	9.730	--	mA
		Push-Pull 2X, V_{OL} = 0.4 V	12.020	19.460	--	mA
		Push-Pull 4X, V_{OL} = 0.4 V	26.150	37.191	--	mA
		Open Drain NMOS 1X, V_{OL} = 0.4 V	12.030	19.460	--	mA
		Open Drain NMOS 2X, V_{OL} = 0.4 V	24.060	38.920	--	mA
		Open Drain NMOS 4X, V_{OL} = 0.4 V	60.071	86.737	--	mA
I_{VDD}	Maximum Average or DC Current Through VDD Pin (Per chip side, see Note 2)	T_J = 85°C	--	--	45	mA
		T_J = 110°C	--	--	21	mA
I_{GND}	Maximum Average or DC Current Through GND Pin (Per chip side, see Note 2)	T_J = 85°C	--	--	45	mA
		T_J = 110°C	--	--	21	mA
V_O	Maximal Voltage Applied to any PIN in High-Impedance State				VDD	V
T_{SU}	Startup Time (see Note 3)	from VDD rising past PON_{THR}	0.462	0.848	2.693	ms
PON_{THR}	Power On Threshold	VDD Level Required to Start Up the Chip	0.963	1.314	1.659	V
$POFF_{THR}$	Power Off Threshold	VDD Level Required to Switch Off the Chip	0.877	1.109	1.288	V
R_{PUP}	Pull Up Resistance	1 M Pull Up	884.96	1074.96	1306.99	kΩ
		100 k Pull Up	91.90	110.17	131.96	kΩ
		10 k Pull Up	8.98	11.64	14.55	kΩ

Symbol	Parameter	Condition/Note	Min.	Typ.	Max.	Unit
R_{PDWN}	Pull Down Resistance	1 M Pull Down	667.10	1074.89	1287.81	kΩ
		100 k Pull Down	92.03	110.34	132.21	kΩ
		10 k Pull Down	9.45	11.55	14.05	kΩ

Note 1: DC or average current through any pin should not exceed value given in Absolute Maximum Conditions.
Note 2: The GreenPAK's power rails are divided in two sides. Pins 2, 3, 4, 5, 6 and 7 are connected to one side, pins 9,10, 11, 12, 13 and 14 to another.
Note 3: VDD ramp rising speed must be less than 0.6 V/µs after power on. Violating this specification may cause chip to restart.

5.5 Typical Delay Estimated for Each Macrocell

Table 1. Typical Delay Estimated for Each Macrocell

Symbol	Parameter	Note	VDD=1.8V		VDD=3.3V		VDD=5.0V		Unit
			Rising	Falling	Rising	Falling	Rising	Falling	
tpd	Delay	LUT 2-bit	17.43	15.33	6.31	6.09	4.20	4.31	ns
tpd	Delay	LUT 2-bit (Shared with DFF/Latch)	21.53	20.67	8.13	8.33	5.45	6.01	ns
tpd	Delay	LUT 3-bit	18.49	15.69	6.74	6.31	4.49	4.52	ns
tpd	Delay	LUT 3-bit (Shared with DFF/Latch)	23.04	21.51	8.74	8.75	5.86	6.37	ns
tpd	Delay	LUT 3-bit (Shared with Pipe Delay)	25.65	24.01	9.37	9.47	6.67	7.32	ns
tpd	Delay	LUT 3-bit (Shared with CNT/DLY)	23.17	20.67	8.62	8.32	5.73	6.05	ns
tpd	Delay	LUT 4-bit (Shared with PGEN)	21.13	22.27	9.07	8.97	6.04	6.46	ns
tpd	Delay	LUT 4-bit (Shared with CNT/DLY)	25.42	22.29	9.54	9.02	6.41	6.59	ns
tpd	Delay	DFF (Shared with 2-bit LUT)	27.25	28.68	10.67	10.78	7.30	7.51	ns
tpd	Delay	DFF (Shared with 3-bit LUT)	27.87	28.96	10.87	10.93	7.44	7.61	ns
tpd	Delay	DFF (Shared with 3-bit LUT) nReset	--	29.84	--	12.41	--	8.95	ns
tpd	Delay	DFF (Shared with 3-bit LUT) nSet	--	36.73	--	14.00	--	9.42	ns
tpd	Delay	DFF	23.01	23.77	8.91	8.73	5.95	6.15	ns
tpd	Delay	DFF nReset	--	23.64	--	9.71	--	7.11	ns
tpd	Delay	DFF nSet	--	31.5	--	11.4	--	7.68	ns
tpd	Delay	CNT/DLY opposite to selected edge delay	46.61	36.87	18.56	15.62	12.53	11.23	ns
tpd	Delay	CNT/DLY (Shared) opposite to selected edge delay	47.30	37.16	18.78	15.78	12.68	11.77	ns
tpd	Delay	CNT/DLY Both edge detect	49.5	52.9	20.07	20.84	13.81	14.32	ns
tpd	Delay	CNT/DLY Rising edge detect	52.39	--	21.32	--	14.67	--	ns
tpd	Delay	CNT/DLY Falling edge detect	--	55.94	--	22.15	--	15.27	ns
tw	Width	CNT/DLY Both edge detect	25.17	24.93	11.98	12.01	8.76	8.83	ns
tw	Width	CNT/DLY Rising edge detect	25.76	--	12.14	--	8.86	--	ns
tw	Width	CNT/DLY Falling edge detect	--	24.51	--	11.79	--	8.57	ns
tpd	Delay	Latch (Shared with 2-bit LUT)	26.25	25.43	10.2	10.43	6.99	7.58	ns
tpd	Delay	Latch (Shared with 3-bit LUT)	26.93	25.72	10.42	10.6	7.11	7.72	ns
tpd	Delay	Latch (Shared with 3-bit LUT) nReset	--	31.8	--	13.17	--	9.61	ns
tpd	Delay	Latch (Shared with 3-bit LUT) nSet	--	34.23	--	12.97	--	8.76	ns
tpd	Delay	Latch	21.28	19.87	8.17	8.13	5.51	5.92	ns
tpd	Delay	Latch nReset	--	25.45	--	10.52	--	7.74	ns
tpd	Delay	Latch nSet	--	28.36	--	10.37	--	6.76	ns
tpd	Delay	Pipe Delay (Shared)	33.44	34.93	13.39	13.21	9.40	9.17	ns
tpd	Delay	Pipe Delay (Shared) nReset	--	35.42	--	15.07	--	11.24	ns
tpd	Delay	PGEN (Shared)	22.44	23.52	8.69	9.00	5.77	6.01	ns
tpd	Delay	PGEN (Shared) nReset to 0	--	21.73	--	8.88	--	6.60	ns
tpd	Delay	PGEN (Shared) nReset to 1	22.81	--	9.75	--	6.99	--	ns
tpd	Delay	PDLY 1Cells Both edge detect	30.71	35.23	12.00	13.45	8.42	9.26	ns
tpd	Delay	PDLY 1Cells delayed output Both edge detect	191.41	195.73	75.44	76.67	48.41	49.32	ns

Symbol	Parameter	Note	VDD=1.8V		VDD=3.3V		VDD=5.0V		Unit
			Rising	Falling	Rising	Falling	Rising	Falling	
tpd	Delay	PDLY 1Cells delayed output Rising edge detect	192.15	--	75.71	--	48.65	--	ns
tpd	Delay	PDLY 1Cells delayed output Falling edge detect	--	195.73	--	76.60	--	49.42	ns
tpd	Delay	PDLY 1Cells Rising edge detect	31.32	--	12.33	--	8.65	--	ns
tpd	Delay	PDLY 1Cells Falling edge detect	--	35.52	--	13.63	--	9.36	ns
tpd	Delay	PDLY 2Cells Both edge detect	30.68	35.23	12.04	13.47	8.44	9.25	ns
tpd	Delay	PDLY 2Cells delayed output Both edge detect	358.75	362.80	139.97	141.13	88.68	89.64	ns
tpd	Delay	PDLY 2Cells delayed output Rising edge detect	359.61	--	140.37	--	88.92	--	ns
tpd	Delay	PDLY 2Cells delayed output Falling edge detect	--	362.93	--	141.33	--	89.66	ns
tpd	Delay	PDLY 2Cells Rising edge detect	31.35	--	12.33	--	8.65	--	ns
tpd	Delay	PDLY 2Cells Falling edge detect	--	35.49	--	13.60	--	9.37	ns
tpd	Delay	PDLY 3Cells Both edge detect	30.65	35.25	12.04	13.51	8.43	9.26	ns
tpd	Delay	PDLY 3Cells delayed output Both edge detect	517.41	521.47	202.97	204.20	128.17	129.08	ns
tpd	Delay	PDLY 3Cells delayed output Rising edge detect	518.35	--	203.44	--	128.36	--	ns
tpd	Delay	PDLY 3Cells delayed output Falling edge detect	--	522.00	--	204.27	--	129.16	ns
tpd	Delay	PDLY 3Cells Rising edge detect	31.35	--	12.33	--	8.68	--	ns
tpd	Delay	PDLY 3Cells Falling edge detect	--	35.60	--	13.65	--	9.37	ns
tpd	Delay	PDLY 4Cells Both edge detect	30.76	35.23	12.03	13.53	8.42	9.25	ns
tpd	Delay	PDLY 4Cells delayed output Both edge detect	684.15	688.20	267.31	268.47	168.33	169.41	ns
tpd	Delay	PDLY 4Cells delayed output Rising edge detect	685.08	--	267.57	--	168.46	--	ns
tpd	Delay	PDLY 4Cells delayed output Falling edge detect	--	688.67	--	268.47	--	169.54	ns
tpd	Delay	PDLY 4Cells Rising edge detect	31.37	--	12.35	--	8.66	--	ns
tpd	Delay	PDLY 4Cells Falling edge detect	--	35.73	--	13.63	--	9.35	ns
tpd	Delay	PDLY Both edge delay Delayed output 1CELLs Rising	382.08	382.60	166.57	167.53	121.00	122.74	ns
tpd	Delay	PDLY Both edge delay Delayed output 2CELLs Rising	730.35	730.80	319.84	321.13	232.80	234.41	ns
tpd	Delay	PDLY Both edge delay Delayed output 3CELLs Rising	1074.28	1075.93	471.71	473.47	343.46	345.28	ns
tpd	Delay	PDLY Both edge delay Delayed output 4CELLs Rising	1421.41	1422.60	624.77	626.47	455.13	456.94	ns
tw	Width	PDLY 1Cells Both edge detect	344.67	346.13	153.20	153.73	111.89	112.43	ns
tw	Width	PDLY 1Cells delayed output Both edge detect	348.67	350.20	152.07	152.73	110.93	111.13	ns
tw	Width	PDLY 1Cells delayed output Rising edge detect	348.80	--	152.20	--	110.80	--	ns
tw	Width	PDLY 1Cells delayed output Falling edge detect	--	349.93	--	152.87	--	111.39	ns

Symbol	Parameter	Note	VDD=1.8V		VDD=3.3V		VDD=5.0V		Unit
			Rising	Falling	Rising	Falling	Rising	Falling	
tw	Width	PDLY 1Cells Rising edge detect	344.67	--	153.27	--	111.95	--	ns
tw	Width	PDLY 1Cells Falling edge detect	--	345.80	--	153.73	--	112.43	ns
tw	Width	PDLY 2Cells Both edge detect	692.87	694.27	306.80	307.33	223.53	224.33	ns
tw	Width	PDLY 2Cells delayed output Both edge detect	687.40	688.73	301.60	302.27	220.20	220.80	ns
tw	Width	PDLY 2Cells delayed output Rising edge detect	687.33	--	301.93	--	219.93	--	ns
tw	Width	PDLY 2Cells delayed output Falling edge detect	--	688.60	--	302.47	--	220.47	ns
tw	Width	PDLY 2Cells Rising edge detect	693.00	--	306.87	--	223.87	--	ns
tw	Width	PDLY 2Cells Falling edge detect	--	693.73	--	307.33	--	224.13	ns
tw	Width	PDLY 3Cells Both edge detect	1036.87	1039.20	458.53	459.93	334.20	335.27	ns
tw	Width	PDLY 3Cells delayed output Both edge detect	1034.47	1036.87	452.07	453.20	329.47	330.27	ns
tw	Width	PDLY 3Cells delayed output Rising edge detect	1034.33	--	452.27	--	329.20	--	ns
tw	Width	PDLY 3Cells delayed output Falling edge detect	--	1036.80	--	453.27	--	330.00	ns
tw	Width	PDLY 3Cells Rising edge detect	1036.73	--	458.73	--	334.47	--	ns
tw	Width	PDLY 3Cells Falling edge detect	--	1038.73	--	459.73	--	335.13	ns
tw	Width	PDLY 4Cells Both edge detect	1383.47	1385.73	611.73	612.67	445.93	446.80	ns
tw	Width	PDLY 4Cells delayed output Both edge detect	1371.27	1373.67	600.93	602.07	439.00	439.93	ns
tw	Width	PDLY 4Cells delayed output Rising edge detect	1371.47	--	601.13	--	438.73	--	ns
tw	Width	PDLY 4Cells delayed output Falling edge detect	--	1373.80	--	602.20	--	439.73	ns
tw	Width	PDLY 4Cells Rising edge detect	1383.40	--	611.67	--	446.07	--	ns
tw	Width	PDLY 4Cells Falling edge detect	--	1385.13	--	612.60	--	446.53	ns
tpd	Delay	Digital Input without Schmitt trigger -- NMOS	--	34.18	--	13.60	--	9.47	ns
tpd	Delay	Digital Input without Schmitt trigger -- NMOS 2x	--	31.88	--	12.85	--	8.97	ns
tpd	Delay	Digital Input without Schmitt trigger -- NMOS 4x	--	31.80	--	12.51	--	8.80	ns
tpd	Delay	Digital Input without Schmitt trigger -- PMOS	41.12	--	15.24	--	10.58	--	ns
tpd	Delay	Digital Input without Schmitt trigger -- PMOS 2x	40.29	--	14.93	--	10.38	--	ns
tpd	Delay	Digital Input with Schmitt Trigger -- Push Pull	41.10	35.59	15.64	15.03	10.89	10.69	ns
tpd	Delay	Low Voltage Digital Input -- Push Pull	41.67	476.4	15.39	--	10.49	120.93	ns
tpd	Delay	Digital Input without Schmitt trigger -- 3-state	40.28	34.33	15.11	14.38	10.46	10.23	ns
tpd	Delay	Digital Input without Schmitt trigger -- 3-state 2x	38.65	33.95	14.50	13.95	10.11	9.94	ns

Symbol	Parameter	Note	VDD=1.8V		VDD=3.3V		VDD=5.0V		Unit
			Rising	Falling	Rising	Falling	Rising	Falling	
tpd	Delay	Digital Input without Schmitt trigger -- 3-state 4x	37.83	33.03	14.14	13.54	9.93	9.67	ns
tpd	Delay	Digital Input without Schmitt trigger -- Push Pull Z to 1	42.03	--	15.61	--	10.78	--	ns
tpd	Delay	Digital Input without Schmitt trigger -- Push Pull Z to 0	--	36.09	--	13.83	--	9.51	ns
tpd	Delay	Digital Input without Schmitt Trigger -- Push Pull 1x	40.92	35.45	15.32	14.79	10.60	10.52	ns
tpd	Delay	Digital Input without Schmitt Trigger -- Push Pull 2x	39.61	34.98	14.8	14.37	10.31	10.17	ns
tpd	Delay	Digital Input without Schmitt Trigger -- Push Pull 4x	37.84	33.40	14.11	13.80	9.93	9.92	ns

5.6 Typical Current Consumption

Table 2. Typical Current Consumption

Note	VDD = 1.8V	VDD = 3.3V	VDD = 5.0V	Unit
Quiescent current	0.08	0.16	0.25	uA
Low frequency OSC; Clock predivider by 1	0.37	0.48	0.67	uA
Low frequency OSC; Clock predivider by 16	0.36	0.46	0.64	uA
RC OSC 25kHz; First Clock predivider by 1	4.85	5.24	6.07	uA
RC OSC 25kHz; First Clock predivider by 8	4.77	5.08	5.81	uA
RC OSC 2MHz; First Clock predivider by 1	23.94	35.78	51.44	uA
RC OSC 2MHz; First Clock predivider by 8	16.70	21.17	27.94	uA
Ring OSC; First Clock predivider by 1	70.80	83.81	116.94	uA
Ring OSC; First Clock predivider by 16	57.82	57.31	71.86	uA
ACMP; Hysteresis 0mv/25mV; Low bandwidth Disable; Input PIN10; Gain 0.25x - 1x	47.49	39.65	43.72	uA
ACMP; Hysteresis 0mV/25mV; Low bandwidth Enable; Input PIN10; Gain 1x	42.50	34.64	38.71	uA
Bandgap	37.06	29.18	33.26	uA
VREF	79.08	71.38	75.46	uA
PGA; Single-end mode; Gain 0.25x;	97.58	119.37	132.18	uA
PGA; Single-end mode; Gain 0.5x;	103.04	119.59	131.32	uA
PGA; Single-end mode; Gain 1x	69.44	73.44	77.36	uA
PGA; Single-end mode; Gain 2x	116.42	91.50	111.10	uA
PGA; Single-end mode; Gain 4x	117.87	97.20	114.72	uA
DAC0; Power on	48.24	40.40	44.47	uA
DAC1; DCMP1 Input	62.83	55.04	59.11	uA
ADC; Single-end mode; Vref: 1.2 V; Force analog part Enable; Speed selection 100 kHz + RC OSC 25 kHz; First Clock predivider by 1; Sample rate 1.56 kHz	172.24	166.10	171.01	uA
ADC; Single-end mode; Vref: 1.2 V; Force analog part Enable; Speed selection 100 kHz + RC OSC 25 kHz; First Clock predivider by 16; Sample rate 97.66 Hz	172.58	166.00	170.76	uA
ADC; Single-end mode; Vref: 1.2 V; Force analog part Enable; Speed selection 100 kHz + RC OSC 2 MHz; First Clock predivider by 16; Sample rate 7.81 kHz	190.91	196.84	216.93	uA
ADC; Single-end mode; Vref: 1.2 V; Force analog part Enable; Speed selection 100 kHz + RC OSC 2 MHz; First Clock predivider by 1; Sample rate 125.00 kHz	195.71	208.71	255.56	uA
ADC; Single-end mode; Vref: 1.2 V; Force analog part Enable; Speed selection 100 kHz + Ring OSC; First Clock predivider by 16; Sample rate 106.45 kHz	224.60	297.64	380.98	uA
ADC; Single-end mode; Vref: 1.2 V; Force analog part Enable; Speed selection 100 kHz + Ring OSC; First Clock predivider by 1; Sample rate 1.70 MHz	260.15	342.27	697.94	uA

5.7 OSC Specifications

5.7.1 25 kHz RC Oscillator

Table 3. 25 kHz RC OSC frequency limits

Power Supply Range (VDD) V	Temperature Range					
	+25 °C		0 °C ... +85 °C		-40 °C ... +85 °C	
	Minimum Value, kHz	Maximum Value, kHz	Minimum Value, kHz	Maximum Value, kHz	Minimum Value, kHz	Maximum Value, kHz
1.8 V ±5%	24.599	25.444	23.979	25.859	23.571	26.960
3.3 V ±10%	24.894	25.101	23.973	25.664	23.813	26.605
5 V ±10%	24.739	25.428	23.976	25.714	23.689	26.550
2.5 V - 4.5 V	24.842	25.147	23.937	25.691	23.803	26.642
1.71 V….5.5 V	24.380	25.701	23.891	25.989	23.429	27.036

Table 4. 25 kHz RC OSC frequency error (error calculated relative to nominal value)

Power Supply Range (VDD) V	Temperature Range					
	+25 °C		0 °C ... +85 °C		-40 °C ... +85 °C	
	Error (% at Minimum)	Error (% at Maximum)	Error (% at Minimum)	Error (% at Maximum)	Error (% at Minimum)	Error (% at Maximum)
1.8 V ±5%	-1.60%	1.78%	-4.08%	3.43%	-5.72%	7.84%
3.3 V ±10%	-0.43%	0.41%	-4.11%	2.66%	-4.75	6.42%
5 V ±10%	-1.04%	1.71%	-4.10%	2.85%	-5.25%	6.20%
2.5 V - 4.5 V	-0.63%	0.59%	-4.25%	2.76%	-4.79%	6.57%
1.71 V….5.5 V	-2.48%	2.80%	-4.44%	3.95%	-6.29%	8.14%

5.7.2 2 MHz RC Oscillator

Table 5. 2 MHz RC OSC frequency limits

Power Supply Range (VDD) V	Temperature Range					
	+25 °C		0 °C ... +85 °C		-40 °C ... +85 °C	
	Minimum Value, MHz	Maximum Value, MHz	Minimum Value, MHz	Maximum Value, MHz	Minimum Value, MHz	Maximum Value, MHz
1.8 V ±5%	1.953	2.028	1.894	2.060	1.866	2.121
3.3 V ±10%	1.972	2.031	1.928	2.075	1.832	2.095
5 V ±10%	1.944	2.173	1.905	2.200	1.802	2.200
2.5 V - 4.5 V	1.924	2.069	1.884	2.106	1.783	2.106
1.71 V….5.5 V	1.832	2.180	1.782	2.191	1.782	2.209

Table 6. 2 MHz RC OSC frequency error (error calculated relative to nominal value)

Power Supply Range (VDD) V	Temperature Range					
	+25 °C		0 °C ... +85 °C		-40 °C ... +85 °C	
	Error (% at Minimum)	Error (% at Maximum)	Error (% at Minimum)	Error (% at Maximum)	Error (% at Minimum)	Error (% at Maximum)
1.8 V ±5%	-2.36%	1.38%	-5.29%	3.02%	-6.69%	6.04%
3.3 V ±10%	-1.40%	1.57%	-3.59%	3.76%	-8.38%	4.76%
5 V ±10%	-2.82%	8.64%	-4.77%	10.00%	-9.88%	10.00%
2.5 V - 4.5 V	-3.82%	3.46%	-5.80%	5.30%	-10.86%	5.30%
1.71 V….5.5 V	-8.43%	9.02%	-10.89%	9.56%	-10.89%	10.45%

5.7.3 25 MHz Ring Oscillator

Table 7. 25 MHz Ring OSC Frequency Limits

Power Supply Range (VDD) V	Temperature Range					
	+25 °C		0 °C ... +85 °C		-40 °C ... +85 °C	
	Minimum Value, MHz	Maximum Value, MHz	Minimum Value, MHz	Maximum Value, MHz	Minimum Value, MHz	Maximum Value, MHz
1.8 V ±5%	22.482	28.084	21.855	28.084	21.855	28.084
3.3 V ±10%	23.647	28.092	23.330	28.092	22.561	28.092
5 V ±10%	23.312	28.167	22.992	28.176	22.224	28.176
2.5 V - 4.5 V	23.617	28.095	23.299	28.095	22.528	28.095
1.71 V….5.5 V	22.482	28.167	21.855	28.176	21.855	28.176

Table 8. 25 MHz Ring OSC Frequency Error (Error Calculated Relative to Nominal Value)

Power Supply Range (VDD) V	Temperature Range					
	+25 °C		0 °C ... +85 °C		-40 °C ... +85 °C	
	Error (% at Minimum)	Error (% at Maximum)	Error (% at Minimum)	Error (% at Maximum)	Error (% at Minimum)	Error (% at Maximum)
1.8 V ±5%	-11.83%	10.13%	-14.30%	10.13%	-14.30%	10.13%
3.3 V ±10%	-7.27%	10.16%	-8.51%	10.16%	-11.52%	10.16%
5 V ±10%	-8.58%	10.46%	-9.84%	10.49%	-12.85%	10.49%
2.5 V - 4.5 V	-7.38%	10.18%	-8.63%	10.18%	-11.66%	10.18%
1.71 V….5.5 V	-11.83%	10.46%	-14.30%	10.49%	-14.30%	10.49%

5.7.4 1.9 kHz LF Oscillator

Table 9. 1.9 kHz LF OSC Frequency Limits

Power Supply Range (VDD) V	Temperature Range					
	+25 °C		0 °C ... +85 °C		-40 °C ... +85 °C	
	Minimum Value, kHz	Maximum Value, kHz	Minimum Value, kHz	Maximum Value, kHz	Minimum Value, kHz	Maximum Value, kHz
1.8 V ±5%	1.619	2.264	1.606	2.273	1.537	2.289
3.3 V ±10%	1.604	2.251	1.592	2.260	1.525	2.272
5 V ±10%	1.602	2.277	1.590	2.285	1.525	2.291
2.5 V - 4.5 V	1.601	2.258	1.588	2.266	1.522	2.281
1.71 V….5.5 V	1.601	2.277	1.588	2.285	1.522	2.291

Table 10. 1.9 kHz LF OSC Frequency Error (Error Calculated Relative to Nominal Value)

Power Supply Range (VDD) V	Temperature Range					
	+25 °C		0 °C ... +85 °C		-40 °C ... +85 °C	
	Error (% at Minimum)	Error (% at Maximum)	Error (% at Minimum)	Error (% at Maximum)	Error (% at Minimum)	Error (% at Maximum)
1.8 V ±5%	-14.80%	19.18%	-15.48%	19.64%	-19.13	20.46%
3.3 V ±10%	-15.58%	18.46%	-16.23%	18.91%	-19.74%	19.56%
5 V ±10%	-15.69%	19.84%	-16.33%	20.27%	-19.75%	20.57%
2.5 V - 4.5 V	-15.74%	18.82%	-16.43%	19.25%	-19.88%	20.03%
1.71 V….5.5 V	-15.74%	19.84%	-16.43%	20.27%	-19.88%	20.57%

5.7.5 OSC Power On Delay

Table 11. Oscillators Power On Delay at Room Temperature, RC OSC Power Setting: "Auto Power On", RC OSC Clock to Matrix Input: "Enable"

Power Supply Range (VDD) V	LF OSC		RC OSC 2 MHz		RC OSC 25 kHz		RING OSC	
	Typical Value, µs	Maximum Value, µs	Typical Value, ns	Maximum Value, ns	Typical Value, µs	Maximum Value, µs	Typical Value, ns	Maximum Value, µs
1.71	496.70	691.9	717.73	1290.3	40.72	41.79	126	69.8
1.80	494.51	690.6	697.27	1172.2	40.77	41.87	109	62.6
1.89	492.70	687.3	680.73	1080.7	40.77	41.75	102	51.1
2.50	482.97	681.5	621.87	1228.4	40.94	41.84	77	19.1
2.70	480.31	680.1	613.00	989.0	41.01	42.04	72	17.2
3.00	476.72	677.1	604.33	924.5	41.15	42.13	70	15.3
3.30	473.21	675.9	598.27	878.4	41.28	42.36	66	8.4
3.60	469.91	674.1	594.67	845.8	41.38	42.30	65	7.0
4.20	463.03	665.7	589.20	803.0	41.62	42.92	61	5.4
4.50	459.00	661.3	586.67	790.2	41.72	42.90	60	5.7
5.00	451.72	641.8	579.60	773.9	41.66	42.78	57	4.5
5.50	442.70	609.03	564.07	1165.3	41.30	42.46	56	3.8

5.8 ACMP Specifications

Table 12. ACMP Specifications

Symbol	Parameter	Description/Note	Conditions	Min.	Typ.	Max.	Unit
V_{ACMP}	ACMP Input Voltage Range	Positive Input	VDD = 1.8 V ± 5 %	0	--	V_{DD}	V
		Negative Input		0	--	1.1	V
		Positive Input	VDD = 3.3 V ± 10 %	0	--	V_{DD}	V
		Negative Input		0	--	1.2	V
		Positive Input	VDD = 5.0 V ± 10 %	0	--	V_{DD}	V
		Negative Input		0	--	1.2	V
V_{offset}	ACMP Input Offset Voltage	Low Bandwidth - Enable, Vhys = 0 mV, Gain = 1, Vref = (50..1200) mV, VDD = (1.71..5.5) V	T = 25°C	-10.2	--	9.0	mV
			T = (-40..85)°C	-15.3	--	13.4	mV
		Low Bandwidth - Disable, Vhys = 0 mV, Gain =1, Vref = (50..1200) mV, VDD = (1.71..5.5) V	T = 25°C	-6.8	--	6.3	mV
			T = (-40..85)°C	-7.2	--	6.6	mV
t_{start}	ACMP Start Time	ACMP Power On delay, Minimal required wake time for the “Wake and Sleep function”, Regulator and Charge Pump set to automatic ON/OFF	BG = 550 µs, T = 25°C VDD = (1.71..5.5) V	--	406.7	1735.7	µS
			BG = 550 µs, T = (-40..85)°C VDD = (1.71..5.5) V	--	468.3	4411.9	µS
			BG = 100 µs, T = 25°C VDD = 2.7..5.5 V	--	157.3	507.5	µS
			BG = 100 µs, T = (-40..85)°C VDD = 2.7..5.5 V	--	171.2	1402.1	µS