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### 1.0 Overview

The SLG46169 provides a small, low power component for commonly used mixed-signal functions. The user creates their circuit design by programming the one time Non-Volatile Memory (NVM) to configure the interconnect logic, the I/O Pins and the macrocells of the SLG46169. This highly versatile device allows a wide variety of mixed-signal functions to be designed within a very small, low power single integrated circuit. The macrocells in the device include the following:

- Two Analog Comparators (ACMP)
- Two Voltage References (Vref)
- Nine Combinatorial Look Up Tables (LUTs)
  - Two 2-bit LUTs
  - Seven 3-bit LUTs
- Nine Combination Function Macrocells
  - Four Selectable DFF/Latch or 2-bit LUTs
  - Two Selectable DFF/Latch or 3-bit LUTs
  - One Selectable Pipe Delay or 3-bit LUT
  - Two Selectable CNT/DLY or 4-bit LUTs
- Five Counter / Delay Generators (CNT/DLY)
  - One 14-bit delay/counter
  - One 14-bit delay/counter with external clock/reset
  - Three 8-bit delays/counters
- Pipe Delay – 16 stage/3 output (Part of Combination Function Macrocell)
- Programmable Delay
- Additional Logic Functions – 2 Inverters / 2 Deglitch Filters
- RC Oscillator (RC OSC)



## 2.0 Pin Description

### 2.1 Functional and Programming Pin Description

Pin #	Pin Name	Function	Programming Function
1	VDD	Power Supply	Power Supply
2	GPI	General Purpose Input	V <sub>PP</sub> (Programming Voltage)
3	GPIO	General Purpose I/O	N/A
4	GPIO	General Purpose I/O with OE	N/A
5	GPIO	General Purpose I/O or Analog Comparator 0 (+)	N/A
6	GPIO	General Purpose I/O with OE or Analog Comparator 0 (-)	N/A
7	GPIO	General Purpose I/O with OE	N/A
8	GPIO	General Purpose I/O or Analog Comparator 1 (+)	N/A
9	GND	Ground	Ground
10	GPIO	General Purpose I/O with OE	Programming Mode Control
11	GPIO	General Purpose I/O	Programming ID Pin
12	GPIO	General Purpose I/O with OE	Programming SDIO Pin
13	GPIO	General Purpose I/O with OE and Vref output (VREF)	Programming SRDWB Pin
14	GPIO	General Purpose I/O or External Clock Input	Programming SCL Pin



### 3.0 User Programmability

Non-volatile memory (NVM) is used to configure the SLG46169's connection matrix routing and macrocells. The NVM is One-Time-Programmable (OTP). However, Silego's GreenPAK development tools can be used to configure the connection matrix and macrocells, without programming the NVM, to allow on-chip emulation. This configuration will remain active on the device as long as it remains powered and can be re-written as needed to facilitate rapid design changes.

When a design is ready for in-circuit testing, the same GreenPAK development tools can be used to program the NVM and create samples for small quantity builds. Once the NVM is programmed, the device will retain this configuration for the duration of its lifetime.

Once the design is finalized, the design file can be forwarded to Silego to integrate into the production process.

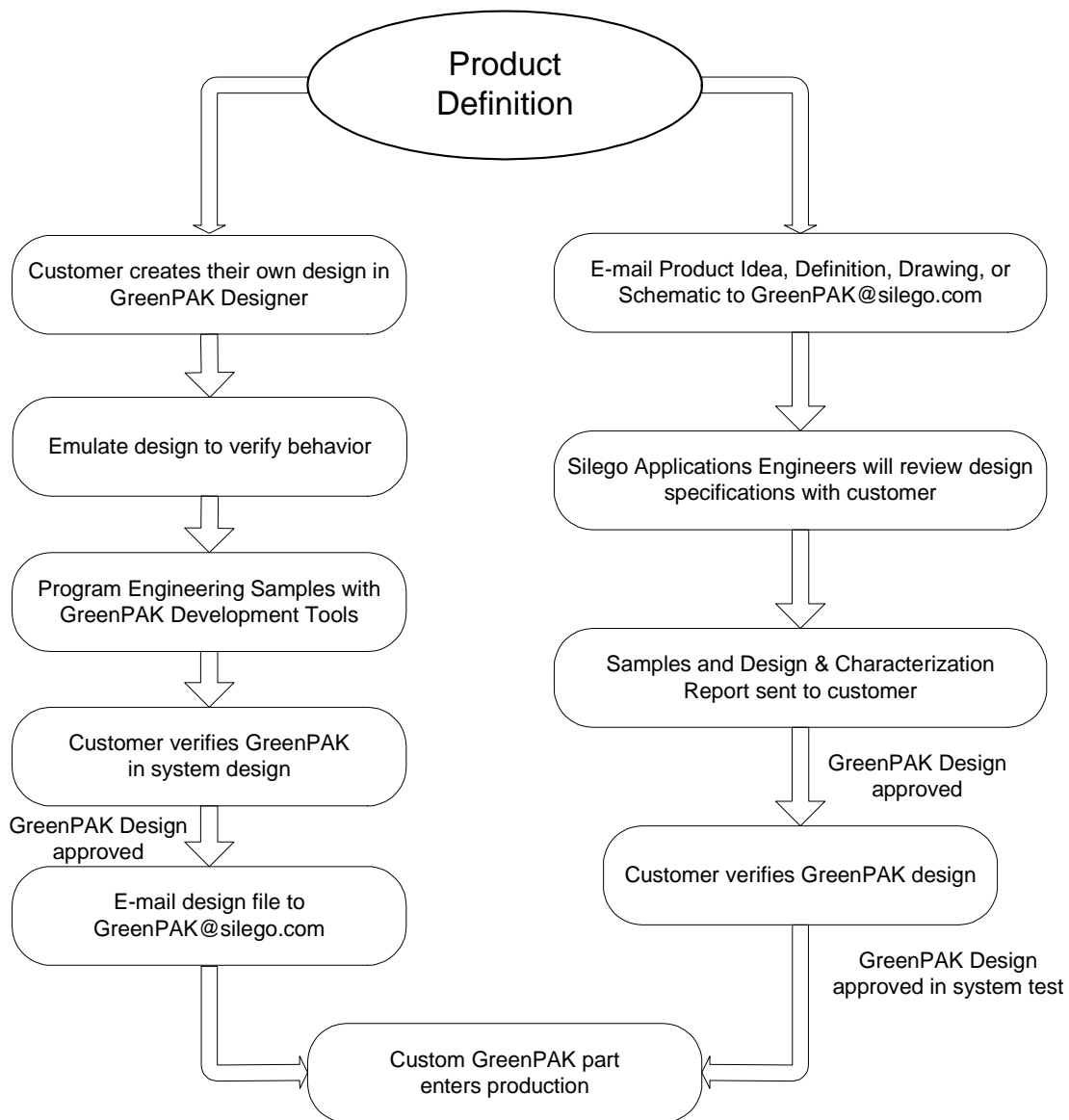


Figure 1. Steps to create a custom Silego GreenPAK device



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**4.0 Ordering Information**

Part Number	Type
SLG46169V	14-pin STQFN
SLG46169VTR	14-pin STQFN - Tape and Reel (3k units)



## 5.0 Electrical Specifications

### 5.1 Absolute Maximum Conditions

Parameter		Min.	Max.	Unit
Supply voltage on VDD relative to GND		-0.5	7	V
DC Input voltage		GND - 0.5	VDD + 0.5	V
Maximum Average or DC Current (Through pin)	Push-Pull 1x	--	8	mA
	Push-Pull 2x	--	10	
	OD 1x	--	8	
	OD 2x	--	12	
	OD 4x	--	25	
Current at Input Pin		-1.0	1.0	mA
Storage Temperature Range		-65	150	°C
Junction Temperature		--	150	°C
ESD Protection (Human Body Model)		2000	--	V
ESD Protection (Charged Device Model)		1300	--	V
Moisture Sensitivity Level		1		

### 5.2 Electrical Characteristics (1.8 V $\pm$ 5% V<sub>DD</sub>)

Symbol	Parameter	Condition/Note	Min.	Typ.	Max.	Unit
V <sub>DD</sub>	Supply Voltage		1.71	1.80	1.89	V
T <sub>A</sub>	Operating Temperature		-40	25	85	°C
V <sub>PP</sub>	Programming Voltage		7.25	7.50	7.75	V
V <sub>ACMP</sub>	ACMP Input Voltage Range	Positive Input	0	--	V <sub>DD</sub>	V
		Negative Input	0	--	1.1	V
V <sub>IH</sub>	HIGH-Level Input Voltage	Logic Input	1.100	--	--	V
		Logic Input with Schmitt Trigger	1.270	--	--	V
		Low-Level Logic Input	0.980	--	--	V
V <sub>IL</sub>	LOW-Level Input Voltage	Logic Input	--	--	0.690	V
		Logic Input with Schmitt Trigger	--	--	0.440	V
		Low-Level Logic Input	--	--	0.520	V
I <sub>LKG</sub>	Input Leakage (Absolute Value)		--	1	1000	nA
V <sub>OH</sub>	HIGH-Level Output Voltage	Push-Pull 1X, Open Drain PMOS 1X, I <sub>OH</sub> = 100 $\mu$ A	1.690	1.789	--	V
		Push-Pull 2X, Open Drain PMOS 2X, I <sub>OH</sub> = 100 $\mu$ A	1.700	1.794	--	V



Symbol	Parameter	Condition/Note	Min.	Typ.	Max.	Unit
V <sub>OL</sub>	LOW-Level Output Voltage	Push-Pull 1X, I <sub>OL</sub> = 100 μA	--	0.008	0.030	V
		Push-Pull 2X, I <sub>OL</sub> = 100 μA	--	0.004	0.010	V
		Open Drain NMOS 1X, I <sub>OL</sub> = 100 μA	--	0.005	0.020	V
		Open Drain NMOS 2X, I <sub>OL</sub> = 100 μA	--	0.003	0.010	V
		Open Drain NMOS 4X, I <sub>OL</sub> = 100 μA	--	0.003	0.004	V
I <sub>OH</sub>	HIGH-Level Output Current (see Note 1)	Push-Pull 1X, Open Drain PMOS 1X, V <sub>OH</sub> = V <sub>DD</sub> - 0.2 V	1.066	1.703	--	mA
		Push-Pull 2X, Open Drain PMOS 2X, V <sub>OH</sub> = V <sub>DD</sub> - 0.2 V	2.216	3.406	--	mA
I <sub>OL</sub>	LOW-Level Output Current (see Note 1)	Push-Pull 1X, V <sub>OL</sub> = 0.15 V	0.917	1.689	--	mA
		Push-Pull 2X, V <sub>OL</sub> = 0.15 V	1.834	3.378	--	mA
		Open Drain NMOS 1X, V <sub>OL</sub> = 0.15 V	1.375	2.534	--	mA
		Open Drain NMOS 2X, V <sub>OL</sub> = 0.15 V	2.750	5.068	--	mA
		Open Drain NMOS 4X Drive, V <sub>OL</sub> = 0.15 V	5.500	10.136	--	mA
I <sub>VDD</sub>	Maximum Average or DC Current Through VDD Pin (Per chip side, see Note 2)	T <sub>J</sub> = 85°C	--	--	45	mA
		T <sub>J</sub> = 110°C	--	--	22	mA
I <sub>GND</sub>	Maximum Average or DC Current Through GND Pin (Per chip side, see Note 2)	T <sub>J</sub> = 85°C	--	--	84	mA
		T <sub>J</sub> = 110°C	--	--	40	mA
T <sub>SU</sub>	Startup Time	from VDD rising past 1.35 V	--	0.3	--	ms
PON <sub>THR</sub>	Power On Threshold	V <sub>DD</sub> Level Required to Start Up the Chip	1.180	1.353	1.516	V
POFF <sub>THR</sub>	Power Off Threshold	V <sub>DD</sub> Level Required to Switch Off the Chip	0.730	0.914	1.103	V

Note 1: DC or average current through any pin should not exceed value given in Absolute Maximum Conditions.  
 Note 2: The GreenPAK's power rails are divided in two sides. Pins 2, 3, 4, 5, 6, 7 and 8 are connected to one side, pins 10, 11, 12, 13 and 14 to another.

**5.3 Electrical Characteristics (3.3 V ±10% V<sub>DD</sub>)**

Symbol	Parameter	Condition/Note	Min.	Typ.	Max.	Unit
V <sub>DD</sub>	Supply Voltage		3.0	3.3	3.6	V
T <sub>A</sub>	Operating Temperature		-40	25	85	°C
V <sub>PP</sub>	Programming Voltage		7.25	7.50	7.75	V
V <sub>ACMP</sub>	ACMP Input Voltage Range	Positive Input	0	--	V <sub>DD</sub>	V
		Negative Input	0	--	1.2	V





Symbol	Parameter	Condition/Note	Min.	Typ.	Max.	Unit
V <sub>IH</sub>	HIGH-Level Input Voltage	Logic Input	1.780	--	--	V
		Logic Input with Schmitt Trigger	2.130	--	--	V
		Low-Level Logic Input	1.130	--	--	V
V <sub>IL</sub>	LOW-Level Input Voltage	Logic Input	--	--	1.210	V
		Logic Input with Schmitt Trigger	--	--	0.950	V
		Low-Level Logic Input	--	--	0.690	V
I <sub>LKG</sub>	Input Leakage (Absolute Value)		--	1	1000	nA
V <sub>OH</sub>	HIGH-Level Output Voltage	Push-Pull 1X, Open Drain PMOS 1X, I <sub>OH</sub> = 3 mA	2.735	3.120	--	V
		Push-Pull 2X, Open Drain PMOS 2X, I <sub>OH</sub> = 3 mA	2.870	3.210	--	V
V <sub>OL</sub>	LOW-Level Output Voltage	Push-Pull 1X, I <sub>OL</sub> = 3 mA	--	0.130	0.228	V
		Push-Pull 2X, I <sub>OL</sub> = 3 mA	--	0.060	0.108	V
		Open Drain NMOS 1X, I <sub>OL</sub> = 3 mA	--	0.080	0.147	V
		Open Drain NMOS 2X, I <sub>OL</sub> = 3 mA	--	0.040	0.080	V
		Open Drain NMOS 4X, I <sub>OL</sub> = 3 mA	--	0.027	0.034	V
I <sub>OH</sub>	HIGH-Level Output Current (see Note 1)	Push-Pull 1X, Open Drain PMOS 1X, V <sub>OH</sub> = 2.4 V	6.045	12.080	--	mA
		Push-Pull 2X, Open Drain PMOS 2X, V <sub>OH</sub> = 2.4 V	11.522	24.160	--	mA
I <sub>OL</sub>	LOW-Level Output Current (see Note 1)	Push-Pull 1X, V <sub>OL</sub> = 0.4 V	4.875	8.244	--	mA
		Push-Pull 2X, V <sub>OL</sub> = 0.4 V	9.750	16.488	--	mA
		Open Drain NMOS 1X, V <sub>OL</sub> = 0.4 V	7.313	12.370	--	mA
		Open Drain NMOS 2X, V <sub>OL</sub> = 0.4 V	14.541	24.740	--	mA
		Open Drain NMOS 4X Drive, V <sub>OL</sub> = 0.4 V	25.801	49.480	--	mA
I <sub>VDD</sub>	Maximum Average or DC Current Through VDD Pin (Per chip side, see Note 2)	T <sub>J</sub> = 85°C	--	--	45	mA
		T <sub>J</sub> = 110°C	--	--	22	mA
I <sub>GND</sub>	Maximum Average or DC Current Through GND Pin (Per chip side, see Note 2)	T <sub>J</sub> = 85°C	--	--	84	mA
		T <sub>J</sub> = 110°C	--	--	40	mA
T <sub>SU</sub>	Startup Time	from VDD rising past 1.35 V	--	0.3	--	ms
PON <sub>THR</sub>	Power On Threshold	V <sub>DD</sub> Level Required to Start Up the Chip	1.180	1.353	1.516	V
POFF <sub>THR</sub>	Power Off Threshold	V <sub>DD</sub> Level Required to Switch Off the Chip	0.730	0.914	1.103	V



Symbol	Parameter	Condition/Note	Min.	Typ.	Max.	Unit
<i>Note 1: DC or average current through any pin should not exceed value given in Absolute Maximum Conditions.</i>						
<i>Note 2: The GreenPAK's power rails are divided in two sides. Pins 2, 3, 4, 5, 6, 7 and 8 are connected to one side, pins 10, 11, 12, 13 and 14 to another.</i>						



## 5.4 Electrical Characteristics (5 V ±10% V<sub>DD</sub>)

Symbol	Parameter	Condition/Note	Min.	Typ.	Max.	Unit
V <sub>DD</sub>	Supply Voltage		4.5	5.0	5.5	V
T <sub>A</sub>	Operating Temperature		-40	25	85	°C
V <sub>PP</sub>	Programming Voltage		7.25	7.50	7.75	V
V <sub>ACMP</sub>	ACMP Input Voltage Range	Positive Input	0	--	V <sub>DD</sub>	V
		Negative Input	0	--	1.2	V
V <sub>IH</sub>	HIGH-Level Input Voltage	Logic Input	2.640	--	--	V
		Logic Input with Schmitt Trigger	3.160	--	--	V
		Low-Level Logic Input	1.230	--	--	V
V <sub>IL</sub>	LOW-Level Input Voltage	Logic Input	--	--	1.840	V
		Logic Input with Schmitt Trigger	--	--	1.510	V
		Low-Level Logic Input	--	--	0.780	V
I <sub>LGK</sub>	Input leakage (Absolute Value)		--	1	1000	nA
V <sub>OH</sub>	HIGH-Level Output Voltage	Push-Pull 1X, Open Drain PMOS 1X, I <sub>OH</sub> = 5 mA	4.190	4.780	--	V
		Push-Pull 2X, Open Drain PMOS 2X, I <sub>OH</sub> = 5 mA	4.320	4.890	--	V
V <sub>OL</sub>	LOW-Level Output Voltage	Push-Pull 1X, I <sub>OL</sub> = 5 mA	--	0.157	0.270	V
		Push-Pull 2X, I <sub>OL</sub> = 5 mA	--	0.076	0.130	V
		Open Drain NMOS 1X, I <sub>OL</sub> = 5 mA	--	0.102	0.180	V
		Open Drain NMOS 2X, I <sub>OL</sub> = 5 mA	--	0.051	0.110	V
		Open Drain NMOS 4X, I <sub>OL</sub> = 5 mA	--	0.035	0.045	V
I <sub>OH</sub>	HIGH-Level Output Current (see Note 1)	Push-Pull 1X, Open Drain PMOS 1X, V <sub>OH</sub> = 2.4 V	22.080	34.040	--	mA
		Push-Pull 2X, Open Drain PMOS 2X, V <sub>OH</sub> = 2.4 V	41.690	68.080	--	mA
I <sub>OL</sub>	LOW-Level Output Current (see Note 1)	Push-Pull 1X, V <sub>OL</sub> = 0.4 V	7.215	11.580	--	mA
		Push-Pull 2X, V <sub>OL</sub> = 0.4 V	13.831	23.160	--	mA
		Open Drain NMOS 1X, V <sub>OL</sub> = 0.4 V	10.820	17.380	--	mA
		Open Drain NMOS 2X, V <sub>OL</sub> = 0.4 V	17.343	34.760	--	mA
		Open Drain NMOS 4X Drive, V <sub>OL</sub> = 0.4 V	30.964	69.520	--	mA
I <sub>VDD</sub>	Maximum Average or DC Current Through VDD Pin (Per chip side, see Note 2)	T <sub>J</sub> = 85°C	--	--	45	mA
		T <sub>J</sub> = 110°C	--	--	22	mA



Symbol	Parameter	Condition/Note	Min.	Typ.	Max.	Unit
$I_{GND}$	Maximum Average or DC Current Through GND Pin (Per chip side, see Note 2)	$T_J = 85^{\circ}\text{C}$	--	--	84	mA
		$T_J = 110^{\circ}\text{C}$	--	--	40	mA
$T_{SU}$	Startup Time	from VDD rising past 1.35 V	--	0.3	--	ms
$PON_{THR}$	Power On Threshold	$V_{DD}$ Level Required to Start Up the Chip	1.180	1.353	1.516	V
$POFF_{THR}$	Power Off Threshold	$V_{DD}$ Level Required to Switch Off the Chip	0.730	0.914	1.103	V

Note 1: DC or average current through any pin should not exceed value given in Absolute Maximum Conditions.

Note 2: The GreenPAK's power rails are divided in two sides. Pins 2, 3, 4, 5, 6, 7 and 8 are connected to one side, pins 10, 11, 12, 13 and 14 to another.



## 5.5 IDD Estimator

Table 1. Typical Current estimated for each macrocell

Symbol	Parameter	Note	V <sub>DD</sub> = 1.8 V	V <sub>DD</sub> = 3.3V	V <sub>DD</sub> = 5.0V	Unit
I	Current	Chip Quiescent	0.5	0.8	1.0	μA
		Vref	64	78	75	μA
		Vref Buffer (each)	0.5	12	12	μA
		OSC 25 kHz, predivide = 1	3.4	5.1	7	μA
		OSC 2 MHz, predivide = 1	44	85	135	μA
		OSC 2 MHz, predivide = 8	23	33	41	μA
		1x push-pull + 4 pF @ 25 kHz	0.4	5	16	μA
		1x push-pull + 4 pF @ 2 MHz	22	47	106	μA
		1st ACMP used (includes Vref)	73	86	81	μA
		Each additional ACMP add	3.7	4.1	4.8	μA

## 5.6 Timing Estimator

Table 2. Typical Delay estimated for each macrocell

Symbol	Parameter	Note	V <sub>DD</sub> = 1.8 V		V <sub>DD</sub> = 3.3V		V <sub>DD</sub> = 5.0V		Unit
			rising	falling	rising	falling	rising	falling	
tpd	Delay	Digital input to PP 1X	42	45	17	19	12	13	ns
tpd	Delay	Digital Input with Schmitt Trigger to PP 1X	42	43	16	17	18	12	ns
tpd	Delay	Low Voltage Digital input to PP 1X	45	428	17	177	12	120	ns
tpd	Delay	Digital input to PMOS	42	-	17	-	12	-	ns
tpd	Delay	Digital input to NMOS	-	80	-	27	-	18	ns
tpd	Delay	Output enable from pin, OE Hi-Z to 1	53	-	21	-	15	-	ns
tpd	Delay	Output enable from pin, OE Hi-Z to 0	50	-	20	-	14	-	ns
tpd	Delay	LUT2bit(LATCH)	34	33	14	13	10	9	ns
tpd	Delay	LATCH(LUT2bit)	30	34	14	13	10	9	ns
tpd	Delay	LUT3bit(LATCH)	38	37	18	15	13	10	ns
tpd	Delay	LATCH+nRESET(LUT3bit)	45	42	21	17	15	12	ns
tpd	Delay	LUT4bit	28	33	14	13	10	9	ns
tpd	Delay	LUT2bt	19	26	10	10	7	7	ns
tpd	Delay	LUT3bit	28	34	14	13	10	9	ns
tpd	Delay	CNT/DLY	40	38	18	15	13	11	ns
tpd	Delay	P_DLY1C	380	377	166	163	123	120	ns
tpd	Delay	P_DLY2C	720	718	314	312	233	231	ns
tpd	Delay	P_DLY3C	1061	1060	462	460	343	341	ns
tpd	Delay	P_DLY4C	1396	1400	609	609	451	451	ns
tpd	Delay	Filter	200	200	78	78	53	53	ns
tpd	Delay	ACMP (5mV across inputs)	3000	3000	2000	2000	2000	2000	ns
tw	width	I/O with 1X push pull (min transmitted)	20	20	20	20	20	20	ns
tw	width	filter (min transmitted)	150	150	55	55	35	35	ns



## 5.7 Typical Counter/Delay Offset Measurements

Table 3. Typical Counter/Delay Offset Measurements

Parameter	RC OSC Freq	RC OSC Power	V <sub>DD</sub> = 1.8 V	V <sub>DD</sub> = 3.3V	V <sub>DD</sub> = 5.0V	Unit
offset	25kHz	auto	19	14	12	μs
offset	2MHz	auto	7	4	4	μs
frequency settling time	25kHz	auto	19	14	12	μs
frequency settling time	2MHz	auto	14	14	14	μs
variable (CLK period)	25kHz	forced	0-40	0-40	0-40	μs
variable (CLK period)	2MHz	forced	0-0.5	0-0.5	0-0.5	μs
tpd (non-delayed edge)	25kHz/2MHz	either	35	14	10	ns

## 5.8 Expected Delays and Widths

Table 4. Expected Delays and Widths for Programmable Delay (typical)

Symbol	Parameter	Note	V <sub>DD</sub> = 1.8 V	V <sub>DD</sub> = 3.3V	V <sub>DD</sub> = 5.0V	Unit
time1	Width, 1 cell	mode:(any)edge detect, edge detect output	325	150	110	ns
time1	Width, 2 cell	mode:(any)edge detect, edge detect output	740	300	225	ns
time1	Width, 3 cell	mode:(any)edge detect, edge detect output	1020	450	340	ns
time1	Width, 4 cell	mode:(any)edge detect, edge detect output	1350	600	450	ns
time2	Delay, 1 cell	mode:(any)edge detect, edge detect output	44	18	14	ns
time2	Delay, 2 cell	mode:(any)edge detect, edge detect output	44	18	14	ns
time2	Delay, 3 cell	mode:(any)edge detect, edge detect output	44	18	14	ns
time2	Delay, 4 cell	mode:(any)edge detect, edge detect output	44	18	14	ns
time1	Width, 1 cell	mode: delayed (any)edge detect, delayed edge detect output	340	150	110	ns
time1	Width, 2 cell	mode: delayed (any)edge detect, delayed edge detect output	670	300	220	ns
time1	Width, 3 cell	mode: delayed (any)edge detect, delayed edge detect output	1000	450	335	ns
time1	Width, 4 cell	mode: delayed (any)edge detect, delayed edge detect output	1340	600	450	ns
time2	Delay, 1 cell	mode: delayed (any)edge detect, delayed edge detect output	570	220	140	ns
time2	Delay, 2 cell	mode: delayed (any)edge detect, delayed edge detect output	570	220	140	ns
time2	Delay, 3 cell	mode: delayed (any)edge detect, delayed edge detect output	570	220	140	ns
time2	Delay, 4 cell	mode: delayed (any)edge detect, delayed edge detect output	570	220	140	ns
time2	Delay, 1 cell	mode: both edge delay, edge detect output	382	375	126	ns
time2	Delay, 2 cell	mode: both edge delay, edge detect output	713	169	237	ns
time2	Delay, 3 cell	mode: both edge delay, edge detect output	1045	318	350	ns
time2	Delay, 4 cell	mode: both edge delay, edge detect output	1370	466	460	ns
time2	Delay, 1 cell	mode: both edge delay, delayed edge detect output	900	613	250	ns
time2	Delay, 2 cell	mode: both edge delay, delayed edge detect output	1250	520	360	ns

**Table 4. Expected Delays and Widths for Programmable Delay (typical)**

Symbol	Parameter	Note	V <sub>DD</sub> = 1.8 V	V <sub>DD</sub> = 3.3V	V <sub>DD</sub> = 5.0V	Unit
time2	Delay, 3 cell	mode: both edge delay, delayed edge detect output	1600	680	480	ns
time2	Delay, 4 cell	mode: both edge delay, delayed edge detect output	1900	815	600	ns

### 5.9 Typical Pulse Width Performance

**Table 5. Typical Pulse Width Performance**

Parameter	V <sub>DD</sub> = 1.8 V	V <sub>DD</sub> = 3.3V	V <sub>DD</sub> = 5.0V	Unit
Filtered Pulse Width for Filter 0 and Filter 1	< 150	< 55	< 35	ns

### 5.10 OSC Specifications

**Table 6. 25 kHz RC OSC frequency limits**

Power Supply Range (VDD) V	Temperature Range			
	+25 °C		-40 °C ... +85 °C	
	Minimum Value, kHz	Maximum Value, kHz	Minimum Value, kHz	Maximum Value, kHz
1.8 V ±5%	24.044	25.969	19.924	29.122
3.3 V ±10%	24.395	25.609	20.383	28.363
5 V ±10%	24.297	25.702	20.371	28.337
2.5 V ... 4.5 V	24.163	25.873	20.288	28.397
1.71 V... 5.5 V	23.506	28.006	19.381	29.378

**Table 7. 25 kHz RC OSC frequency error (error calculated relative to nominal value)**

Power Supply Range (VDD) V	Temperature Range			
	+25 °C		-40 °C ... +85 °C	
	Error (% at Minimum)	Error (% at Maximum)	Error (% at Minimum)	Error (% at Maximum)
1.8 V ±5%	-3.82%	3.88%	-20.30%	16.49%
3.3 V ±10%	-2.42%	2.44%	-18.47%	13.45%
5 V ±10%	-2.81%	2.81%	-18.52%	13.35%
2.5 V ... 4.5 V	-3.35%	3.49%	-18.85%	13.58%
1.71 V... 5.5 V	-5.98%	12.02%	-22.48%	17.51%



## 5.10.1 2 MHz RC Oscillator

Table 8. 2 MHz RC OSC frequency limits

Power Supply Range (VDD) V	Temperature Range			
	+25 °C		-40 °C ... +85 °C	
	Minimum Value, MHz	Maximum Value, MHz	Minimum Value, MHz	Maximum Value, MHz
1.8 V ±5%	1.855	2.137	1.583	2.395
3.3 V ±10%	1.903	2.097	1.557	2.350
5 V ±10%	1.892	2.106	1.550	2.347
2.5 V ... 4.5 V	1.879	2.125	1.541	2.372
1.71 V... 5.5 V	1.754	2.197	1.450	2.541

Table 9. 2 MHz RC OSC frequency error (error calculated relative to nominal value)

Power Supply Range (VDD) V	Temperature Range			
	+25 °C		-40 °C ... +85 °C	
	Error (% at Minimum)	Error (% at Maximum)	Error (% at Minimum)	Error (% at Maximum)
1.8 V ±5%	-7.26%	6.85%	-20.83%	19.73%
3.3 V ±10%	-4.85%	4.83%	-22.15%	17.49%
5 V ±10%	-5.38%	5.30%	-22.49%	17.33%
2.5 V ... 4.5 V	-6.07%	6.27%	-22.96%	18.59%
1.71 V... 5.5 V	-12.28%	9.84%	-27.52%	27.07%





## 5.10.2 OSC Power On delay

Table 10. Oscillators Power On delay at T=(-40..+85) °C, DLY/CNT Counter data = 100; RC OSC power setting: "Auto Power On"

Power Supply Range (VDD) V	RC OSC 2 MHz		RC OSC 25 kHz	
	Typical Value, $\mu$ s	Maximum Value, $\mu$ s	Typical Value, $\mu$ s	Maximum Value, $\mu$ s
1.71	8.80	12.78	19.34	24.22
1.80	8.26	12.07	18.80	24.37
1.89	7.76	11.47	18.28	23.99
2.50	5.76	8.57	15.45	19.91
2.70	5.42	7.86	14.64	18.85
3.00	5.10	7.24	13.58	17.80
3.30	4.90	7.14	12.52	16.96
3.60	4.79	7.22	11.36	16.20
4.20	4.69	7.33	9.58	12.69
4.50	4.66	7.22	8.83	11.51
5.00	4.60	7.12	7.69	9.79
5.50	4.54	7.00	6.75	8.45



**5.11 ACMP Specifications**

**Table 11. ACMP Specifications**

Symbol	Parameter	Description/Note	Conditions	Min.	Typ.	Max.	Unit
V <sub>ACMP</sub>	ACMP Input Voltage Range	Positive Input	VDD = 1.8 V ± 5 %	0	--	V <sub>DD</sub>	V
		Negative Input		0	--	1.1	V
		Positive Input	VDD = 3.3 V ± 10 %	0	--	V <sub>DD</sub>	V
		Negative Input		0	--	1.2	V
		Positive Input	VDD = 5.0 V ± 10 %	0	--	V <sub>DD</sub>	V
		Negative Input		0	--	1.2	V
V <sub>offset</sub>	ACMP Input Offset Voltage	Low Bandwidth - Enable, V <sub>hys</sub> = 0 mV, Gain = 1, V <sub>ref</sub> = 1000 mV, VDD = (1.71..5.5) V	T = 25°C	-6.2	--	7.5	mV
			T = (-40..85)°C	-14.1	--	15.2	mV
		Low Bandwidth - Disable, V <sub>hys</sub> = 0 mV, Gain = 1, V <sub>ref</sub> = 1000 mV, VDD = (1.71..5.5) V	T = 25°C	-6.5	--	7.5	mV
			T = (-40..85)°C	-8.3	--	10.1	mV
V <sub>boffset</sub>	ACMP Buffer Input Offset Voltage	VDD = (1.71..5.5) V	T = 25°C	-28.2	--	16.3	mV
t <sub>start</sub>	ACMP Start Time	Hysteresis: disable; Low bandwidth: disable; IN+ Gain: disable; IN+ source: PIN4 (Pull Up 10k); IN- source: 50 mV	T = 25°C VDD = (1.71..5.5) V	--	47.1	101.5	μS
			T = (-40..85)°C VDD = (1.71..5.5) V	--	47.0	113.3	μS
V <sub>HYS</sub>	Built-in Hysteresis	V <sub>HYS</sub> = 25 mV V <sub>IL</sub> = V <sub>in</sub> - V <sub>HYS</sub> /2 V <sub>IH</sub> = V <sub>in</sub> + V <sub>HYS</sub> /2	LB - Enabled, T = 25°C	0.0	--	33.1	mV
			LB - Disabled, T = 25°C	0.0	--	35.4	mV
		V <sub>HYS</sub> = 50 mV V <sub>IL</sub> = V <sub>in</sub> - V <sub>HYS</sub> /2 V <sub>IH</sub> = V <sub>in</sub> + V <sub>HYS</sub> /2	LB - Enabled, T = 25°C	7.1	--	51.7	mV
			LB - Disabled, T = 25°C	9.8	--	60.4	mV
		V <sub>HYS</sub> = 200 mV V <sub>IL</sub> = V <sub>in</sub> - V <sub>HYS</sub> /2 V <sub>IH</sub> = V <sub>in</sub> + V <sub>HYS</sub> /2	LB - Enabled, T = 25°C	77.5	--	228.4	mV
			LB - Disabled, T = 25°C	91.2	--	223.5	mV
		V <sub>HYS</sub> = 25 mV V <sub>IL</sub> = V <sub>in</sub> - V <sub>HYS</sub> /2 V <sub>IH</sub> = V <sub>in</sub> + V <sub>HYS</sub> /2	LB - Enabled, T = (-40...+85)°C	0.0	--	46.7	mV
			LB - Disabled, T = (-40...+85)°C	0.0	--	46.5	mV
		V <sub>HYS</sub> = 50 mV V <sub>IL</sub> = V <sub>in</sub> - V <sub>HYS</sub> /2 V <sub>IH</sub> = V <sub>in</sub> + V <sub>HYS</sub> /2	LB - Enabled, T = (-40...+85)°C	0.0	--	160.2	mV
			LB - Disabled, T = (-40...+85)°C	0.0	--	121.5	mV
		V <sub>HYS</sub> = 200 mV V <sub>IL</sub> = V <sub>in</sub> - V <sub>HYS</sub> /2 V <sub>IH</sub> = V <sub>in</sub> + V <sub>HYS</sub> /2	LB - Enabled, T = (-40...+85)°C	24.2	--	261.1	mV
			LB - Disabled, T = (-40...+85)°C	25.0	--	325.3	mV



Symbol	Parameter	Description/Note	Conditions	Min.	Typ.	Max.	Unit	
R <sub>sin</sub>	Series Input Resistance	Gain = 1x		--	100.0	--	MΩ	
		Gain = 0.5x		--	1.0	--	MΩ	
		Gain = 0.33x		--	0.8	--	MΩ	
		Gain = 0.25x		--	1.0	--	MΩ	
PROP	Propagation Delay, Response Time	Low Bandwidth - Disable, Gain = 1, VDD=(1.71..3.3)V, Overdrive=2 mV	Low to High, T = 25°C	--	2.87	5.69	μS	
			High to Low, T = 25°C	--	2.79	5.12	μS	
G	Gain error (including threshold and internal Vref error), T = (-40...+85)°C	G = 1, VDD = (1.71..5.5) V	Vref = (50...1200) mV	--	1	--		
				G = 0.5, VDD = (1.71..5.5) V	-1.25%	--	0.95%	
				G = 0.33, VDD = (1.71..5.5) V	-1.79%	--	1.39%	
				G = 0.25, VDD = (1.71..5.5) V	-2.18%	--	1.57%	
Vref	Internal Vref error, Vref = (50...1200) mV	VDD = (1.71..5.5) V	T = 25°C	-1.91%	--	1.79%		
			T = (-40...+85)°C	-7.87%	--	5.58%		



## 6.0 Summary of Macrocell Function

### 6.1 I/O Pins

- Digital Input (low voltage or normal voltage, with or without Schmitt Trigger)
- Open Drain Outputs
- Push Pull Outputs
- Analog I/O
- 10 k $\Omega$ /100 k $\Omega$ /1 M $\Omega$  pull-up/pull-down resistors
- 40 mA Open Drain 4X Drive output

### 6.2 Connection Matrix

- Digital matrix for circuit connections based on user design

### 6.3 Analog Comparators (2 total)

- Selectable hysteresis 0 mV/25 mV/50 mV/200 mV
- Bandwidth control
- Selectable gain

### 6.4 Voltage Reference

- Used for references on Analog Comparators
- Can also be driven to external pins

### 6.5 Combinational Logic Look Up Tables (LUTs – 9 total)

- Two 2-bit Lookup Tables
- Seven 3-bit Lookup Tables

### 6.6 Combination Function Macrocells (9 total)

- Four Selectable DFF/Latch or 2-bit LUTs
- Two Selectable DFF/Latch or 3-bit LUTs
- One Selectable Pipe Delay or 3-bit LUT
- Two Selectable CNT/DLY or 4-bit LUTs

### 6.7 Delays/Counters (5 total)

- Two 14-bit delay/counters: Range 1-16384 clock cycles
- Three 8-bit delays/counters: Range 1-255 clock cycles

### 6.8 Pipe Delay (Part of Combination Function Macrocell)

- 16 stage / 3 output
- One 1 stage fixed output
- Two 1-16 stage selectable outputs.

### 6.9 Programmable Delay

- 150 ns/300 ns/450 ns /600 ns @ 3.3 V
- Includes Edge Detection function

### 6.10 Additional Logic Functions (4 total)

- Two Inverter macrocells
- Two Deglitch filter macrocells



### 6.11 RC Oscillator

- 25 kHz and 2 MHz selectable frequency
- First stage divider (4): OSC/1, OSC/2, OSC/4, and OSC/8
- Second stage divider (5): OSC/1, OSC/4, selectable (OSC/8, OSC/12, OSC/24, or OSC/64), OSC/3, and additional OSC/3 (from selectable output)



## 7.0 I/O Pins

The SLG46169 has a total of 12 multi-function I/O pins which can function as either a user defined Input or Output, as well as serving as a special function (such as outputting the voltage reference), or serving as a signal for programming of the on-chip Non Volatile Memory (NVM).

Normal Mode pin definitions are as follows:

- Pin 1:  $V_{DD}$  power supply
- Pin 2: general purpose input
- Pin 3: general purpose input or output
- Pin 4: general purpose input or output with OE
- Pin 5: general purpose input or output or analog comparator 0(+)
- Pin 6: general purpose input or output with OE or analog comparator 0(-)
- Pin 7: general purpose input or output with OE
- Pin 8: general purpose input or output or analog comparator 1(+)
- Pin 9: ground
- Pin 10: general purpose input or output with OE
- Pin 11: general purpose input or output
- Pin 12: general purpose input or output with OE
- Pin 13: general purpose input or output with OE and Vref output (VREF)
- Pin 14: general purpose input or output or external clock input

Programming Mode pin definitions are as follows:

- Pin1:  $V_{DD}$  power supply
- Pin 2:  $V_{PP}$  programming voltage
- Pin 9: ground
- Pin 10: programming mode control
- Pin 11: programming ID pin
- Pin 12: programming SDIO pin
- Pin 13: programming SRDWB pin
- Pin 14: programming SCL pin

Of the 12 user defined I/O pins on the SLG46169, all but one of the pins (Pin 2) can serve as both digital input and digital output. Pin 2 can only serve as a digital input pin.

### 7.1 Input Modes

Each I/O pin can be configured as a digital input pin with/without buffered Schmitt Trigger, or can also be configured as a low voltage digital input. Pins 5, 6 and 8 can also be configured to serve as analog inputs to the on-chip comparators. Pins 12 and 13 can also be configured as analog reference voltage outputs.

### 7.2 Output Modes

Pins 3, 4, 5, 6, 7, 8, 10, 11, 12, 13 and 14 can all be configured as digital output pins.

### 7.3 Pull Up/Down Resistors

All I/O pins have the option for user selectable resistors connected to the input structure. The selectable values on these resistors are 10 k $\Omega$ , 100 k $\Omega$  and 1 M $\Omega$ . In the case of Pin 2, the resistors are fixed to a pull-down configuration. In the case of all other I/O pins, the internal resistors can be configured as either pull-up or pull-downs.



## 7.4 I/O Register Settings

### 7.4.1 PIN 2 Register Settings

Table 12. PIN 2 Register Settings

Signal Function	Register Bit Address	Register Definition
PIN 2 Mode Control	<830:829>	00: Digital Input without Schmitt Trigger 01: Digital Input with Schmitt Trigger 10: Low Voltage Digital Input 11: Reserved
PIN 2 Pull Down Resistor Value Selection	<832:831>	00: Floating 01: 10 kΩ Resistor 10: 100 kΩ Resistor 11: 1 MΩ Resistor



### 7.4.2 PIN 3 Register Settings

Table 13. PIN 3 Register Settings

Signal Function	Register Bit Address	Register Definition
PIN 3 Mode Control	<842:840>	000: Digital Input without Schmitt Trigger 001: Digital Input with Schmitt Trigger 010: Low Voltage Digital Input 011: Reserved 100: Push Pull 101: Open Drain NMOS 110: Open Drain PMOS 111: Open Drain NMOS
PIN 3 Pull Up/Down Resistor Value Selection	<844:843>	00: Floating 01: 10 kΩ Resistor 10: 100 kΩ Resistor 11: 1 MΩ Resistor
PIN 3 Pull Up/Down Resistor Selection	<845>	0: Pull Down Resistor 1: Pull Up Resistor
PIN 3 Driver Strength Selection	<846>	0: 1X 1: 2X

### 7.4.3 PIN 4 Register Settings

Table 14. PIN 4 Register Settings

Signal Function	Register Bit Address	Register Definition
PIN 4 Mode Control (sig_pin4_oe =0)	<848:847>	00: Digital Input without Schmitt Trigger 01: Digital Input with Schmitt Trigger 10: Low Voltage Digital Input 11: Reserved
PIN 4 Mode Control (sig_pin4_oe =1)	<850:849>	00: Push Pull 1X 01: Push Pull 2X 10: Open Drain NMOS 1X 11: Open Drain NMOS 2X
PIN 4 Pull Up/Down Resistor Value Selection	<852:851>	00: Floating 01: 10 kΩ Resistor 10: 100 kΩ Resistor 11: 1 MΩ Resistor
PIN 4 Pull Up/Down Resistor Selection	<853>	0: Pull Down Resistor 1: Pull Up Resistor





### 7.4.4 PIN 5 Register Settings

Table 15. PIN 5 Register Settings

Signal Function	Register Bit Address	Register Definition
PIN 5 Mode Control	<856:854>	000: Digital Input without Schmitt Trigger 001: Digital Input with Schmitt Trigger 010: Low Voltage Digital Input 011: Analog Input/Output 100: Push Pull 101: Open Drain NMOS 110: Open Drain PMOS 111: Analog Input & Open Drain
PIN 5 Pull Up/Down Resistor Value Selection	<858:857>	00: Floating 01: 10 kΩ Resistor 10: 100 kΩ Resistor 11: 1 MΩ Resistor
PIN 5 Pull Up/Down Resistor Selection	<859>	0: Pull Down Resistor 1: Pull Up Resistor
PIN 5 Driver Strength Selection	<860>	0: 1X 1: 2X

### 7.4.5 PIN 6 Register Settings

Table 16. PIN 6 Register Settings

Signal Function	Register Bit Address	Register Definition
PIN 6 Mode Control (sig_pin6_oe =0)	<862:861>	00: Digital Input without Schmitt Trigger 01: Digital Input with Schmitt Trigger 10: Low Voltage Digital Input 11: Analog Input/Output
PIN 6 Mode Control (sig_pin6_oe =1)	<864:863>	00: Push Pull 1X 01: Push Pull 2X 10: Open Drain NMOS 1X 11: Open Drain NMOS 2X
PIN 6 Pull Up/Down Resistor Value Selection	<866:865>	00: Floating 01: 10 kΩ Resistor 10: 100 kΩ Resistor 11: 1 MΩ Resistor
PIN 6 Pull Up/Down Resistor Selection	<867>	0: Pull Down Resistor 1: Pull Up Resistor

### 7.4.6 PIN 7 Register Settings

Table 17. PIN 7 Register Settings

Signal Function	Register Bit Address	Register Definition
PIN 7 Mode Control (sig_pin7_oe =0)	<876:875>	00: Digital Input without Schmitt Trigger 01: Digital Input with Schmitt Trigger 10: Low Voltage Digital Input 11: Reserved
PIN 7 Mode Control (sig_pin7_oe =1)	<878:877>	00: Push Pull 1X 01: Push Pull 2X 10: Open Drain NMOS 1X 11: Open Drain NMOS 2X



**Table 17. PIN 7 Register Settings**

Signal Function	Register Bit Address	Register Definition
PIN 7 Pull Up/Down Resistor Value Selection	<880:879>	00: Floating 01: 10 k $\Omega$ Resistor 10: 100 k $\Omega$ Resistor 11: 1 M $\Omega$ Resistor
PIN 7 Pull Up/Down Resistor Selection	<881>	0: Pull Down Resistor 1: Pull Up Resistor