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SLG46170

GreenPAK
Programmable Mixed-signal Matrix

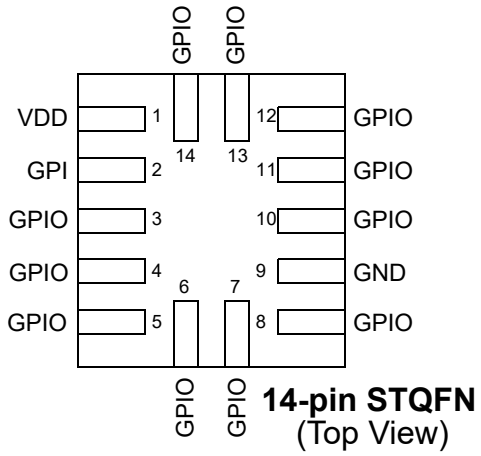
Features

- Logic & Mixed Signal Circuits
- Highly Versatile Macrocells
- Read Back Protection (Read Lock)
- 1.8V (±5%) to 5V (±10%) Supply
- Operating Temperature Range: -40°C to 85°C
- RoHS Compliant / Halogen-Free
- 14-pin STQFN: 2 x 2.2 x 0.55 mm, 0.4 mm pitch

Applications

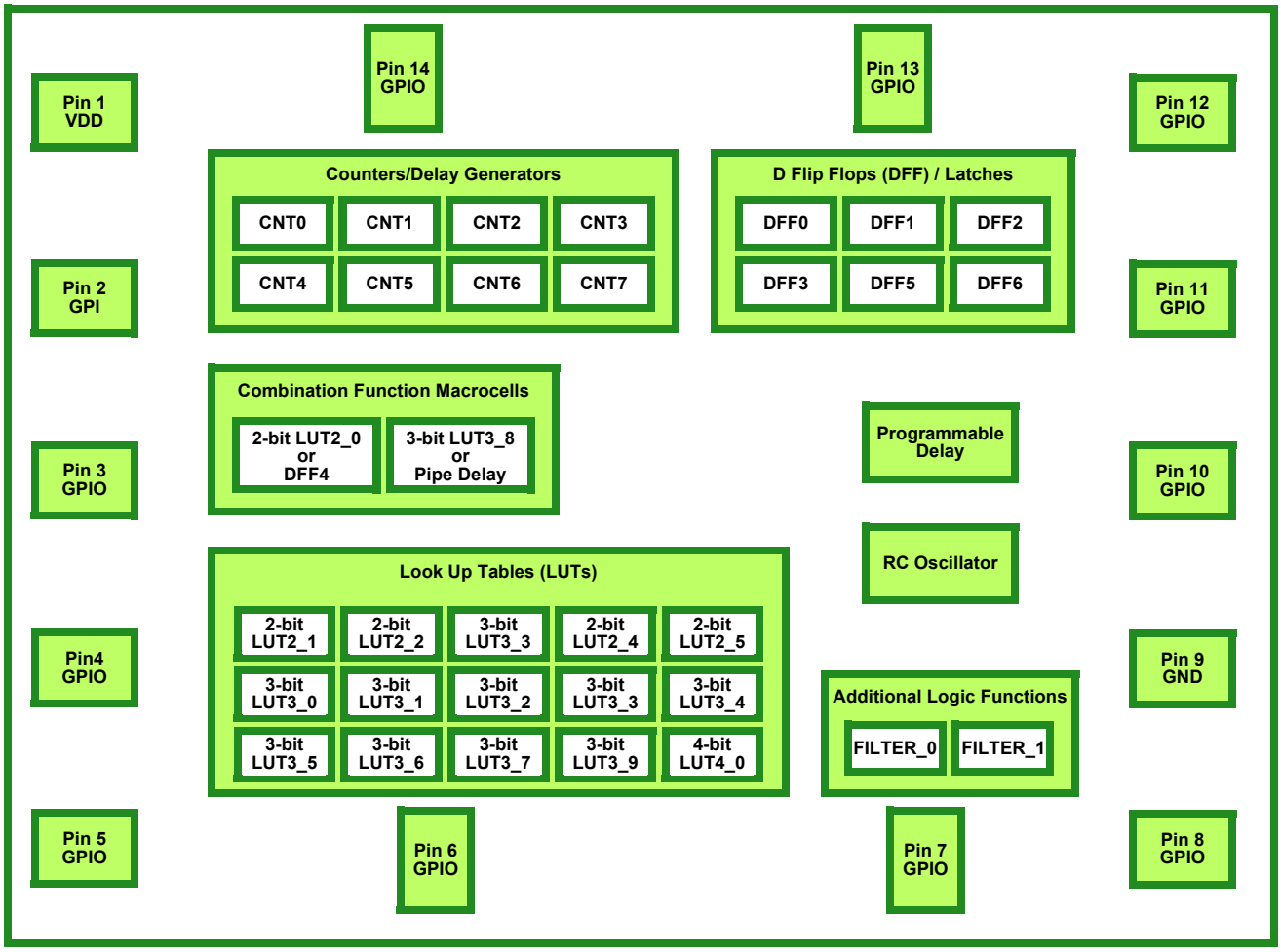
- Personal Computers and Servers
- PC Peripherals
- Consumer Electronics
- Data Communications Equipment
- Handheld and Portable Electronics

Pin Configuration



14-pin STQFN
(Top View)

Block Diagram



1.0 Overview

The SLG46170 provides a small, low power component for commonly used mixed-signal functions. The user creates their circuit design by programming the one time Non-Volatile Memory (NVM) to configure the interconnect logic, the I/O Pins and the macrocells of the SLG46170. This highly versatile device allows a wide variety of mixed-signal functions to be designed within a very small, low power single integrated circuit. The macrocells in the device include the following:

- Fifteen Combinatorial Look Up Tables (LUTs)
  - Five 2-bit LUTs
  - Nine 3-bit LUTs
  - One 4-bit LUT
- Two Combination Function Macrocells
  - One Selectable FF/Latch or 2-bit LUT
  - One Selectable Pipe Delay or 3-bit LUT
    - Pipe Delay – 16 stage / 3 output
- Eight Counter / Delay Generators (CNT/DLY)
  - One 14-bit delay/counter
  - One 14-bit delay/counter with external clock/reset
  - Four 8-bit delays/counters
  - Two 8-bit delays/counters with external clock/reset
- Six D Flip-Flop / Latches (DFF)
- Pipe Delay – 16 stage/3 output (Part of Combination Function Macrocell)
- Programmable Delay
- Additional Logic Functions – 2 Deglitch Filters
- RC Oscillator (RC OSC)

2.0 Pin Description

2.1 Functional and Programming Pin Description

Pin #	Pin Name	Function	Programming Function
1	VDD	Power Supply	Power Supply
2	GPI	General Purpose Input	V_{PP} (Programming Voltage)
3	GPIO	General Purpose I/O	N/A
4	GPIO	General Purpose I/O	N/A
5	GPIO	General Purpose I/O	N/A
6	GPIO	General Purpose I/O	N/A
7	GPIO	General Purpose I/O	N/A
8	GPIO	General Purpose I/O	N/A
9	GND	Ground	Ground
10	GPIO	General Purpose I/O	Programming Mode Control
11	GPIO	General Purpose I/O	Programming ID Pin
12	GPIO	General Purpose I/O	Programming SDIO Pin
13	GPIO	General Purpose I/O	Programming SRDWB Pin
14	GPIO	General Purpose I/O or External Clock	Programming SCL Pin

3.0 User Programmability

Non-volatile memory (NVM) is used to configure the SLG46170's connection matrix routing and macrocells. The NVM is One-Time-Programmable (OTP). However, Silego's GreenPAK development tools can be used to configure the connection matrix and macrocells, without programming the NVM, to allow on-chip emulation. This configuration will remain active on the device as long as it remains powered and can be re-written as needed to facilitate rapid design changes.

When a design is ready for in-circuit testing, the same GreenPAK development tools can be used to program the NVM and create samples for small quantity builds. Once the NVM is programmed, the device will retain this configuration for the duration of its lifetime.

Once the design is finalized, the design file can be forwarded to Silego to integrate into the production process.

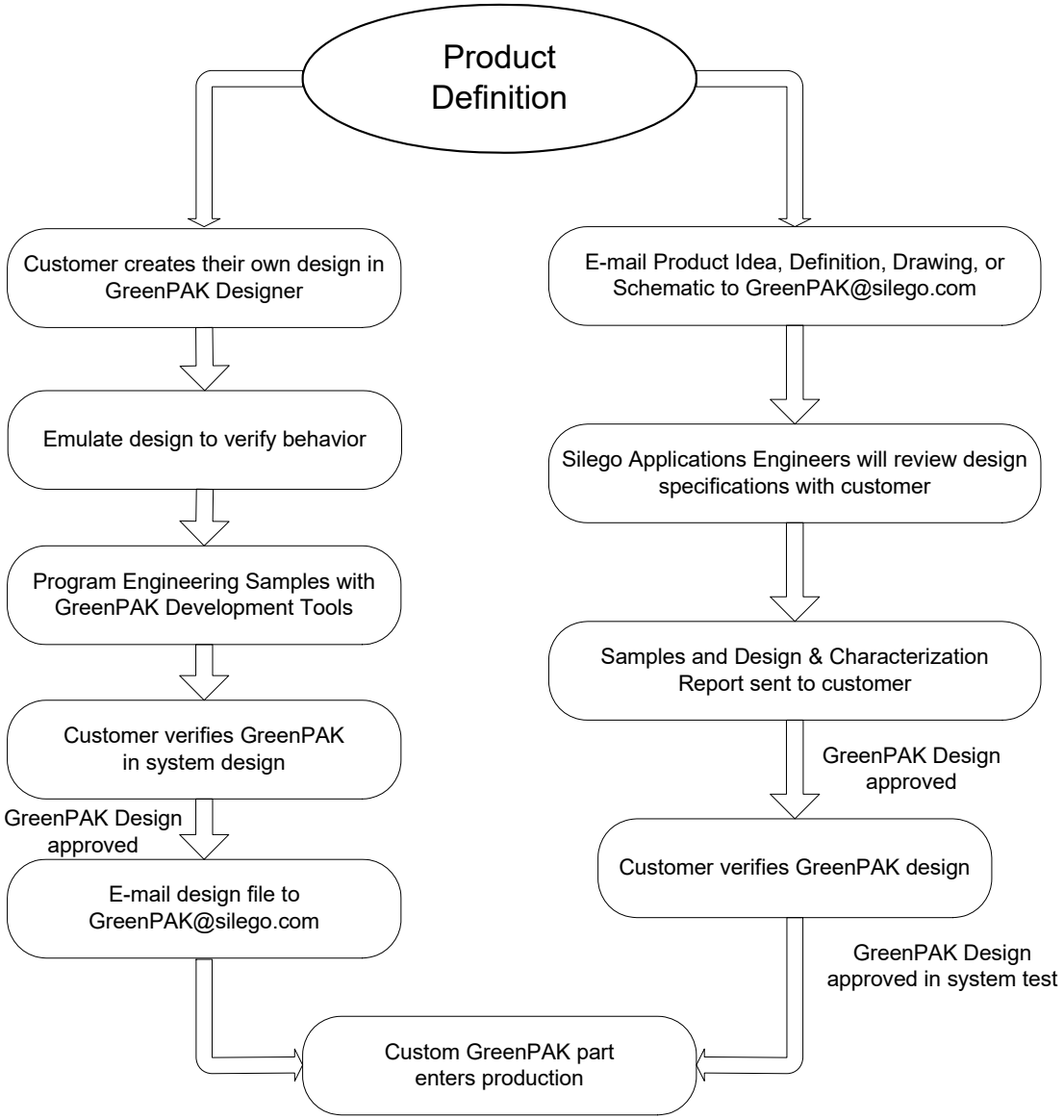


Figure 1. Steps to create a custom Silego GreenPAK device

4.0 Ordering Information

Part Number	Type
SLG46170V	14-pin STQFN
SLG46170VTR	14-pin STQFN - Tape and Reel (3k units)

5.0 Electrical Specifications

5.1 Absolute Maximum Conditions

Parameter		Min.	Max.	Unit
Supply voltage on VDD relative to GND		-0.5	7	V
DC Input voltage		GND - 0.5	VDD + 0.5	V
Maximum Average or DC Current (Through pin)	Push-Pull 1x	--	8	mA
	Push-Pull 2x	--	10	
	OD 1x	--	8	
	OD 2x	--	12	
	OD 4x	--	25	
Current at Input Pin		-1.0	1.0	mA
Storage Temperature Range		-65	150	°C
Junction Temperature		--	150	°C
ESD Protection (Human Body Model)		2000	--	V
ESD Protection (Charged Device Model)		1300	--	V
Moisture Sensitivity Level		1		

5.2 Electrical Characteristics (1.8 V ±5% V_{DD})

Symbol	Parameter	Condition/Note	Min.	Typ.	Max.	Unit
V_{DD}	Supply Voltage		1.71	1.80	1.89	V
T_A	Operating Temperature		-40	25	85	°C
V_{PP}	Programming Voltage		7.25	7.50	7.75	V
V_{IH}	HIGH-Level Input Voltage	Logic Input	1.100	--	--	V
		Logic Input with Schmitt Trigger	1.270	--	--	V
		Low-Level Logic Input	0.980	--	--	V
V_{IL}	LOW-Level Input Voltage	Logic Input	--	--	0.690	V
		Logic Input with Schmitt Trigger	--	--	0.440	V
		Low-Level Logic Input	--	--	0.520	V
I_{LKG}	Input Leakage (Absolute Value)		--	1	1000	nA
V_{OH}	HIGH-Level Output Voltage	Push-Pull 1X, Open Drain PMOS 1X, I_{OH} = 100 µA	1.690	1.789	--	V
		Push-Pull 2X, Open Drain PMOS 2X, I_{OH} = 100 µA	1.700	1.794	--	V
V_{OL}	LOW-Level Output Voltage	Push-Pull 1X, I_{OL}= 100 µA	--	0.008	0.030	V
		Push-Pull 2X, I_{OL}= 100 µA	--	0.004	0.010	V
		Open Drain NMOS 1X, I_{OL}= 100 µA	--	0.005	0.020	V
		Open Drain NMOS 2X, I_{OL}= 100 µA	--	0.003	0.010	V
		Open Drain NMOS 4X, I_{OL}= 100 µA	--	0.003	0.004	V

Symbol	Parameter	Condition/Note	Min.	Typ.	Max.	Unit
I_{OH}	HIGH-Level Output Current (see Note 1)	Push-Pull 1X, Open Drain PMOS 1X, $V_{OH} = V_{DD} - 0.2$	1.066	1.703	--	mA
		Push-Pull 1X, Open Drain PMOS 1X, $V_{OH} = V_{DD} - 0.2$	2.216	3.406	--	mA
I_{OL}	LOW-Level Output Current (see Note 1)	Push-Pull 1X, V_{OL} = 0.15 V	0.917	1.689	--	mA
		Push-Pull 2X, V_{OL} = 0.15 V	1.834	3.378	--	mA
		Open Drain NMOS 1X, V_{OL} = 0.15 V	1.375	2.534	--	mA
		Open Drain NMOS 2X, V_{OL} = 0.15 V	2.750	5.068	--	mA
		Open Drain NMOS 4X Drive, V_{OL} = 0.15 V	5.500	10.136	--	mA
I_{VDD}	Maximum Average or DC Current Through VDD Pin (Per chip side, see Note 2)	T_J = 85°C	--	--	45	mA
		T_J = 110°C	--	--	22	mA
I_{GND}	Maximum Average or DC Current Through GND Pin (Per chip side, see Note 2)	T_J = 85°C	--	--	84	mA
		T_J = 110°C	--	--	40	mA
T_{SU}	Startup Time	from VDD rising past 1.35 V	--	0.3	--	ms
PON_{THR}	Power On Threshold	V_{DD} Level Required to Start Up the Chip	1.096	1.353	1.528	V
$POFF_{THR}$	Power Off Threshold	V_{DD} Level Required to Switch Off the Chip	0.759	0.933	1.125	V

Note 1: DC or average current through any pin should not exceed value given in Absolute Maximum Conditions.
Note 2: The GreenPAK's power rails are divided in two sides. Pins 2, 3, 4, 5, 6, 7 and 8 are connected to one side, pins 10, 11, 12, 13 and 14 to another.

5.3 Electrical Characteristics (3.3V ±10% V_{DD})

Symbol	Parameter	Condition/Note	Min.	Typ.	Max.	Unit
V_{DD}	Supply Voltage		3.0	3.3	3.6	V
T_A	Operating Temperature		-40	25	85	°C
V_{PP}	Programming Voltage		7.25	7.50	7.75	V
V_{IH}	HIGH-Level Input Voltage	Logic Input	1.780	--	--	V
		Logic Input with Schmitt Trigger	2.130	--	--	V
		Low-Level Logic Input	1.130	--	--	V
V_{IL}	LOW-Level Input Voltage	Logic Input	--	--	1.210	V
		Logic Input with Schmitt Trigger	--	--	0.950	V
		Low-Level Logic Input	--	--	0.690	V
I_{LKG}	Input Leakage (Absolute Value)		--	1	1000	nA
V_{OH}	HIGH-Level Output Voltage	Push-Pull 1X,Open Drain PMOS 1X, I_{OH} = 3 mA	2.735	3.120	--	V
		Push-Pull 2X, Open Drain PMOS 2X, I_{OH} = 3 mA	2.870	3.210	--	V
V_{OL}	LOW-Level Output Voltage	Push-Pull 1X, I_{OL}= 3 mA	--	0.130	0.228	V
		Push-Pull 2X, I_{OL}= 3 mA	--	0.060	0.108	V
		Open Drain NMOS 1X, I_{OL}= 3 mA	--	0.080	0.147	V
		Open Drain NMOS 2X, I_{OL}= 3 mA	--	0.040	0.080	V
		Open Drain NMOS 4X, I_{OL}= 3 mA	--	0.027	0.034	V
I_{OH}	HIGH-Level Output Current (see Note 1)	Push-Pull 1X, Open Drain PMOS 1X, V_{OH} = 2.4 V	6.045	12.080	--	mA
		Push-Pull 2X, Open Drain PMOS 2X, V_{OH} = 2.4 V	11.522	24.160	--	mA
I_{OL}	LOW-Level Output Current (see Note 1)	Push-Pull 1X, V_{OL} = 0.4 V	4.875	8.244	--	mA
		Push-Pull 2X, V_{OL} = 0.4 V	9.750	16.488	--	mA
		Open Drain NMOS 1X, V_{OL} = 0.4 V	7.313	12.370	--	mA
		Open Drain NMOS 2X, V_{OL} = 0.4 V	14.541	24.740	--	mA
		Open Drain NMOS 4X Drive, V_{OL} = 0.4 V	25.801	49.480	--	mA
I_{VDD}	Maximum Average or DC Current Through VDD Pin (Per chip side, see Note 2)	T_J = 85°C	--	--	45	mA
		T_J = 110°C	--	--	22	mA
I_{GND}	Maximum Average or DC Current Through GND Pin (Per chip side, see Note 2)	T_J = 85°C	--	--	84	mA
		T_J = 110°C	--	--	40	mA
T_{SU}	Startup Time	from VDD rising past 1.35 V	--	0.3	--	ms

Symbol	Parameter	Condition/Note	Min.	Typ.	Max.	Unit
PON_{THR}	Power On Threshold	V_{DD} Level Required to Start Up the Chip	1.096	1.353	1.528	V
$POFF_{THR}$	Power Off Threshold	V_{DD} Level Required to Switch Off the Chip	0.759	0.933	1.125	V

Note 1: DC or average current through any pin should not exceed value given in Absolute Maximum Conditions.
Note 2: The GreenPAK's power rails are divided in two sides. Pins 2, 3, 4, 5, 6, 7 and 8 are connected to one side, pins 10, 11, 12, 13 and 14 to another.

5.4 Electrical Characteristics (5 V ±10% V_{DD})

Symbol	Parameter	Condition/Note	Min.	Typ.	Max.	Unit
V_{DD}	Supply Voltage		4.5	5.0	5.5	V
T_A	Operating Temperature		-40	25	85	°C
V_{PP}	Programming Voltage		7.25	7.50	7.75	V
V_{IH}	HIGH-Level Input Voltage	Logic Input	2.640	--	--	V
		Logic Input with Schmitt Trigger	3.160	--	--	V
		Low-Level Logic Input	1.230	--	--	V
V_{IL}	LOW-Level Input Voltage	Logic Input	--	--	1.840	V
		Logic Input with Schmitt Trigger	--	--	1.510	V
		Low-Level Logic Input	--	--	0.780	V
I_{LGK}	Input leakage (Absolute Value)		--	1	1000	nA
V_{OH}	HIGH-Level Output Voltage	Push-Pull 1X,Open Drain PMOS 1X, I_{OH} = 5 mA	4.190	4.780	--	V
		Push-Pull 2X, Open Drain PMOS 2X, I_{OH} = 5 mA	4.320	4.890	--	V
V_{OL}	LOW-Level Output Voltage	Push-Pull 1X, I_{OL}= 5 mA	--	0.157	0.270	V
		Push-Pull 2X, I_{OL}= 5 mA	--	0.076	0.130	V
		Open Drain NMOS 1X, I_{OL}= 5 mA	--	0.102	0.180	V
		Open Drain NMOS 2X, I_{OL}= 5 mA	--	0.051	0.110	V
		Open Drain NMOS 4X, I_{OL}= 5 mA	--	0.035	0.045	V
I_{OH}	HIGH-Level Output Current (see Note 1)	Push-Pull 1X, Open Drain PMOS 1X, V_{OH} = 2.4 V	22.080	34.040	--	mA
		Push-Pull 2X, Open Drain PMOS 2X, V_{OH} = 2.4 V	41.690	68.080	--	mA
I_{OL}	LOW-Level Output Current (see Note 1)	Push-Pull 1X, V_{OL} = 0.4 V	7.215	11.580	--	mA
		Push-Pull 2X, V_{OL} = 0.4 V	13.831	23.160	--	mA
		Open Drain NMOS 1X, V_{OL} = 0.4 V	10.820	17.380	--	mA
		Open Drain NMOS 2X, V_{OL} = 0.4 V	17.343	34.760	--	mA
		Open Drain NMOS 4X Drive, V_{OL} = 0.4 V	30.964	69.520	--	mA
I_{VDD}	Maximum Average or DC Current Through VDD Pin (Per chip side, see Note 2)	T_J = 85°C	--	--	45	mA
		T_J = 110°C	--	--	22	mA
I_{GND}	Maximum Average or DC Current Through GND Pin (Per chip side, see Note 2)	T_J = 85°C	--	--	84	mA
		T_J = 110°C	--	--	40	mA
T_{SU}	Startup Time	from VDD rising past 1.35 V	--	0.3	--	ms

Symbol	Parameter	Condition/Note	Min.	Typ.	Max.	Unit
PON_{THR}	Power On Threshold	V_{DD} Level Required to Start Up the Chip	1.096	1.353	1.528	V
$POFF_{THR}$	Power Off Threshold	V_{DD} Level Required to Switch Off the Chip	0.759	0.933	1.125	V

Note 1: DC or average current through any pin should not exceed value given in Absolute Maximum Conditions.
Note 2: The GreenPAK's power rails are divided in two sides. Pins 2, 3, 4, 5, 6, 7 and 8 are connected to one side, pins 10, 11, 12, 13 and 14 to another.

5.5 IDD Estimator

Table 1. Typical Current estimated for each macrocell.

Symbol	Parameter	Note	V_{DD} = 1.8 V	V_{DD} = 3.3V	V_{DD} = 5.0V	Unit
I	Current	Chip Quiescent	0.5	0.8	1.0	µA
		OSC 25 kHz, predivide = 1	3.2	5.1	7.3	µA
		OSC 25 kHz, predivide = 8	3.0	4.4	6.0	µA
		OSC 2 MHz, predivide = 1	38.5	78.2	136.2	µA
		OSC 2 MHz, predivide = 8	18.3	25.7	35.5	µA

5.6 Timing Estimator

Table 2. Typical Delay estimated for each macrocell.

Symbol	Parameter	Note	V_{DD} = 1.8 V		V_{DD} = 3.3V		V_{DD} = 5.0V		Unit
			rising	falling	rising	falling	rising	falling	
tpd	Delay	Digital input to PP 1X	42	45	17	19	12	13	ns
tpd	Delay	Digital Input with Schmitt Trigger to PP 1X	42	43	16	17	18	12	ns
tpd	Delay	Low Voltage Digital input to PP 1X	45	428	17	177	12	120	ns
tpd	Delay	Digital input to PMOS	42	-	17	-	12	-	ns
tpd	Delay	Digital input to NMOS	-	80	-	27	-	18	ns
tpd	Delay	Output enable from pin, OE Hi-Z to 1	53	-	21	-	15	-	ns
tpd	Delay	Output enable from pin, OE Hi-Z to 0	50	-	20	-	14	-	ns
tpd	Delay	LUT2bit(LATCH)	34	33	14	13	10	9	ns
tpd	Delay	LATCH(LUT2bit)	30	34	14	13	10	9	ns
tpd	Delay	LUT3bit(LATCH)	38	37	18	15	13	10	ns
tpd	Delay	LATCH+nRESET(LUT3bit)	45	42	21	17	15	12	ns
tpd	Delay	LUT4bit	28	33	14	13	10	9	ns
tpd	Delay	LUT2bt	19	26	10	10	7	7	ns
tpd	Delay	LUT3bit	28	34	14	13	10	9	ns
tpd	Delay	CNT/DLY	40	38	18	15	13	11	ns
tpd	Delay	P_DLY1C	380	377	166	163	123	120	ns
tpd	Delay	P_DLY2C	720	718	314	312	233	231	ns
tpd	Delay	P_DLY3C	1061	1060	462	460	343	341	ns
tpd	Delay	P_DLY4C	1396	1400	609	609	451	451	ns
tpd	Delay	Filter	200	200	78	78	53	53	ns
tpd	Delay	ACMP (5mV across inputs)	3000	3000	2000	2000	2000	2000	ns
tw	width	I/O with 1X push pull (min transmitted)	20	20	20	20	20	20	ns
tw	width	filter (min transmitted)	150	150	55	55	35	35	ns

5.7 Typical Counter/Delay Offset Measurements

Table 3. Typical Counter/Delay Offset Measurements.

Parameter	RC OSC Freq	RC OSC Power	V_{DD} = 1.8 V	V_{DD} = 3.3V	V_{DD} = 5.0V	Unit
offset	25kHz	auto	19	14	12	µs
offset	2MHz	auto	7	4	4	µs
frequency settling time	25kHz	auto	19	14	12	µs

Table 3. Typical Counter/Delay Offset Measurements.

Parameter	RC OSC Freq	RC OSC Power	V_{DD} = 1.8 V	V_{DD} = 3.3V	V_{DD} = 5.0V	Unit
frequency settling time	2MHz	auto	14	14	14	µs
variable (CLK period)	25kHz	forced	0-40	0-40	0-40	µs
variable (CLK period)	2MHz	forced	0-0.5	0-0.5	0-0.5	µs
tpd (non-delayed edge)	25kHz/2MHz	either	35	14	10	ns

5.8 Expected Delays and Widths

Table 4. Expected Delays and Widths for Programmable Delay (typical).

Symbol	Parameter	Note	V_{DD} = 1.8 V	V_{DD} = 3.3V	V_{DD} = 5.0V	Unit
time1	Width, 1 cell	mode:(any)edge detect, edge detect output	325	150	110	ns
time1	Width, 2 cell	mode:(any)edge detect, edge detect output	740	300	225	ns
time1	Width, 3 cell	mode:(any)edge detect, edge detect output	1020	450	340	ns
time1	Width, 4 cell	mode:(any)edge detect, edge detect output	1350	600	450	ns
time2	Delay, 1 cell	mode:(any)edge detect, edge detect output	44	18	14	ns
time2	Delay, 2 cell	mode:(any)edge detect, edge detect output	44	18	14	ns
time2	Delay, 3 cell	mode:(any)edge detect, edge detect output	44	18	14	ns
time2	Delay, 4 cell	mode:(any)edge detect, edge detect output	44	18	14	ns
time1	Width, 1 cell	mode: delayed (any)edge detect, delayed edge detect output	340	150	110	ns
time1	Width, 2 cell	mode: delayed (any)edge detect, delayed edge detect output	670	300	220	ns
time1	Width, 3 cell	mode: delayed (any)edge detect, delayed edge detect output	1000	450	335	ns
time1	Width, 4 cell	mode: delayed (any)edge detect, delayed edge detect output	1340	600	450	ns
time2	Delay, 1 cell	mode: delayed (any)edge detect, delayed edge detect output	570	220	140	ns
time2	Delay, 2 cell	mode: delayed (any)edge detect, delayed edge detect output	570	220	140	ns
time2	Delay, 3 cell	mode: delayed (any)edge detect, delayed edge detect output	570	220	140	ns
time2	Delay, 4 cell	mode: delayed (any)edge detect, delayed edge detect output	570	220	140	ns
time2	Delay, 1 cell	mode: both edge delay, edge detect output	382	375	126	ns
time2	Delay, 2 cell	mode: both edge delay, edge detect output	713	169	237	ns
time2	Delay, 3 cell	mode: both edge delay, edge detect output	1045	318	350	ns
time2	Delay, 4 cell	mode: both edge delay, edge detect output	1370	466	460	ns
time2	Delay, 1 cell	mode: both edge delay, delayed edge detect output	900	613	250	ns
time2	Delay, 2 cell	mode: both edge delay, delayed edge detect output	1250	520	360	ns
time2	Delay, 3 cell	mode: both edge delay, delayed edge detect output	1600	680	480	ns
time2	Delay, 4 cell	mode: both edge delay, delayed edge detect output	1900	815	600	ns

5.9 Typical Pulse Width Performance

Table 5. Typical Pulse Width Performance.

Parameter	V_{DD} = 1.8 V	V_{DD} = 3.3V	V_{DD} = 5.0V	Unit
Filtered Pulse Width for Filter 0 and Filter 1	< 150	< 55	< 35	ns

5.10 OSC Specifications

Table 6. 25 kHz RC OSC frequency limits at T = 25 °C

Power Supply Range (VDD) V	Minimum Value, kHz	Maximum Value, kHz
1.8 V ±5%	24.069	25.960
3.3 V ±10%	24.397	25.620
5 V ±10%	24.048	25.962
2.5 V ... 4.5 V	24.214	25.868
1.71 V… 5.5 V	23.703	27.515

Table 7. 25 kHz RC OSC frequency error (error calculated relative to nominal value) at T = 25 °C

Power Supply Range (VDD) V	Error (% at Minimum)	Error (% at Maximum)
1.8 V ±5%	-3.73%	3.84%
3.3 V ±10%	-2.41%	2.48%
5 V ±10%	-3.81%	3.85%
2.5 V ... 4.5 V	-3.14%	3.47%
1.71 V… 5.5 V	-5.19%	10.06%

5.10.1 2 MHz RC Oscillator

Table 8. 2 MHz RC OSC frequency limits at T = 25 °C

Power Supply Range (VDD) V	Minimum Value, MHz	Maximum Value, MHz
1.8 V ±5%	1.855	2.133
3.3 V ±10%	1.911	2.089
5 V ±10%	1.873	2.130
2.5 V ... 4.5 V	1.894	2.110
1.71 V… 5.5 V	1.760	2.164

Table 9. 2 MHz RC OSC frequency error (error calculated relative to nominal value) at T = 25 °C

Power Supply Range (VDD) V	Error (% at Minimum)	Error (% at Maximum)
1.8 V ±5%	-7.25%	6.67%
3.3 V ±10%	-4.44%	4.43%
5 V ±10%	-6.33%	6.50%
2.5 V ... 4.5 V	-5.28%	5.52%
1.71 V… 5.5 V	-12.00%	8.19%

5.10.2 OSC Power On delay

Table 10. Oscillators Power On delay at T=(-40..+85) °C, DLY/CNT Counter data = 100; RC OSC power setting: "Auto Power On"

Power Supply Range (VDD) V	RC OSC 2 MHz		RC OSC 25 kHz	
	Typical Value, µs	Maximum Value, µs	Typical Value, µs	Maximum Value, µs
1.71	8.80	12.78	19.34	24.22
1.80	8.26	12.07	18.80	24.37
1.89	7.76	11.47	18.28	23.99
2.50	5.76	8.57	15.45	19.91
2.70	5.42	7.86	14.64	18.85
3.00	5.10	7.24	13.58	17.80
3.30	4.90	7.14	12.52	16.96
3.60	4.79	7.22	11.36	16.20
4.20	4.69	7.33	9.58	12.69
4.50	4.66	7.22	8.83	11.51
5.00	4.60	7.12	7.69	9.79
5.50	4.54	7.00	6.75	8.45

6.0 Summary of Macrocell Function

6.1 I/O Pins

- Digital Input (low voltage or normal voltage, with or without Schmitt Trigger)
- Open Drain Outputs
- Push Pull Outputs
- 10 kΩ/100 kΩ/1 MΩ pull-up/pull-down resistors
- 40 mA Open Drain 4X Drive output

6.2 Connection Matrix

- Digital matrix for circuit connections based on user design

6.3 Combinational Logic Look Up Tables (LUTs – 15 total)

- Five 2-bit Lookup Tables
- Nine 3-bit Lookup Tables
- One 4-bit Lookup Tables

6.4 Combination Function Macrocell (2 total)

- One Selectable FF/Latch or 2-bit LUT
- One Selectable Pipe Delay or 3-bit LUT

6.5 Delays/Counters (8 total)

- Two 14-bit delay/counters: Range 1-16384 clock cycles
- Four 8-bit delays/counters: Range 1-255 clock cycles
- Two 8-bit delays/counters with external clock/reset: Range 1-255 clock cycles

6.6 Digital Storage Elements (6 total)

- Six D Flip-Flops or Latches

6.7 Pipe Delay (Part of Combination Function Macrocell)

- 16 stage / 3 output
- One 1 stage fixed output
- Two 1-16 stage selectable outputs.

6.8 Programmable Delay

- 150 ns/300 ns/450 ns /600 ns @ 3.3 V
- Includes Edge Detection function

6.9 Additional Logic Functions (2 total)

- Two Deglitch filter macrocells

6.10 RC Oscillator

- 25 kHz and 2 MHz selectable frequency
- First stage divider (4): OSC/1, OSC/2, OSC/4, and OSC/8
- Second stage divider (5): OSC/1, OSC/4, selectable (OSC/8, OSC/12, OSC/24, or OSC/64), OSC/3, and additional OSC/3 (from selectable output)

7.0 I/O Pins

The SLG46170 has a total of 12 multi-function I/O pins which can function as either a user defined Input or Output, as well as serving as a special function (such as outputting the voltage reference), or serving as a signal for programming of the on-chip Non Volatile Memory (NVM).

Normal Mode pin definitions are as follows:

- Pin 2: general purpose input
- Pin 3: general purpose input or output
- Pin 4: general purpose input or output
- Pin 5: general purpose input or output
- Pin 6: general purpose input or output
- Pin 7: general purpose input or output
- Pin 8: general purpose input or output
- Pin 10: general purpose input or output
- Pin 11: general purpose input or output
- Pin 12: general purpose input or output
- Pin 13: general purpose input or output
- Pin 14: general purpose input or output or external clock

Programming Mode pin definitions are as follows;

- Pin 1: Vdd power supply
- Pin 2: Vpp programming voltage
- Pin 9: ground
- Pin 10: programming mode control
- Pin 11: programming ID pin
- Pin 12: programming SDIO pin
- Pin 13: programming SRDWB pin
- Pin 14: programming SCL pin

Of the 12 user defined I/O pins on the SLG46170, all but one of the pins (Pin 2) can serve as both digital input and digital output. Pin 2 can only serve as a digital input pin.

7.1 Input Modes

Each I/O pin can be configured as a digital input pin with/without buffered Schmitt Trigger, or can also be configured as a low voltage digital input.

7.2 Output Modes

Pins 3, 4, 5, 6, 7, 8, 10, 11, 12, 13 and 14 can all be configured as digital output pins.

7.3 Pull Up/Down Resistors

All I/O pins have the option for user selectable resistors connected to the input structure. The selectable values on these resistors are 10 kΩ, 100 kΩ and 1 MΩ. In the case of Pin 2, the resistors are fixed to a pull-down configuration. In the case of all other I/O pins, the internal resistors can be configured as either pull-up or pull-downs.

7.4 I/O Register Settings

7.4.1 PIN 2 Register Settings

Table 11. PIN 2 Register Settings

Signal Function	Register Bit Address	Register Definition
PIN 2 Mode Control	<845:844>	00: Digital Input without Schmitt Trigger 01: Digital Input with Schmitt Trigger 10: Low Voltage Digital Input 11: Reserved
PIN 2 Pull Down Resistor Value Selection	<847:846>	00: Floating 01: 10 kΩ Resistor 10: 100 kΩ Resistor 11: 1 MΩ Resistor

7.4.2 PIN 3 Register Settings

Table 12. PIN 3 Register Settings

Signal Function	Register Bit Address	Register Definition
PIN 3 Mode Control	<857:855>	000: Digital Input without Schmitt Trigger 001: Digital Input with Schmitt Trigger 010: Low Voltage Digital Input 011: Reserved 100: Push Pull 101: Open Drain NMOS 110: Open Drain PMOS 111: Reserved
PIN 3 Pull Up/Down Resistor Value Selection	<859:858>	00: Floating 01: 10 kΩ Resistor 10: 100 kΩ Resistor 11: 1 MΩ Resistor
PIN 3 Pull Up/Down Resistor Selection	<860>	0: Pull Down Resistor 1: Pull Up Resistor
PIN 3 Driver Strength Selection	<861>	0: 1X 1: 2X

7.4.3 PIN 4 Register Settings

Table 13. PIN 4 Register Settings

Signal Function	Register Bit Address	Register Definition
PIN 4 Mode Control	<864:862>	000: Digital Input without Schmitt Trigger 001: Digital Input with Schmitt Trigger 010: Low Voltage Digital Input 011: Reserved 100: Push Pull 101: Open Drain NMOS 110: Open Drain PMOS 111: Reserved
PIN 4 Pull Up/Down Resistor Value Selection	<866:865>	00: Floating 01: 10 kΩ Resistor 10: 100 kΩ Resistor 11: 1 MΩ Resistor
PIN 4 Pull Up/Down Resistor Selection	<867>	0: Pull Down Resistor 1: Pull Up Resistor
PIN 4 Driver Strength Selection	<868>	0: 1X 1: 2X

7.4.4 PIN 5 Register Settings

Table 14. PIN 5 Register Settings

Signal Function	Register Bit Address	Register Definition
PIN 5 Mode Control	<871:869>	000: Digital Input without Schmitt Trigger 001: Digital Input with Schmitt Trigger 010: Low Voltage Digital Input 011: Reserved 100: Push Pull 101: Open Drain NMOS 110: Open Drain PMOS 111: Reserved
PIN 5 Pull Up/Down Resistor Value Selection	<873:872>	00: Floating 01: 10 kΩ Resistor 10: 100 kΩ Resistor 11: 1 MΩ Resistor
PIN 5 Pull Up/Down Resistor Selection	<874>	0: Pull Down Resistor 1: Pull Up Resistor
PIN 5 Driver Strength Selection	<875>	0: 1X 1: 2X

7.4.5 PIN 6 Register Settings

Table 15. PIN 6 Register Settings

Signal Function	Register Bit Address	Register Definition
PIN 6 Mode Control	<878:876>	000: Digital Input without Schmitt Trigger 001: Digital Input with Schmitt Trigger 010: Low Voltage Digital Input 011: Reserved 100: Push Pull 101: Open Drain NMOS 110: Open Drain PMOS 111: Reserved
PIN 6 Pull Up/Down Resistor Value Selection	<880:879>	00: Floating 01: 10 kΩ Resistor 10: 100 kΩ Resistor 11: 1 MΩ Resistor
PIN 6 Pull Up/Down Resistor Selection	<881>	0: Pull Down Resistor 1: Pull Up Resistor
PIN 6 Driver Strength Selection	<882>	0: 1X 1: 2X

7.4.6 PIN 7 Register Settings

Table 16. PIN 7 Register Settings

Signal Function	Register Bit Address	Register Definition
PIN 7 Mode Control	<892:890>	000: Digital Input without Schmitt Trigger 001: Digital Input with Schmitt Trigger 010: Low Voltage Digital Input 011: Reserved 100: Push Pull 101: Open Drain NMOS 110: Open Drain PMOS 111: Reserved
PIN 7 Pull Up/Down Resistor Value Selection	<894:893>	00: Floating 01: 10 kΩ Resistor 10: 100 kΩ Resistor 11: 1 MΩ Resistor
PIN 7 Pull Up/Down Resistor Selection	<895>	0: Pull Down Resistor 1: Pull Up Resistor
PIN 7 Driver Strength Selection	<896>	0: 1X 1: 2X

7.4.7 PIN 8 Register Settings

Table 17. PIN 8 Register Settings

Signal Function	Register Bit Address	Register Definition
PIN 8 Mode Control	<899:897>	000: Digital Input without Schmitt Trigger 001: Digital Input with Schmitt Trigger 010: Low Voltage Digital Input 011: Reserved 100: Push Pull 101: Open Drain NMOS 110: Open Drain PMOS 111: Reserved
PIN 8 Pull Up/Down Resistor Value Selection	<901:900>	00: Floating 01: 10 kΩ Resistor 10: 100 kΩ Resistor 11: 1 MΩ Resistor
PIN 8 Pull Up/Down Resistor Selection	<902>	0: Pull Down Resistor 1: Pull Up Resistor
PIN 8 Driver Strength Selection	<903>	0: 1X 1: 2X
PIN 8 4X Drive (4X, NMOS Open Drain) Selection	<904>	0: 4X Drive Off 1: 4X Drive On (if <897:899> = '101')

7.4.8 PIN 10 Register Settings

Table 18. PIN 10 Register Settings

Signal Function	Register Bit Address	Register Definition
PIN 10 Mode Control	<936:934>	000: Digital Input without Schmitt Trigger 001: Digital Input with Schmitt Trigger 010: Low Voltage Digital Input 011: Reserved 100: Push Pull 101: Open Drain NMOS 110: Open Drain PMOS 111: Reserved
PIN 10 Pull Up/Down Resistor Value Selection	<938:937>	00: Floating 01: 10 kΩ Resistor 10: 100 kΩ Resistor 11: 1 MΩ Resistor
PIN 10 Pull Up/Down Resistor Selection	<939>	0: Pull Down Resistor 1: Pull Up Resistor
PIN 10 Driver Strength Selection	<940>	0: 1X 1: 2X

7.4.9 PIN 11 Register Settings

Table 19. PIN 11 Register Settings

Signal Function	Register Bit Address	Register Definition
PIN 11 Mode Control	<943:941>	000: Digital Input without Schmitt Trigger 001: Digital Input with Schmitt Trigger 010: Low Voltage Digital Input 011: Reserved 100: Push Pull 101: Open Drain NMOS 110: Open Drain PMOS 111: Reserved
PIN 11 Pull Up/Down Resistor Value Selection	<945:944>	00: Floating 01: 10 kΩ Resistor 10: 100 kΩ Resistor 11: 1 MΩ Resistor
PIN 11 Pull Up/Down Resistor Selection	<946>	0: Pull Down Resistor 1: Pull Up Resistor
PIN 11 Driver Strength Selection	<947>	0: 1X 1: 2X

7.4.10 PIN 12 Register Settings

Table 20. PIN 12 Register Settings

Signal Function	Register Bit Address	Register Definition
PIN 12 Mode Control	<950:948>	000: Digital Input without Schmitt Trigger 001: Digital Input with Schmitt Trigger 010: Low Voltage Digital Input 011: Reserved 100: Push Pull 101: Open Drain NMOS 110: Open Drain PMOS 111: Reserved
PIN 12 Pull Up/Down Resistor Value Selection	<952:951>	00: Floating 01: 10 kΩ Resistor 10: 100 kΩ Resistor 11: 1 MΩ Resistor
PIN 12 Pull Up/Down Resistor Selection	<953>	0: Pull Down Resistor 1: Pull Up Resistor
PIN 12 Driver Strength Selection	<954>	0: 1X 1: 2X

7.4.11 PIN 13 Register Settings

Table 21. PIN 13 Register Settings

Signal Function	Register Bit Address	Register Definition
PIN 13 Mode Control	<957:955>	000: Digital Input without Schmitt Trigger 001: Digital Input with Schmitt Trigger 010: Low Voltage Digital Input 011: Reserved 100: Push Pull 101: Open Drain NMOS 110: Open Drain PMOS 111: Reserved
PIN 13 Pull Up/Down Resistor Value Selection	<959:958>	00: Floating 01: 10 kΩ Resistor 10: 100 kΩ Resistor 11: 1 MΩ Resistor
PIN 13 Pull Up/Down Resistor Selection	<960>	0: Pull Down Resistor 1: Pull Up Resistor
PIN 13 Driver Strength Selection	<961>	0: 1X 1: 2X

7.4.12 PIN 14 Register Settings

Table 22. PIN 14 Register Settings

Signal Function	Register Bit Address	Register Definition
PIN 14 Mode Control	<964:962>	000: Digital Input without Schmitt Trigger 001: Digital Input with Schmitt Trigger 010: Low Voltage Digital Input 011: Reserved 100: Push Pull 101: Open Drain NMOS 110: Open Drain PMOS 111: Reserved
PIN 14 Pull Up/Down Resistor Value Selection	<966:965>	00: Floating 01: 10 kΩ Resistor 10: 100 kΩ Resistor 11: 1 MΩ Resistor
PIN 14 Pull Up/Down Resistor Selection	<967>	0: Pull Down Resistor 1: Pull Up Resistor
PIN 14 Driver Strength Selection	<968>	0: 1X 1: 2X