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SLG46535

GreenPAK
Programmable Mixed-signal Matrix with Asynchronous State Machine and Dual Supply

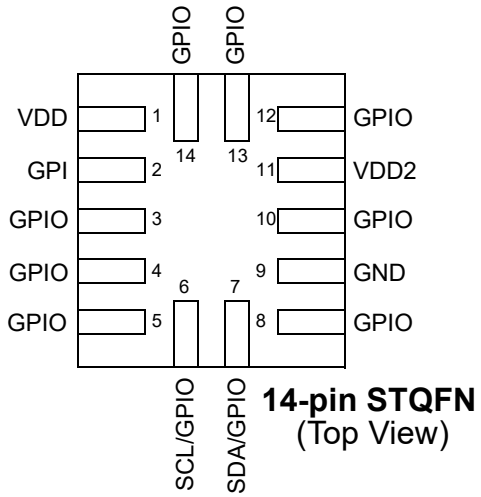
Features

- Logic & Mixed Signal Circuits
- Highly Versatile Macrocells
- Read Back Protection (Read Lock)
- 1.8 V (±5%) to 5 V (±10%) VDD
- 1.8 V (±5%) to 5 V (±10%) VDD2 (VDD2 ≤ VDD)
- Operating Temperature Range: -40°C to 85°C
- RoHS Compliant / Halogen-Free
- 14-pin STQFN: 2 x 2.2 x 0.55 mm, 0.4 mm pitch

Applications

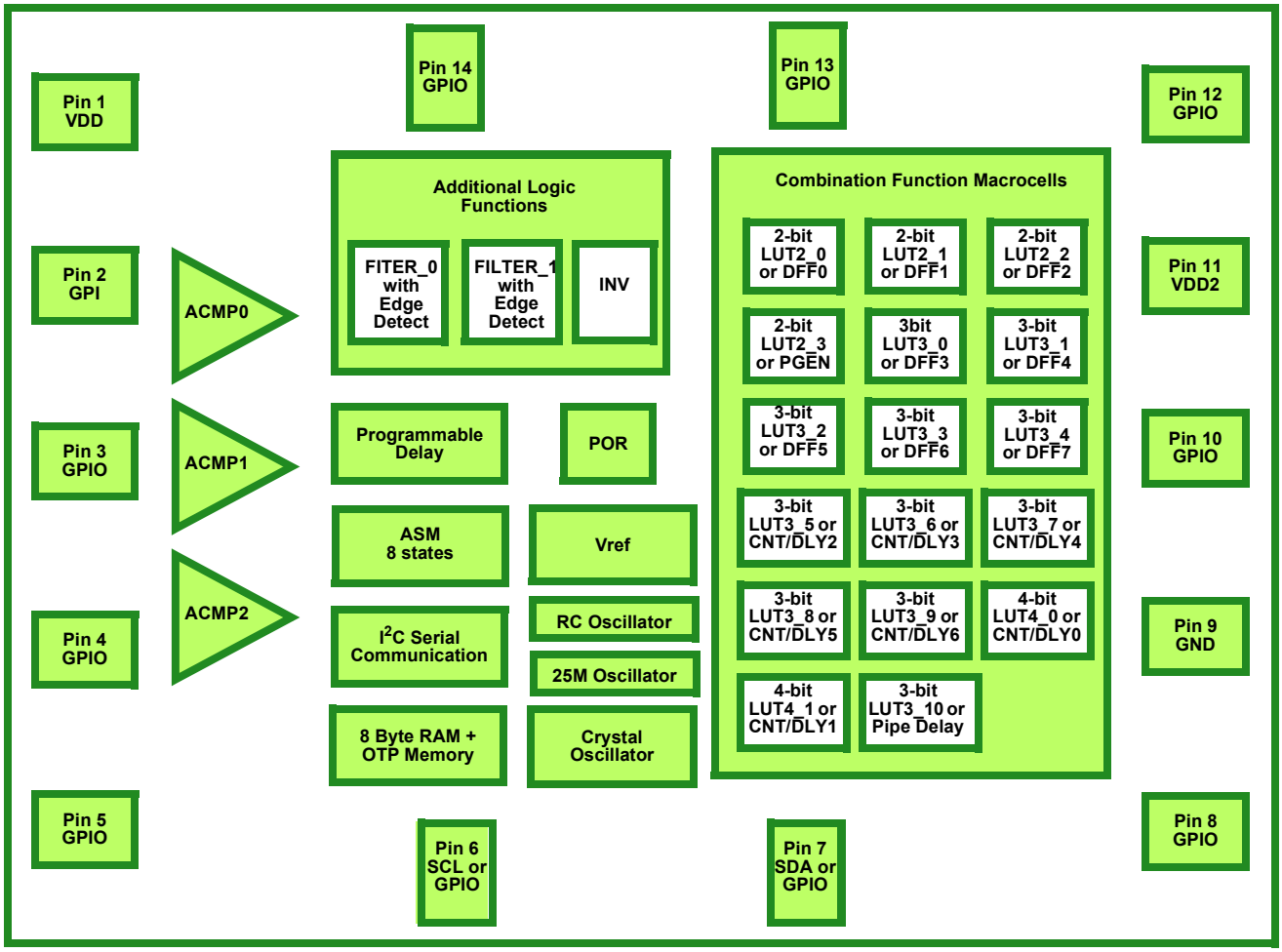
- Personal Computers and Servers
- PC Peripherals
- Consumer Electronics
- Data Communications Equipment
- Handheld and Portable Electronics

Pin Configuration



14-pin STQFN
(Top View)

Block Diagram



1.0 Overview

The SLG46535 provides a small, low power component for commonly used mixed-signal functions. The user creates their circuit design by programming the one time Non-Volatile Memory (NVM) to configure the interconnect logic, the I/O Pins and the macrocells of the SLG46535. This highly versatile device allows a wide variety of mixed-signal functions to be designed within a very small, low power single integrated circuit.

The additional power supply (VDD2) on the SLG46535 provides the ability to interface two independent voltage domains within the same design. Users can configure pins, dedicated to each power supply, as inputs, outputs, or both (controlled dynamically by internal logic) to both VDD and VDD2 voltage domains. Using the available macrocells designers can implement mixed-signal functions bridging both domains or simply pass through level-translation in both High to Low and Low to High directions.

The macrocells in the device include the following:

- Three Analog Comparators (ACMP)
- Nineteen Combination Function Macrocells
  - Three Selectable DFF/Latch or 2-bit LUTs
  - One Selectable Continuous DFF/Latch or 3-bit LUT
  - Four Selectable DFF/Latch or 3-bit LUTs
  - One Selectable Pipe Delay or 3-bit LUT
  - One Selectable Programmable Function Generator or 2-bit LUT
  - Five 8-bit delays/counters or 3-bit LUTs
  - Two 16-bit delays/counters or 4-bit LUTs
  - Two Deglitch Filters with Edge Detectors
- Asynchronous State Machine
  - Eight States
  - Flexible input logic from state transitions
- Serial Communications
  - I^2C Protocol compliant
- Pipe Delay – 16 stage/3 output (Part of Combination Function Macrocell)
- Programmable Delay
- Additional Logic Function
  - One Inverter
- Two Oscillators (OSC)
  - Configurable 25 kHz/2 MHz
  - 25 MHz RC Oscillator
- Crystal Oscillator
- Power-On-Reset (POR)
- Eight Byte RAM + OTP User Memory
  - RAM Memory space that is readable and writable via I^2C
  - User defined initial values transferred from OTP

2.0 Pin Description

2.1 Functional Pin Description

Pin #	Pin Name	Function
1	VDD	Power Supply 1
2	GPI	General Purpose Input
3	GPIO	General Purpose I/O
4	GPIO	General Purpose I/O or Analog Comparator 0 (+)
5	GPIO	General Purpose I/O with OE or Analog Comparator 0 (-)
6	SCL/GPIO	General Purpose I/O SCL or GPIOD (NMOS open drain only)
7	SDA/GPIO	General Purpose I/O SDA or GPIOD (NMOS open drain only)
8	GPIO	General Purpose I/O with OE or Analog Comparator 1 (+)
9	GND	Ground
10	GPIO	General Purpose I/O or Analog Comparator 1 (-)
11	VDD2	Power Supply 2
12	GPIO	General Purpose I/O with OE
13	GPIO	General Purpose I/O
14	GPIO	General Purpose I/O or External Clock Input

3.0 User Programmability

Non-volatile memory (NVM) is used to configure the SLG46535's connection matrix routing and macrocells. The NVM is One-Time-Programmable (OTP). However, Silego's GreenPAK development tools can be used to configure the connection matrix and macrocells, without programming the NVM, to allow on-chip emulation. This configuration will remain active on the device as long as it remains powered and can be re-written as needed to facilitate rapid design changes.

When a design is ready for in-circuit testing, the same GreenPAK development tools can be used to program the NVM and create samples for small quantity builds. Once the NVM is programmed, the device will retain this configuration for the duration of its lifetime.

Once the design is finalized, the design file can be forwarded to Silego to integrate into the production process.

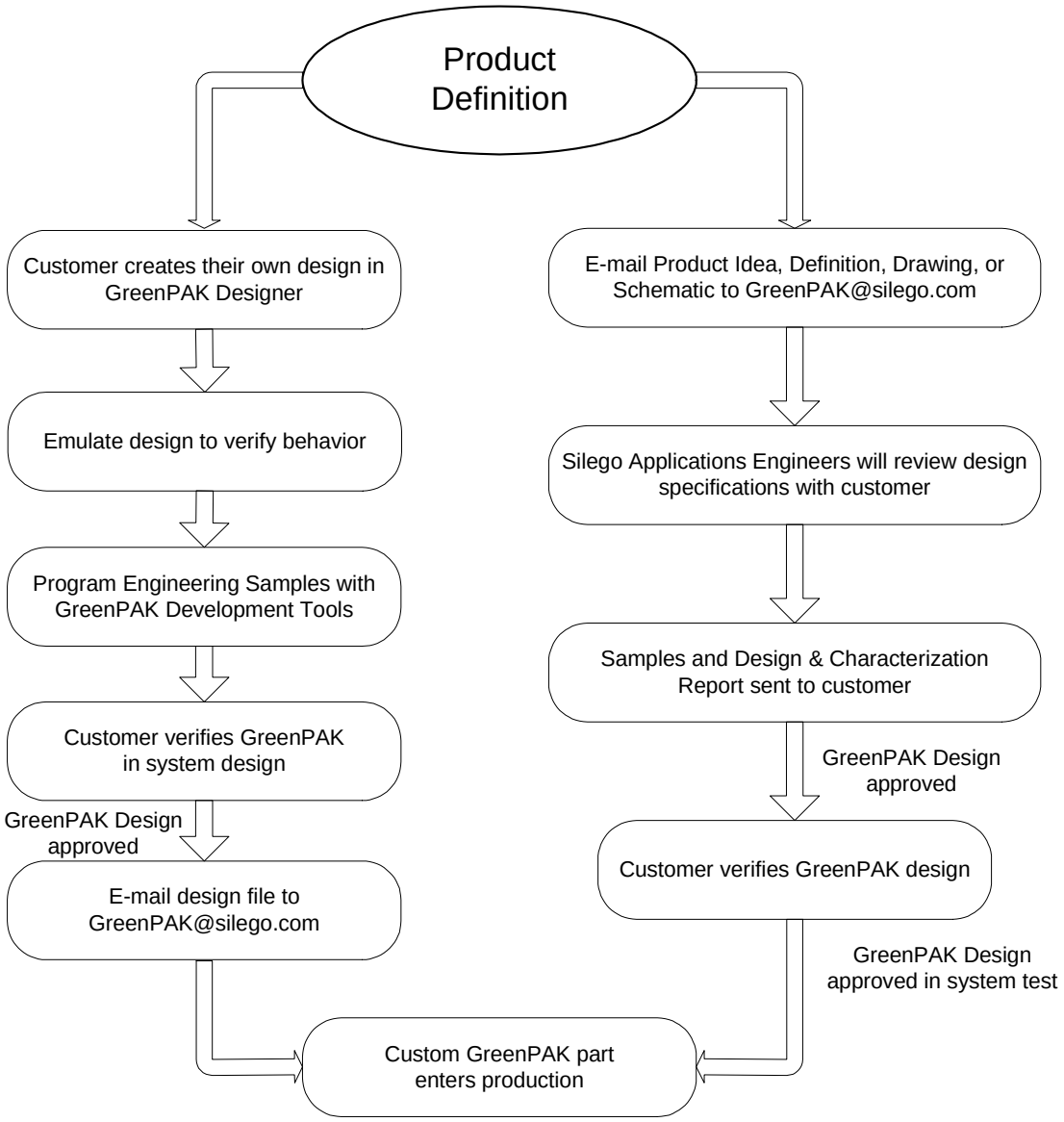


Figure 1. Steps to create a custom Silego GreenPAK device

4.0 Ordering Information

Part Number	Type
SLG46535V	14-pin STQFN
SLG46535VTR	14-pin STQFN - Tape and Reel (3k units)

5.0 Electrical Specifications

5.1 Absolute Maximum Conditions

Parameter		Min.	Max.	Unit
Supply voltage on VDD relative to GND		-0.5	7	V
Supply voltage on VDD2 relative to GND		-0.5	VDD + 0.5	V
DC Input voltage	Pins 2, 3, 4, 5, 6, 7, 8	GND - 0.5	VDD + 0.5	V
	Pins 10, 12, 13, 14		VDD2 + 0.5	
Maximum Average or DC Current (Through pin)	Push-Pull 1x	--	11	mA
	Push-Pull 2x	--	16	
	OD 1x	--	11	
	OD 2x	--	21	
	OD 4x	--	43	
Current at Input Pin		-1.0	1.0	mA
Storage Temperature Range		-65	150	°C
Junction Temperature		--	150	°C
ESD Protection (Human Body Model)		2000	--	V
ESD Protection (Charged Device Model)		500	--	V
Moisture Sensitivity Level		1		

5.2 Electrical Characteristics (1.8 V ±5% V_{DD})

Symbol	Parameter	Condition/Note	Min.	Typ.	Max.	Unit
V_{DD}	Supply Voltage Pin 1	VDD2 ≤ VDD	1.71	1.8	1.89	V
I_Q	Quiescent Current	Static Inputs and Outputs	--	0.46	--	µA
T_A	Operating Temperature		-40	25	85	°C
V_{PP}	Programming Voltage		7.25	7.50	7.75	V
V_{ACMP}	ACMP Input Voltage Range	Positive Input	0	--	V_{DD}	V
		Negative Input	0	--	1.2	V
V_{IH}	HIGH-Level Input Voltage PIN 2, 3, 4, 5, 6, 7, 8	Logic Input	1.06	--	V_{DD}	V
		Logic Input with Schmitt Trigger	1.28	--	V_{DD}	V
		Low-Level Logic Input	0.94	--	V_{DD}	V
V_{IL}	LOW-Level Input Voltage PIN 2, 3, 4, 5, 6, 7, 8	Logic Input	0	--	0.76	V
		Logic Input with Schmitt Trigger	0	--	0.49	V
		Low-Level Logic Input	0	--	0.52	V
V_{HYS}	Schmitt Trigger Hysteresis Voltage PIN 2, 3, 4, 5, 6, 7, 8	Logic Input with Schmitt Trigger	0.10	0.41	0.66	V
I_{LKG}	Input leakage (Absolute Value) PIN 2, 3, 4, 5, 6, 7, 8		--	1	1000	nA
V_{OH}	HIGH-Level Output Voltage PIN 2, 3, 4, 5, 6, 7, 8	Push-Pull, I_{OH} = 100 µA, 1X Drive	1.69	1.79	--	V
		PMOS OD, I_{OH} = 100 µA, 1X Drive	1.69	1.79	--	V
		Push-Pull, I_{OH} = 100 µA, 2X Drive	1.70	1.79	--	V
		PMOS OD, I_{OH} = 100 µA, 2X Drive	1.70	1.79	--	V
V_{OL}	LOW-Level Output Voltage PIN 2, 3, 4, 5, 6, 7, 8	Push-Pull, I_{OL}= 100 µA, 1X Drive	--	0.01	0.03	V
		Push-Pull, I_{OL} = 100 µA, 2X Drive	--	0.01	0.01	V
		Open Drain, I_{OL} = 100 µA, 1X Drive	--	0.01	0.02	V
		Open Drain, I_{OL} = 100 µA, 2X Drive	--	0.01	0.02	V
		Open Drain NMOS 4X, I_{OL} = 100 µA	--	0.001	0.002	V
I_{OH}	HIGH-Level Output Pulse Current (see Note 1) PIN 2, 3, 4, 5, 6, 7, 8	Push-Pull, V_{OH} = V_{DD} - 0.2, 1X Drive	1.07	1.70	--	mA
		PMOS OD, V_{OH} = V_{DD} - 0.2, 1X Drive	1.07	1.70	--	mA
		Push-Pull, V_{OH} = V_{DD} - 0.2, 2X Drive	2.22	3.41	--	mA
		PMOS OD, V_{OH} = V_{DD} - 0.2, 2X Drive	2.22	3.41	--	mA
I_{OL}	LOW-Level Output Pulse Current (see Note 1) PIN 2, 3, 4, 5, 6, 7, 8	Push-Pull, V_{OL} = 0.15 V, 1X Drive	0.92	1.69	--	mA
		Push-Pull, V_{OL} = 0.15 V, 2X Drive	1.83	3.38	--	mA
		Open Drain, V_{OL} = 0.15 V, 1X Drive	1.38	2.53	--	mA
		Open Drain, V_{OL} = 0.15 V, 2X Drive	2.75	5.07	--	mA
		Open Drain NMOS 4X, V_{OL} = 0.15 V	7.21	9.00	--	mA
I_{VDD}	Maximum Average or DC Current Through VDD Pin (Per chip side, see Note 2)	T_J = 85°C	--	--	45	mA
		T_J = 110°C	--	--	22	mA

Symbol	Parameter	Condition/Note	Min.	Typ.	Max.	Unit
I_{GND}	Maximum Average or DC Current Through GND Pin (Per chip side, see Note 2)	T_J = 85°C	--	--	86	mA
		T_J = 110°C	--	--	41	mA
V_O	Maximal Voltage Applied to any PIN in High-Impedance State		--	--	V_{DD}	V
T_{SU}	Startup Time	from VDD rising past PON_{THR}	0.63	1.36	1.87	ms
PON_{THR}	Power On Threshold	V_{DD} Level Required to Start Up the Chip	1.41	1.54	1.66	V
$POFF_{THR}$	Power Off Threshold	V_{DD} Level Required to Switch Off the Chip	1.00	1.15	1.31	V
R_{PUP}	Pull Up Resistance	1 M Pull Up	859.8	1097.1	1358.9	kΩ
		100 k Pull Up	86.47	110.13	136.18	kΩ
		10 k Pull Up	10.82	12.86	15.36	kΩ
R_{PDWN}	Pull Down Resistance	1 M Pull Down	873.9	1097.0	1359.0	kΩ
		100 k Pull Down	88.89	110.53	136.55	kΩ
		10 k Pull Down	9.65	12.75	15.76	kΩ

Note 1: DC or average current through any pin should not exceed value given in Absolute Maximum Conditions.
Note 2: The GreenPAK's power rails are divided in two sides. Pins 2, 3, 4, 5, 6, 7 and 8 are connected to one side, pins 10, 12, 13 and 14 to another.

5.3 Electrical Characteristics (3.3 V ±10% V_{DD})

Symbol	Parameter	Condition/Note	Min.	Typ.	Max.	Unit
V_{DD}	Supply Voltage Pin 1	VDD2 ≤ VDD	3.0	3.3	3.6	V
I_Q	Quiescent Current	Static Inputs and Outputs	--	0.81	--	µA
T_A	Operating Temperature		-40	25	85	°C
V_{PP}	Programming Voltage		7.25	7.50	7.75	V
V_{ACMP}	ACMP Input Voltage Range	Positive Input	0	--	V_{DD}	V
		Negative Input	0	--	1.2	V
V_{IH}	HIGH-Level Input Voltage PIN 2, 3, 4, 5, 6, 7, 8	Logic Input	1.81	--	V_{DD}	V
		Logic Input with Schmitt Trigger	2.14	--	V_{DD}	V
		Low-Level Logic Input	1.06	--	V_{DD}	V
V_{IL}	LOW-Level Input Voltage PIN 2, 3, 4, 5, 6, 7, 8	Logic Input	0	--	1.31	V
		Logic Input with Schmitt Trigger	0	--	0.97	V
		Low-Level Logic Input	0	--	0.67	V
V_{HYS}	Schmitt Trigger Hysteresis Voltage PIN 2, 3, 4, 5, 6, 7, 8	Logic Input with Schmitt Trigger	0.29	0.62	0.94	V
I_{LGK}	Input leakage (Absolute Value) PIN 2, 3, 4, 5, 6, 7, 8		--	1	1000	nA
V_{OH}	HIGH-Level Output Voltage PIN 2, 3, 4, 5, 6, 7, 8	Push-Pull, I_{OH} = 3 mA, 1X Drive	2.74	3.12	--	V
		PMOS OD, I_{OH} = 3 mA, 1X Drive	2.74	3.12	--	V
		Push-Pull, I_{OH} = 3 mA, 2X Drive	2.87	3.21	--	V
		PMOS OD, I_{OH} = 3 mA, 2X Drive	2.87	3.21	--	V
V_{OL}	LOW-Level Output Voltage PIN 2, 3, 4, 5, 6, 7, 8	Push-Pull, I_{OL}= 3 mA, 1X Drive	--	0.13	0.23	V
		Push-Pull, I_{OL} = 3 mA, 2X Drive	--	0.06	0.11	V
		Open Drain, I_{OL} = 3 mA, 1X Drive	--	0.08	0.15	V
		Open Drain, I_{OL} = 3 mA, 2X Drive	--	0.04	0.08	V
		Open Drain NMOS 4X, I_{OL} = 3 mA	--	0.02	0.04	V
I_{OH}	HIGH-Level Output Pulse Current (see Note 1) PIN 2, 3, 4, 5, 6, 7, 8	Push-Pull, V_{OH} = 2.4 V, 1X Drive	6.05	12.08	--	mA
		PMOS OD, V_{OH} = 2.4 V, 1X Drive	6.05	12.08	--	mA
		Push-Pull, V_{OH} = 2.4 V, 2X Drive	11.54	24.16	--	mA
		PMOS OD, V_{OH} = 2.4 V, 2X Drive	11.52	24.16	--	mA
I_{OL}	LOW-Level Output Pulse Current (see Note 1) PIN 2, 3, 4, 5, 6, 7, 8	Push-Pull, V_{OL} = 0.4 V, 1X Drive	4.88	8.24	--	mA
		Push-Pull, V_{OL} = 0.4 V, 2X Drive	9.75	16.49	--	mA
		Open Drain, V_{OL} = 0.4 V, 1X Drive	7.31	12.37	--	mA
		Open Drain, V_{OL} = 0.4 V, 2X Drive	14.54	24.74	--	mA
		Open Drain NMOS 4X, V_{OL} = 0.4 V	31.32	41.06	--	mA
I_{VDD}	Maximum Average or DC Current Through VDD Pin (Per chip side, see Note 2)	T_J = 85°C	--	--	45	mA
		T_J = 110°C	--	--	22	mA

Symbol	Parameter	Condition/Note	Min.	Typ.	Max.	Unit
I_{GND}	Maximum Average or DC Current Through GND Pin (Per chip side, see Note 2)	T_J = 85°C	--	--	86	mA
		T_J = 110°C	--	--	41	mA
V_O	Maximal Voltage Applied to any PIN in High-Impedance State		--	--	V_{DD}	V
T_{SU}	Startup Time	from VDD rising past PON_{THR}	0.61	1.24	1.65	ms
PON_{THR}	Power On Threshold	V_{DD} Level Required to Start Up the Chip	1.41	1.54	1.66	V
$POFF_{THR}$	Power Off Threshold	V_{DD} Level Required to Switch Off the Chip	1.00	1.15	1.31	V
R_{PUP}	Pull Up Resistance	1 M Pull Up	873.2	1094.7	1364.3	kΩ
		100 k Pull Up	85.17	109.30	135.52	kΩ
		10 k Pull Up	9.61	11.86	14.73	kΩ
R_{PDWN}	Pull Down Resistance	1 M Pull Down	862.5	1096.3	1357.4	kΩ
		100 k Pull Down	87.95	109.76	136.06	kΩ
		10 k Pull Down	8.66	11.81	15.05	kΩ

Note 1: DC or average current through any pin should not exceed value given in Absolute Maximum Conditions.
Note 2: The GreenPAK's power rails are divided in two sides. Pins 2, 3, 4, 5, 6, 7 and 8 are connected to one side, pins 10, 12, 13 and 14 to another.

5.4 Electrical Characteristics (5 V ±10% V_{DD})

Symbol	Parameter	Condition/Note	Min.	Typ.	Max.	Unit
V_{DD}	Supply Voltage Pin 1	VDD2 ≤ VDD	4.5	5.0	5.5	V
I_Q	Quiescent Current	Static Inputs and Outputs	--	1.26	--	µA
T_A	Operating Temperature		-40	25	85	°C
V_{PP}	Programming Voltage		7.25	7.50	7.75	V
V_{ACMP}	ACMP Input Voltage Range	Positive Input	0	--	V_{DD}	V
		Negative Input	0	--	1.2	V
V_{IH}	HIGH-Level Input Voltage	Logic Input	2.68	--	V_{DD}	V
		Logic Input with Schmitt Trigger	3.34	--	V_{DD}	V
		Low-Level Logic Input	1.15	--	V_{DD}	V
V_{IL}	LOW-Level Input Voltage	Logic Input	0	--	1.96	V
		Logic Input with Schmitt Trigger	0	--	1.41	V
		Low-Level Logic Input	0	--	0.77	V
V_{HYS}	Schmitt Trigger Hysteresis Voltage PIN 2, 3, 4, 5, 6, 7, 8	Logic Input with Schmitt Trigger	0.44	0.90	1.38	V
I_{LGK}	Input leakage (Absolute Value) PIN 2, 3, 4, 5, 6, 7, 8		--	1	1000	nA
V_{OH}	HIGH-Level Output Voltage PIN 2, 3, 4, 5, 6, 7, 8	Push-Pull, I_{OH} = 5 mA, 1X Drive	4.15	4.76	--	V
		PMOS OD, I_{OH} = 5 mA, 1X Drive	4.16	4.76	--	V
		Push-Pull, I_{OH} = 5 mA, 2X Drive	4.32	4.89	--	V
		PMOS OD, I_{OH} = 5 mA, 2X Drive	4.33	4.89	--	V
V_{OL}	LOW-Level Output Voltage PIN 2, 3, 4, 5, 6, 7, 8	Push-Pull, I_{OL}= 5 mA, 1X Drive	--	0.19	0.24	V
		Push-Pull, I_{OL} =5 mA, 2X Drive	--	0.09	0.12	V
		Open Drain, I_{OL} = 5 mA, 1X Drive	--	0.12	0.16	V
		Open Drain, I_{OL} = 5 mA, 2X Drive	--	0.07	0.08	V
		Open Drain NMOS 4X, I_{OL} = 5 mA	--	0.03	0.05	V
I_{OH}	HIGH-Level Output Pulse Current (see Note 1) PIN 2, 3, 4, 5, 6, 7, 8	Push-Pull, V_{OH} = 2.4 V, 1X Drive	22.08	34.04	--	mA
		PMOS OD, V_{OH} = 2.4 V, 1X Drive	22.08	34.04	--	mA
		Push-Pull, V_{OH} = 2.4 V, 2X Drive	41.76	68.08	--	mA
		PMOS OD, V_{OH} = 2.4 V, 2X Drive	41.69	68.08	--	mA
I_{OL}	LOW-Level Output Pulse Current (see Note 1) PIN 2, 3, 4, 5, 6, 7, 8	Push-Pull, V_{OL} = 0.4 V, 1X Drive	7.22	11.58	--	mA
		Push-Pull, V_{OL} = 0.4 V, 2X Drive	13.83	23.16	--	mA
		Open Drain, V_{OL} = 0.4 V, 1X Drive	10.82	17.38	--	mA
		Open Drain, V_{OL} = 0.4 V, 2X Drive	17.34	34.76	--	mA
		Open Drain NMOS 4X, V_{OL} = 0.4 V	41.06	55.18	--	mA
I_{VDD}	Maximum Average or DC Current Through VDD Pin (Per chip side, see Note 2)	T_J = 85°C	--	--	45	mA
		T_J = 110°C	--	--	22	mA

Symbol	Parameter	Condition/Note	Min.	Typ.	Max.	Unit
I_{GND}	Maximum Average or DC Current Through GND Pin (Per chip side, see Note 2)	T_J = 85°C	--	--	86	mA
		T_J = 110°C	--	--	41	mA
V_O	Maximal Voltage Applied to any PIN in High-Impedance State		--	--	V_{DD}	V
T_{SU}	Startup Time	from VDD rising past PON_{THR}	0.60	1.23	1.61	ms
PON_{THR}	Power On Threshold	V_{DD} Level Required to Start Up the Chip	1.41	1.54	1.66	V
$POFF_{THR}$	Power Off Threshold	V_{DD} Level Required to Switch Off the Chip	1.00	1.15	1.31	V
R_{PUP}	Pull Up Resistance	1 M Pull Up	864.6	1093.4	1348.1	kΩ
		100 k Pull Up	84.32	108.97	135.24	kΩ
		10 k Pull Up	8.74	11.37	14.52	kΩ
R_{PDWN}	Pull Down Resistance	1 M Pull Down	873.3	1096.1	1370.5	kΩ
		100 k Pull Down	87.57	109.48	135.89	kΩ
		10 k Pull Down	7.95	11.33	14.78	kΩ

Note 1: DC or average current through any pin should not exceed value given in Absolute Maximum Conditions.
Note 2: The GreenPAK's power rails are divided in two sides. Pins 2, 3, 4, 5, 6, 7 and 8 are connected to one side, pins 10, 12, 13 and 14 to another.

5.5 Electrical Characteristics (1.8 V ±5% V_{DD2})

Symbol	Parameter	Condition/Note	Min.	Typ.	Max.	Unit
V_{DD2}	Supply Voltage Pin 9	VDD2 ≤ VDD	1.71	--	V_{DD}	V
V_{IH2}	HIGH-Level Input Voltage PIN 10, 12, 13, 14	Logic Input, V_{DD2} = 1.8 V	1.06	--	V_{DD2}	V
		Logic Input with Schmitt Trigger, V_{DD2} = 1.8 V	1.28	--	V_{DD2}	V
		Low-Level Logic Input, V_{DD2} = 1.8 V	0.94	--	V_{DD2}	V
V_{IL2}	LOW-Level Input Voltage PIN 10, 12, 13, 14	Logic Input, V_{DD2} = 1.8 V	0	--	0.76	V
		Logic Input with Schmitt Trigger, V_{DD2} = 1.8 V	0	--	0.49	V
		Low-Level Logic Input, V_{DD2} = 1.8 V	0	--	0.52	V
V_{HYS}	Schmitt Trigger Hysteresis Voltage PIN 10, 12, 13, 14	Logic Input with Schmitt Trigger, V_{DD2} = 1.8 V	0.10	0.41	0.66	V
I_{LKG}	Input leakage (Absolute Value) PIN 10, 12, 13, 14		--	1	1000	nA
V_{OH2}	HIGH-Level Output Voltage PIN 10, 12, 13, 14	Push-Pull 1X, Open Drain PMOS 1X, I_{OH} = 100 µA, V_{DD2} = 1.8 V	1.68	1.79	--	V
		Push-Pull 2X, Open Drain PMOS 2X, I_{OH} = 100 µA, V_{DD2} = 1.8 V	1.70	1.79	--	V
		Push-Pull 4X, Open Drain PMOS 4X, I_{OH} = 100 µA, V_{DD2} = 1.8 V	1.70	1.79	--	V
V_{OL2}	LOW-Level Output Voltage PIN 10, 12, 13, 14	Push-Pull 1X, I_{OL}= 100 µA, V_{DD2} = 1.8 V	--	0.010	0.015	V
		Push-Pull 2X, I_{OL} = 100 µA, V_{DD2} = 1.8 V	--	0.007	0.010	V
		Push-Pull 4X, I_{OL} = 100 µA, V_{DD2} = 1.8 V	--	0.004	0.015	V
		Open Drain NMOS 1X, I_{OL} = 100 µA, V_{DD2} = 1.8 V	--	0.007	0.010	V
		Open Drain NMOS 2X, I_{OL} = 100 µA, V_{DD2} = 1.8 V	--	0.003	0.010	V
I_{OH2}	HIGH-Level Output Pulse Current (see Note 1) PIN 10, 12, 13, 14	Push-Pull 1X,Open Drain PMOS 1X, V_{OH} = V_{DD} - 0.2, V_{DD2} = 1.8 V	1.03	1.70	--	mA
		Push-Pull 2X, Open Drain PMOS 2X, V_{OH} = V_{DD} - 0.2, V_{DD2} = 1.8 V	2.03	3.41	--	mA
I_{OL2}	LOW-Level Output Pulse Current (see Note 1) PIN 10, 12, 13, 14	Push-Pull 1X, V_{OL} = 0.15 V, V_{DD2} = 1.8 V	0.92	1.66	--	mA
		Push-Pull 2X, V_{OL} = 0.15 V, V_{DD2} = 1.8 V	1.83	3.30	--	mA
		Push-Pull 4X, V_{OL} = 0.15 V, V_{DD2} = 1.8 V	4.81	6.50	--	mA
		Open Drain NMOS 1X, V_{OL} = 0.15 V, V_{DD2} = 1.8 V	1.38	2.53	--	mA
		Open Drain NMOS 2X, V_{OL} = 0.15 V, V_{DD2} = 1.8 V	2.75	5.07	--	mA

Symbol	Parameter	Condition/Note	Min.	Typ.	Max.	Unit
I_{VDD}	Maximum Average or DC Current Through VDD Pin (Per chip side, see Note 2)	T_J = 85°C	--	--	45	mA
		T_J = 110°C	--	--	22	mA
I_{GND}	Maximum Average or DC Current Through GND Pin (Per chip side, see Note 2)	T_J = 85°C	--	--	86	mA
		T_J = 110°C	--	--	41	mA

Note 1: DC or average current through any pin should not exceed value given in Absolute Maximum Conditions.
Note 2: The GreenPAK's power rails are divided in two sides. Pins 2, 3, 4, 5, 6, 7 and 8 are connected to one side, pins 10, 12, 13 and 14 to another.

5.6 Electrical Characteristics (3.3 V ±10% V_{DD2})

Symbol	Parameter	Condition/Note	Min.	Typ.	Max.	Unit
V_{DD2}	Supply Voltage Pin 9	VDD2 ≤ VDD	1.71	--	V_{DD}	V
V_{IH2}	HIGH-Level Input Voltage PIN 10, 12, 13, 14	Logic Input, V_{DD2} = 1.8 V	1.06	--	V_{DD2}	V
		Logic Input with Schmitt Trigger, V_{DD2} = 1.8 V	1.28	--	V_{DD2}	V
		Low-Level Logic Input, V_{DD2} = 1.8 V	0.94	--	V_{DD2}	V
V_{IL2}	LOW-Level Input Voltage PIN 10, 12, 13, 14	Logic Input, V_{DD2} = 1.8 V	0	--	0.76	V
		Logic Input with Schmitt Trigger, V_{DD2} = 1.8 V	0	--	0.49	V
		Low-Level Logic Input, V_{DD2} = 1.8 V	0	--	0.52	V
V_{HYS}	Schmitt Trigger Hysteresis Voltage PIN 10, 12, 13, 14	Logic Input with Schmitt Trigger, V_{DD2} = 1.8 V	0.29	0.62	0.94	V
I_{LGK}	Input leakage (Absolute Value) PIN 10, 12, 13, 14		--	1	1000	nA
V_{OH2}	HIGH-Level Output Voltage PIN 10, 12, 13, 14	Push-Pull, I_{OH} = 100 µA, 1X Drive, V_{DD2} = 1.8 V	1.69	1.79	--	V
		PMOS OD, I_{OH} = 100 µA, 1X Drive, V_{DD2} = 1.8 V	1.69	1.79	--	V
		Push-Pull, I_{OH} = 100 µA, 2X Drive, V_{DD2} = 1.8 V	1.70	1.79	--	V
		PMOS OD, I_{OH} = 100 µA, 2X Drive, V_{DD2} = 1.8 V	1.70	1.79	--	V
V_{OL2}	LOW-Level Output Voltage PIN 10, 12, 13, 14	Push-Pull 1X Drive, I_{OL}= 100 µA, V_{DD2} = 1.8 V	--	0.01	0.03	V
		Push-Pull 2X Drive, I_{OL} = 100 µA, V_{DD2} = 1.8 V	--	0.01	0.01	V
		Open Drain NMOS 1X Drive, I_{OL} = 100 µA, V_{DD2} = 1.8 V	--	0.01	0.02	V
		Open Drain NMOS 2X Drive, I_{OL} = 100 µA, V_{DD2} = 1.8 V	--	0.01	0.02	V
I_{OH2}	HIGH-Level Output Pulse Current (see Note 1) PIN 10, 12, 13, 14	Push-Pull, V_{OH} = V_{DD} - 0.2, 1X Drive, V_{DD2} = 1.8 V	1.07	1.70	--	mA
		PMOS OD, V_{OH} = V_{DD} - 0.2, 1X Drive, V_{DD2} = 1.8 V	1.07	1.70	--	mA
		Push-Pull, V_{OH} = V_{DD} - 0.2, 2X Drive, V_{DD2} = 1.8 V	2.22	3.41	--	mA
		PMOS OD, V_{OH} = V_{DD} - 0.2, 2X Drive, V_{DD2} = 1.8 V	2.22	3.41	--	mA

Symbol	Parameter	Condition/Note	Min.	Typ.	Max.	Unit
I_{OL2}	LOW-Level Output Pulse Current (see Note 1) PIN 10, 12, 13, 14	Push-Pull, V_{OL} = 0.15 V, 1X Drive, V_{DD2} = 1.8 V	0.92	1.69	--	mA
		Push-Pull, V_{OL} = 0.15 V, 2X Drive, V_{DD2} = 1.8 V	1.83	3.38	--	mA
		Open Drain, V_{OL} = 0.15 V, 1X Drive, V_{DD2} = 1.8 V	1.38	2.53	--	mA
		Open Drain, V_{OL} = 0.15 V, 2X Drive, V_{DD2} = 1.8 V	2.75	5.07	--	mA
		Open Drain, V_{OL} = 0.15 V, 4X Drive, V_{DD2} = 1.8 V	5.50	10.14	--	mA
V_{IH2}	HIGH-Level Input Voltage PIN 10, 12, 13, 14	Logic Input, V_{DD2} = 3.3 V	1.81	--	V_{DD}	V
		Logic Input with Schmitt Trigger, V_{DD2} = 3.3 V	2.14	--	V_{DD}	V
		Low-Level Logic Input, V_{DD2} = 3.3 V	1.06	--	V_{DD}	V
V_{IL2}	LOW-Level Input Voltage PIN 10, 12, 13, 14	Logic Input, V_{DD2} = 3.3 V	0	--	1.31	V
		Logic Input with Schmitt Trigger, V_{DD2} = 3.3 V	0	--	0.97	V
		Low-Level Logic Input, V_{DD2} = 3.3 V	0	--	0.67	V
V_{OH2}	HIGH-Level Output Voltage PIN 10, 12, 13, 14	Push-Pull, I_{OH} = 3 mA, 1X Drive, V_{DD2} = 3.3 V	2.70	3.12	--	V
		PMOS OD, I_{OH} = 3 mA, 1X Drive, V_{DD2} = 3.3 V	2.70	3.12	--	V
		Push-Pull, I_{OH} = 3 mA, 2X Drive, V_{DD2} = 3.3 V	2.85	3.21	--	V
		PMOS OD, I_{OH} = 3 mA, 2X Drive, V_{DD2} = 3.3 V	2.86	3.21	--	V
V_{OL2}	LOW-Level Output Voltage PIN 10, 12, 13, 14	Push-Pull, I_{OL}= 3 mA, 1X Drive, V_{DD2} = 3.3 V	--	0.13	0.23	V
		Push-Pull, I_{OL} = 3 mA, 2X Drive, V_{DD2} = 3.3 V	--	0.06	0.11	V
		Open Drain, I_{OL} = 3 mA, 1X Drive, V_{DD2} = 3.3 V	--	0.08	0.15	V
		Open Drain, I_{OL} = 3 mA, 2X Drive, V_{DD2} = 3.3 V	--	0.04	0.08	V
I_{OH2}	HIGH-Level Output Current PIN 10, 12, 13, 14	Push-Pull, V_{OH} = 2.4 V, 1X Drive, V_{DD2} = 3.3 V	6.05	12.08	--	mA
		PMOS OD, V_{OH} = 2.4 V, 1X Drive, V_{DD2} = 3.3 V	6.05	12.08	--	mA
		Push-Pull, V_{OH} = 2.4 V, 2X Drive, V_{DD2} = 3.3 V	11.54	24.16	--	mA
		PMOS OD, V_{OH} = 2.4 V, 2X Drive, V_{DD2} = 3.3 V	11.52	24.16	--	mA

Symbol	Parameter	Condition/Note	Min.	Typ.	Max.	Unit
I_{OL2}	LOW-Level Output Current PIN 10, 12, 13, 14	Push-Pull, V_{OL} = 0.4 V, 1X Drive, V_{DD2} = 3.3 V	4.88	8.24	--	mA
		Push-Pull, V_{OL} = 0.4 V, 2X Drive, V_{DD2} = 3.3 V	9.75	16.49	--	mA
		Open Drain, V_{OL} = 0.4 V, 1X Drive, V_{DD2} = 3.3 V	7.31	12.37	--	mA
		Open Drain, V_{OL} = 0.4 V, 2X Drive, V_{DD2} = 3.3 V	14.54	24.74	--	mA
I_{VDD}	Maximum Average or DC Current Through VDD Pin (Per chip side, see Note 2)	T_J = 85°C	--	--	45	mA
		T_J = 110°C	--	--	22	mA
I_{GND}	Maximum Average or DC Current Through GND Pin (Per chip side, see Note 2)	T_J = 85°C	--	--	86	mA
		T_J = 110°C	--	--	41	mA

Note 1: DC or average current through any pin should not exceed value given in Absolute Maximum Conditions.
Note 2: The GreenPAK's power rails are divided in two sides. Pins 2, 3, 4, 5, 6, 7 and 8 are connected to one side, pins 10, 12, 13 and 14 to another.

5.7 Electrical Characteristics (5 V ±10% V_{DD2})

Symbol	Parameter	Condition/Note	Min.	Typ.	Max.	Unit
V_{DD2}	Supply Voltage	VDD2 ≤ VDD	1.71	--	V_{DD}	V
V_{IH2}	HIGH-Level Input Voltage PIN 10, 12, 13, 14	Logic Input, V_{DD2} = 1.8 V	1.06	--	V_{DD2}	V
		Logic Input with Schmitt Trigger, V_{DD2} = 1.8 V	1.28	--	V_{DD2}	V
		Low-Level Logic Input, V_{DD2} = 1.8 V	0.94	--	V_{DD2}	V
V_{IL2}	LOW-Level Input Voltage PIN 10, 12, 13, 14	Logic Input, V_{DD2} = 1.8 V	0	--	0.76	V
		Logic Input with Schmitt Trigger, V_{DD2} = 1.8 V	0	--	0.49	V
		Low-Level Logic Input, V_{DD2} = 1.8 V	0	--	0.52	V
V_{HYS}	Schmitt Trigger Hysteresis Voltage PIN 10, 12, 13, 14	Logic Input with Schmitt Trigger, V_{DD2} = 1.8 V	0.29	0.62	0.94	V
I_{LGK}	Input leakage (Absolute Value) PIN 10, 12, 13, 14		--	1	1000	nA
V_{OH2}	HIGH-Level Output Voltage PIN 10, 12, 13, 14	Push-Pull, I_{OH} = 100 µA, 1X Drive, V_{DD2} = 1.8 V	1.69	1.79	--	V
		PMOS OD, I_{OH} = 100 µA, 1X Drive, V_{DD2} = 1.8 V	1.69	1.79	--	V
		Push-Pull, I_{OH} = 100 µA, 2X Drive, V_{DD2} = 1.8 V	1.70	1.79	--	V
		PMOS OD, I_{OH} = 100 µA, 2X Drive, V_{DD2} = 1.8 V	1.70	1.79	--	V
V_{OL2}	LOW-Level Output Voltage PIN 10, 12, 13, 14	Push-Pull 1X Drive, I_{OL}= 100 µA, V_{DD2} = 1.8 V	--	0.01	0.03	V
		Push-Pull 2X Drive, I_{OL} = 100 µA, V_{DD2} = 1.8 V	--	0.01	0.01	V
		Open Drain NMOS 1X Drive, I_{OL} = 100 µA, V_{DD2} = 1.8 V	--	0.01	0.02	V
		Open Drain NMOS 2X Drive, I_{OL} = 100 µA, V_{DD2} = 1.8 V	--	0.01	0.02	V
I_{OH2}	HIGH-Level Output Pulse Current (see Note 1) PIN 10, 12, 13, 14	Push-Pull, V_{OH} = V_{DD} - 0.2, 1X Drive, V_{DD2} = 1.8 V	1.07	1.70	--	mA
		PMOS OD, V_{OH} = V_{DD} - 0.2, 1X Drive, V_{DD2} = 1.8 V	1.07	1.70	--	mA
		Push-Pull, V_{OH} = V_{DD} - 0.2, 2X Drive, V_{DD2} = 1.8 V	2.22	3.41	--	mA
		PMOS OD, V_{OH} = V_{DD} - 0.2, 2X Drive, V_{DD2} = 1.8 V	2.22	3.41	--	mA

Symbol	Parameter	Condition/Note	Min.	Typ.	Max.	Unit
I_{OL2}	LOW-Level Output Pulse Current (see Note 1) PIN 10, 12, 13, 14	Push-Pull, V_{OL} = 0.15 V, 1X Drive, V_{DD2} = 1.8 V	0.92	1.69	--	mA
		Push-Pull, V_{OL} = 0.15 V, 2X Drive, V_{DD2} = 1.8 V	1.83	3.38	--	mA
		Open Drain, V_{OL} = 0.15 V, 1X Drive, V_{DD2} = 1.8 V	1.38	2.53	--	mA
		Open Drain, V_{OL} = 0.15 V, 2X Drive, V_{DD2} = 1.8 V	2.75	5.07	--	mA
		Open Drain, V_{OL} = 0.15 V, 4X Drive, V_{DD2} = 1.8 V	5.50	10.14	--	mA
V_{IH2}	HIGH-Level Input Voltage PIN 10, 12, 13, 14	Logic Input, V_{DD2} = 3.3 V	1.81	--	V_{DD}	V
		Logic Input with Schmitt Trigger, V_{DD2} = 3.3 V	2.14	--	V_{DD}	V
		Low-Level Logic Input, V_{DD2} = 3.3 V	1.06	--	V_{DD}	V
V_{IL2}	LOW-Level Input Voltage PIN 10, 12, 13, 14	Logic Input, V_{DD2} = 3.3 V	0	--	1.31	V
		Logic Input with Schmitt Trigger, V_{DD2} = 3.3 V	0	--	0.97	V
		Low-Level Logic Input, V_{DD2} = 3.3 V	0	--	0.67	V
V_{OH2}	HIGH-Level Output Voltage PIN 10, 12, 13, 14	Push-Pull, I_{OH} = 3 mA, 1X Drive, V_{DD2} = 3.3 V	2.70	3.12	--	V
		PMOS OD, I_{OH} = 3 mA, 1X Drive, V_{DD2} = 3.3 V	2.70	3.12	--	V
		Push-Pull, I_{OH} = 3 mA, 2X Drive, V_{DD2} = 3.3 V	2.85	3.21	--	V
		PMOS OD, I_{OH} = 3 mA, 2X Drive, V_{DD2} = 3.3 V	2.86	3.21	--	V
V_{OL2}	LOW-Level Output Voltage PIN 10, 12, 13, 14	Push-Pull, I_{OL}= 3 mA, 1X Drive, V_{DD2} = 3.3 V	--	0.13	0.23	V
		Push-Pull, I_{OL} = 3 mA, 2X Drive, V_{DD2} = 3.3 V	--	0.06	0.11	V
		Open Drain, I_{OL} = 3 mA, 1X Drive, V_{DD2} = 3.3 V	--	0.08	0.15	V
		Open Drain, I_{OL} = 3 mA, 2X Drive, V_{DD2} = 3.3 V	--	0.04	0.08	V
I_{OH2}	HIGH-Level Output Pulse Current (see Note 1) PIN 10, 12, 13, 14	Push-Pull, V_{OH} = 2.4 V, 1X Drive, V_{DD2} = 3.3 V	6.05	12.08	--	mA
		PMOS OD, V_{OH} = 2.4 V, 1X Drive, V_{DD2} = 3.3 V	6.05	12.08	--	mA
		Push-Pull, V_{OH} = 2.4 V, 2X Drive, V_{DD2} = 3.3 V	11.54	24.16	--	mA
		PMOS OD, V_{OH} = 2.4 V, 2X Drive, V_{DD2} = 3.3 V	11.52	24.16	--	mA

Symbol	Parameter	Condition/Note	Min.	Typ.	Max.	Unit
I_{OL2}	LOW-Level Output Pulse Current (see Note 1) PIN 10, 12, 13, 14	Push-Pull, V_{OL} = 0.4 V, 1X Drive, V_{DD2} = 3.3 V	4.88	8.24	--	mA
		Push-Pull, V_{OL} = 0.4 V, 2X Drive, V_{DD2} = 3.3 V	9.75	16.49	--	mA
		Open Drain, V_{OL} = 0.4 V, 1X Drive, V_{DD2} = 3.3 V	7.31	12.37	--	mA
		Open Drain, V_{OL} = 0.4 V, 2X Drive, V_{DD2} = 3.3 V	14.54	24.74	--	mA
V_{IH2}	HIGH-Level Input Voltage PIN 10, 12, 13, 14	Logic Input, V_{DD2} = 5.0 V	2.68	--	V_{DD}	V
		Logic Input with Schmitt Trigger, V_{DD2} = 5.0 V	3.34	--	V_{DD}	V
		Low-Level Logic Input, V_{DD2} = 5.0 V	1.15	--	V_{DD}	V
V_{IL2}	LOW-Level Input Voltage PIN 10, 12, 13, 14	Logic Input, V_{DD2} = 5.0 V	0	--	1.96	V
		Logic Input with Schmitt Trigger, V_{DD2} = 5.0 V	0	--	1.41	V
		Low-Level Logic Input, V_{DD2} = 5.0 V	0	--	0.77	V
V_{OH2}	HIGH-Level Output Voltage PIN 10, 12, 13, 14	Push-Pull, I_{OH} = 5 mA, 1X Drive, V_{DD2} = 5.0 V	4.15	4.76	--	V
		PMOS OD, I_{OH} = 5 mA, 1X Drive, V_{DD2} = 5.0 V	4.16	4.76	--	V
		Push-Pull, I_{OH} = 5 mA, 2X Drive, V_{DD2} = 5.0 V	4.32	4.89	--	V
		PMOS OD, I_{OH} = 5 mA, 2X Drive, V_{DD2} = 5.0 V	4.33	4.89	--	V
V_{OL2}	LOW-Level Output Voltage PIN 10, 12, 13, 14	Push-Pull, I_{OL}= 5 mA, 1X Drive, V_{DD2} = 5.0 V	--	0.19	0.24	V
		Push-Pull, I_{OL} = 5 mA, 2X Drive, V_{DD2} = 5.0 V	--	0.09	0.12	V
		Open Drain, I_{OL} = 5 mA, 1X Drive, V_{DD2} = 5.0 V	--	0.12	0.16	V
		Open Drain, I_{OL} = 5 mA, 2X Drive, V_{DD2} = 5.0 V	--	0.07	0.08	V
I_{OH2}	HIGH-Level Output Pulse Current (see Note 1) PIN 10, 12, 13, 14	Push-Pull, V_{OH} = 2.4 V, 1X Drive, V_{DD2} = 5.0 V	22.08	34.04	--	mA
		PMOS OD, V_{OH} = 2.4 V, 1X Drive, V_{DD2} = 5.0 V	22.08	34.04	--	mA
		Push-Pull, V_{OH} = 2.4 V, 2X Drive, V_{DD2} = 5.0 V	41.76	68.08	--	mA
		PMOS OD, V_{OH} = 2.4 V, 2X Drive, V_{DD2} = 5.0	41.69	68.08	--	mA
I_{OL2}	LOW-Level Output Pulse Current (see Note 1) PIN 10, 12, 13, 14	Push-Pull, V_{OL} = 0.4 V, 1X Drive, V_{DD2} = 5.0 V	7.22	11.58	--	mA
		Push-Pull, V_{OL} = 0.4 V, 2X Drive, V_{DD2} = 5.0 V	13.83	23.16	--	mA
		Open Drain, V_{OL} = 0.4 V, 1X Drive, V_{DD2} = 5.0 V	10.82	17.38	--	mA
		Open Drain, V_{OL} = 0.4 V, 2X Drive, V_{DD2} = 5.0 V	17.34	34.76	--	mA

Symbol	Parameter	Condition/Note	Min.	Typ.	Max.	Unit
I_{VDD}	Maximum Average or DC Current Through VDD Pin (Per chip side, see Note 2)	T_J = 85°C	--	--	45	mA
		T_J = 110°C	--	--	22	mA
I_{GND}	Maximum Average or DC Current Through GND Pin (Per chip side, see Note 2)	T_J = 85°C	--	--	86	mA
		T_J = 110°C	--	--	41	mA

Note 1: DC or average current through any pin should not exceed value given in Absolute Maximum Conditions.
Note 2: The GreenPAK's power rails are divided in two sides. Pins 2, 3, 4, 5, 6, 7 and 8 are connected to one side, pins 10, 12, 13 and 14 to another.

5.8 I²C Specifications

Symbol	Parameter	Condition/Note	Min.	Typ.	Max.	Unit
F_{SCL}	Clock Frequency, SCL	V_{DD} = (1.71...5.5) V	--	--	400	kHz
t_{LOW}	Clock Pulse Width Low	V_{DD} = (1.71...5.5) V	1300			ns
t_{HIGH}	Clock Pulse Width High	V_{DD} = (1.71...5.5) V	600	--	--	ns
t_I	Input Filter Spike Suppression (SCL, SDA)	V_{DD} = 1.8 V ± 5 %	--	--	95	ns
		V_{DD} = 3.3 V ± 10%			95	
		V_{DD} = 5.0 V ± 10 %			111	
t_{AA}	Clock Low to Data Out Valid	V_{DD} = (1.71...5.5) V	--	--	900	ns
t_{BUF}	Bus Free Time between Stop and Start	V_{DD} = (1.71...5.5) V	1300	--	--	ns
t_{HD_STA}	Start Hold Time	V_{DD} = (1.71...5.5) V	600	--	--	ns
t_{SU_STA}	Start Set-up Time	V_{DD} = (1.71...5.5) V	600	--	--	ns
t_{HD_DAT}	Data Hold Time	V_{DD} = (1.71...5.5) V	0	--	--	ns
t_{SU_DAT}	Data Set-up Time	V_{DD} = (1.71...5.5) V	100	--	--	ns
t_R	Inputs Rise Time	V_{DD} = (1.71...5.5) V	--	--	300	ns
t_F	Inputs Fall Time	V_{DD} = (1.71...5.5) V	--	--	300	ns
t_{SU_STO}	Stop Set-up Time	V_{DD} = (1.71...5.5) V	600	--	--	ns
t_{DH}	Data Out Hold Time	V_{DD} = (1.71...5.5) V	50	--	--	ns

5.9 Asynchronous State Machine (ASM) Specifications

Table 1. ASM Specifications

Symbol	Parameter	Condition	Min	Typ	Max	Unit
tst_out_delay	Asynchronous State Machine Output Delay Time	V_{DD} = 1.8 V ± 5 %	104	--	213	ns
		V_{DD} = 3.3 V ± 10 %	44	--	89	
		V_{DD} = 5.0 V ± 10 %	32	--	58	
tst_out	Asynchronous State Machine Output Transition Time	V_{DD} = 1.8 V ± 5 %	--	--	165	ns
		V_{DD} = 3.3 V ± 10 %	--	--	70	
		V_{DD} = 5.0 V ± 10 %	--	--	45	
tst_pulse	Asynchronous State Machine Input Pulse Acceptance Time	V_{DD} = 1.8 V ± 5 %	14	--	--	ns
		V_{DD} = 3.3 V ± 10 %	6	--	--	
		V_{DD} = 5.0 V ± 10 %	5	--	--	
tst_comp	Asynchronous State Machine Input Compete Time	V_{DD} = 1.8 V ± 5 %	--	--	20	ns
		V_{DD} = 3.3 V ± 10 %	--	--	8	
		V_{DD} = 5.0 V ± 10 %	--	--	5	

5.10 IDD Estimator

Table 2. Typical Current Estimated for Each Macrocell at T=25°C

Symbol	Parameter	Note	V_{DD}/V_{DD2} = 1.8 V	V_{DD}/V_{DD2} = 3.3V	V_{DD}/V_{DD2} = 5.0V	Unit
I	Current	Chip Quiescent, IDD1	0.45	0.75	1.12	µA
		Chip Quiescent, IDD2	0.015	0.021	0.029	µA
		OSC 2 MHz, predivide = 1	41.48	64.00	94.89	µA
		OSC 2 MHz, predivide = 8	25.68	32.41	43.22	µA
		OSC 25 kHz, predivide = 1	7.16	7.94	9.25	µA
		OSC 25 kHz, predivide = 8	6.97	7.60	8.68	µA
		OSC 25 MHz, predivide = 1	87.25	238.27	428.66	µA
		OSC 25 MHz, predivide = 8	78.01	212.45	390.17	µA
		ACMP (each)	54.96	52.64	60.81	µA
		ACMP with buffer (each)	75.06	72.74	81.25	µA
		Vref (each)	49.70	47.32	55.60	µA
		Vref with Buffer (each)	71.93	71.27	79.62	µA

5.11 Timing Estimator

Table 3. Typical Delay Estimated for Each Macrocell at T=25°C

Symbol	Parameter	Note	V_{DD}/V_{DD2} = 1.8 V		V_{DD}/V_{DD2} = 3.3V		V_{DD}/V_{DD2} = 5.0V		Unit
			rising	falling	rising	falling	rising	falling	
tpd	Delay	Digital Input to PP 1X	42	45	17	19	12	13	ns
tpd	Delay	Digital Input with Schmitt Trigger to PP 1X	42	43	16	17	18	12	ns
tpd	Delay	Low Voltage Digital input to PP 1X	45	428	17	177	12	120	ns
tpd	Delay	Digital input to PMOS output	42	-	17	-	12	-	ns
tpd	Delay	Digital input to NMOS output	-	80	-	27	-	18	ns

Table 3. Typical Delay Estimated for Each Macrocell at T=25°C

Symbol	Parameter	Note	V_{DD}/V_{DD2} = 1.8 V		V_{DD}/V_{DD2} = 3.3V		V_{DD}/V_{DD2} = 5.0V		Unit
			rising	falling	rising	falling	rising	falling	
tpd	Delay	Output enable from pin, OE Hi-Z to 1	53	-	21	-	15	-	ns
tpd	Delay	Output enable from pin, OE Hi-Z to 0	50	-	20	-	14	-	ns
tpd	Delay	LUT2bit (LATCH)	34	33	14	13	10	9	ns
tpd	Delay	LATCH (LUT2bit)	30	34	14	13	10	9	ns
tpd	Delay	LUT3bit (LATCH)	38	37	18	15	13	10	ns
tpd	Delay	LATCH+nRESET (LUT3bit)	45	42	21	17	15	12	ns
tpd	Delay	LUT4bit	28	33	14	13	10	9	ns
tpd	Delay	LUT2bt	19	26	10	10	7	7	ns
tpd	Delay	LUT3bit	28	34	14	13	10	9	ns
tpd	Delay	CNT/DLY Logic	40	38	18	15	13	11	ns
tpd	Delay	P_DLY1C	367	356	165	160	123	119	ns
tpd	Delay	P_DLY2C	720	718	314	312	233	231	ns
tpd	Delay	P_DLY3C	1061	1060	462	460	343	341	ns
tpd	Delay	P_DLY4C	1396	1400	609	609	451	451	ns
tpd	Delay	Filter	200	200	78	78	53	53	ns
tpd	Delay	ACMP (5 mV overdrive, IN- = 600 mV)	3000	3000	2000	2000	2000	2000	ns
tw	width	I/O with 1X push pull (min transmitted)	20	20	20	20	20	20	ns
tw	width	filter (min transmitted)	150	150	55	55	35	35	ns

5.12 Typical Counter/Delay Offset Measurements

Table 4. Typical Counter/Delay Offset Measurements

Parameter	RC OSC Freq	RC OSC Power	V_{DD} = 1.8 V	V_{DD} = 3.3V	V_{DD} = 5.0V	Unit
Offset (Power On Delay)	25 kHz	auto	1.6	1.6	1.6	µs
Offset (Power On Delay), fast start	25 kHz	auto	2.1	2.1	2.1	µs
Offset (Power On Delay)	2 MHz	auto	0.4	0.2	0.2	µs
Offset (Power On Delay), fast start	2 MHz	auto	0.7	0.5	0.4	µs
Offset (Power On Delay)	25 MHz	auto	0.01	0.05	0.04	µs
Frequency settling time	25 kHz	auto	19	14	12	µs
Frequency settling time	2 MHz	auto	14	14	14	µs
Variable (CLK period)	25 kHz	forced	0-40	0-40	0-40	µs
Variable (CLK period)	2 MHz	forced	0-0.5	0-0.5	0-0.5	µs
Variable (CLK period)	25 MHz		0-0.04	0-0.04	0-0.04	µs
Tpd (non-delayed edge)	25 kHz/ 2 MHz	either	35	14	10	ns

5.13 Expected Delays and Widths

Table 5. Expected Delays and Widths (typical)

Symbol	Parameter	Note	V_{DD} = 1.8 V	V_{DD} = 3.3V	V_{DD} = 5.0V	Unit
Width	Width, 1 cell	mode:(any)edge detect, edge detect output	296	135	101	ns
Width	Width, 2 cell	mode:(any)edge detect, edge detect output	597	272	203	ns
Width	Width, 3 cell	mode:(any)edge detect, edge detect output	898	410	305	ns
Width	Width, 4 cell	mode:(any)edge detect, edge detect output	1195	546	407	ns
time1	Delay, 1 cell	mode:(any)edge detect, edge detect output	55	24	18	ns
time1	Delay, 2 cell	mode:(any)edge detect, edge detect output	55	24	18	ns
time1	Delay, 3 cell	mode:(any)edge detect, edge detect output	55	24	18	ns
time1	Delay, 4 cell	mode:(any)edge detect, edge detect output	55	24	18	ns
time2	Delay, 1 cell	mode: both edge delay, edge detect output	367	165	106	ns
time2	Delay, 2 cell	mode: both edge delay, edge detect output	667	300	193	ns
time2	Delay, 3 cell	mode: both edge delay, edge detect output	968	440	279	ns
time2	Delay, 4 cell	mode: both edge delay, edge detect output	1265	575	365	ns

5.14 Typical Pulse Width Performance

Table 6. Typical Pulse Width Performance at T=25°C

Parameter	V_{DD} = 1.8 V	V_{DD} = 3.3V	V_{DD} = 5.0V	Unit
Filtered Pulse Width for Filter 0	< 114	< 47	< 30	ns
Filtered Pulse Width for Filter 1	< 75	< 30	< 19	ns

5.15 OSC Specifications

Table 7. 25 kHz RC OSC0 frequency limits

Power Supply Range (VDD) V	Temperature Range					
	+25 °C		0 °C ... +85 °C		-40 °C ... +85 °C	
	Minimum Value, kHz	Maximum Value, kHz	Minimum Value, kHz	Maximum Value, kHz	Minimum Value, kHz	Maximum Value, kHz
1.8 V ±5%	23.792	26.288	23.275	27.089	21.728	29.173
3.3 V ±10%	24.473	25.526	23.357	26.028	23.357	27.002
5 V ±10%	24.316	25.939	23.309	26.177	23.309	27.181
2.5 V ... 4.5 V	24.438	25.559	23.336	26.051	23.336	27.038
1.71 V… 5.5 V	23.354	26.670	22.828	27.483	21.301	29.545

Table 8. 25 kHz RC OSC0 frequency error (error calculated relative to nominal value)

Power Supply Range (VDD) V	Temperature Range					
	+25 °C		0 °C ... +85 °C		-40 °C ... +85 °C	
	Error (% at Minimum)	Error (% at Maximum)	Error (% at Minimum)	Error (% at Maximum)	Error (% at Minimum)	Error (% at Maximum)
1.8 V ±5%	-4.83%	5.15%	-6.90%	8.36%	-13.09%	16.69%
3.3 V ±10%	-2.11%	2.10%	-6.57%	4.11%	-6.57%	8.01%
5 V ±10%	-2.73%	3.76%	-6.76%	4.71%	-6.76%	8.72%
2.5 V ... 4.5 V	-2.25%	2.24%	-6.66%	4.21%	-6.66%	8.15%
1.71 V… 5.5 V	-6.58%	6.68%	-8.69%	9.93%	-14.80%	18.18%