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SLG46537

GreenPAK
Programmable Mixed-signal Matrix with Asynchronous State Machine

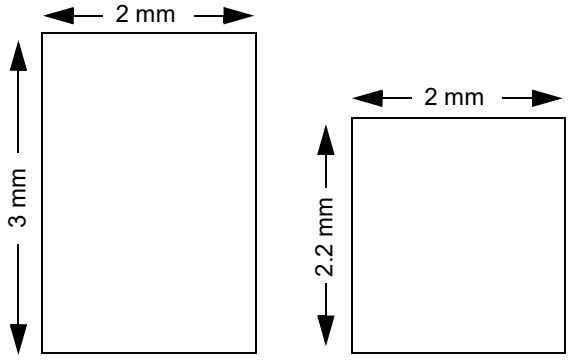
Features

- Logic & Mixed Signal Circuits
- Highly Versatile Macrocells
- Read Back Protection (Read Lock)
- 1.8 V (±5%) to 5 V (±10%) Supply
- Operating Temperature Range: -40°C to 85°C
- RoHS Compliant / Halogen-Free
- 20-pin STQFN: 2 x 3 x 0.55 mm, 0.4 mm pitch or
  22-pin MSTQFN: 2 x 2.2 x 0.55 mm, 0.4 mm pitch

Applications

- Personal Computers and Servers
- PC Peripherals
- Consumer Electronics
- Data Communications Equipment
- Handheld and Portable Electronics

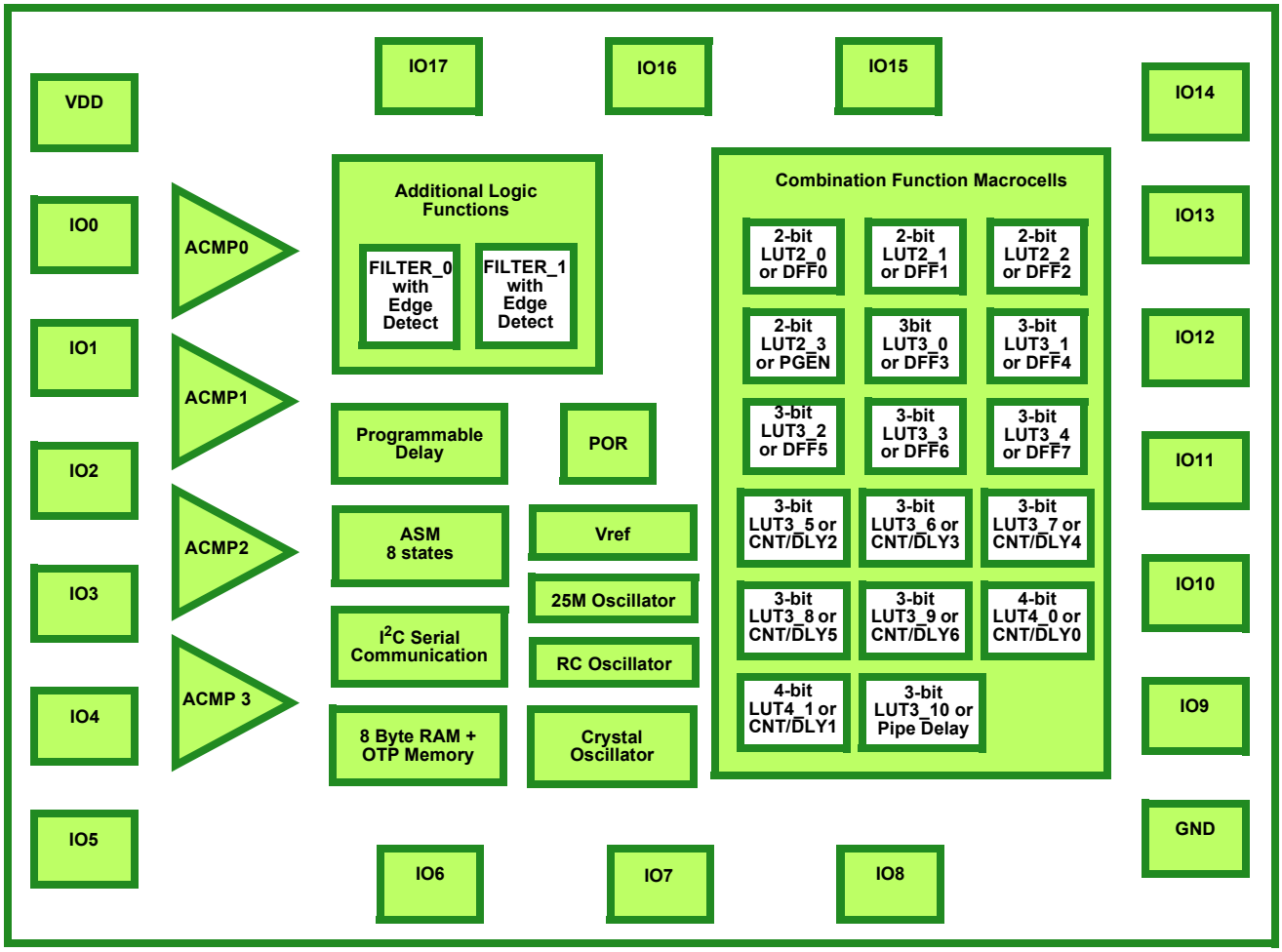
Available Package Options



STQFN-20 (Top View) **MSTQFN-22 (Top View)**

Packages drawn to scale

Block Diagram



1.0 Overview

The SLG46537 provides a small, low power component for commonly used mixed-signal functions. The user creates their circuit design by programming the one time Non-Volatile Memory (NVM) to configure the interconnect logic, the I/O Pins and the macrocells of the SLG46537. This highly versatile device allows a wide variety of mixed-signal functions to be designed within a very small, low power single integrated circuit. The macrocells in the device include the following:

- Four Analog Comparators (ACMP)
- Two Voltage References (Vref)
- Nineteen Combination Function Macrocells
  - Three Selectable DFF/Latch or 2-bit LUTs
  - One Selectable Continuous DFF/Latch or 3-bit LUT
  - Four Selectable DFF/Latch or 3-bit LUTs
  - One Selectable Pipe Delay or 3-bit LUT
  - One Selectable Programmable Pattern Generator or 2-bit LUT
  - Five 8-bit delays/counters or 3-bit LUTs
  - Two 16-bit delays/counters or 4-bit LUTs
  - Two Deglitch Filters with Edge Detectors
- Asynchronous State Machine
  - Eight States
  - Flexible input logic from state transitions
- Serial Communications
  - I^2C Protocol compliant
- Pipe Delay – 16 stage/3 output (Part of Combination Function Macrocell)
- Programmable Delay
- Two Oscillators (OSC)
  - Configurable 25 kHz/2 MHz
  - 25 MHz RC Oscillator
- Crystal Oscillator
- Power-On-Reset (POR)
- Eight Byte RAM + OTP User Memory
  - RAM Memory space that is readable and writable via I^2C
  - User defined initial values transferred from OTP
- Analog Temperature Sensor

2.0 Pin Description

2.1 Functional Pin Description

STQFN 20L Pin #	MSTQFN 22L Pin#	Pin Name	Signal Name	Function	Input Options	Output Options
1	16	VDD	VDD	Power Supply	--	--
2	1	IO0	IO0	General Purpose Input	Digital Input without Schmitt Trigger	--
					Digital Input with Schmitt Trigger	--
					Low Voltage Digital Input	--
3	2	IO1	IO1	General Purpose I/O with OE*	Digital Input without Schmitt Trigger	Push-Pull (1x) (2x)
					Digital Input with Schmitt Trigger	Open Drain NMOS (1x) (2x)
					Low Voltage Digital Input	--
4	3	IO2	IO2	General Purpose I/O	Digital Input without Schmitt Trigger	Push-Pull (1x) (2x)
					Digital Input with Schmitt Trigger	Open Drain NMOS (1x) (2x)
					Low Voltage Digital Input	Open Drain PMOS (1x) (2x)
5	4	IO3	IO3	General Purpose I/O with OE*	Digital Input without Schmitt Trigger	Push-Pull (1x) (2x)
					Digital Input with Schmitt Trigger	Open Drain NMOS (1x) (2x)
					Low Voltage Digital Input	--
6	5	IO4	IO4	General Purpose I/O	Digital Input without Schmitt Trigger	Push-Pull (1x) (2x)
					Digital Input with Schmitt Trigger	Open Drain NMOS (1x) (2x)
					Low Voltage Digital Input	Open Drain PMOS (1x) (2x)
			ACMP0+	Analog Comparator 0 Positive Input	Analog	--
7	6	IO5	IO5	General Purpose I/O with OE*	Digital Input without Schmitt Trigger	Push-Pull (1x) (2x)
					Digital Input with Schmitt Trigger	Open Drain NMOS (1x) (2x)
					Low Voltage Digital Input	--
			ACMP0-	Analog Comparator 0 Negative Input	Analog	--

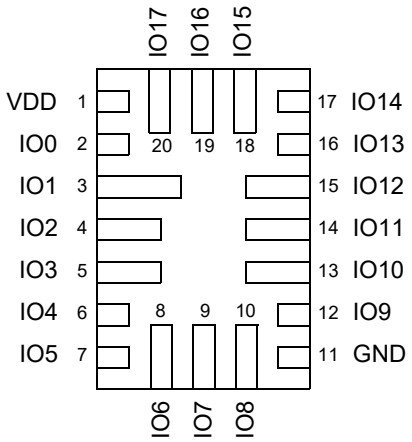
STQFN 20L Pin #	MSTQFN 22L Pin#	Pin Name	Signal Name	Function	Input Options	Output Options
8	19	IO6	IO6	General Purpose I/O	Digital Input without Schmitt Trigger	Open Drain NMOS (1x) (2x)
					Digital Input with Schmitt Trigger	--
					Low Voltage Digital Input	--
			SCL	I^2C Serial Clock	Digital Input without Schmitt Trigger	Open Drain NMOS
					Digital Input with Schmitt Trigger	Open Drain NMOS
					Low Voltage Digital Input	Open Drain NMOS
9	7	IO7	IO7	General Purpose I/O	Digital Input without Schmitt Trigger	Open Drain NMOS (1x) (2x)
					Digital Input with Schmitt Trigger	--
					Low Voltage Digital Input	--
			SDA	I^2C Serial Data	Digital Input without Schmitt Trigger	Open Drain NMOS
					Digital Input with Schmitt Trigger	Open Drain NMOS
					Low Voltage Digital Input	Open Drain NMOS
10	8	IO8	IO8	General Purpose I/O with OE*	Digital Input without Schmitt Trigger	Push-Pull (1x) (2x)
					Digital Input with Schmitt Trigger	Open Drain NMOS (1x) (2x) (4x)
					Low Voltage Digital Input	Open Drain PMOS (1x) (2x)
			ACMP1+	Analog Comparator 1 Positive Input	Analog	--
11	20	GND	GND	Ground	--	--
12	21	IO9	IO9	General Purpose I/O	Digital Input without Schmitt Trigger	Push-Pull (1x) (2x)
					Digital Input with Schmitt Trigger	Open Drain NMOS (1x) (2x) (4x)
					Low Voltage Digital Input	--
			EXT_VREF	Analog Comparator Negative Input	Analog	--
13	11	IO10	IO10	General Purpose I/O with OE*	Digital Input without Schmitt Trigger	Push-Pull (1x) (2x)
					Digital Input with Schmitt Trigger	Open Drain NMOS (1x) (2x)
					Low Voltage Digital Input	--
			ACMP2+	Analog Comparator 2 Positive Input	Analog	--
			ACMP3+	Analog Comparator 3 Positive Input	Analog	--

STQFN 20L Pin #	MSTQFN 22L Pin#	Pin Name	Signal Name	Function	Input Options	Output Options
14	12	IO11	IO11	General Purpose I/O with OE*	Digital Input without Schmitt Trigger	Push-Pull (1x) (2x)
					Digital Input with Schmitt Trigger	Open Drain NMOS (1x) (2x)
					Low Voltage Digital Input	--
			ACMP2-	Analog Comparator 2 Negative Input	Analog	--
			ACMP3-	Analog Comparator 3 Negative Input	Analog	--
15	22	IO12	IO12	General Purpose I/O	Digital Input without Schmitt Trigger	Push-Pull (1x) (2x)
					Digital Input with Schmitt Trigger	Open Drain NMOS (1x) (2x)
					Low Voltage Digital Input	Open Drain PMOS (1x) (2x)
			ACMP3+	Analog Comparator 3 Positive Input	Analog	--
16	13	IO13	IO13	General Purpose I/O with OE*	Digital Input without Schmitt Trigger	Push-Pull (1x) (2x)
					Digital Input with Schmitt Trigger	Open Drain NMOS (1x) (2x)
					Low Voltage Digital Input	--
			XTAL0	External Crystal Connection 0	--	Analog
17	14	IO14	IO14	General Purpose I/O	Digital Input without Schmitt Trigger	Push-Pull (1x) (2x)
					Digital Input with Schmitt Trigger	Open Drain NMOS (1x) (2x)
					Low Voltage Digital Input	Open Drain PMOS (1x) (2x)
			XTAL1	External Crystal Connection 1	Analog	--
			EXT_CLK0	External Clock Connection 0	Digital Input without Schmitt Trigger	--
					Digital Input with Schmitt Trigger	--
					Low Voltage Digital Input	--

STQFN 20L Pin #	MSTQFN 22L Pin#	Pin Name	Signal Name	Function	Input Options	Output Options
18	18	IO15	IO15	General Purpose I/O with OE*	Digital Input without Schmitt Trigger	Push-Pull (1x) (2x)
					Digital Input with Schmitt Trigger	Open Drain NMOS (1x) (2x)
					Low Voltage Digital Input	--
			VREF0	Voltage Reference 0 Output	--	Analog
			EXT_CLK1	External Clock Connection 1	Digital Input without Schmitt Trigger	--
					Digital Input with Schmitt Trigger	--
					Low Voltage Digital Input	--
19	15	IO16	IO16	General Purpose I/O with OE*	Digital Input without Schmitt Trigger	Push-Pull (1x) (2x)
					Digital Input with Schmitt Trigger	Open Drain NMOS (1x) (2x)
					Low Voltage Digital Input	--
			VREF0	Voltage Reference 0 Output	--	Analog
20	17	IO17	IO17	General Purpose I/O	Digital Input without Schmitt Trigger	Push-Pull (1x) (2x)
					Digital Input with Schmitt Trigger	Open Drain NMOS (1x) (2x)
					Low Voltage Digital Input	Open Drain PMOS (1x) (2x)
			EXT_CLK2	External Clock Connection 2	Digital Input without Schmitt Trigger	--
					Digital Input with Schmitt Trigger	--
					Low Voltage Digital Input	--
--	9	NC	NC	No Connection	--	--
--	10	NC	NC	No Connection	--	--

*Note: * General Purpose I/O's with OE can be used to implement bidirectional signals under user control via Connection Matrix to OE signal in I/O structure.*

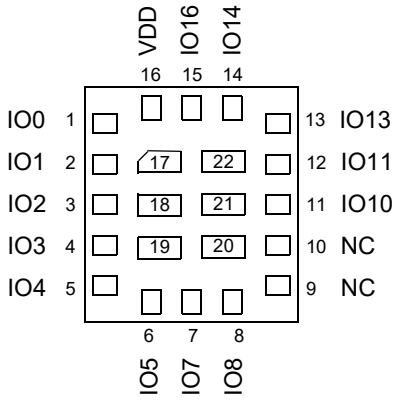
2.2 Pin Configuration - STQFN20L



STQFN-20
(Top View)

Pin #	Signal Name	Pin Functions
1	VDD	
2	IO0	GPI
3	IO1	GPIO with OE
4	IO2	GPIO
5	IO3	GPIO with OE
6	IO4	GPIO / ACMP0+
7	IO5	GPIO with OE / ACMP0-
8	IO6	GPIO / SCL
9	IO7	GPIO / SDA
10	IO8	GPIO with OE/ ACMP1+
11	GND	GND
12	IO9	GPIO / ACMP0- / ACMP1- / ACMP2- / ACMP3-
13	IO10	GPIO with OE / ACMP2+ / ACMP3+
14	IO11	GPIO with OE / ACMP2- / ACMP3-
15	IO12	GPIO / ACMP3+
16	IO13	GPIO with OE / XTAL0
17	IO14	GPIO / XTAL1 / EXT_CLK0
18	IO15	GPIO with OE / VREF0 / EXT_CLK1
19	IO16	GPIO with OE / VREF0
20	IO17	GPIO / EXT_CLK2

2.3 Pin Configuration - MSTQFN-22L



17 IO17
18 IO15
19 IO6
20 GND
21 IO9
22 IO12

MSTQFN-22L
(Top View)

Pin #	Signal Name	Pin Functions
1	IO0	GPI
2	IO1	GPIO with OE
3	IO2	GPIO
4	IO3	GPIO with OE
5	IO4	GPIO / ACMP0+
6	IO5	GPIO with OE
7	IO7	GPIO / SDA
8	IO8	GPIO with OE/ ACMP1+
9	NC	
10	NC	
11	IO10	GPIO with OE / ACMP2+ / ACMP3+
12	IO11	GPIO with OE / ACMP2- / ACMP3-
13	IO13	GPIO with OE / XTAL0
14	IO14	GPIO / XTAL1 / EXT_CLK0
15	IO16	GPIO with OE / VREF0
16	VDD	
17	IO17	GPIO / EXT_CLK2
18	IO15	GPIO with OE / VREF0 / EXT_CLK1
19	IO6	GPIO / SCL
20	GND	GND
21	IO9	GPIO / ACMP0- / ACMP1- / ACMP2- / ACMP3-
22	IO12	GPIO / ACMP3+

Legend:

OE: Output Enable
ACMPx+: ACMPx Positive Input
ACMPx-: ACMPx Negative Input
SCL/OD: I^2C Clock Input/ NMOS Open Drain Output Only
SDA/OD: I^2C Data Input/ NMOS Open Drain Output Only
VREFx: Voltage Reference Output
EXT_CLKx: External Clock Input

3.0 User Programmability

The SLG46537 is a user programmable device with One-Time-Programmable (OTP) memory elements that are able to construct combinatorial logic elements. Three of the I/O Pins provide a connection for the bit patterns into the OTP on board memory. A programming development kit allows the user the ability to create initial devices. Once the design is finalized, the programming code (.gpx file) is forwarded to Silego to integrate into a production process.

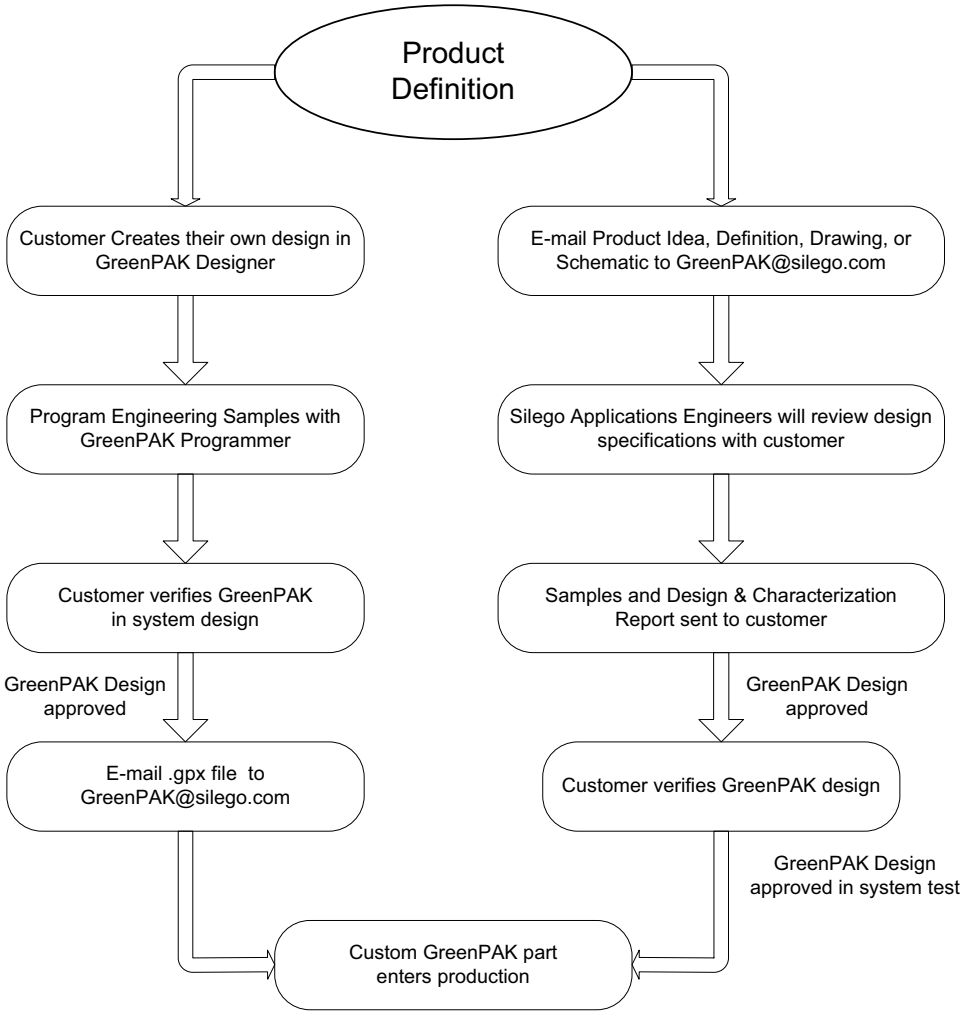


Figure 1. Steps to create a custom Silego GreenPAK device

4.0 Ordering Information

Part Number	Type
SLG46537V	20-pin STQFN
SLG46537VTR	20-pin STQFN - Tape and Reel (3k units)
SLG46537M	22-pin MSTQFN
SLG46537MTR	22-pin MSTQFN - Tape and Reel (3k units)

5.0 Electrical Specifications

5.1 Absolute Maximum Conditions

Parameter		Min.	Max.	Unit
Supply voltage on VDD relative to GND		-0.5	7	V
DC Input voltage		GND - 0.5	VDD + 0.5	V
Maximum Average or DC Current (Through pin)	Push-Pull 1x	--	11	mA
	Push-Pull 2x	--	16	
	OD 1x	--	11	
	OD 2x	--	21	
	OD 4x	--	43	
Current at Input Pin		-1.0	1.0	mA
Storage Temperature Range		-65	150	°C
Junction Temperature		--	150	°C
ESD Protection (Human Body Model)		2000	--	V
ESD Protection (Charged Device Model)		1300	--	V
Moisture Sensitivity Level		1		

5.2 Electrical Characteristics (1.8 V ±5% V_{DD})

Symbol	Parameter	Condition/Note	Min.	Typ.	Max.	Unit
V_{DD}	Supply Voltage		1.71	1.80	1.89	V
T_A	Operating Temperature		-40	25	85	°C
V_{PP}	Programming Voltage		7.25	7.50	7.75	V
V_{ACMP}	ACMP Input Voltage Range	Positive Input	0	--	V_{DD}	V
		Negative Input	0	--	1.2	V
V_{IH}	HIGH-Level Input Voltage	Logic Input	1.06	--	V_{DD}	V
		Logic Input with Schmitt Trigger	1.28	--	V_{DD}	V
		Low-Level Logic Input	0.94	--	V_{DD}	V
V_{IL}	LOW-Level Input Voltage	Logic Input	0	--	0.76	V
		Logic Input with Schmitt Trigger	0	--	0.49	V
		Low-Level Logic Input	0	--	0.52	V
V_{HYS}	Schmitt Trigger Hysteresis Voltage	Logic Input with Schmitt Trigger	0.10	0.41	0.66	V
I_{LKG}	Input leakage (Absolute Value)		--	1	1000	nA
V_{OH}	HIGH-Level Output Voltage	Push-Pull, I_{OH} = 100 µA, 1X Drive	1.69	1.79	--	V
		PMOS OD, I_{OH} = 100 µA, 1X Drive	1.69	1.79	--	V
		Push-Pull, I_{OH} = 100 µA, 2X Drive	1.70	1.79	--	V
		PMOS OD, I_{OH} = 100 µA, 2X Drive	1.70	1.79	--	V

Symbol	Parameter	Condition/Note	Min.	Typ.	Max.	Unit
V_{OL}	LOW-Level Output Voltage	Push-Pull, I_{OL}= 100 µA, 1X Drive	--	0.009	0.013	V
		Push-Pull, I_{OL} = 100 µA, 2X Drive	--	0.004	0.006	V
		Open Drain, I_{OL} = 100 µA, 1X Drive	--	0.006	0.009	V
		Open Drain, I_{OL} = 100 µA, 2X Drive	--	0.003	0.004	V
		Open Drain NMOS 4X, I_{OL} = 100 µA	--	0.001	0.002	V
I_{OH}	HIGH-Level Output Pulse Current (see Note 1)	Push-Pull, V_{OH} = V_{DD} - 0.2, 1X Drive	1.07	1.70	--	mA
		PMOS OD, V_{OH} = V_{DD} - 0.2, 1X Drive	1.07	1.70	--	mA
		Push-Pull, V_{OH} = V_{DD} - 0.2, 2X Drive	2.22	3.41	--	mA
		PMOS OD, V_{OH} = V_{DD} - 0.2, 2X Drive	2.22	3.41	--	mA
I_{OL}	LOW-Level Output Pulse Current (see Note 1)	Push-Pull, V_{OL} = 0.15 V, 1X Drive	0.92	1.69	--	mA
		Push-Pull, V_{OL} = 0.15 V, 2X Drive	1.83	3.38	--	mA
		Open Drain, V_{OL} = 0.15 V, 1X Drive	1.38	2.53	--	mA
		Open Drain, V_{OL} = 0.15 V, 2X Drive	2.75	5.07	--	mA
		Open Drain NMOS 4X, V_{OL} = 0.15 V	7.21	9.00	--	mA
I_{VDD}	Maximum Average or DC Current Through VDD Pin (Per chip side, see Note 2)	T_J = 85°C	--	--	45	mA
		T_J = 110°C	--	--	22	mA
I_{GND}	Maximum Average or DC Current Through GND Pin (Per chip side, see Note 2)	T_J = 85°C	--	--	86	mA
		T_J = 110°C	--	--	41	mA
V_O	Maximal Voltage Applied to any PIN in High-Impedance State		--	--	V_{DD}	V
T_{SU}	Startup Time	From VDD rising past PON_{THR}	0.63	1.36	1.87	ms
PON_{THR}	Power On Threshold	V_{DD} Level Required to Start Up the Chip	1.41	1.54	1.66	V
$POFF_{THR}$	Power Off Threshold	V_{DD} Level Required to Switch Off the Chip	1.00	1.15	1.31	V
R_{PUP}	Pull Up Resistance	1 M Pull Up	859.8	1097.1	1358.9	kΩ
		100 k Pull Up	86.47	110.13	136.18	kΩ
		10 k Pull Up	10.82	12.86	15.36	kΩ
R_{PDWN}	Pull Down Resistance	1 M Pull Down	873.9	1097.0	1359.0	kΩ
		100 k Pull Down	88.89	110.53	136.55	kΩ
		10 k Pull Down	9.65	12.75	15.76	kΩ

Note 1: DC or average current through any pin should not exceed value given in Absolute Maximum Conditions.
Note 2: The GreenPAK's power rails are divided in two sides. IOs 0, 1, 2, 3, 4, 5, 6, 7 and 8 are connected to one side, IOs 9, 10, 11, 12, 13, 14, 15, 16 and 17 to another.

5.3 Electrical Characteristics (3.3 V ±10% V_{DD})

Symbol	Parameter	Condition/Note	Min.	Typ.	Max.	Unit
V_{DD}	Supply Voltage		3.0	3.3	3.6	V
T_A	Operating Temperature		-40	25	85	°C
V_{PP}	Programming Voltage		7.25	7.50	7.75	V
V_{ACMP}	ACMP Input Voltage Range	Positive Input	0	--	V_{DD}	V
		Negative Input	0	--	1.2	V
V_{IH}	HIGH-Level Input Voltage	Logic Input	1.81	--	V_{DD}	V
		Logic Input with Schmitt Trigger	2.14	--	V_{DD}	V
		Low-Level Logic Input	1.06	--	V_{DD}	V
V_{IL}	LOW-Level Input Voltage	Logic Input	0	--	1.31	V
		Logic Input with Schmitt Trigger	0	--	0.97	V
		Low-Level Logic Input	0	--	0.67	V
V_{HYS}	Schmitt Trigger Hysteresis Voltage	Logic Input with Schmitt Trigger	0.29	0.62	0.94	V
I_{LGK}	Input leakage (Absolute Value)		--	1	1000	nA
V_{OH}	HIGH-Level Output Voltage	Push-Pull, I_{OH} = 3 mA, 1X Drive	2.70	3.12	--	V
		PMOS OD, I_{OH} = 3 mA, 1X Drive	2.70	3.12	--	V
		Push-Pull, I_{OH} = 3 mA, 2X Drive	2.85	3.21	--	V
		PMOS OD, I_{OH} = 3 mA, 2X Drive	2.86	3.21	--	V
V_{OL}	LOW-Level Output Voltage	Push-Pull, I_{OL}= 3 mA, 1X Drive	--	0.13	0.23	V
		Push-Pull, I_{OL} = 3 mA, 2X Drive	--	0.06	0.11	V
		Open Drain, I_{OL} = 3 mA, 1X Drive	--	0.08	0.15	V
		Open Drain, I_{OL} = 3 mA, 2X Drive	--	0.04	0.08	V
		Open Drain NMOS 4X, I_{OL} = 3 mA	--	0.02	0.04	V
I_{OH}	HIGH-Level Output Pulse Current (see Note 1)	Push-Pull, V_{OH} = 2.4 V, 1X Drive	6.05	12.08	--	mA
		PMOS OD, V_{OH} = 2.4 V, 1X Drive	6.05	12.08	--	mA
		Push-Pull, V_{OH} = 2.4 V, 2X Drive	11.54	24.16	--	mA
		PMOS OD, V_{OH} = 2.4 V, 2X Drive	11.52	24.16	--	mA
I_{OL}	LOW-Level Output Pulse Current (see Note 1)	Push-Pull, V_{OL} = 0.4 V, 1X Drive	4.88	8.24	--	mA
		Push-Pull, V_{OL} = 0.4 V, 2X Drive	9.75	16.49	--	mA
		Open Drain, V_{OL} = 0.4 V, 1X Drive	7.31	12.37	--	mA
		Open Drain, V_{OL} = 0.4 V, 2X Drive	14.54	24.74	--	mA
		Open Drain NMOS 4X, V_{OL} = 0.4 V	31.32	41.06	--	mA
I_{VDD}	Maximum Average or DC Current Through VDD Pin (Per chip side, see Note 2)	T_J = 85°C	--	--	45	mA
		T_J = 110°C	--	--	22	mA
I_{GND}	Maximum Average or DC Current Through GND Pin (Per chip side, see Note 2)	T_J = 85°C	--	--	86	mA
		T_J = 110°C	--	--	41	mA

Symbol	Parameter	Condition/Note	Min.	Typ.	Max.	Unit
V_O	Maximal Voltage Applied to any PIN in High-Impedance State		--	--	V_{DD}	V
T_{SU}	Startup Time	From VDD rising past PON_{THR}	0.61	1.24	1.65	ms
PON_{THR}	Power On Threshold	V_{DD} Level Required to Start Up the Chip	1.41	1.54	1.66	V
$POFF_{THR}$	Power Off Threshold	V_{DD} Level Required to Switch Off the Chip	1.00	1.15	1.31	V
R_{PUP}	Pull Up Resistance	1 M Pull Up	873.2	1094.7	1364.3	kΩ
		100 k Pull Up	85.17	109.30	135.52	kΩ
		10 k Pull Up	9.61	11.86	14.73	kΩ
R_{PDWN}	Pull Down Resistance	1 M Pull Down	862.5	1096.3	1357.4	kΩ
		100 k Pull Down	87.95	109.76	136.06	kΩ
		10 k Pull Down	8.66	11.81	15.05	kΩ

Note 1: DC or average current through any pin should not exceed value given in Absolute Maximum Conditions.
Note 2: The GreenPAK's power rails are divided in two sides. IOs 0, 1, 2, 3, 4, 5, 6, 7 and 8 are connected to one side, IOs 9, 10, 11, 12, 13, 14, 15, 16 and 17 to another.

5.4 Electrical Characteristics (5 V ±10% V_{DD})

Symbol	Parameter	Condition/Note	Min.	Typ.	Max.	Unit
V_{DD}	Supply Voltage		4.5	5.0	5.5	V
T_A	Operating Temperature		-40	25	85	°C
V_{PP}	Programming Voltage		7.25	7.50	7.75	V
V_{ACMP}	ACMP Input Voltage Range	Positive Input	0	--	V_{DD}	V
		Negative Input	0	--	1.2	V
V_{IH}	HIGH-Level Input Voltage	Logic Input	2.68	--	V_{DD}	V
		Logic Input with Schmitt Trigger	3.34	--	V_{DD}	V
		Low-Level Logic Input	1.15	--	V_{DD}	V
V_{IL}	LOW-Level Input Voltage	Logic Input	0	--	1.96	V
		Logic Input with Schmitt Trigger	0	--	1.41	V
		Low-Level Logic Input	0	--	0.77	V
V_{HYS}	Schmitt Trigger Hysteresis Voltage	Logic Input with Schmitt Trigger	0.44	0.90	1.38	V
I_{LGK}	Input leakage (Absolute Value)		--	1	1000	nA
V_{OH}	HIGH-Level Output Voltage	Push-Pull, I_{OH} = 5 mA, 1X Drive	4.15	4.76	--	V
		PMOS OD, I_{OH} = 5 mA, 1X Drive	4.16	4.76	--	V
		Push-Pull, I_{OH} = 5 mA, 2X Drive	4.32	4.89	--	V
		PMOS OD, I_{OH} = 5 mA, 2X Drive	4.33	4.89	--	V
V_{OL}	LOW-Level Output Voltage	Push-Pull, I_{OL}= 5 mA, 1X Drive	--	0.19	0.24	V
		Push-Pull, I_{OL} =5 mA, 2X Drive	--	0.09	0.12	V
		Open Drain, I_{OL} = 5 mA, 1X Drive	--	0.12	0.16	V
		Open Drain, I_{OL} = 5 mA, 2X Drive	--	0.07	0.08	V
		Open Drain NMOS 4X, I_{OL} = 5 mA	--	0.03	0.05	V
I_{OH}	HIGH-Level Output Pulse Current (see Note 1)	Push-Pull, V_{OH} = 2.4 V, 1X Drive	22.08	34.04	--	mA
		PMOS OD, V_{OH} = 2.4 V, 1X Drive	22.08	34.04	--	mA
		Push-Pull, V_{OH} = 2.4 V, 2X Drive	41.76	68.08	--	mA
		PMOS OD, V_{OH} = 2.4 V, 2X Drive	41.69	68.08	--	mA
I_{OL}	LOW-Level Output Pulse Current (see Note 1)	Push-Pull, V_{OL} = 0.4 V, 1X Drive	7.22	11.58	--	mA
		Push-Pull, V_{OL} = 0.4 V, 2X Drive	13.83	23.16	--	mA
		Open Drain, V_{OL} = 0.4 V, 1X Drive	10.82	17.38	--	mA
		Open Drain, V_{OL} = 0.4 V, 2X Drive	17.34	34.76	--	mA
		Open Drain NMOS 4X, V_{OL} = 0.4 V	41.06	55.18	--	mA
I_{VDD}	Maximum Average or DC Current Through VDD Pin (Per chip side, see Note 2)	T_J = 85°C	--	--	45	mA
		T_J = 110°C	--	--	22	mA
I_{GND}	Maximum Average or DC Current Through GND Pin (Per chip side, see Note 2)	T_J = 85°C	--	--	86	mA
		T_J = 110°C	--	--	41	mA

Symbol	Parameter	Condition/Note	Min.	Typ.	Max.	Unit
V_O	Maximal Voltage Applied to any PIN in High-Impedance State		--	--	V_{DD}	V
T_{SU}	Startup Time	From VDD rising past PON_{THR}	0.60	1.23	1.61	ms
PON_{THR}	Power On Threshold	V_{DD} Level Required to Start Up the Chip	1.41	1.54	1.66	V
$POFF_{THR}$	Power Off Threshold	V_{DD} Level Required to Switch Off the Chip	1.00	1.15	1.31	V
R_{PUP}	Pull Up Resistance	1 M Pull Up	864.6	1093.4	1348.1	kΩ
		100 k Pull Up	84.32	108.97	135.24	kΩ
		10 k Pull Up	8.74	11.37	14.52	kΩ
R_{PDWN}	Pull Down Resistance	1 M Pull Down	873.3	1096.1	1370.5	kΩ
		100 k Pull Down	87.57	109.48	135.89	kΩ
		10 k Pull Down	7.95	11.33	14.78	kΩ

Note 1: DC or average current through any pin should not exceed value given in Absolute Maximum Conditions.
Note 2: The GreenPAK's power rails are divided in two sides. IOs 0, 1, 2, 3, 4, 5, 6, 7 and 8 are connected to one side, IOs 9, 10, 11, 12, 13, 14, 15, 16 and 17 to another.

5.5 I^2C Specifications

Symbol	Parameter	Condition/Note	Min.	Typ.	Max.	Unit
F_{SCL}	Clock Frequency, SCL	V_{DD} = (1.71...5.5) V	--	--	400	kHz
t_{LOW}	Clock Pulse Width Low	V_{DD} = (1.71...5.5) V	1300	--	--	ns
t_{HIGH}	Clock Pulse Width High	V_{DD} = (1.71...5.5) V	600	--	--	ns
t_I	Input Filter Spike Suppression (SCL, SDA)	V_{DD} = 1.8 V ± 5 %	--	--	95	ns
		V_{DD} = 3.3 V ± 10%	--	--	95	
		V_{DD} = 5.0 V ± 10 %	--	--	111	
t_{AA}	Clock Low to Data Out Valid	V_{DD} = (1.71...5.5) V	--	--	900	ns
t_{BUF}	Bus Free Time between Stop and Start	V_{DD} = (1.71...5.5) V	1300	--	--	ns
t_{HD_STA}	Start Hold Time	V_{DD} = (1.71...5.5) V	600	--	--	ns
t_{SU_STA}	Start Set-up Time	V_{DD} = (1.71...5.5) V	600	--	--	ns
t_{HD_DAT}	Data Hold Time	V_{DD} = (1.71...5.5) V	0	--	--	ns
t_{SU_DAT}	Data Set-up Time	V_{DD} = (1.71...5.5) V	100	--	--	ns
t_R	Inputs Rise Time	V_{DD} = (1.71...5.5) V	--	--	300	ns
t_F	Inputs Fall Time	V_{DD} = (1.71...5.5) V	--	--	300	ns
t_{SU_STO}	Stop Set-up Time	V_{DD} = (1.71...5.5) V	600	--	--	ns
t_{DH}	Data Out Hold Time	V_{DD} = (1.71...5.5) V	50	--	--	ns

5.6 Asynchronous State Machine (ASM) Specifications

Table 1. ASM Specifications

Symbol	Parameter	Condition	Min	Typ	Max	Unit
tst_out_delay	Asynchronous State Machine Output Delay Time	V_{DD} = 1.8 V ± 5 %	104	--	213	ns
		V_{DD} = 3.3 V ± 10 %	44	--	89	
		V_{DD} = 5.0 V ± 10 %	32	--	58	
tst_out	Asynchronous State Machine Output Transition Time	V_{DD} = 1.8 V ± 5 %	--	--	165	ns
		V_{DD} = 3.3 V ± 10 %	--	--	70	
		V_{DD} = 5.0 V ± 10 %	--	--	45	
tst_pulse	Asynchronous State Machine Input Pulse Acceptance Time	V_{DD} = 1.8 V ± 5 %	14	--	--	ns
		V_{DD} = 3.3 V ± 10 %	6	--	--	
		V_{DD} = 5.0 V ± 10 %	5	--	--	
tst_comp	Asynchronous State Machine Input Compete Time	V_{DD} = 1.8 V ± 5 %	--	--	20	ns
		V_{DD} = 3.3 V ± 10 %	--	--	8	
		V_{DD} = 5.0 V ± 10 %	--	--	5	

5.7 IDD Estimator

Table 2. Typical Current Estimated for Each Macrocell at T=25°C

Symbol	Parameter	Note	V_{DD} = 1.8 V	V_{DD} = 3.3V	V_{DD} = 5.0V	Unit
I	Current	Chip Quiescent	0.45	0.75	1.12	µA
		OSC 2 MHz, predivide = 1	41.48	64.00	94.89	µA
		OSC 2 MHz, predivide = 8	25.68	32.41	43.22	µA
		OSC 25 kHz, predivide = 1	7.16	7.94	9.25	µA
		OSC 25 kHz, predivide = 8	6.97	7.60	8.68	µA
		OSC 25 MHz, predivide = 1	87.25	238.27	428.66	µA
		OSC 25 MHz, predivide = 1, Force On	87.25	238.27	428.67	µA
		OSC 25 MHz, predivide = 8	78.01	212.45	390.17	µA
		ACMP (each)	54.96	52.64	60.81	µA
		ACMP with buffer (each)	75.06	72.74	81.25	µA
		Vref (each)	49.70	47.32	55.60	µA
		Vref with buffer (each)	71.93	71.27	79.62	µA

5.8 Timing Estimator

Table 3. Typical Delay Estimated for Each Macrocell at T=25°C

Symbol	Parameter	Note	V_{DD} = 1.8 V		V_{DD} = 3.3V		V_{DD} = 5.0V		Unit
			rising	falling	rising	falling	rising	falling	
tpd	Delay	Digital Input to PP 1X	45	50	19	21	14	15	ns
tpd	Delay	Digital Input with Schmitt Trigger to PP 1X	44	49	19	21	14	15	ns
tpd	Delay	Low Voltage Digital input to PP 1X	46	447	19	195	14	134	ns
tpd	Delay	Digital input to PMOS output	44	-	19	-	14	-	ns
tpd	Delay	Digital input to NMOS output	-	81	-	30	-	20	ns
tpd	Delay	Output enable from pin, OE Hi-Z to 1	48	-	20	-	15	-	ns
tpd	Delay	Output enable from pin, OE Hi-Z to 0	-	46	-	20	-	14	ns
tpd	Delay	LUT2bit(LATCH)	34	33	14	13	10	9	ns
tpd	Delay	LATCH(LUT2bit)	30	34	14	13	10	9	ns
tpd	Delay	LUT3bit(LATCH)	38	37	18	15	13	10	ns
tpd	Delay	LATCH+nRESET(LUT3bit)	45	42	21	17	15	12	ns
tpd	Delay	LATCH	33	35	14	14	11	10	ns
tpd	Delay	LUT4bit	28	33	14	13	10	9	ns
tpd	Delay	LUT2bit	31	31	14	13	10	9	ns
tpd	Delay	LUT3bit	35	33	15	13	11	10	ns
tpd	Delay	CNT/DLY Logic	62	68	27	29	19	20	ns
tpd	Delay	DFF	32	28	14	12	11	9	ns
tpd	Delay	P_DLY1C	367	356	165	160	123	119	ns
tpd	Delay	P_DLY2C	667	656	303	297	225	221	ns
tpd	Delay	P_DLY3C	968	956	440	434	327	322	ns
tpd	Delay	P_DLY4C	1265	1252	576	570	428	423	ns
tpd	Delay	Filter	213	210	84	83	55	55	ns
tpd	Delay	ACMP (5 mV overdrive, IN- = 600 mV)	1600	1900	1500	1800	1600	1800	ns
tw	Pulse Width	I/O with 1X push pull (min transmitted)	20	20	20	20	20	20	ns
tw	Pulse Width	filter (min transmitted)	150	150	55	55	35	35	ns

5.9 Typical Counter/Delay Offset Measurements

Table 4. Typical Counter/Delay Offset Measurements

Parameter	RC OSC Freq	RC OSC Power	V_{DD} = 1.8 V	V_{DD} = 3.3V	V_{DD} = 5.0V	Unit
Offset (Power On Delay)	25 kHz	auto	1.6	1.6	1.6	µs
Offset (Power On Delay), fast start	25 kHz	auto	2.1	2.1	2.1	µs
Offset (Power On Delay)	2 MHz	auto	0.4	0.2	0.2	µs
Offset (Power On Delay), fast start	2 MHz	auto	0.7	0.5	0.4	µs
Offset (Power On Delay)	25 MHz	auto	0.01	0.05	0.04	µs
Frequency settling time	25 kHz	auto	19	14	12	µs
Frequency settling time	2 MHz	auto	14	14	14	µs
Variable (CLK period)	25 kHz	forced	0-40	0-40	0-40	µs

Table 4. Typical Counter/Delay Offset Measurements

Parameter	RC OSC Freq	RC OSC Power	V_{DD} = 1.8 V	V_{DD} = 3.3V	V_{DD} = 5.0V	Unit
Variable (CLK period)	2 MHz	forced	0-0.5	0-0.5	0-0.5	µs
Variable (CLK period)	25 MHz		0-0.04	0-0.04	0-0.04	µs
Tpd (non-delayed edge)	25 kHz/ 2 MHz	either	35	14	10	ns

5.10 Expected Delays and Widths

Table 5. Expected Delays and Widths (typical)

Symbol	Parameter	Note	V_{DD} = 1.8 V	V_{DD} = 3.3V	V_{DD} = 5.0V	Unit
tw	Pulse Width, 1 cell	mode:(any)edge detect, edge detect output	296	135	101	ns
tw	Pulse Width, 2 cell	mode:(any)edge detect, edge detect output	597	272	203	ns
tw	Pulse Width, 3 cell	mode:(any)edge detect, edge detect output	898	410	305	ns
tw	Pulse Width, 4 cell	mode:(any)edge detect, edge detect output	1195	546	407	ns
time1	Delay, 1 cell	mode:(any)edge detect, edge detect output	55	24	18	ns
time1	Delay, 2 cell	mode:(any)edge detect, edge detect output	55	24	18	ns
time1	Delay, 3 cell	mode:(any)edge detect, edge detect output	55	24	18	ns
time1	Delay, 4 cell	mode:(any)edge detect, edge detect output	55	24	18	ns
time2	Delay, 1 cell	mode: both edge delay, edge detect output	367	165	106	ns
time2	Delay, 2 cell	mode: both edge delay, edge detect output	667	300	193	ns
time2	Delay, 3 cell	mode: both edge delay, edge detect output	968	440	279	ns
time2	Delay, 4 cell	mode: both edge delay, edge detect output	1265	575	365	ns

5.11 Typical Pulse Width Performance

Table 6. Typical Pulse Width Performance at T = 25°C

Parameter	V_{DD} = 1.8 V	V_{DD} = 3.3V	V_{DD} = 5.0V	Unit
Filtered Pulse Width for Filter 0	< 114	< 47	< 30	ns
Filtered Pulse Width for Filter 1	<75	<30	<19	ns

5.12 OSC Specifications

Table 7. 25 kHz RC OSC0 frequency limits

Power Supply Range (VDD) V	Temperature Range					
	+25 °C		0 °C ... +85 °C		-40 °C ... +85 °C	
	Minimum Value, kHz	Maximum Value, kHz	Minimum Value, kHz	Maximum Value, kHz	Minimum Value, kHz	Maximum Value, kHz
1.8 V ±5%	23.792	26.288	23.275	27.089	21.728	29.173
3.3 V ±10%	24.473	25.526	23.357	26.028	23.357	27.002
5 V ±10%	24.316	25.939	23.309	26.177	23.309	27.181
2.5 V ... 4.5 V	24.438	25.559	23.336	26.051	23.336	27.038
1.71 V… 5.5 V	23.354	26.670	22.828	27.483	21.301	29.545

Table 8. 25 kHz RC OSC0 frequency error (error calculated relative to nominal value)

Power Supply Range (VDD) V	Temperature Range					
	+25 °C		0 °C ... +85 °C		-40 °C ... +85 °C	
	Error (% at Minimum)	Error (% at Maximum)	Error (% at Minimum)	Error (% at Maximum)	Error (% at Minimum)	Error (% at Maximum)
1.8 V ±5%	-4.83%	5.15%	-6.90%	8.36%	-13.09%	16.69%
3.3 V ±10%	-2.11%	2.10%	-6.57%	4.11%	-6.57%	8.01%
5 V ±10%	-2.73%	3.76%	-6.76%	4.71%	-6.76%	8.72%
2.5 V ... 4.5 V	-2.25%	2.24%	-6.66%	4.21%	-6.66%	8.15%
1.71 V… 5.5 V	-6.58%	6.68%	-8.69%	9.93%	-14.80%	18.18%

5.12.1 2 MHz RC Oscillator

Table 9. 2 MHz RC OSC0 frequency limits

Power Supply Range (VDD) V	Temperature Range					
	+25 °C		0 °C ... +85 °C		-40 °C ... +85 °C	
	Minimum Value, MHz	Maximum Value, MHz	Minimum Value, MHz	Maximum Value, MHz	Minimum Value, MHz	Maximum Value, MHz
1.8 V ±5%	1.915	2.062	1.832	2.103	1.810	2.144
3.3 V ±10%	1.937	2.070	1.858	2.132	1.813	2.145
5 V ±10%	1.894	2.233	1.853	2.270	1.767	2.270
2.5 V ... 4.5 V	1.907	2.124	1.836	2.171	1.784	2.171
1.71 V… 5.5 V	1.760	2.274	1.706	2.305	1.629	2.305

Table 10. 2 MHz RC OSC0 frequency error (error calculated relative to nominal value)

Power Supply Range (VDD) V	Temperature Range					
	+25 °C		0 °C ... +85 °C		-40 °C ... +85 °C	
	Error (% at Minimum)	Error (% at Maximum)	Error (% at Minimum)	Error (% at Maximum)	Error (% at Minimum)	Error (% at Maximum)
1.8 V ±5%	-4.26%	3.12%	-8.38%	5.17%	-9.50%	7.20%
3.3 V ±10%	-3.14%	3.49%	-7.10%	6.58%	-9.33%	7.24%
5 V ±10%	-5.31%	11.66%	-7.37%	13.50%	-11.67%	13.50%
2.5 V ... 4.5 V	-4.65%	6.18%	-8.22%	8.57%	-10.81%	8.57%
1.71 V… 5.5 V	-12.01%	13.72%	-14.69%	15.23%	-18.57%	15.23%

5.12.2 25 MHz RC Oscillator

Table 11. 25 MHz RC OSC1 frequency limits

Power Supply Range (VDD) V	Temperature Range					
	+25 °C		0 °C ... +85 °C		-40 °C ... +85 °C	
	Minimum Value, MHz	Maximum Value, MHz	Minimum Value, MHz	Maximum Value, MHz	Minimum Value, MHz	Maximum Value, MHz
2.5 V ±10%	22.316	27.220	21.771	27.572	21.771	27.912
3.3 V ±10%	23.430	26.220	22.389	26.679	22.389	27.014
5 V ±10%	23.289	26.651	22.500	27.305	22.500	27.486
2.5 V ... 4.5 V	23.383	26.220	20.725	26.679	20.725	27.014
1.71 V… 5.5 V	12.643	26.220	12.203	26.679	11.317	27.014

Table 12. 25 MHz RC OSC1 frequency error (error calculated relative to nominal value)

Power Supply Range (VDD) V	Temperature Range					
	+25 °C		0 °C ... +85 °C		-40 °C ... +85 °C	
	Error (% at Minimum)	Error (% at Maximum)	Error (% at Minimum)	Error (% at Maximum)	Error (% at Minimum)	Error (% at Maximum)
2.5 V ±10%	-10.73%	8.88%	-12.92%	10.29%	-12.92%	11.65%
3.3 V ±10%	-6.28%	4.88%	-10.44%	6.72%	-10.44%	8.06%
5 V ±10%	-6.84%	6.61%	-10.00%	9.22%	-10.00%	9.95%
2.5 V ... 4.5 V	-14.47%	4.88%	-17.10%	6.72%	-17.10%	8.06%
1.71 V… 5.5 V	-49.43%	4.88%	-51.19%	6.72%	-54.73%	8.06%

Note: 25 MHz RC OSC1 performance is not guaranteed at VDD < 2.5 V.

5.12.3 OSC Power On delay

Table 13. Oscillators Power On delay at room temperature, DLY/CNT Counter data = 100; RC OSC power setting: "Auto Power On", RC osc clock to matrix input: "Enable"

Power Supply Range (VDD) V	RC OSC0 2 MHz		RC OSC0 25 kHz		RC OSC1	
	Typical Value, ns	Maximum Value, ns	Typical Value, µs	Maximum Value, µs	Typical Value, ns	Maximum Value, ns
1.71	372.7	407.3	0.40	0.57	71.2	87.3
1.80	349.2	379.5	0.38	0.41	65.0	78.7
1.89	330.3	358.0	0.35	0.41	59.7	71.3
2.30	277.2	298.1	0.29	0.31	43.0	54.0
2.50	262.0	281.9	0.28	0.30	39.6	48.1
2.70	250.2	269.8	0.26	0.30	36.7	43.5
3.00	236.6	256.7	0.25	0.44	33.2	39.8
3.30	226.7	247.4	0.23	0.47	30.4	36.8
3.60	219.0	239.9	0.22	0.46	28.2	34.3
4.20	207.4	229.2	0.37	0.50	25.8	30.6
4.50	202.8	224.5	1.63	1.92	25.0	29.2
5.00	196.3	218.7	1.67	2.05	24.3	27.5
5.50	190.8	213.3	1.69	1.99	23.7	26.8

Table 14. Oscillators Power On delay at room temperature, DLY/CNT Counter data = 100; RC OSC power setting: "Auto Power On", RC osc clock to matrix input: "Enable", Fast Start-up Time Mode

Power Supply Range (VDD) V	RC OSC0 2 MHz		RC OSC1 25 kHz	
	Typical Value, ns	Maximum Value, ns	Typical Value, µs	Maximum Value, µs
1.71	327.9	360.0	0.68	0.76
1.80	309.9	338.3	0.64	0.64
1.89	295.5	323.1	0.61	0.70
2.30	254.9	278.1	0.53	21.93
2.50	243.1	266.1	3.23	21.88
2.70	234.1	257.1	16.68	21.94
3.00	223.7	246.8	19.25	21.90
3.30	215.7	239.1	19.22	21.77
3.60	209.4	232.9	19.21	21.74
4.20	199.5	223.4	19.17	21.78
4.50	195.5	219.8	19.15	21.69
5.00	189.8	214.6	19.12	21.71
5.50	184.9	209.8	19.05	21.75

5.13 ACMP Specifications

Table 15. ACMP Specifications

Symbol	Parameter	Description/Note	Conditions	Min.	Typ.	Max.	Unit
V_{ACMP}	ACMP Input Voltage Range	Positive Input	VDD = 1.8 V ± 5 %	0	--	V_{DD}	V
		Negative Input		0	--	1.2	V
		Positive Input	VDD = 3.3 V ± 10 %	0	--	V_{DD}	V
		Negative Input		0	--	1.2	V
		Positive Input	VDD = 5.0 V ± 10 %	0	--	V_{DD}	V
		Negative Input		0	--	1.2	V
V_{offset}	ACMP Input Offset Voltage	Low Bandwidth - Enable, Vhys = 0 mV, Gain = 1, Vref = (50..1200) mV, VDD = (1.71..5.5) V	T = 25°C	-9.1	--	8.4	mV
			T = (-40..85)°C	-10.9	--	10.9	mV
		Low Bandwidth - Disable, Vhys = 0 mV, Gain =1, Vref = (50..1200) mV, VDD = (1.71..5.5) V	T = 25°C	-7.5	--	7.2	mV
			T = (-40..85)°C	-10.7	--	10.5	mV
t_{start}	ACMP Start Time	ACMP Power On delay, Minimal required wake time for the "Wake and Sleep function", Regulator and Charge Pump set to automatic ON/OFF	BG = 550 µs, T = 25°C VDD = (1.71..5.5) V	--	609.7	862.2	µS
			BG = 550 µs, T = (-40..85)°C VDD = (1.71..5.5) V	--	675.0	1028.8	µS
			BG = 100 µs, T = 25°C VDD = 2.7..5.5 V	--	132.4	176.2	µS
			BG = 100 µs, T = (-40..85)°C VDD = 2.7..5.5 V	--	149.4	213.5	µS
		ACMP Power On delay, Minimal required wake time for the "Wake and Sleep function", Regulator and Charge Pump always OFF	BG = 550 µs, T = 25°C VDD = (3..5.5) V	--	609.5	862.0	µS
			BG = 550 µs, T = (-40..85)°C VDD = (3..5.5) V	--	674.6	1027.5	µS
			BG = 100 µs, T = 25°C VDD = 3..5.5 V	--	131.6	176.0	µS
			BG = 100 µs, T = (-40..85)°C VDD = 3..5.5 V	--	149.2	213.3	µS

Symbol	Parameter	Description/Note	Conditions	Min.	Typ.	Max.	Unit
V_{HYS}	Built-in Hysteresis	V_{HYS} = 25 mV V_{IL} = Vin - V_{HYS}/2 V_{IH} = Vin + V_{HYS}/2	LB - Enabled, T = 25°C	7.32	--	35.5	mV
			LB - Disabled, T = 25°C	10.0	--	38.5	mV
		V_{HYS} = 50 mV V_{IL} = Vin - V_{HYS} V_{IH} = V_{HYS}	LB - Enabled, T = 25°C	42.9	--	57.8	mV
			LB - Disabled, T = 25°C	44.2	--	54.3	mV
		V_{HYS} = 200 mV V_{IL} = Vin - V_{HYS} V_{IH} = V_{HYS}	LB - Enabled, T = 25°C	192.7	--	208.7	mV
			LB - Disabled, T = 25°C	193.3	--	204.8	mV
		V_{HYS} = 25 mV V_{IL} = Vin - V_{HYS}/2 V_{IH} = Vin + V_{HYS}/2	LB - Enabled, T = (-40…+85)°C	0.0	--	58.0	mV
			LB - Disabled, T = (-40…+85)°C	0.0	--	52.9	mV
		V_{HYS} = 50 mV V_{IL} = Vin - V_{HYS} V_{IH} = V_{HYS}	LB - Enabled, T = (-40…+85)°C	22.5	--	86.9	mV
			LB - Disabled, T = (-40…+85)°C	29.2	--	76.5	mV
		V_{HYS} = 200 mV V_{IL} = Vin - V_{HYS} V_{IH} = V_{HYS}	LB - Enabled, T = (-40…+85)°C	157.1	--	251.6	mV
			LB - Disabled, T = (-40…+85)°C	160.2	--	245.3	mV
R_{sin}	Series Input Resistance	Gain = 1x		--	100.0	--	MΩ
		Gain = 0.5x		--	1.0	--	MΩ
		Gain = 0.33x		--	0.8	--	MΩ
		Gain = 0.25x		--	1.0	--	MΩ
PROP	Propagation Delay, Response Time	Low Bandwidth - Enable, Gain = 1, VDD=(1.71..3.3)V, Overdrive=5 mV	Low to High, T = (-40…+85)°C	--	103.93	1853.68	µS
			High to Low, T = (-40…+85)°C	--	101.06	1656.70	µS
		Low Bandwidth - Disable, Gain = 1, VDD=(1.71..3.3)V, Overdrive=5 mV	Low to High, T = (-40…+85)°C	--	68.29	1753.33	µS
			High to Low, T = (-40…+85)°C	--	63.06	1568.55	µS
		Low Bandwidth - Enable, Gain = 1, VDD=(3.3..5.5)V, Overdrive=5 mV	Low to High, T = (-40…+85)°C	--	30.62	167.56	µS
			High to Low, T = (-40…+85)°C	--	33.54	181.40	µS
		Low Bandwidth - Disable, Gain = 1, VDD=(3.3..5.5)V, Overdrive=5 mV	Low to High, T = (-40…+85)°C	--	5.00	32.61	µS
			High to Low, T = (-40…+85)°C	--	5.24	33.88	µS

Symbol	Parameter	Description/Note	Conditions	Min.	Typ.	Max.	Unit
G	Gain error (including threshold and internal Vref error), T = (-40…+85)°C	G = 1, VDD = 1.71 V	Vref = 50…1200 mV	--	1	--	
		G = 1, VDD = 3.3 V		--	1	--	
		G = 1, VDD = 5.5 V		--	1	--	
		G = 0.5, VDD = 1.71 V		-1.00%	--	0.93%	
		G = 0.5, VDD = 3.3 V		-0.96%	--	0.82%	
		G = 0.5, VDD = 5.5 V		-1.04%	--	0.90%	
		G = 0.33, VDD = 1.71V		-1.75%	--	2.10%	
		G = 0.33, VDD = 3.3 V		-1.95%	--	1.69%	
		G = 0.33, VDD = 5.5 V		-2.03%	--	1.77%	
		G = 0.25, VDD = 1.71V		-1.91%	--	2.13%	
		G = 0.25, VDD = 3.3 V		-1.98%	--	1.80%	
		G = 0.25, VDD = 5.5 V		-2.12%	--	1.90%	
Vref	Internal Vref error, Vref = 1200 mV	VDD = 1.8 V ± 5 %	T = 25°C	-0.58%	--	0.56%	
			T = (-40…+85)°C	-1.01%	--	0.70%	
		VDD = 3.3 V ± 10 %	T = 25°C	-0.59%	--	0.58%	
			T = (-40…+85)°C	-1.06%	--	0.72%	
		VDD = 5.0 V ± 10 %	T = 25°C	-0.64%	--	0.60%	
			T = (-40…+85)°C	-1.16%	--	0.74%	
	Internal Vref error, Vref = 1000 mV	VDD = 1.8 V ± 5 %	T = 25°C	-0.57%	--	0.58%	
			T = (-40…+85)°C	-1.14%	--	0.76%	
		VDD = 3.3 V ± 10 %	T = 25°C	-0.59%	--	0.58%	
			T = (-40…+85)°C	-1.04%	--	0.73%	
		VDD = 5.0 V ± 10 %	T = 25°C	-0.67%	--	0.64%	
			T = (-40…+85)°C	-1.15%	--	0.73%	
	Internal Vref error, Vref = 500 mV	VDD = 1.8 V ± 5 %	T = 25°C	-0.64%	--	0.64%	
			T = (-40…+85)°C	-1.11%	--	0.75%	
		VDD = 3.3 V ± 10 %	T = 25°C	-0.63%	--	0.63%	
			T = (-40…+85)°C	-1.10%	--	0.78%	
		VDD = 5.0 V ± 10 %	T = 25°C	-0.72%	--	0.70%	
			T = (-40…+85)°C	-1.15%	--	0.80%	