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SLG46538

GreenPAK
Programmable Mixed-signal Matrix
with Asynchronous State Machine and Dual Supply

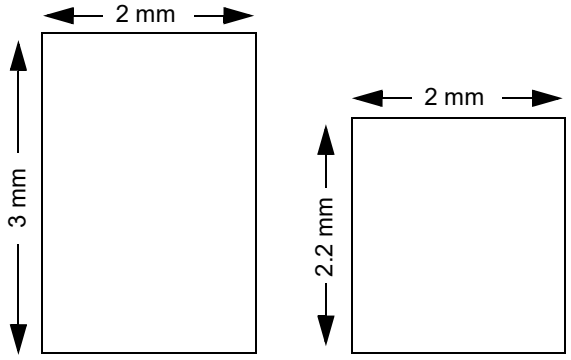
Features

- Logic & Mixed Signal Circuits
- Highly Versatile Macrocells
- Read Back Protection (Read Lock)
- 1.8 V (±5%) to 5 V (±10%) VDD
- 1.8 V (±5%) to 5 V (±10%) VDD2 (VDD2 ≤ VDD)
- Operating Temperature Range: -40°C to 85°C
- RoHS Compliant / Halogen-Free
- 20-pin STQFN: 2 x 3 x 0.55 mm, 0.4 mm pitch or
  22-pin MSTQFN: 2x 2.2 x 0.55 mm, 0.4 mm pitch

Applications

- Personal Computers and Servers
- PC Peripherals
- Consumer Electronics
- Data Communications Equipment
- Handheld and Portable Electronics

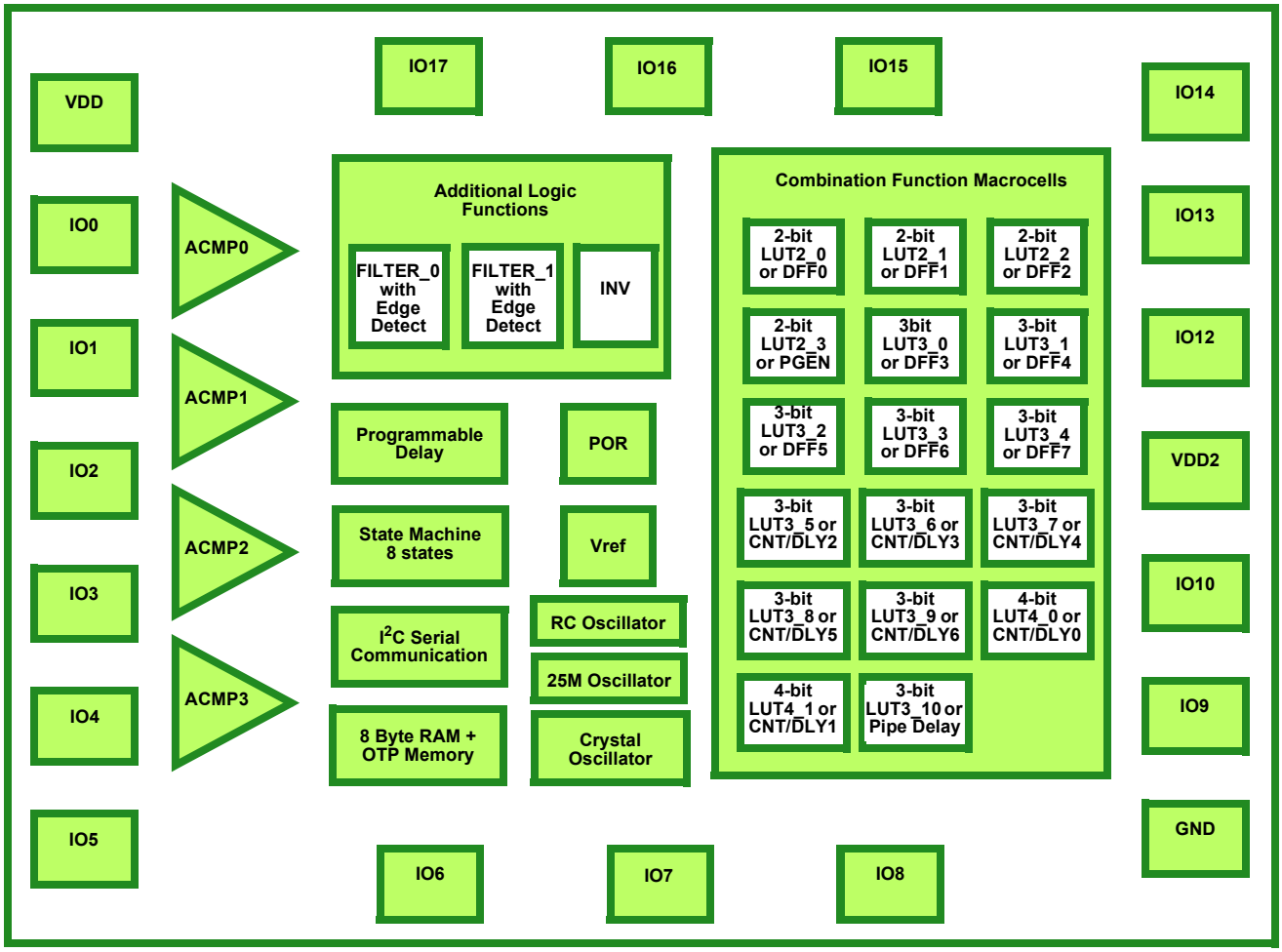
Available Package Options



STQFN-20 (Top View) **MSTQFN-22 (Top View)**

Packages drawn to scale

Block Diagram



1.0 Overview

The SLG46538 provides a small, low power component for commonly used mixed-signal functions. The user creates their circuit design by programming the one time Non-Volatile Memory (NVM) to configure the interconnect logic, the I/O Pins and the macrocells of the SLG46538. This highly versatile device allows a wide variety of mixed-signal functions to be designed within a very small, low power single integrated circuit.

The additional power supply (VDD2) on the SLG46538 provides the ability to interface two independent voltage domains within the same design. Users can configure pins, dedicated to each power supply, as inputs, outputs, or both (controlled dynamically by internal logic) to both VDD and VDD2 voltage domains. Using the available macrocells designers can implement mixed-signal functions bridging both domains or simply pass through level-translation in both High to Low and Low to High directions.

The macrocells in the device include the following:

- Four Analog Comparators (ACMP)
- Two Voltage References (Vref)
- Nineteen Combination Function Macrocells
  - Three Selectable DFF/Latch or 2-bit LUTs
  - One Selectable Continuous DFF/Latch or 3-bit LUT
  - Four Selectable DFF/Latch or 3-bit LUTs
  - One Selectable Pipe Delay or 3-bit LUT
  - One Selectable Programmable Function Generator or 2-bit LUT
  - Five 8-bit delays/counters or 3-bit LUTs
  - Two 16-bit delays/counters or 4-bit LUTs
  - Two Deglitch Filters with Edge Detectors
- State Machine
  - Eight States
  - Flexible input logic from state transitions
- Serial Communications
  - I^2C Protocol compliant
- Pipe Delay – 16 stage/3 output (Part of Combination Function Macrocell)
- Programmable Delay
- Additional Logic Function
  - One Inverter
- Two Oscillators (OSC)
  - Configurable 25 kHz/2 MHz
  - 25MHz RC Oscillator
- Crystal Oscillator
- Power-On-Reset (POR)
- Eight Byte RAM + OTP User Memory
  - RAM Memory space that is readable and writable via I^2C
  - User defined initial values transferred from OTP

2.0 Pin Description

2.1 Functional Pin Description

STQFN 20L Pin #	MSTQFN 22L Pin#	Pin Name	Signal Name	Function	Input Options	Output Options
1	16	VDD	VDD	Power Supply	--	--
2	1	IO0	IO0	General Purpose Input	Digital Input without Schmitt Trigger	--
					Digital Input with Schmitt Trigger	--
					Low Voltage Digital Input	--
3	2	IO1	IO1	General Purpose I/O with OE*	Digital Input without Schmitt Trigger	Push-Pull (1x) (2x)
					Digital Input with Schmitt Trigger	Open Drain NMOS (1x) (2x)
					Low Voltage Digital Input	--
4	3	IO2	IO2	General Purpose I/O	Digital Input without Schmitt Trigger	Push-Pull (1x) (2x)
					Digital Input with Schmitt Trigger	Open Drain NMOS (1x) (2x)
					Low Voltage Digital Input	Open Drain PMOS (1x) (2x)
5	4	IO3	IO3	General Purpose I/O with OE*	Digital Input without Schmitt Trigger	Push-Pull (1x) (2x)
					Digital Input with Schmitt Trigger	Open Drain NMOS (1x) (2x)
					Low Voltage Digital Input	--
6	5	IO4	IO4	General Purpose I/O	Digital Input without Schmitt Trigger	Push-Pull (1x) (2x)
					Digital Input with Schmitt Trigger	Open Drain NMOS (1x) (2x)
					Low Voltage Digital Input	Open Drain PMOS (1x) (2x)
			ACMP0+	Analog Comparator 0 Positive Input	Analog	--
7	6	IO5	IO5	General Purpose I/O with OE*	Digital Input without Schmitt Trigger	Push-Pull (1x) (2x)
					Digital Input with Schmitt Trigger	Open Drain NMOS (1x) (2x)
					Low Voltage Digital Input	--
			ACMP0-	Analog Comparator 0 Negative Input	Analog	--

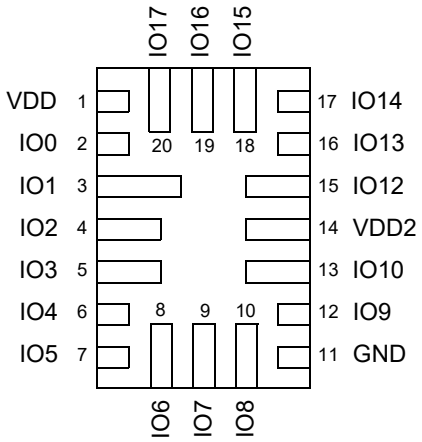
STQFN 20L Pin #	MSTQFN 22L Pin#	Pin Name	Signal Name	Function	Input Options	Output Options
8	19	IO6	IO6	General Purpose I/O	Digital Input without Schmitt Trigger	Open Drain NMOS (1x) (2x)
					Digital Input with Schmitt Trigger	--
					Low Voltage Digital Input	--
			SCL	I2C Serial Clock	Digital Input without Schmitt Trigger	Open Drain NMOS
					Digital Input with Schmitt Trigger	Open Drain NMOS
					Low Voltage Digital Input	Open Drain NMOS
9	7	IO7	IO7	General Purpose I/O	Digital Input without Schmitt Trigger	Open Drain NMOS (1x) (2x)
					Digital Input with Schmitt Trigger	--
					Low Voltage Digital Input	--
			SDA	I2C Serial Data	Digital Input without Schmitt Trigger	Open Drain NMOS
					Digital Input with Schmitt Trigger	Open Drain NMOS
					Low Voltage Digital Input	Open Drain NMOS
10	8	IO8	IO8	General Purpose I/O with OE*	Digital Input without Schmitt Trigger	Push-Pull (1x) (2x)
					Digital Input with Schmitt Trigger	Open Drain NMOS (1x) (2x) (4x)
					Low Voltage Digital Input	Open Drain PMOS (1x) (2x)
			ACMP1+	Analog Comparator 1 Positive Input	Analog	--
11	20	GND	GND	Ground	--	--
12	21	IO9	IO9	General Purpose I/O	Digital Input without Schmitt Trigger	Push-Pull (1x) (2x)
					Digital Input with Schmitt Trigger	Open Drain NMOS (1x) (2x) (4x)
					Low Voltage Digital Input	--
			EXT_VREF	Analog Comparator Negative Input	Analog	--
13	11	IO10	IO10	General Purpose I/O with OE*	Digital Input without Schmitt Trigger	Push-Pull (1x) (2x)
					Digital Input with Schmitt Trigger	Open Drain NMOS (1x) (2x)
					Low Voltage Digital Input	--
			ACMP2+	Analog Comparator 2 Positive Input	Analog	--
			ACMP3+	Analog Comparator 3 Positive Input	Analog	--
14	12	VDD2	VDD2	Power Supply	--	--

STQFN 20L Pin #	MSTQFN 22L Pin#	Pin Name	Signal Name	Function	Input Options	Output Options
15	22	IO12	IO12	General Purpose I/O	Digital Input without Schmitt Trigger	Push-Pull (1x) (2x)
					Digital Input with Schmitt Trigger	Open Drain NMOS (1x) (2x)
					Low Voltage Digital Input	Open Drain PMOS (1x) (2x)
			ACMP3+	Analog Comparator 3 Positive Input	Analog	--
16	13	IO13	IO13	General Purpose I/O with OE*	Digital Input without Schmitt Trigger	Push-Pull (1x) (2x)
					Digital Input with Schmitt Trigger	Open Drain NMOS (1x) (2x)
					Low Voltage Digital Input	--
			XTAL0	External Crystal Connection 0	--	Analog
17	14	IO14	IO14	General Purpose I/O	Digital Input without Schmitt Trigger	Push-Pull (1x) (2x)
					Digital Input with Schmitt Trigger	Open Drain NMOS (1x) (2x)
					Low Voltage Digital Input	Open Drain PMOS (1x) (2x)
			XTAL1	External Crystal Connection 1	Analog	--
			EXT_CLK0	External Clock Connection 0	Digital Input without Schmitt Trigger	--
					Digital Input with Schmitt Trigger	--
					Low Voltage Digital Input	--
18	18	IO15	IO15	General Purpose I/O with OE*	Digital Input without Schmitt Trigger	Push-Pull (1x) (2x)
					Digital Input with Schmitt Trigger	Open Drain NMOS (1x) (2x)
					Low Voltage Digital Input	--
			VREF0	Voltage Reference 0 Output	--	Analog
			EXT_CLK1	External Clock Connection 1	Digital Input without Schmitt Trigger	--
					Digital Input with Schmitt Trigger	--
					Low Voltage Digital Input	--
19	15	IO16	IO16	General Purpose I/O with OE*	Digital Input without Schmitt Trigger	Push-Pull (1x) (2x)
					Digital Input with Schmitt Trigger	Open Drain NMOS (1x) (2x)
					Low Voltage Digital Input	--
			VREF0	Voltage Reference 0 Output	--	Analog

STQFN 20L Pin #	MSTQFN 22L Pin#	Pin Name	Signal Name	Function	Input Options	Output Options
20	17	IO17	IO17	General Purpose I/O	Digital Input without Schmitt Trigger	Push-Pull (1x) (2x)
					Digital Input with Schmitt Trigger	Open Drain NMOS (1x) (2x)
					Low Voltage Digital Input	Open Drain PMOS (1x) (2x)
			EXT_CLK2	External Clock Connection 2	Digital Input without Schmitt Trigger	--
					Digital Input with Schmitt Trigger	--
					Low Voltage Digital Input	--
--	9	NC	NC	No Connection	--	--
--	10	NC	NC	No Connection	--	--

*Note: * General Purpose I/O's with OE can be used to implement bidirectional signals under user control via Connection Matrix to OE signal in I/O structure.*

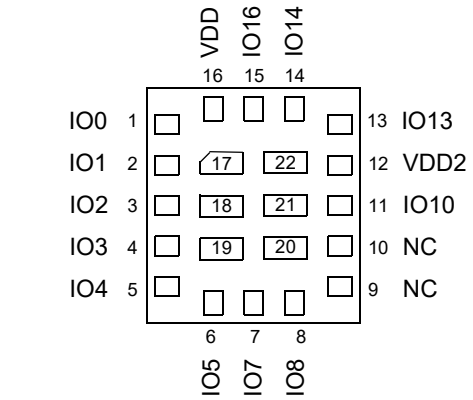
2.2 Pin Configuration - STQFN20L



STQFN-20 (Top View)

Pin #	Signal Name	Pin Functions
1	VDD	
2	IO0	GPI
3	IO1	GPIO with OE
4	IO2	GPIO
5	IO3	GPIO with OE
6	IO4	GPIO / ACMP0+
7	IO5	GPIO with OE / ACMP0-
8	IO6	GPIO / SCL
9	IO7	GPIO / SDA
10	IO8	GPIO with OE/ ACMP1+
11	GND	GND
12	IO9	GPIO / ACMP0- / ACMP1- / ACMP2- / ACMP3-
13	IO10	GPIO with OE / ACMP2+ / ACMP3+
14	VDD2	
15	IO12	GPIO / ACMP3+
16	IO13	GPIO with OE / XTAL0
17	IO14	GPIO / XTAL1 / EXT_CLK0
18	IO15	GPIO with OE / VREF0 / EXT_CLK1
19	IO16	GPIO with OE / VREF0
20	IO17	GPIO / EXT_CLK2

2.3 Pin Configuration - MSTQFN-22L



17 IO17
18 IO15
19 IO6
20 GND
21 IO9
22 IO12

MSTQFN-22L
(Top View)

Pin #	Signal Name	Pin Functions
1	IO0	GPI
2	IO1	GPIO with OE
3	IO2	GPIO
4	IO3	GPIO with OE
5	IO4	GPIO / ACMP0+
6	IO5	GPIO with OE
7	IO7	GPIO / SDA
8	IO8	GPIO with OE/ ACMP1+
9	NC	
10	NC	
11	IO10	GPIO with OE / ACMP2+ / ACMP3+
12	VDD2	
13	IO13	GPIO with OE / XTAL0
14	IO14	GPIO / XTAL1 / EXT_CLK0
15	IO16	GPIO with OE / VREF0
16	VDD	
17	IO17	GPIO / EXT_CLK2
18	IO15	GPIO with OE / VREF0 / EXT_CLK1
19	IO6	GPIO / SCL
20	GND	GND
21	IO9	GPIO / ACMP0- / ACMP1- / ACMP2- / ACMP3-
22	IO12	GPIO / ACMP3+

Legend:

OE: Output Enable
ACMPx+: ACMPx Positive Input
ACMPx-: ACMPx Negative Input
SCL/OD: I^2C Clock Input/ NMOS Open Drain Output Only
SDA/OD: I^2C Data Input/ NMOS Open Drain Output Only
VREFx: Voltage Reference Output
EXT_CLKx: External Clock Input

3.0 User Programmability

Non-volatile memory (NVM) is used to configure the SLG46538's connection matrix routing and macrocells. The NVM is One-Time-Programmable (OTP). However, Silego's GreenPAK development tools can be used to configure the connection matrix and macrocells, without programming the NVM, to allow on-chip emulation. This configuration will remain active on the device as long as it remains powered and can be re-written as needed to facilitate rapid design changes.

When a design is ready for in-circuit testing, the same GreenPAK development tools can be used to program the NVM and create samples for small quantity builds. Once the NVM is programmed, the device will retain this configuration for the duration of its lifetime.

Once the design is finalized, the design file can be forwarded to Silego to integrate into the production process.

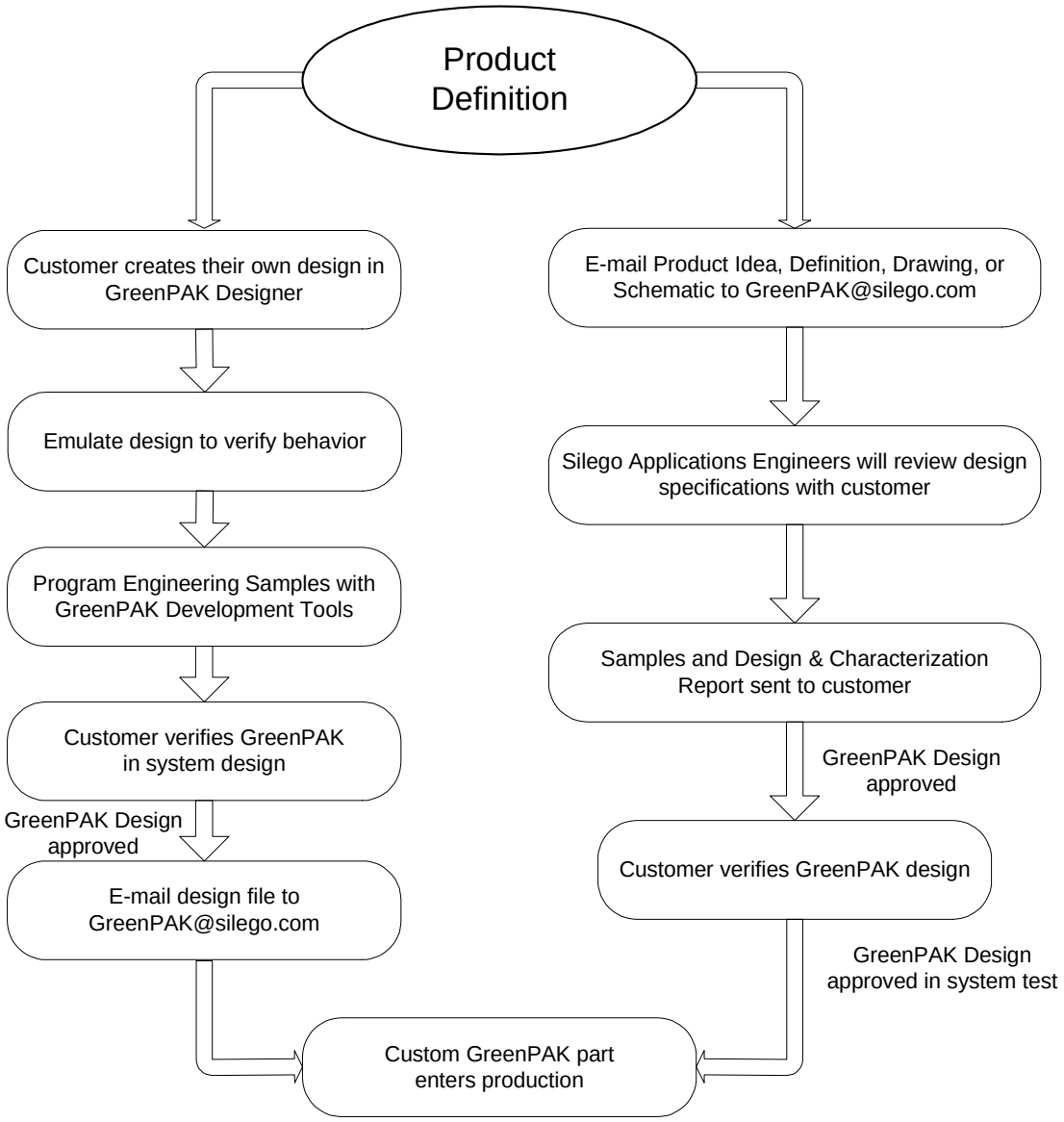


Figure 1. Steps to create a custom Silego GreenPAK device

4.0 Ordering Information

Part Number	Type
SLG46538V	20-pin STQFN
SLG46538VTR	20-pin STQFN - Tape and Reel (3k units)
SLG46538M	22-pin MSTQFN
SLG46538MTR	22-pin MSTQFN - Tape and Reel (3k units)

5.0 Electrical Specifications

5.1 Absolute Maximum Conditions

Parameter		Min.	Max.	Unit
Supply voltage on VDD relative to GND		-0.5	7	V
Supply voltage on VDD2 relative to GND		-0.5	VDD + 0.5	V
DC Input voltage	IOs 0, 1, 2, 3, 4, 5, 6, 7, 8	GND - 0.5	VDD + 0.5	V
	IOs 9, 10, 12, 13, 14, 15, 16, 17		VDD2 + 0.5	
Maximum Average or DC Current (Through pin)	Push-Pull 1x	--	11	mA
	Push-Pull 2x	--	16	
	OD 1x	--	11	
	OD 2x	--	21	
	OD 4x	--	43	
Current at Input Pin		-1.0	1.0	mA
Storage Temperature Range		-65	150	°C
Junction Temperature		--	150	°C
ESD Protection (Human Body Model)		2000	--	V
ESD Protection (Charged Device Model)		500	--	V
Moisture Sensitivity Level		1		

5.2 Electrical Characteristics (1.8 V ±5% V_{DD})

Symbol	Parameter	Condition/Note	Min.	Typ.	Max.	Unit
V_{DD}	Supply Voltage VDD Pin	VDD2 ≤ VDD	1.71	1.8	1.89	V
I_Q	Quiescent Current	Static Inputs and Outputs	--	0.46	--	µA
T_A	Operating Temperature		-40	25	85	°C
V_{PP}	Programming Voltage		7.25	7.50	7.75	V
V_{ACMP}	ACMP Input Voltage Range	Positive Input	0	--	V_{DD}	V
		Negative Input	0	--	1.2	V
V_{IH}	HIGH-Level Input Voltage IOs 0, 1, 2, 3, 4, 5, 6, 7, 8	Logic Input	1.06	--	V_{DD}	V
		Logic Input with Schmitt Trigger	1.28	--	V_{DD}	V
		Low-Level Logic Input	0.94	--	V_{DD}	V
V_{IL}	LOW-Level Input Voltage IOs 0, 1, 2, 3, 4, 5, 6, 7, 8	Logic Input	0	--	0.76	V
		Logic Input with Schmitt Trigger	0	--	0.49	V
		Low-Level Logic Input	0	--	0.52	V
V_{HYS}	Schmitt Trigger Hysteresis Voltage IOs 0, 1, 2, 3, 4, 5, 6, 7, 8	Logic Input with Schmitt Trigger	0.10	0.41	0.66	V
I_{LKG}	Input leakage (Absolute Value) IOs 0, 1, 2, 3, 4, 5, 6, 7, 8		--	1	1000	nA
V_{OH}	HIGH-Level Output Voltage IOs 0, 1, 2, 3, 4, 5, 6, 7, 8	Push-Pull, I_{OH} = 100 µA, 1X Drive	1.69	1.79	--	V
		PMOS OD, I_{OH} = 100 µA, 1X Drive	1.69	1.79	--	V
		Push-Pull, I_{OH} = 100 µA, 2X Drive	1.70	1.79	--	V
		PMOS OD, I_{OH} = 100 µA, 2X Drive	1.70	1.79	--	V
V_{OL}	LOW-Level Output Voltage IOs 0, 1, 2, 3, 4, 5, 6, 7, 8	Push-Pull, I_{OL}= 100 µA, 1X Drive	--	0.01	0.03	V
		Push-Pull, I_{OL} = 100 µA, 2X Drive	--	0.01	0.01	V
		Open Drain, I_{OL} = 100 µA, 1X Drive	--	0.01	0.02	V
		Open Drain, I_{OL} = 100 µA, 2X Drive	--	0.01	0.02	V
		Open Drain NMOS 4X, IO8, I_{OL} = 100 µA	--	0.001	0.002	V
I_{OH}	HIGH-Level Output Pulse Current (see Note 1) IOs 0, 1, 2, 3, 4, 5, 6, 7, 8	Push-Pull, V_{OH} = V_{DD} - 0.2, 1X Drive	1.07	1.70	--	mA
		PMOS OD, V_{OH} = V_{DD} - 0.2, 1X Drive	1.07	1.70	--	mA
		Push-Pull, V_{OH} = V_{DD} - 0.2, 2X Drive	2.22	3.41	--	mA
		PMOS OD, V_{OH} = V_{DD} - 0.2, 2X Drive	2.22	3.41	--	mA
I_{OL}	LOW-Level Output Pulse Current (see Note 1) IOs 0, 1, 2, 3, 4, 5, 6, 7, 8	Push-Pull, V_{OL} = 0.15 V, 1X Drive	0.92	1.69	--	mA
		Push-Pull, V_{OL} = 0.15 V, 2X Drive	1.83	3.38	--	mA
		Open Drain, V_{OL} = 0.15 V, 1X Drive	1.38	2.53	--	mA
		Open Drain, V_{OL} = 0.15 V, 2X Drive	2.75	5.07	--	mA
		Open Drain NMOS 4X, IO8, V_{OL} = 0.15 V	7.21	9.00	--	mA
I_{VDD}	Maximum Average or DC Current Through VDD Pin (Per chip side, see Note 2)	T_J = 85°C	--	--	45	mA
		T_J = 110°C	--	--	22	mA

Symbol	Parameter	Condition/Note	Min.	Typ.	Max.	Unit
I_{GND}	Maximum Average or DC Current Through GND Pin (Per chip side, see Note 2)	T_J = 85°C	--	--	86	mA
		T_J = 110°C	--	--	41	mA
V_O	Maximal Voltage Applied to any PIN in High-Impedance State		--	--	V_{DD}	V
T_{SU}	Startup Time	from VDD rising past PON_{THR}	0.63	1.36	1.87	ms
PON_{THR}	Power On Threshold	V_{DD} Level Required to Start Up the Chip	1.41	1.54	1.66	V
$POFF_{THR}$	Power Off Threshold	V_{DD} Level Required to Switch Off the Chip	1.00	1.15	1.31	V
R_{PUP}	Pull Up Resistance	1 M Pull Up	859.8	1097.1	1358.9	kΩ
		100 k Pull Up	86.47	110.13	136.18	kΩ
		10 k Pull Up	10.82	12.86	15.36	kΩ
R_{PDWN}	Pull Down Resistance	1 M Pull Down	873.9	1097.0	1359.0	kΩ
		100 k Pull Down	88.89	110.53	136.55	kΩ
		10 k Pull Down	9.65	12.75	15.76	kΩ

Note 1: DC or average current through any pin should not exceed value given in Absolute Maximum Conditions.
Note 2: The GreenPAK's power rails are divided in two sides. IOs 0, 1, 2, 3, 4, 5, 6, 7 and 8 are connected to one side, IOs 9, 10, 12, 13, 14, 15, 16 and 17 to another.

5.3 Electrical Characteristics (3.3 V ±10% V_{DD})

Symbol	Parameter	Condition/Note	Min.	Typ.	Max.	Unit
V_{DD}	Supply Voltage VDD Pin	VDD2 ≤ VDD	3.0	3.3	3.6	V
I_Q	Quiescent Current	Static Inputs and Outputs	--	0.81	--	µA
T_A	Operating Temperature		-40	25	85	°C
V_{PP}	Programming Voltage		7.25	7.50	7.75	V
V_{ACMP}	ACMP Input Voltage Range	Positive Input	0	--	V_{DD}	V
		Negative Input	0	--	1.2	V
V_{IH}	HIGH-Level Input Voltage IOs 0, 1, 2, 3, 4, 5, 6, 7, 8	Logic Input	1.81	--	V_{DD}	V
		Logic Input with Schmitt Trigger	2.14	--	V_{DD}	V
		Low-Level Logic Input	1.06	--	V_{DD}	V
V_{IL}	LOW-Level Input Voltage IOs 0, 1, 2, 3, 4, 5, 6, 7, 8	Logic Input	0	--	1.31	V
		Logic Input with Schmitt Trigger	0	--	0.97	V
		Low-Level Logic Input	0	--	0.67	V
V_{HYS}	Schmitt Trigger Hysteresis Voltage IOs 0, 1, 2, 3, 4, 5, 6, 7, 8	Logic Input with Schmitt Trigger	0.29	0.62	0.94	V
I_{LGK}	Input leakage (Absolute Value) IOs 0, 1, 2, 3, 4, 5, 6, 7, 8		--	1	1000	nA
V_{OH}	HIGH-Level Output Voltage IOs 0, 1, 2, 3, 4, 5, 6, 7, 8	Push-Pull, I_{OH} = 3 mA, 1X Drive	2.74	3.12	--	V
		PMOS OD, I_{OH} = 3 mA, 1X Drive	2.74	3.12	--	V
		Push-Pull, I_{OH} = 3 mA, 2X Drive	2.87	3.21	--	V
		PMOS OD, I_{OH} = 3 mA, 2X Drive	2.87	3.21	--	V
V_{OL}	LOW-Level Output Voltage IOs 0, 1, 2, 3, 4, 5, 6, 7, 8	Push-Pull, I_{OL}= 3 mA, 1X Drive	--	0.13	0.23	V
		Push-Pull, I_{OL} = 3 mA, 2X Drive	--	0.06	0.11	V
		Open Drain, I_{OL} = 3 mA, 1X Drive	--	0.08	0.15	V
		Open Drain, I_{OL} = 3 mA, 2X Drive	--	0.04	0.08	V
		Open Drain NMOS 4X, IO8, I_{OL} = 3 mA	--	0.02	0.04	V
I_{OH}	HIGH-Level Output Pulse Current (see Note 1) IOs 0, 1, 2, 3, 4, 5, 6, 7, 8	Push-Pull, V_{OH} = 2.4 V, 1X Drive	6.05	12.08	--	mA
		PMOS OD, V_{OH} = 2.4 V, 1X Drive	6.05	12.08	--	mA
		Push-Pull, V_{OH} = 2.4 V, 2X Drive	11.54	24.16	--	mA
		PMOS OD, V_{OH} = 2.4 V, 2X Drive	11.52	24.16	--	mA
I_{OL}	LOW-Level Output Pulse Current (see Note 1) IOs 0, 1, 2, 3, 4, 5, 6, 7, 8	Push-Pull, V_{OL} = 0.4 V, 1X Drive	4.88	8.24	--	mA
		Push-Pull, V_{OL} = 0.4 V, 2X Drive	9.75	16.49	--	mA
		Open Drain, V_{OL} = 0.4 V, 1X Drive	7.31	12.37	--	mA
		Open Drain, V_{OL} = 0.4 V, 2X Drive	14.54	24.74	--	mA
		Open Drain NMOS 4X, IO8, V_{OL} = 0.4 V	31.32	41.06	--	mA
I_{VDD}	Maximum Average or DC Current Through VDD Pin (Per chip side, see Note 2)	T_J = 85°C	--	--	45	mA
		T_J = 110°C	--	--	22	mA

Symbol	Parameter	Condition/Note	Min.	Typ.	Max.	Unit
I_{GND}	Maximum Average or DC Current Through GND Pin (Per chip side, see Note 2)	T_J = 85°C	--	--	86	mA
		T_J = 110°C	--	--	41	mA
V_O	Maximal Voltage Applied to any PIN in High-Impedance State		--	--	V_{DD}	V
T_{SU}	Startup Time	from VDD rising past PON_{THR}	0.61	1.24	1.65	ms
PON_{THR}	Power On Threshold	V_{DD} Level Required to Start Up the Chip	1.41	1.54	1.66	V
$POFF_{THR}$	Power Off Threshold	V_{DD} Level Required to Switch Off the Chip	1.00	1.15	1.31	V
R_{PUP}	Pull Up Resistance	1 M Pull Up	873.2	1094.7	1364.3	kΩ
		100 k Pull Up	85.17	109.30	135.52	kΩ
		10 k Pull Up	9.61	11.86	14.73	kΩ
R_{PDWN}	Pull Down Resistance	1 M Pull Down	862.5	1096.3	1357.4	kΩ
		100 k Pull Down	87.95	109.76	136.06	kΩ
		10 k Pull Down	8.66	11.81	15.05	kΩ

Note 1: DC or average current through any pin should not exceed value given in Absolute Maximum Conditions.
Note 2: The GreenPAK's power rails are divided in two sides. IOs 0, 1, 2, 3, 4, 5, 6, 7 and 8 are connected to one side, IOs 9, 10, 12, 13, 14, 15, 16 and 17 to another.

5.4 Electrical Characteristics (5 V ±10% V_{DD})

Symbol	Parameter	Condition/Note	Min.	Typ.	Max.	Unit
V_{DD}	Supply Voltage VDD Pin	VDD2 ≤ VDD	4.5	5.0	5.5	V
I_Q	Quiescent Current	Static Inputs and Outputs	--	1.26	--	µA
T_A	Operating Temperature		-40	25	85	°C
V_{PP}	Programming Voltage		7.25	7.50	7.75	V
V_{ACMP}	ACMP Input Voltage Range	Positive Input	0	--	V_{DD}	V
		Negative Input	0	--	1.2	V
V_{IH}	HIGH-Level Input Voltage	Logic Input	2.68	--	V_{DD}	V
		Logic Input with Schmitt Trigger	3.34	--	V_{DD}	V
		Low-Level Logic Input	1.15	--	V_{DD}	V
V_{IL}	LOW-Level Input Voltage	Logic Input	0	--	1.96	V
		Logic Input with Schmitt Trigger	0	--	1.41	V
		Low-Level Logic Input	0	--	0.77	V
V_{HYS}	Schmitt Trigger Hysteresis Voltage IOs 0, 1, 2, 3, 4, 5, 6, 7, 8	Logic Input with Schmitt Trigger	0.44	0.90	1.38	V
I_{LGK}	Input leakage (Absolute Value) IOs 0, 1, 2, 3, 4, 5, 6, 7, 8		--	1	1000	nA
V_{OH}	HIGH-Level Output Voltage IOs 0, 1, 2, 3, 4, 5, 6, 7, 8	Push-Pull, I_{OH} = 5 mA, 1X Drive	4.15	4.76	--	V
		PMOS OD, I_{OH} = 5 mA, 1X Drive	4.16	4.76	--	V
		Push-Pull, I_{OH} = 5 mA, 2X Drive	4.32	4.89	--	V
		PMOS OD, I_{OH} = 5 mA, 2X Drive	4.33	4.89	--	V
V_{OL}	LOW-Level Output Voltage IOs 0, 1, 2, 3, 4, 5, 6, 7, 8	Push-Pull, I_{OL}= 5 mA, 1X Drive	--	0.19	0.24	V
		Push-Pull, I_{OL} =5 mA, 2X Drive	--	0.09	0.12	V
		Open Drain, I_{OL} = 5 mA, 1X Drive	--	0.12	0.16	V
		Open Drain, I_{OL} = 5 mA, 2X Drive	--	0.07	0.08	V
		Open Drain NMOS 4X, IO8, I_{OL} = 5 mA	--	0.03	0.05	V
I_{OH}	HIGH-Level Output Pulse Current (see Note 1) IOs 0, 1, 2, 3, 4, 5, 6, 7, 8	Push-Pull, V_{OH} = 2.4 V, 1X Drive	22.08	34.04	--	mA
		PMOS OD, V_{OH} = 2.4 V, 1X Drive	22.08	34.04	--	mA
		Push-Pull, V_{OH} = 2.4 V, 2X Drive	41.76	68.08	--	mA
		PMOS OD, V_{OH} = 2.4 V, 2X Drive	41.69	68.08	--	mA
I_{OL}	LOW-Level Output Pulse Current (see Note 1) IOs 0, 1, 2, 3, 4, 5, 6, 7, 8	Push-Pull, V_{OL} = 0.4 V, 1X Drive	7.22	11.58	--	mA
		Push-Pull, V_{OL} = 0.4 V, 2X Drive	13.83	23.16	--	mA
		Open Drain, V_{OL} = 0.4 V, 1X Drive	10.82	17.38	--	mA
		Open Drain, V_{OL} = 0.4 V, 2X Drive	17.34	34.76	--	mA
		Open Drain NMOS 4X, IO8, V_{OL} = 0.4 V	41.06	55.18	--	mA
I_{VDD}	Maximum Average or DC Current Through VDD Pin (Per chip side, see Note 2)	T_J = 85°C	--	--	45	mA
		T_J = 110°C	--	--	22	mA

Symbol	Parameter	Condition/Note	Min.	Typ.	Max.	Unit
I_{GND}	Maximum Average or DC Current Through GND Pin (Per chip side, see Note 2)	T_J = 85°C	--	--	86	mA
		T_J = 110°C	--	--	41	mA
V_O	Maximal Voltage Applied to any PIN in High-Impedance State		--	--	V_{DD}	V
T_{SU}	Startup Time	from VDD rising past PON_{THR}	0.60	1.23	1.61	ms
PON_{THR}	Power On Threshold	V_{DD} Level Required to Start Up the Chip	1.41	1.54	1.66	V
$POFF_{THR}$	Power Off Threshold	V_{DD} Level Required to Switch Off the Chip	1.00	1.15	1.31	V
R_{PUP}	Pull Up Resistance	1 M Pull Up	864.6	1093.4	1348.1	kΩ
		100 k Pull Up	84.32	108.97	135.24	kΩ
		10 k Pull Up	8.74	11.37	14.52	kΩ
R_{PDWN}	Pull Down Resistance	1 M Pull Down	873.3	1096.1	1370.5	kΩ
		100 k Pull Down	87.57	109.48	135.89	kΩ
		10 k Pull Down	7.95	11.33	14.78	kΩ

Note 1: DC or average current through any pin should not exceed value given in Absolute Maximum Conditions.
Note 2: The GreenPAK's power rails are divided in two sides. IOs 0, 1, 2, 3, 4, 5, 6, 7 and 8 are connected to one side, IOs 9, 10, 12, 13, 14, 15, 16 and 17 to another.

5.5 Electrical Characteristics (1.8 V ±5% V_{DD2})

Symbol	Parameter	Condition/Note	Min.	Typ.	Max.	Unit
V_{DD2}	Supply Voltage VDD2 Pin	VDD2 ≤ VDD	1.71	--	V_{DD}	V
V_{IH2}	HIGH-Level Input Voltage IOs 9, 10, 12, 13, 14, 15, 16, 17	Logic Input, V_{DD2} = 1.8 V	1.06	--	V_{DD2}	V
		Logic Input with Schmitt Trigger, V_{DD2} = 1.8 V	1.28	--	V_{DD2}	V
		Low-Level Logic Input, V_{DD2} = 1.8 V	0.94	--	V_{DD2}	V
V_{IL2}	LOW-Level Input Voltage IOs 9, 10, 12, 13, 14, 15, 16, 17	Logic Input, V_{DD2} = 1.8 V	0	--	0.76	V
		Logic Input with Schmitt Trigger, V_{DD2} = 1.8 V	0	--	0.49	V
		Low-Level Logic Input, V_{DD2} = 1.8 V	0	--	0.52	V
V_{HYS}	Schmitt Trigger Hysteresis Voltage IOs 9, 10, 12, 13, 14, 15, 16, 17	Logic Input with Schmitt Trigger, V_{DD2} = 1.8 V	0.10	0.41	0.66	V
I_{LKG}	Input leakage (Absolute Value) IOs 9, 10, 12, 13, 14, 15, 16, 17		--	1	1000	nA
V_{OH2}	HIGH-Level Output Voltage IOs 9, 10, 12, 13, 14, 15, 16, 17	Push-Pull 1X, Open Drain PMOS 1X, I_{OH} = 100 µA, V_{DD2} = 1.8 V	1.68	1.79	--	V
		Push-Pull 2X, Open Drain PMOS 2X, I_{OH} = 100 µA, V_{DD2} = 1.8 V	1.70	1.79	--	V
V_{OL2}	LOW-Level Output Voltage IOs 9, 10, 12, 13, 14, 15, 16, 17	Push-Pull 1X, I_{OL}= 100 µA, V_{DD2} = 1.8 V	--	0.010	0.015	V
		Push-Pull 2X, I_{OL} = 100 µA, V_{DD2} = 1.8 V	--	0.007	0.010	V
		Open Drain NMOS 1X, I_{OL} = 100 µA, V_{DD2} = 1.8 V	--	0.007	0.010	V
		Open Drain NMOS 2X, I_{OL} = 100 µA, V_{DD2} = 1.8 V	--	0.003	0.010	V
		Open Drain NMOS 4X, IO9, I_{OL} = 100 µA, V_{DD2} = 1.8 V	--	0.001	0.004	V
I_{OH2}	HIGH-Level Output Pulse Current (see Note 1) IOs 9, 10, 12, 13, 14, 15, 16, 17	Push-Pull 1X,Open Drain PMOS 1X, V_{OH} = V_{DD} - 0.2, V_{DD2} = 1.8 V	1.03	1.70	--	mA
		Push-Pull 2X, Open Drain PMOS 2X, V_{OH} = V_{DD} - 0.2, V_{DD2} = 1.8 V	2.03	3.41	--	mA
I_{OL2}	LOW-Level Output Pulse Current (see Note 1) IOs 9, 10, 12, 13, 14, 15, 16, 17	Push-Pull 1X, V_{OL} = 0.15 V, V_{DD2} = 1.8 V	0.92	1.66	--	mA
		Push-Pull 2X, V_{OL} = 0.15 V, V_{DD2} = 1.8 V	1.83	3.30	--	mA
		Open Drain NMOS 1X, V_{OL} = 0.15 V, V_{DD2} = 1.8 V	1.38	2.53	--	mA
		Open Drain NMOS 2X, V_{OL} = 0.15 V, V_{DD2} = 1.8 V	2.75	5.07	--	mA
		Open Drain NMOS 4X, IO9, V_{OL} = 0.15 V, V_{DD2} = 1.8 V	5.50	10.14	--	mA
I_{VDD}	Maximum Average or DC Current Through VDD Pin (Per chip side, see Note 2)	T_J = 85°C	--	--	45	mA
		T_J = 110°C	--	--	22	mA

Symbol	Parameter	Condition/Note	Min.	Typ.	Max.	Unit
I_{GND}	Maximum Average or DC Current Through GND Pin (Per chip side, see Note 2)	T_J = 85°C	--	--	86	mA
		T_J = 110°C	--	--	41	mA

Note 1: DC or average current through any pin should not exceed value given in Absolute Maximum Conditions.
Note 2: The GreenPAK's power rails are divided in two sides. IOs 0, 1, 2, 3, 4, 5, 6, 7 and 8 are connected to one side, IOs 9, 10, 12, 13, 14, 15, 16 and 17 to another.

5.6 Electrical Characteristics (3.3 V ±10% V_{DD2})

Symbol	Parameter	Condition/Note	Min.	Typ.	Max.	Unit
V_{DD2}	Supply Voltage VDD2 Pin	VDD2 ≤ VDD	1.71	--	V_{DD}	V
V_{IH2}	HIGH-Level Input Voltage IOs 9, 10, 12, 13, 14, 15, 16, 17	Logic Input, V_{DD2} = 1.8 V	1.06	--	V_{DD2}	V
		Logic Input with Schmitt Trigger, V_{DD2} = 1.8 V	1.28	--	V_{DD2}	V
		Low-Level Logic Input, V_{DD2} = 1.8 V	0.94	--	V_{DD2}	V
V_{IL2}	LOW-Level Input Voltage IOs 9, 10, 12, 13, 14, 15, 16, 17	Logic Input, V_{DD2} = 1.8 V	0	--	0.76	V
		Logic Input with Schmitt Trigger, V_{DD2} = 1.8 V	0	--	0.49	V
		Low-Level Logic Input, V_{DD2} = 1.8 V	0	--	0.52	V
V_{HYS}	Schmitt Trigger Hysteresis Voltage IOs 9, 10, 12, 13, 14, 15, 16, 17	Logic Input with Schmitt Trigger, V_{DD2} = 1.8 V	0.29	0.62	0.94	V
I_{LGK}	Input leakage (Absolute Value) IOs 9, 10, 12, 13, 14, 15, 16, 17		--	1	1000	nA
V_{OH2}	HIGH-Level Output Voltage IOs 9, 10, 12, 13, 14, 15, 16, 17	Push-Pull, PMOS OD, I_{OH} = 100 µA, 1X Drive, V_{DD2} = 1.8 V	1.69	1.79	--	V
		Push-Pull, PMOS OD, I_{OH} = 100 µA, 2X Drive, V_{DD2} = 1.8 V	1.70	1.79	--	V
V_{OL2}	LOW-Level Output Voltage IOs 9, 10, 12, 13, 14, 15, 16, 17	Push-Pull 1X Drive, I_{OL}= 100 µA, V_{DD2} = 1.8 V	--	0.01	0.03	V
		Push-Pull 2X Drive, I_{OL} = 100 µA, V_{DD2} = 1.8 V	--	0.01	0.01	V
		Open Drain NMOS 1X Drive, I_{OL} = 100 µA, V_{DD2} = 1.8 V	--	0.01	0.02	V
		Open Drain NMOS 2X Drive, I_{OL} = 100 µA, V_{DD2} = 1.8 V	--	0.01	0.02	V
		Open Drain NMOS 4X, IO9, I_{OL} = 100 µA, V_{DD2} = 1.8 V	--	0.001	0.002	V
I_{OH2}	HIGH-Level Output Pulse Current (see Note 1) IOs 9, 10, 12, 13, 14, 15, 16, 17	Push-Pull, PMOS OD, V_{OH} = V_{DD} - 0.2, 1X Drive, V_{DD2} = 1.8 V	1.07	1.70	--	mA
		Push-Pull, PMOS OD, V_{OH} = V_{DD} - 0.2, 2X Drive, V_{DD2} = 1.8 V	2.22	3.41	--	mA
I_{OL2}	LOW-Level Output Pulse Current (see Note 1) IOs 9, 10, 12, 13, 14, 15, 16, 17	Push-Pull, V_{OL} = 0.15 V, 1X Drive, V_{DD2} = 1.8 V	0.92	1.69	--	mA
		Push-Pull, V_{OL} = 0.15 V, 2X Drive, V_{DD2} = 1.8 V	1.83	3.38	--	mA
		Open Drain NMOS, V_{OL} = 0.15 V, 1X Drive, V_{DD2} = 1.8 V	1.38	2.53	--	mA
		Open Drain NMOS, V_{OL} = 0.15 V, 2X Drive, V_{DD2} = 1.8 V	2.75	5.07	--	mA
		Open Drain NMOS 4X, IO9, V_{OL} = 0.15 V, V_{DD2} = 1.8 V	7.21	9.00	--	mA

Symbol	Parameter	Condition/Note	Min.	Typ.	Max.	Unit
V_{IH2}	HIGH-Level Input Voltage IOs 9, 10, 12, 13, 14, 15, 16, 17	Logic Input, V_{DD2} = 3.3 V	1.81	--	V_{DD}	V
		Logic Input with Schmitt Trigger, V_{DD2} = 3.3 V	2.14	--	V_{DD}	V
		Low-Level Logic Input, V_{DD2} = 3.3 V	1.06	--	V_{DD}	V
V_{IL2}	LOW-Level Input Voltage IOs 9, 10, 12, 13, 14, 15, 16, 17	Logic Input, V_{DD2} = 3.3 V	0	--	1.31	V
		Logic Input with Schmitt Trigger, V_{DD2} = 3.3 V	0	--	0.97	V
		Low-Level Logic Input, V_{DD2} = 3.3 V	0	--	0.67	V
V_{OH2}	HIGH-Level Output Voltage IOs 9, 10, 12, 13, 14, 15, 16, 17	Push-Pull, I_{OH} = 3 mA, 1X Drive, V_{DD2} = 3.3 V	2.70	3.12	--	V
		PMOS OD, I_{OH} = 3 mA, 1X Drive, V_{DD2} = 3.3 V	2.70	3.12	--	V
		Push-Pull, I_{OH} = 3 mA, 2X Drive, V_{DD2} = 3.3 V	2.85	3.21	--	V
		PMOS OD, I_{OH} = 3 mA, 2X Drive, V_{DD2} = 3.3 V	2.86	3.21	--	V
V_{OL2}	LOW-Level Output Voltage IOs 9, 10, 12, 13, 14, 15, 16, 17	Push-Pull, I_{OL}= 3 mA, 1X Drive, V_{DD2} = 3.3 V	--	0.13	0.23	V
		Push-Pull, I_{OL} = 3 mA, 2X Drive, V_{DD2} = 3.3 V	--	0.06	0.11	V
		Open Drain, I_{OL} = 3 mA, 1X Drive, V_{DD2} = 3.3 V	--	0.08	0.15	V
		Open Drain, I_{OL} = 3 mA, 2X Drive, V_{DD2} = 3.3 V	--	0.04	0.08	V
		Open Drain NMOS 4X, IO9, I_{OL} = 3 mA, V_{DD2} = 3.3 V	--	0.02	0.04	V
I_{OH2}	HIGH-Level Output Pulse Current (see Note 1) IOs 9, 10, 12, 13, 14, 15, 16, 17	Push-Pull, V_{OH} = 2.4 V, 1X Drive, V_{DD2} = 3.3 V	6.05	12.08	--	mA
		PMOS OD, V_{OH} = 2.4 V, 1X Drive, V_{DD2} = 3.3 V	6.05	12.08	--	mA
		Push-Pull, V_{OH} = 2.4 V, 2X Drive, V_{DD2} = 3.3 V	11.54	24.16	--	mA
		PMOS OD, V_{OH} = 2.4 V, 2X Drive, V_{DD2} = 3.3 V	11.52	24.16	--	mA
I_{OL2}	LOW-Level Output Pulse Current (see Note 1) IOs 9, 10, 12, 13, 14, 15, 16, 17	Push-Pull, V_{OL} = 0.4 V, 1X Drive, V_{DD2} = 3.3 V	4.88	8.24	--	mA
		Push-Pull, V_{OL} = 0.4 V, 2X Drive, V_{DD2} = 3.3 V	9.75	16.49	--	mA
		Open Drain, V_{OL} = 0.4 V, 1X Drive, V_{DD2} = 3.3 V	7.31	12.37	--	mA
		Open Drain, V_{OL} = 0.4 V, 2X Drive, V_{DD2} = 3.3 V	14.54	24.74	--	mA
		Open Drain NMOS 4X, IO9, V_{DD2} = 3.3 V	31.32	41.06	--	mA
I_{VDD}	Maximum Average or DC Current Through VDD Pin (Per chip side, see Note 2)	T_J = 85°C	--	--	45	mA
		T_J = 110°C	--	--	22	mA

Symbol	Parameter	Condition/Note	Min.	Typ.	Max.	Unit
I_{GND}	Maximum Average or DC Current Through GND Pin (Per chip side, see Note 2)	T_J = 85°C	--	--	86	mA
		T_J = 110°C	--	--	41	mA

Note 1: DC or average current through any pin should not exceed value given in Absolute Maximum Conditions.
Note 2: The GreenPAK's power rails are divided in two sides. IOs 0, 1, 2, 3, 4, 5, 6, 7 and 8 are connected to one side, IOs 9, 10, 12, 13, 14, 15, 16 and 17 to another.

5.7 Electrical Characteristics (5 V ±10% V_{DD2})

Symbol	Parameter	Condition/Note	Min.	Typ.	Max.	Unit
V_{DD2}	Supply Voltage VDD2 Pin	VDD2 ≤ VDD	1.71	--	V_{DD}	V
V_{IH2}	HIGH-Level Input Voltage IOs 9, 10, 12, 13, 14, 15, 16, 17	Logic Input, V_{DD2} = 1.8 V	1.06	--	V_{DD2}	V
		Logic Input with Schmitt Trigger, V_{DD2} = 1.8 V	1.28	--	V_{DD2}	V
		Low-Level Logic Input, V_{DD2} = 1.8 V	0.94	--	V_{DD2}	V
V_{IL2}	LOW-Level Input Voltage IOs 9, 10, 12, 13, 14, 15, 16, 17	Logic Input, V_{DD2} = 1.8 V	0	--	0.76	V
		Logic Input with Schmitt Trigger, V_{DD2} = 1.8 V	0	--	0.49	V
		Low-Level Logic Input, V_{DD2} = 1.8 V	0	--	0.52	V
V_{HYS}	Schmitt Trigger Hysteresis Voltage IOs 9, 10, 12, 13, 14, 15, 16, 17	Logic Input with Schmitt Trigger, V_{DD2} = 1.8 V	0.29	0.62	0.94	V
I_{LGK}	Input leakage (Absolute Value) IOs 9, 10, 12, 13, 14, 15, 16, 17		--	1	1000	nA
V_{OH2}	HIGH-Level Output Voltage IOs 9, 10, 12, 13, 14, 15, 16, 17	Push-Pull, I_{OH} = 100 µA, 1X Drive, V_{DD2} = 1.8 V	1.69	1.79	--	V
		PMOS OD, I_{OH} = 100 µA, 1X Drive, V_{DD2} = 1.8 V	1.69	1.79	--	V
		Push-Pull, I_{OH} = 100 µA, 2X Drive, V_{DD2} = 1.8 V	1.70	1.79	--	V
		PMOS OD, I_{OH} = 100 µA, 2X Drive, V_{DD2} = 1.8 V	1.70	1.79	--	V
V_{OL2}	LOW-Level Output Voltage IOs 9, 10, 12, 13, 14, 15, 16, 17	Push-Pull 1X Drive, I_{OL}= 100 µA, V_{DD2} = 1.8 V	--	0.01	0.03	V
		Push-Pull 2X Drive, I_{OL} = 100 µA, V_{DD2} = 1.8 V	--	0.01	0.01	V
		Open Drain NMOS 1X Drive, I_{OL} = 100 µA, V_{DD2} = 1.8 V	--	0.01	0.02	V
		Open Drain NMOS 2X Drive, I_{OL} = 100 µA, V_{DD2} = 1.8 V	--	0.01	0.02	V
		Open Drain NMOS 4X, IO9, I_{OL} = 100 µA, V_{DD2} = 1.8 V	--	0.001	0.002	V
I_{OH2}	HIGH-Level Output Pulse Current (see Note 1) IOs 9, 10, 12, 13, 14, 15, 16, 17	Push-Pull, PMOS, V_{OH} = V_{DD} - 0.2, 1X Drive, V_{DD2} = 1.8 V	1.07	1.70	--	mA
		Push-Pull, PMOS, V_{OH} = V_{DD} - 0.2, 2X Drive, V_{DD2} = 1.8 V	2.22	3.41	--	mA

Symbol	Parameter	Condition/Note	Min.	Typ.	Max.	Unit
I_{OL2}	LOW-Level Output Pulse Current (see Note 1) IOs 9, 10, 12, 13, 14, 15, 16, 17	Push-Pull, V_{OL} = 0.15 V, 1X Drive, V_{DD2} = 1.8 V	0.92	1.69	--	mA
		Push-Pull, V_{OL} = 0.15 V, 2X Drive, V_{DD2} = 1.8 V	1.83	3.38	--	mA
		Open Drain NMOS, V_{OL} = 0.15 V, 1X Drive, V_{DD2} = 1.8 V	1.38	2.53	--	mA
		Open Drain NMOS, V_{OL} = 0.15 V, 2X Drive, V_{DD2} = 1.8 V	2.75	5.07	--	mA
		Open Drain NMOS 4X, IO9, V_{OL} = 0.15 V, V_{DD2} = 1.8 V	7.21	9.00	--	mA
V_{IH2}	HIGH-Level Input Voltage IOs 9, 10, 12, 13, 14, 15, 16, 17	Logic Input, V_{DD2} = 3.3 V	1.81	--	V_{DD}	V
		Logic Input with Schmitt Trigger, V_{DD2} = 3.3 V	2.14	--	V_{DD}	V
		Low-Level Logic Input, V_{DD2} = 3.3 V	1.06	--	V_{DD}	V
V_{IL2}	LOW-Level Input Voltage IOs 9, 10, 12, 13, 14, 15, 16, 17	Logic Input, V_{DD2} = 3.3 V	0	--	1.31	V
		Logic Input with Schmitt Trigger, V_{DD2} = 3.3 V	0	--	0.97	V
		Low-Level Logic Input, V_{DD2} = 3.3 V	0	--	0.67	V
V_{OH2}	HIGH-Level Output Voltage IOs 9, 10, 12, 13, 14, 15, 16, 17	Push-Pull, I_{OH} = 3 mA, 1X Drive, V_{DD2} = 3.3 V	2.70	3.12	--	V
		PMOS OD, I_{OH} = 3 mA, 1X Drive, V_{DD2} = 3.3 V	2.70	3.12	--	V
		Push-Pull, I_{OH} = 3 mA, 2X Drive, V_{DD2} = 3.3 V	2.85	3.21	--	V
		PMOS OD, I_{OH} = 3 mA, 2X Drive, V_{DD2} = 3.3 V	2.86	3.21	--	V
V_{OL2}	LOW-Level Output Voltage IOs 9, 10, 12, 13, 14, 15, 16, 17	Push-Pull, I_{OL}= 3 mA, 1X Drive, V_{DD2} = 3.3 V	--	0.13	0.23	V
		Push-Pull, I_{OL} = 3 mA, 2X Drive, V_{DD2} = 3.3 V	--	0.06	0.11	V
		Open Drain, I_{OL} = 3 mA, 1X Drive, V_{DD2} = 3.3 V	--	0.08	0.15	V
		Open Drain, I_{OL} = 3 mA, 2X Drive, V_{DD2} = 3.3 V	--	0.04	0.08	V
		Open Drain NMOS 4X, IO9, I_{OL} = 3 mA, V_{DD2} = 3.3 V	--	0.02	0.04	V
I_{OH2}	HIGH-Level Output Pulse Current (see Note 1) IOs 9, 10, 12, 13, 14, 15, 16, 17	Push-Pull, PMOS OD, V_{OH} = 2.4 V, 1X Drive, V_{DD2} = 3.3 V	6.05	12.08	--	mA
		Push-Pull, PMOS OD, V_{OH} = 2.4 V, 2X Drive, V_{DD2} = 3.3 V	11.54	24.16	--	mA

Symbol	Parameter	Condition/Note	Min.	Typ.	Max.	Unit
I_{OL2}	LOW-Level Output Pulse Current (see Note 1) IOs 9, 10, 12, 13, 14, 15, 16, 17	Push-Pull, V_{OL} = 0.4 V, 1X Drive, V_{DD2} = 3.3 V	4.88	8.24	--	mA
		Push-Pull, V_{OL} = 0.4 V, 2X Drive, V_{DD2} = 3.3 V	9.75	16.49	--	mA
		Open Drain NMOS, V_{OL} = 0.4 V, 1X Drive, V_{DD2} = 3.3 V	7.31	12.37	--	mA
		Open Drain NMOS, V_{OL} = 0.4 V, 2X Drive, V_{DD2} = 3.3 V	14.54	24.74	--	mA
		Open Drain NMOS 4X, IO9, V_{DD2} = 3.3 V	31.32	41.06	--	mA
V_{IH2}	HIGH-Level Input Voltage IOs 9, 10, 12, 13, 14, 15, 16, 17	Logic Input, V_{DD2} = 5.0 V	2.68	--	V_{DD}	V
		Logic Input with Schmitt Trigger, V_{DD2} = 5.0 V	3.34	--	V_{DD}	V
		Low-Level Logic Input, V_{DD2} = 5.0 V	1.15	--	V_{DD}	V
V_{IL2}	LOW-Level Input Voltage IOs 9, 10, 12, 13, 14, 15, 16, 17	Logic Input, V_{DD2} = 5.0 V	0	--	1.96	V
		Logic Input with Schmitt Trigger, V_{DD2} = 5.0 V	0	--	1.41	V
		Low-Level Logic Input, V_{DD2} = 5.0 V	0	--	0.77	V
V_{OH2}	HIGH-Level Output Voltage IOs 9, 10, 12, 13, 14, 15, 16, 17	Push-Pull, PMOS OD, I_{OH} = 3 mA, 1X Drive, V_{DD2} = 5.0 V	4.15	4.76	--	V
		Push-Pull, PMOS OD, I_{OH} = 3 mA, 2X Drive, V_{DD2} = 5.0 V	4.32	4.89	--	V
V_{OL2}	LOW-Level Output Voltage IOs 9, 10, 12, 13, 14, 15, 16, 17	Push-Pull, I_{OL}= 3 mA, 1X Drive, V_{DD2} = 5.0 V	--	0.19	0.24	V
		Push-Pull, I_{OL} = 3 mA, 2X Drive, V_{DD2} = 5.0 V	--	0.09	0.12	V
		Open Drain NMOS, I_{OL} = 3 mA, 1X Drive, V_{DD2} = 5.0 V	--	0.12	0.16	V
		Open Drain NMOS, I_{OL} = 3 mA, 2X Drive, V_{DD2} = 5.0 V	--	0.07	0.08	V
		Open Drain NMOS 4X, IO9, I_{OL} = 3 mA, V_{DD2} = 5.0 V	--	0.03	0.05	V
I_{OH2}	HIGH-Level Output Pulse Current (see Note 1) IOs 9, 10, 12, 13, 14, 15, 16, 17	Push-Pull, V_{OH} = 2.4 V, 1X Drive, V_{DD2} = 5.0 V	22.08	34.04	--	mA
		PMOS OD, V_{OH} = 2.4 V, 1X Drive, V_{DD2} = 5.0 V	22.08	34.04	--	mA
		Push-Pull, V_{OH} = 2.4 V, 2X Drive, V_{DD2} = 5.0 V	41.76	68.08	--	mA
		PMOS OD, V_{OH} = 2.4 V, 2X Drive, V_{DD2} = 5.0	41.69	68.08	--	mA

Symbol	Parameter	Condition/Note	Min.	Typ.	Max.	Unit
I_{OL2}	LOW-Level Output Pulse Current (see Note 1) IOs 9, 10, 12, 13, 14, 15, 16, 17	Push-Pull, V_{OL} = 0.4 V, 1X Drive, V_{DD2} = 5.0 V	7.22	11.58	--	mA
		Push-Pull, V_{OL} = 0.4 V, 2X Drive, V_{DD2} = 5.0 V	13.83	23.16	--	mA
		Open Drain NMOS, V_{OL} = 0.4 V, 1X Drive, V_{DD2} = 5.0 V	10.82	17.38	--	mA
		Open Drain NMOS, V_{OL} = 0.4 V, 2X Drive, V_{DD2} = 5.0 V	17.34	34.76	--	mA
		Open Drain NMOS 4X, IO9, V_{DD2} = 5.0 V	41.06	55.18	--	mA
I_{VDD}	Maximum Average or DC Current Through VDD Pin (Per chip side, see Note 2)	T_J = 85°C	--	--	45	mA
		T_J = 110°C	--	--	22	mA
I_{GND}	Maximum Average or DC Current Through GND Pin (Per chip side, see Note 2)	T_J = 85°C	--	--	86	mA
		T_J = 110°C	--	--	41	mA

Note 1: DC or average current through any pin should not exceed value given in Absolute Maximum Conditions.
Note 2: The GreenPAK's power rails are divided in two sides. IOs 0, 1, 2, 3, 4, 5, 6, 7 and 8 are connected to one side, IOs 9, 10, 12, 13, 14, 15, 16 and 17 to another.

5.8 I²C Specifications

Symbol	Parameter	Condition/Note	Min.	Typ.	Max.	Unit
F_{SCL}	Clock Frequency, SCL	V_{DD} = (1.71...5.5) V	--	--	400	kHz
t_{LOW}	Clock Pulse Width Low	V_{DD} = (1.71...5.5) V	1300	--	--	ns
t_{HIGH}	Clock Pulse Width High	V_{DD} = (1.71...5.5) V	600	--	--	ns
t_I	Input Filter Spike Suppression (SCL, SDA)	V_{DD} = 1.8 V ± 5 %	--	--	95	ns
		V_{DD} = 3.3 V ± 10%	--	--	95	
		V_{DD} = 5.0 V ± 10 %	--	--	111	
t_{AA}	Clock Low to Data Out Valid	V_{DD} = (1.71...5.5) V	--	--	900	ns
t_{BUF}	Bus Free Time between Stop and Start	V_{DD} = (1.71...5.5) V	1300	--	--	ns
t_{HD_STA}	Start Hold Time	V_{DD} = (1.71...5.5) V	600	--	--	ns
t_{SU_STA}	Start Set-up Time	V_{DD} = (1.71...5.5) V	600	--	--	ns
t_{HD_DAT}	Data Hold Time	V_{DD} = (1.71...5.5) V	0	--	--	ns
t_{SU_DAT}	Data Set-up Time	V_{DD} = (1.71...5.5) V	100	--	--	ns
t_R	Inputs Rise Time	V_{DD} = (1.71...5.5) V	--	--	300	ns
t_F	Inputs Fall Time	V_{DD} = (1.71...5.5) V	--	--	300	ns
t_{SU_STO}	Stop Set-up Time	V_{DD} = (1.71...5.5) V	600	--	--	ns
t_{DH}	Data Out Hold Time	V_{DD} = (1.71...5.5) V	50	--	--	ns