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SLG46620

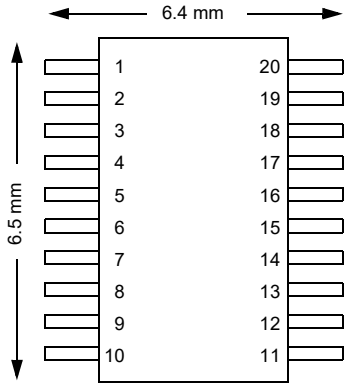
GreenPAK
Programmable Mixed-signal Matrix

Features

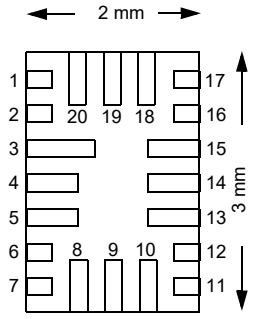
- Logic & Mixed Signal Circuits
- Highly Versatile Macrocells
- Read Back Protection (Read Lock)
- 1.8V (±5%) to 5V (±10%) Supply
- Operating Temperature Range: -40°C to 85°C
- RoHS Compliant / Halogen-Free
- 20-pin STQFN: 2 x 3 x 0.55 mm, 0.4 mm pitch
- 20-pin TSSOP: 6.5 x 6.4 x 1.2 mm, 0.65 mm pitch

Applications

- Personal Computers and Servers
- PC Peripherals
- Consumer Electronics
- Data Communications Equipment
- Handheld and Portable Electronics

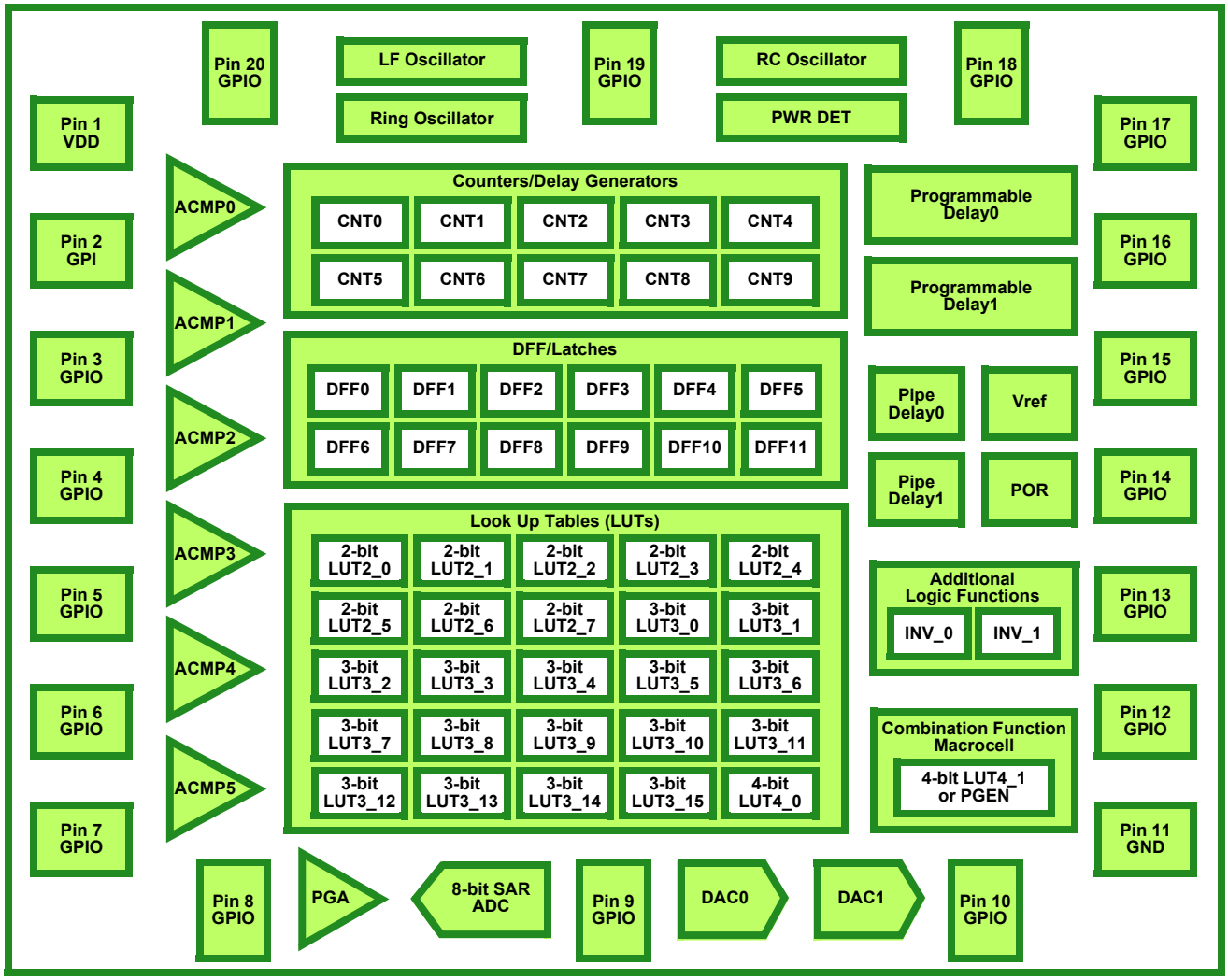


TSSOP-20
(Top View)



STQFN-20
(Top View)

Block Diagram



1.0 Overview

The SLG46620 provides a small, low power component for commonly used mixed-signal functions. The user creates their circuit design by programming the one time Non-Volatile Memory (NVM) to configure the interconnect logic, the I/O Pins and the macrocells of the SLG46620. This highly versatile device allows a wide variety of mixed-signal functions to be designed within a very small, low power single integrated circuit. The macrocells in the device include the following:

- 8-bit Successive Approximation Register Analog-to-Digital Converter (SAR ADC)
- ADC 3-bit Programmable Gain Amplifier (PGA)
- Two Digital-to-Analog Converters (DAC)
- Six Analog Comparators (ACMP)
- Two Voltage References (VREF)
- Twenty Five Combinatorial Look Up Tables (LUTs)
  - Eight 2-bit LUTs
  - Sixteen 3-bit LUTs
  - One 4-bit LUT
- One Combination Function Marcocells
  - Pattern Generator or 4-bit LUT
- Three Digital Comparators/Pulse Width Modulators (DCMPs /PWMs) w/ Selectable Deadband
- Ten Counters/Delays (CNT/DLY)
  - Two 14-bit Delay/Counter
  - One 14-bit Delay/Counter (Wake-Sleep Control)
  - One 14-bit Delay/Counter/Finite State Machine
  - Five 8-bit Delay/Counter
  - One 8-bit Delay/Counter/Finite State Machine
- Twelve D Flip-flops/Latches
- Two Pipe Delays – 16 stage/2 output
- Two Programmable Delays w/ Edge Detection
- Three Internal Oscillators
  - Low-Frequency
  - Ring
  - RC 25 kHz and 2 MHz
- Power-On-Reset (POR)
- Two Bandgaps
- Slave SPI

2.0 Pin Description

2.1 Functional Pin Description

Pin #	Pin Name	Function
1	VDD	Power Supply
2	GPI	General Purpose Input External Reset ADC CLK
3	GPIO	General Purpose I/O with OE ACMP4(+)
4	GPIO	General Purpose I/O ACMP5(+)
5	GPIO	General Purpose I/O with OE ACMP5 (-)
6	GPIO	General Purpose I/O ACMP0(+) / ACMP1(+) / ACMP2(+) / ACMP3(+) / ACMP4(+)
7	GPIO	General Purpose I/O with OE ACMP0(-) / ACMP1(-) / PGA_OUT
8	GPIO	General Purpose I/O POR_O PGA(+)
9	GPIO	General Purpose I/O with OE PGA(-)
10	GPIO	General Purpose I/O with OE ACMP0(-) / ACMP1(-) / ACMP2(-) / ACMP3(-) / ACMP4(-) 4X Drive I/O
11	GND	Ground
12	GPIO	General Purpose I/O ACMP1(+) 4X Drive I/O
13	GPIO	General Purpose I/O with OE ACMP2(+) / ACMP3(+)
14	GPIO	General Purpose I/O with OE ACMP2(-)
15	GPIO	General Purpose I/O ACMP3(+) / ACMP4(+)
16	GPIO	General Purpose I/O with OE AIN MUX/CNT TESTO
17	GPIO	General Purpose I/O ADC Vref_IO
18	GPIO	General Purpose I/O with OE VrefO_2
19	GPIO	General Purpose I/O with OE VrefO_ 1
20	GPIO	General Purpose I/O

3.0 User Programmability

Non-volatile memory (NVM) is used to configure the SLG46620's connection matrix routing and macrocells. The NVM is One-Time-Programmable (OTP). However, Silego's GreenPAK development tools can be used to configure the connection matrix and macrocells, without programming the NVM, to allow on-chip emulation. This configuration will remain active on the device as long as it remains powered and can be re-written as needed to facilitate rapid design changes.

When a design is ready for in-circuit testing, the same GreenPAK development tools can be used to program the NVM and create samples for small quantity builds. Once the NVM is programmed, the device will retain this configuration for the duration of its lifetime.

Once the design is finalized, the design file can be forwarded to Silego to integrate into the production process.

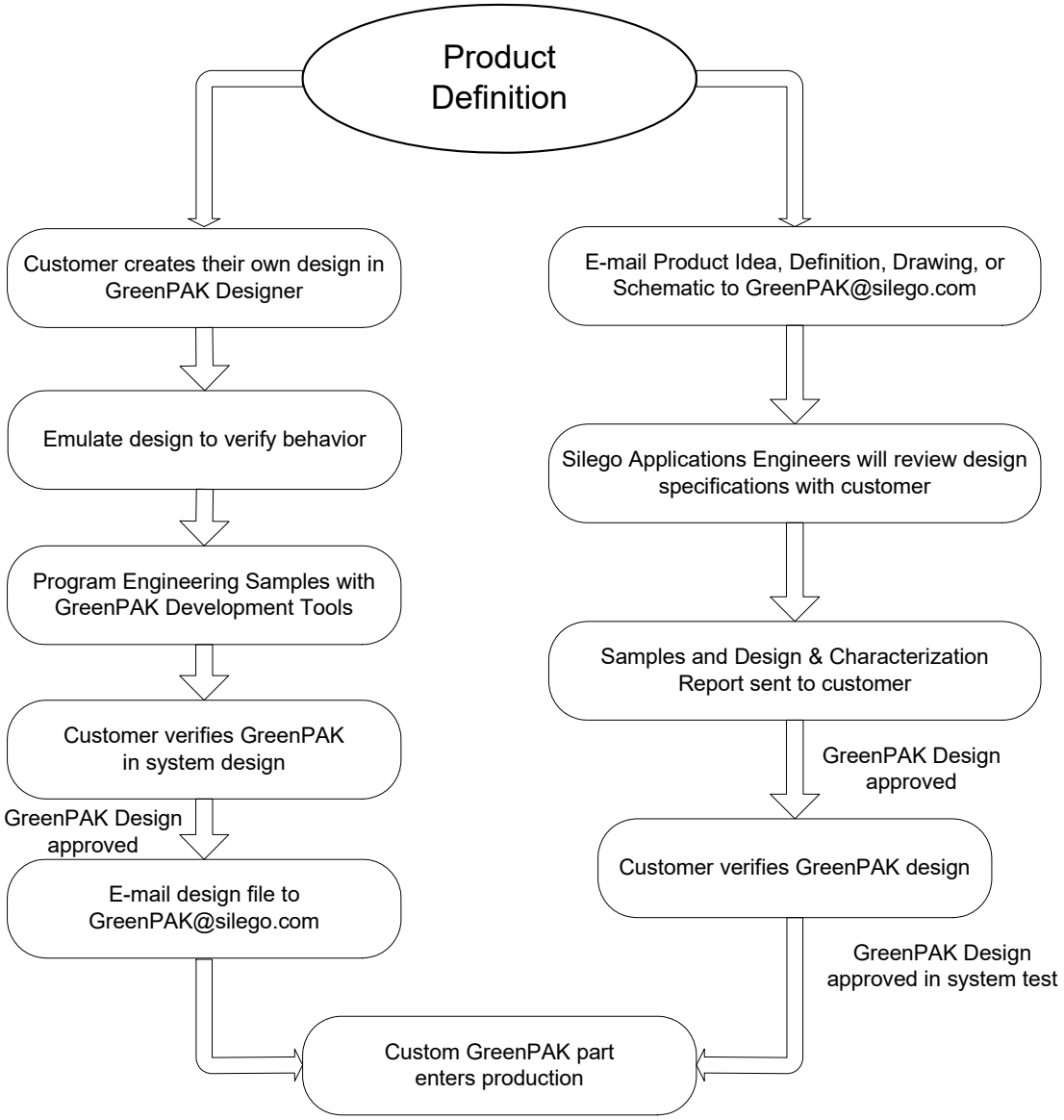


Figure 1. Steps to create a custom Silego GreenPAK device

4.0 Ordering Information

Part Number	Type
SLG46620V	20-pin STQFN
SLG46620VTR	20-pin STQFN - Tape and Reel (3k units)
SLG46620G	20-pin TSSOP
SLG46620GTR	20-pin TSSOP Tape and Reel (4k units)

5.0 Electrical Specifications

5.1 Absolute Maximum Conditions

Parameter		Min.	Max.	Unit
Supply voltage on VDD relative to GND		-0.5	7	V
DC Input voltage		GND - 0.5	VDD + 0.5	V
PGA Input voltage*	Single-ended	--	1.98/G	V
	Differential	--	(1.98 - 0.55)/G	V
	Pseudo-differential	--	(1.98 - 0.18)/G	V
Maximum Average or DC Current (Through pin)	Push-Pull 1x	--	10	mA
	Push-Pull 2x	--	14	
	Push-Pull 4x	--	28	
	OD 1x	--	14	
	OD 2x	--	27	
	OD 4x	--	46	
Current at Input Pin		-1.0	1.0	mA
Storage Temperature Range		-65	150	°C
Junction Temperature		--	150	°C
ESD Protection (Human Body Model)		2000	--	V
ESD Protection (Charged Device Model)		500	--	V
Moisture Sensitivity Level		1		

Note: IN+ relative to GND in Single-ended mode, IN+ and IN- relative to each other in Differential and Pseudo-differential modes.*

5.2 Electrical Characteristics (1.8V ±5% V_{DD})

Symbol	Parameter	Condition/Note	Min.	Typ.	Max.	Unit
V_{DD}	Supply Voltage		1.71	1.80	1.89	V
I_Q	Quiescent Current	Static Inputs and Outputs, all macrocells disabled	--	0.28	--	µA
T_A	Operating Temperature		-40	25	85	°C
V_{PP}	Programming Voltage		7.25	7.50	7.75	V
V_{ACMP}	ACMP Input Voltage Range	Positive Input	0	--	V_{DD}	V
		Negative Input	0	--	1.1	V
V_{IH}	HIGH-Level Input Voltage	Logic Input	1.087	--	V_{DD}	V
		Logic Input with Schmitt Trigger	1.296	--	V_{DD}	V
		Low-Level Logic Input	0.894	--	V_{DD}	V
V_{IL}	LOW-Level Input Voltage	Logic Input	0	--	0.759	V
		Logic Input with Schmitt Trigger	0	--	0.562	V
		Low-Level Logic Input	0	--	0.557	V
V_{HYS}	Schmitt Trigger Hysteresis Voltage	Logic Input with Schmitt Trigger	0.261	0.382	0.521	V

Symbol	Parameter	Condition/Note	Min.	Typ.	Max.	Unit
I_{LKG} (Absolute Value)	ACMP Input Leakage	Vin = 0 V	--	0.05	0.29	nA
		Vin = VDD	--	0.12	0.92	nA
	PGA Input Leakage	Vin = 0 V	--	0.03	0.13	nA
		Vin = VDD	--	0.10	0.49	nA
	Logic Input without Schmitt Trigger (Floating) Leakage	Vin = 0 V	--	0.03	0.39	nA
		Vin = VDD	--	4.02	142.92	nA
	Logic Input with Schmitt Trigger (Floating) Leakage	Vin = 0 V	--	0.03	0.24	nA
		Vin = VDD	--	4.04	143.85	nA
	Low-Level Logic Input (Floating) Leakage	Vin = 0 V	--	0.03	0.23	nA
		Vin = VDD	--	4.03	143.76	nA
V_{OH}	HIGH-Level Output Voltage	Push-Pull 1X, Open Drain PMOS 1X, I_{OH} = 100 µA	1.680	1.788	--	V
		Push-Pull 2X, Open Drain PMOS 2X, I_{OH} = 100 µA	1.685	1.793	--	V
		Push-Pull 4X, Open Drain PMOS 4X, I_{OH} = 100 µA	1.697	1.799	--	V
V_{OL}	LOW-Level Output Voltage	Push-Pull 1X, I_{OL}= 100 µA	--	0.010	0.015	V
		Push-Pull 2X, I_{OL} = 100 µA	--	0.007	0.010	V
		Push-Pull 4X, I_{OL} = 100 µA	--	0.004	0.015	V
		Open Drain NMOS 1X, I_{OL} = 100 µA	--	0.007	0.010	V
		Open Drain NMOS 2X, I_{OL} = 100 µA	--	0.003	0.010	V
		Open Drain NMOS 4X, I_{OL} = 100 µA	--	0.001	0.004	V
I_{OH}	HIGH-Level Output Pulse Current (see Note 1)	Push-Pull 1X,Open Drain PMOS 1X, $V_{OH} = V_{DD}$ - 0.2	1.027	1.703	--	mA
		Push-Pull 2X, Open Drain PMOS 2X, $V_{OH} = V_{DD}$ - 0.2	2.025	3.406	--	mA
		Push-Pull 4X, Open Drain PMOS 4X, $V_{OH} = V_{DD}$ - 0.2	3.916	6.759	--	mA
I_{OL}	LOW-Level Output Pulse Current (see Note 1)	Push-Pull 1X, V_{OL} = 0.15 V	0.917	1.660	--	mA
		Push-Pull 2X, V_{OL} = 0.15 V	1.834	3.285	--	mA
		Push-Pull 4X, V_{OL} = 0.15 V	4.807	6.495	--	mA
		Open Drain NMOS 1X, V_{OL} = 0.15 V	1.375	2.534	--	mA
		Open Drain NMOS 2X, V_{OL} = 0.15 V	2.750	5.068	--	mA
		Open Drain NMOS 4X, V_{OL} = 0.15 V	5.500	10.136	--	mA

Symbol	Parameter	Condition/Note	Min.	Typ.	Max.	Unit
I_{VDD}	Maximum Average or DC Current Through VDD Pin (Per chip side, see Note 2)	T_J = 85°C	--	--	45	mA
		T_J = 110°C	--	--	21	mA
I_{GND}	Maximum Average or DC Current Through GND Pin (Per chip side, see Note 2)	T_J = 85°C	--	--	69	mA
		T_J = 110°C	--	--	33	mA
V_O	Maximal Voltage Applied to any PIN in High-Impedance State		--	--	V_{DD}	V
T_{SU}	Startup Time (see Note 3)	from VDD rising past PON_{THR}	0.526	1.4	5.148	ms
PON_{THR}	Power On Threshold	V_{DD} Level Required to Start Up the Chip	0.950	1.462	1.705	V
$POFF_{THR}$	Power Off Threshold	V_{DD} Level Required to Switch Off the Chip	0.935	1.103	1.281	V
R_{PUP}	Pull Up Resistance	1 M Pull Up	874.85	1059.7	1259.94	kΩ
		100 k Pull Up	88.47	106.37	126.89	kΩ
		10 k Pull Up	10.35	12.19	14.99	kΩ
R_{PDWN}	Pull Down Resistance	1 M Pull Down	664.26	1050.75	1275.36	kΩ
		100 k Pull Down	88.17	106.61	131.27	kΩ
		10 k Pull Down	10.08	12.0	15.87	kΩ

Note 1: DC or average current through any pin should not exceed value given in Absolute Maximum Conditions.
Note 2: The GreenPAK's power rails are divided in two sides. Pins 2, 3, 4, 5, 6, 7, 8, 9 and 10 are connected to one side, pins 12, 13, 14, 15, 16, 17, 18, 19 and 20 to another.
Note 3: VDD ramp rising speed must be less than 0.6 V/µs after power on. Violating this specification may cause chip to restart.

5.3 Electrical Characteristics (3.3V ±10% V_{DD})

Symbol	Parameter	Condition/Note	Min.	Typ.	Max.	Unit
V_{DD}	Supply Voltage		3.0	3.3	3.6	V
I_Q	Quiescent Current	Static Inputs and Outputs, all macrocells disabled	--	0.37	--	µA
T_A	Operating Temperature		-40	25	85	°C
V_{PP}	Programming Voltage		7.25	7.50	7.75	V
V_{ACMP}	ACMP Input Voltage Range	Positive Input	0	--	V_{DD}	V
		Negative Input	0	--	1.2	V
V_{IH}	HIGH-Level Input Voltage	Logic Input	1.949	--	V_{DD}	V
		Logic Input with Schmitt Trigger	2.239	--	V_{DD}	V
		Low-Level Logic Input	1.059	--	V_{DD}	V
V_{IL}	LOW-Level Input Voltage	Logic Input	0	--	1.286	V
		Logic Input with Schmitt Trigger	0	--	1.150	V
		Low-Level Logic Input	0	--	0.686	V
V_{HYS}	Schmitt Trigger Hysteresis Voltage	Logic Input with Schmitt Trigger	0.326	0.469	0.599	V
I_{LKG} (Absolute Value)	ACMP Input Leakage	Vin = 0 V	--	0.30	1.38	nA
		Vin = VDD	--	0.19	1.40	nA
	PGA Input Leakage	Vin = 0 V	--	0.25	0.81	nA
		Vin = VDD	--	0.15	0.75	nA
	Logic Input without Schmitt Trigger (Floating) Leakage	Vin = 0 V	--	0.27	2.11	nA
		Vin = VDD	--	4.45	0.17	nA
	Logic Input with Schmitt Trigger (Floating) Leakage	Vin = 0 V	--	0.27	1.68	nA
		Vin = VDD	--	4.42	173.37	nA
	Low-Level Logic Input (Floating) Leakage	Vin = 0 V	--	0.24	2.24	nA
		Vin = VDD	--	4.37	172.95	nA
V_{OH}	HIGH-Level Output Voltage	Push-Pull 1X, Open Drain PMOS 1X, I_{OH} = 3 mA	2.713	3.095	--	V
		Push-Pull 2X, Open Drain PMOS 2X, I_{OH} = 3 mA	2.858	3.199	--	V
		Push-Pull 4X, Open Drain PMOS 4X, I_{OH} = 3 mA	2.925	3.244	--	V
V_{OL}	LOW-Level Output Voltage	Push-Pull 1X, I_{OL}= 3 mA	--	0.148	0.228	V
		Push-Pull 2X, I_{OL}= 3 mA	--	0.073	0.108	V
		Push-Pull 4X, I_{OL}= 3 mA	--	0.052	0.098	V
		Open Drain NMOS 1X, I_{OL}= 3 mA	--	0.080	0.147	V
		Open Drain NMOS 2X, I_{OL}= 3 mA	--	0.040	0.071	V
		Open Drain NMOS 4X, I_{OL}= 3 mA	--	0.013	0.021	V

Symbol	Parameter	Condition/Note	Min.	Typ.	Max.	Unit
I_{OH}	HIGH-Level Output Pulse Current (see Note 1)	Push-Pull 1X, Open Drain PMOS 1X, V_{OH} = 2.4 V	5.608	10.774	--	mA
		Push-Pull 2X, Open Drain PMOS 2X, V_{OH} = 2.4 V	11.015	21.100	--	mA
		Push-Pull 4X, Open Drain PMOS 4X, V_{OH} = 2.4 V	20.752	39.176	--	mA
I_{OL}	LOW-Level Output Pulse Current (see Note 1)	Push-Pull 1X, V_{OL} = 0.4 V	4.875	7.795	--	mA
		Push-Pull 2X, V_{OL} = 0.4 V	9.750	15.243	--	mA
		Push-Pull 4X, V_{OL} = 0.4 V	20.217	29.887	--	mA
		Open Drain NMOS 1X, V_{OL} = 0.4 V	7.313	12.370	--	mA
		Open Drain NMOS 2X, V_{OL} = 0.4 V	14.626	24.740	--	mA
		Open Drain NMOS 4X, V_{OL} = 0.4 V	29.250	49.480	--	mA
I_{VDD}	Maximum Average or DC Current Through VDD Pin (Per chip side, see Note 2)	T_J = 85°C	--	--	45	mA
		T_J = 110°C	--	--	21	mA
I_{GND}	Maximum Average or DC Current Through GND Pin (Per chip side, see Note 2)	T_J = 85°C	--	--	69	mA
		T_J = 110°C	--	--	33	mA
V_O	Maximal Voltage Applied to any PIN in High-Impedance State		--	--	V_{DD}	V
T_{SU}	Startup Time (see Note 3)	from VDD rising past PON_{THR}	0.660	1.4	3.740	ms
PON_{THR}	Power On Threshold	V_{DD} Level Required to Start Up the Chip	0.953	1.462	1.707	V
$POFF_{THR}$	Power Off Threshold	V_{DD} Level Required to Switch Off the Chip	0.935	1.103	1.281	V
R_{PUP}	Pull Up Resistance	1 M Pull Up	875.91	1059.16	1264.91	kΩ
		100 k Pull Up	86.57	105.72	126.22	kΩ
		10 k Pull Up	9.25	11.10	14.57	kΩ
R_{PDWN}	Pull Down Resistance	1 M Pull Down	666.16	1056.79	1261.68	kΩ
		100 k Pull Down	87.41	105.89	130.8	kΩ
		10 k Pull Down	8.97	11.02	14.31	kΩ

Note 1: DC or average current through any pin should not exceed value given in Absolute Maximum Conditions.
Note 2: The GreenPAK's power rails are divided in two sides. Pins 2, 3, 4, 5, 6, 7, 8, 9 and 10 are connected to one side, pins 12, 13, 14, 15, 16, 17, 18, 19 and 20 to another.
Note 3: VDD ramp rising speed must be less than 0.6 V/µs after power on. Violating this specification may cause chip to restart.

5.4 Electrical Characteristics (5V ±10% V_{DD})

Symbol	Parameter	Condition/Note	Min.	Typ.	Max.	Unit
V_{DD}	Supply Voltage		4.5	5.0	5.5	V
I_Q	Quiescent Current	Static Inputs and Outputs, all macrocells disabled	--	0.47	--	µA
T_A	Operating Temperature		-40	25	85	°C
V_{PP}	Programming Voltage		7.25	7.50	7.75	V
V_{ACMP}	ACMP Input Voltage Range	Positive Input	0	--	V_{DD}	V
		Negative Input	0	--	1.2	V
V_{IH}	HIGH-Level Input Voltage	Logic Input	2.930	--	V_{DD}	V
		Logic Input with Schmitt Trigger	3.333	--	V_{DD}	V
		Low-Level Logic Input	1.157	--	V_{DD}	V
V_{IL}	LOW-Level Input Voltage	Logic Input	0	--	1.910	V
		Logic Input with Schmitt Trigger	0	--	1.778	V
		Low-Level Logic Input	0	--	0.776	V
V_{HYS}	Schmitt Trigger Hysteresis Voltage	Logic Input with Schmitt Trigger	0.425	0.571	0.799	V
I_{LKG} (Absolute Value)	ACMP Input Leakage	Vin = 0 V	--	0.30	1.38	nA
		Vin = VDD	--	0.19	1.40	nA
	PGA Input Leakage	Vin = 0 V	--	0.25	0.81	nA
		Vin = VDD	--	0.15	0.75	nA
	Logic Input without Schmitt Trigger (Floating) Leakage	Vin = 0 V	--	0.27	2.11	nA
		Vin = VDD	--	4.45	172.97	nA
	Logic Input with Schmitt Trigger (Floating) Leakage	Vin = 0 V	--	0.27	1.68	nA
		Vin = VDD	--	4.42	173.37	nA
	Low-Level Logic Input (Floating) Leakage	Vin = 0 V	--	0.24	2.24	nA
		Vin = VDD	--	4.37	172.95	nA
V_{OH}	HIGH-Level Output Voltage	Push-Pull 1X,Open Drain PMOS 1X, I_{OH} = 5 mA	4.159	4.750	--	V
		Push-Pull 2X, Open Drain PMOS 2X, I_{OH} = 5 mA	4.324	4.872	--	V
		Push-Pull 4X, Open Drain PMOS 4X, I_{OH} = 5 mA	4.405	4.930	--	V
V_{OL}	LOW-Level Output Voltage	Push-Pull 1X, I_{OL}= 5 mA	--	0.189	0.270	V
		Push-Pull 2X, I_{OL}= 5 mA	--	0.098	0.131	V
		Push-Pull 4X, I_{OL}= 5 mA	--	0.068	0.131	V
		Open Drain NMOS 1X, I_{OL}= 5 mA	--	0.102	0.180	V
		Open Drain NMOS 2X, I_{OL}= 5 mA	--	0.051	0.090	V
		Open Drain NMOS 4X, I_{OL}= 5 mA	--	0.020	0.028	V

Symbol	Parameter	Condition/Note	Min.	Typ.	Max.	Unit
I_{OH}	HIGH-Level Output Pulse Current (see Note 1)	Push-Pull 1X, Open Drain PMOS 1X, V_{OH} = 2.4 V	20.337	30.010	--	mA
		Push-Pull 2X, Open Drain PMOS 2X, V_{OH} = 2.4 V	39.270	58.446	--	mA
		Push-Pull 4X, Open Drain PMOS 4X, V_{OH} = 2.4 V	74.110	109.086	--	mA
I_{OL}	LOW-Level Output Pulse Current (see Note 1)	Push-Pull 1X, V_{OL} = 0.4 V	6.996	10.438	--	mA
		Push-Pull 2X, V_{OL} = 0.4 V	13.275	20.241	--	mA
		Push-Pull 4X, V_{OL} = 0.4 V	26.739	39.313	--	mA
		Open Drain NMOS 1X, V_{OL} = 0.4 V	10.820	17.380	--	mA
		Open Drain NMOS 2X, V_{OL} = 0.4 V	21.640	34.760	--	mA
		Open Drain NMOS 4X, V_{OL} = 0.4 V	43.290	69.520	--	mA
I_{VDD}	Maximum Average or DC Current Through VDD Pin (Per chip side, see Note 2)	T_J = 85°C	--	--	45	mA
		T_J = 110°C	--	--	21	mA
I_{GND}	Maximum Average or DC Current Through GND Pin (Per chip side, see Note 2)	T_J = 85°C	--	--	69	mA
		T_J = 110°C	--	--	33	mA
V_O	Maximal Voltage Applied to any PIN in High-Impedance State		--	--	V_{DD}	V
T_{SU}	Startup Time (see Note 3)	from VDD rising past PON_{THR}	0.638	1.4	2.914	ms
PON_{THR}	Power On Threshold	V_{DD} Level Required to Start Up the Chip	0.959	1.462	1.708	V
$POFF_{THR}$	Power Off Threshold	V_{DD} Level Required to Switch Off the Chip	0.935	1.103	1.281	V
R_{PUP}	Pull Up Resistance	1 M Pull Up	876.51	1059.03	1260.4	kΩ
		100 k Pull Up	86.43	105.49	126.14	kΩ
		10 k Pull Up	8.44	10.61	14.88	kΩ
R_{PDWN}	Pull Down Resistance	1 M Pull Down	666.45	1057.43	1266.07	kΩ
		100 k Pull Down	87.1	105.64	130.48	kΩ
		10 k Pull Down	8.23	10.54	13.36	kΩ

Note 1: DC or average current through any pin should not exceed value given in Absolute Maximum Conditions.
Note 2: The GreenPAK's power rails are divided in two sides. Pins 2, 3, 4, 5, 6, 7, 8, 9 and 10 are connected to one side, pins 12, 13, 14, 15, 16, 17, 18, 19 and 20 to another.
Note 3: VDD ramp rising speed must be less than 0.6 V/µs after power on. Violating this specification may cause chip to restart.

5.5 Typical Delay Estimated for Each Macrocell

Table 1. Typical Delay Estimated for Each Macrocell

Symbol	Parameter	Note	V_{DD} = 1.8 V		V_{DD} = 3.3V		V_{DD} = 5.0V		Unit
			rising	falling	rising	falling	rising	falling	
tpd	Delay	LUT 2-bit	16.79	15.32	6.37	5.92	4.35	4.18	ns
tpd	Delay	LUT 3-bit	17.89	15.93	6.81	6.22	4.64	4.40	ns
tpd	Delay	LUT 4-bit	19.44	16.86	7.43	6.61	4.98	4.61	ns
tpd	Delay	LUT 4-bit (Shared)	23.75	22.71	9.09	8.88	6.26	6.33	ns
tpd	Delay	DFF	21.56	25.33	8.95	9.12	6.39	6.21	ns
tpd	Delay	DFF nReset	--	26.05	--	10.15	--	7.33	ns
tpd	Delay	DFF nSet	--	27.25	--	10.58	--	7.64	ns
tpd	Delay	CNT/DLY opposite to selected edge delay	46.62	41.53	19.26	17.60	13.17	12.82	ns
tpd	Delay	CNT/DLY (Shared) opposite to selected Edge Delay	47.40	40.50	18.90	17.16	12.92	12.56	ns
tpd	Delay	CNT/DLY Both Edge Detect	51.46	52.6	21.43	21.21	14.98	15	ns
tpd	Delay	CNT/DLY Rising Edge Detect	53.82	--	22.73	--	15.91	--	ns
tpd	Delay	CNT/DLY Falling Edge Detect	--	55.71	--	22.61	--	15.97	ns
tw	Width	CNT/DLY Both Edge Detect	30.16	30.19	13.75	13.75	9.77	9.76	ns
tw	Width	CNT/DLY Rising Edge Detect	30.79	--	13.91	--	9.78	--	ns
tw	Width	CNT/DLY Falling Edge Detect	--	29.32	--	13.55	--	9.55	ns
tpd	Delay	Latch	20.47	22.27	8.48	8.50	5.98	6.21	ns
tpd	Delay	Latch nReset	--	27.95	--	10.98	--	7.96	ns
tpd	Delay	Latch nSet	--	24.86	--	9.60	--	6.96	ns
tpd	Delay	Pipe Delay	32.75	33.91	13.46	12.85	9.51	9.03	ns
tpd	Delay	Pipe Delay nReset	--	35.04	--	14.76	--	11.12	ns
tpd	Delay	PGEN (Shared)	21.94	23.54	8.58	8.94	5.97	6.28	ns
tpd	Delay	PGEN (Shared) nReset to 0	--	23.46	--	8.84	--	6.24	ns
tpd	Delay	PGEN (Shared) nReset to 1	21.70	--	8.46	--	5.95	--	ns
tpd	Delay	PDLY0 1 Cells Both Edge Delay	373.01	374.69	165.49	166.405	120.49	122.21	ns
tpd	Delay	PDLY0 1 Cells Both Edge Detect	29.52	31.79	11.93	12.055	8.26	8.675	ns
tpd	Delay	PDLY0 1 Cells delayed output Both Edge Detect	189.96	192.09	75.25	76.385	48.42	48.735	ns
tpd	Delay	PDLY0 1 Cells delayed output Rising Edge Detect	190.51	--	75.49	--	48.47	--	ns
tpd	Delay	PDLY0 1 Cells delayed output Falling Edge Detect	--	192.49	--	75.955	--	48.75	ns
tpd	Delay	PDLY0 1 Cells Rising Edge Detect	30.12	--	12.27	--	8.48	--	ns
tpd	Delay	PDLY0 1 Cells Falling Edge Detect	--	32.03	--	12.195	--	8.755	ns
tpd	Delay	PDLY0 2 Cells Both Edge Delay	711.16	712.99	317.04	318.305	231.71	233.4	ns
tpd	Delay	PDLY0 2 Cells Both Edge Detect	29.44	31.79	12	12.095	8.24	8.655	ns
tpd	Delay	PDLY0 2 Cells delayed output Both Edge Detect	344.86	346.84	137.37	137.745	87.34	88.14	ns
tpd	Delay	PDLY0 2 Cells delayed output Rising Edge Detect	345.71	--	137.49	--	87.51	--	ns

Table 1. Typical Delay Estimated for Each Macrocell

Symbol	Parameter	Note	V_{DD} = 1.8 V		V_{DD} = 3.3V		V_{DD} = 5.0V		Unit
			rising	falling	rising	falling	rising	falling	
tpd	Delay	PDLY0 2 Cells delayed output Falling Edge Detect	--	347.14	--	137.505	--	88.15	ns
tpd	Delay	PDLY0 2 Cells Rising Edge Detect	30	--	12.29	--	8.51	--	ns
tpd	Delay	PDLY0 2 Cells Falling Edge Detect	--	32.05	--	12.205	--	8.75	ns
tpd	Delay	PDLY0 3 Cells Both Edge Delay	1050.51	1052.99	468.94	470.605	342.81	344.6	ns
tpd	Delay	PDLY0 3 Cells Both Edge Detect	29.46	31.77	11.97	12.095	8.24	8.655	ns
tpd	Delay	PDLY0 3 Cells delayed output Both Edge Detect	502.51	504.39	199.64	200.405	126.61	126.99	ns
tpd	Delay	PDLY0 3 Cells delayed output Rising Edge Detect	503.36	--	199.74	--	126.96	--	ns
tpd	Delay	PDLY0 3 Cells delayed output Falling Edge Detect	--	504.74	--	200.405	--	126.95	ns
tpd	Delay	PDLY0 3 Cells Rising Edge Detect	30.15	--	12.29	--	8.56	--	ns
tpd	Delay	PDLY0 3 Cells Falling Edge Detect	--	32.01	--	12.165	--	8.74	ns
tpd	Delay	PDLY0 4 Cells Both Edge Delay	1390.01	1391.99	620.74	622.155	453.91	455.35	ns
tpd	Delay	PDLY0 4 Cells Both Edge Detect	29.42	31.77	12.02	12.085	8.25	8.65	ns
tpd	Delay	PDLY0 4 Cells delayed output Both Edge Detect	656.81	658.84	261.39	261.655	165.71	166.15	ns
tpd	Delay	PDLY0 4 Cells delayed output Rising Edge Detect	657.56	--	261.74	--	166.01	--	ns
tpd	Delay	PDLY0 4 Cells delayed output Falling Edge Detect	--	659.29	--	261.855	--	166.25	ns
tpd	Delay	PDLY0 4 Cells Rising Edge Detect	30.18	--	12.27	--	8.47	--	ns
tpd	Delay	PDLY0 4 Cells Falling Edge Detect	--	32.03	--	12.215	--	8.77	ns
tw	Width	PDLY0 1 Cells Both Edge Detect Rising pulse	339.9	341.15	153.7	76.85	112.66	113.2	ns
tw	Width	PDLY0 1 Cells delayed output Both Edge Detect Rising pulse	338.35	339.55	152.45	76.225	111.48	112.14	ns
tw	Width	PDLY0 1 Cells delayed output Rising Edge Detect Rising pulse	338.2	--	152.7	--	111.6	--	ns
tw	Width	PDLY0 1 Cells delayed output Falling Edge Detect Falling pulse	--	339.60	--	76.35	--	112.34	ns
tw	Width	PDLY0 1 Cells Rising Edge Detect Rising pulse	340.2	--	153.7	--	112.66	--	ns
tw	Width	PDLY0 1Cells Falling Edge Detect Falling pulse	--	341.00	--	76.85	--	113.08	ns
tw	Width	PDLY0 2 Cells Both Edge Detect Rising pulse	678.3	679.50	305.3	152.65	223.9	224.6	ns
tw	Width	PDLY0 2 Cells delayed output Both Edge Detect Rising pulse	682.1	683.75	302.65	151.325	220.85	221.2	ns
tw	Width	PDLY0 2 Cells delayed output Rising Edge Detect Rising pulse	682.25	--	302.8	--	220.8	--	ns

Table 1. Typical Delay Estimated for Each Macrocell

Symbol	Parameter	Note	V_{DD} = 1.8 V		V_{DD} = 3.3V		V_{DD} = 5.0V		Unit
			rising	falling	rising	falling	rising	falling	
tw	Width	PDLY0 2 Cells delayed output Falling Edge Detect Falling pulse	--	683.65	--	151.4	--	221.2	ns
tw	Width	PDLY0 2 Cells Rising Edge Detect Rising pulse	678.3	--	305.35	--	224.05	--	ns
tw	Width	PDLY0 2 Cells Falling Edge Detect Falling pulse	--	679.35	--	152.675	--	224.7	ns
tw	Width	PDLY0 3 Cells Both Edge Detect Rising pulse	1017.3	1019.45	457	228.5	335.4	335.95	ns
tw	Width	PDLY0 3 Cells delayed output Both Edge Detect Rising pulse	1018.9	1021.55	452.35	226.175	332.3	333.3	ns
tw	Width	PDLY0 3 Cells delayed output Rising Edge Detect Rising pulse	1019.4	--	452.43	--	332.3	--	ns
tw	Width	PDLY0 3 Cells delayed output Falling Edge Detect Falling pulse	--	1021.30	--	226.2125	--	333.03	ns
tw	Width	PDLY0 3 Cells Rising Edge Detect Rising pulse	1017.45	--	457	--	335.45	--	ns
tw	Width	PDLY0 3 Cells Falling Edge Detect Falling pulse	--	1019.1	--	228.5	--	336	ns
tw	Width	PDLY0 4 Cells Both Edge Detect Rising pulse	1355.95	1358.5	608.75	304.375	446.5	447.1	ns
tw	Width	PDLY0 4 Cells delayed output Both Edge Detect Rising pulse	1362.55	1365.3	604.05	302.025	442.35	443.4	ns
tw	Width	PDLY0 4 Cells delayed output Rising Edge Detect Rising pulse	1362.95	--	604.1	--	442.275	--	ns
tw	Width	PDLY0 4 Cells delayed output Falling Edge Detect Falling pulse	--	1365.15	--	302.05	--	443.4	ns
tw	Width	PDLY0 4 Cells Rising Edge Detect Rising pulse	1356.15	--	609.05	--	446.6	--	ns
tw	Width	PDLY0 4 Cells Falling Edge Detect Falling pulse	--	1358.05	--	304.525	--	447.05	ns
tpd	Delay	Inverter (INV)	13.62	16.63	5.81	5.72	4.28	3.71	ns
tpd	Delay	Matrix Cross Connector	15.62	13.76	5.90	5.33	4.06	4.23	ns
tpd	Delay	Digital Input without Schmitt trigger -- NMOS	--	34.31	--	14.06	--	9.85	ns
tpd	Delay	Digital Input without Schmitt trigger -- NMOS 2x	--	32.96	--	13.43	--	9.46	ns
tpd	Delay	Digital Input without Schmitt trigger -- PMOS	45.02	--	16.15	--	10.68	--	ns
tpd	Delay	Digital Input without Schmitt trigger -- PMOS 2x	41.31	--	14.86	--	10.26	--	ns
tpd	Delay	Digital Input with Schmitt Trigger -- Push Pull	43.5	38.99	17.02	16.07	10.76	11.05	ns
tpd	Delay	Low Voltage Digital Input -- Push Pull	43.58	352.00	16.67	142.75	10.29	94.5	ns
tpd	Delay	Digital Input without Schmitt trigger -- Push Pull 1x OE	42.09	37.96	16.07	14.16	10.95	10.21	ns
tpd	Delay	Digital Input without Schmitt trigger -- Push Pull 2x OE	40.33	36.57	15.51	13.99	10.61	9.66	ns

Table 1. Typical Delay Estimated for Each Macrocell

Symbol	Parameter	Note	V_{DD} = 1.8 V		V_{DD} = 3.3V		V_{DD} = 5.0V		Unit
			rising	falling	rising	falling	rising	falling	
tpd	Delay	Digital Input without Schmitt Trigger -- Push Pull 1x	42.77	38.56	16.59	15.83	10.40	10.85	ns
tpd	Delay	Digital Input without Schmitt Trigger -- Push Pull 2x	40.19	37.08	14.91	15.07	10.21	10.55	ns

5.6 Typical Current Consumption

Table 2. Typical Current Consumption

Condition	V_{DD} = 1.8 V	V_{DD} = 3.3V	V_{DD} = 5.0V	Unit
Quiescent current	0.28	0.37	0.47	µA
Low frequency OSC; Clock predivider by 1	0.76	0.89	1.13	µA
Low frequency OSC; Clock predivider by 16	0.74	0.87	1.06	µA
RC OSC 25 kHz; First Clock predivider by 1	5.26	6.02	7.24	µA
RC OSC 25 kHz; First Clock predivider by 8	5.02	5.54	6.45	µA
RC OSC 2 MHz; First Clock predivider by 1	37.47	63.46	96.11	µA
RC OSC 2 MHz; First Clock predivider by 8	18.79	25.22	34.25	µA
Ring OSC; First Clock predivider by 1	90.08	118.36	165.09	µA
Ring OSC; First Clock predivider by 16	63.28	65.39	81.12	µA
ACMP with Internal Vref; Hysteresis 0 mV/25 mV; Low bandwidth Disable; Input PIN6; Buffer 1k; Gain 1x	49.72	42.35	87.13	µA
ACMP with Internal Vref; Hysteresis 0 mV; Low bandwidth Disable; Input Buffered PIN6; Buffer 1k; Gain 1x	54.85	47.85	52.36	µA
ACMP with Internal Vref; Hysteresis 0 mV; Low bandwidth Disable; Input Buffered PIN6; Buffer 5k; Gain 1x	59.91	53.3	58.06	µA
ACMP with Internal Vref; Hysteresis 0 mV; Low bandwidth Disable; Input Buffered PIN6; Buffer 20k; Gain 1x	71.31	65.54	75.34	µA
ACMP with Internal Vref; Hysteresis 0 mV; Low bandwidth Disable; Input Buffered PIN6; Buffer 50k; Gain 1x	93.00	88.94	95.01	µA
ACMP with Internal Vref; Hysteresis 0 mV; Low bandwidth Disable; Input VDD; Buffer 1k	51.41	47.49	53.34	µA
ACMP with Internal Vref; Hysteresis 0 mV; Low bandwidth Disable; Input VDD; Buffer 1k; Gain 1x	51.53	44.23	48.39	µA
ACMP with Internal Vref; Hysteresis 0 mV/25 mV; Low bandwidth Enable; Input PIN6; Buffer 1k; Gain 1x	44.57	37.16	41.32	µA
Bandgap	38.97	31.31	35.47	µA
Bandgap + VREF0/1 output	81.93	75.28	79.42	µA
Bandgap + DAC0	50.52	43.13	47.28	µA
Bandgap + DAC1	64.92	57.86	62.01	µA
PGA; Single-end mode; Gain 0.25x; External output Disable	86.28	80.88	86.17	µA
PGA; Single-end mode; Gain 0.5x; External output Disable	86.31	80.92	86.21	µA
PGA; Single-end mode; Gain 1x	63.39	56.32	60.49	µA
PGA; Single-end mode; Gain 2x	91.84	81.25	86.55	µA
PGA; Single-end mode; Gain 4x	87.16	81.79	87.13	µA
ADC; Single-end mode; Vref: 1.2 V; Force analog part Enable; Speed selection 100 kHz + RC OSC 25kHz; First Clock predivider by 1; Sample rate 1.56 kHz	175.97	172.4	172.78	µA

Table 2. Typical Current Consumption

Condition	V_{DD} = 1.8 V	V_{DD} = 3.3V	V_{DD} = 5.0V	Unit
ADC; Single-end mode; Vref: 1.2 V; Force analog part Enable; Speed selection 100 kHz + RC OSC 25kHz; First Clock predivider by 16; Sample rate 97.66 Hz	176.12	172.69	177.92	µA
ADC; Single-end mode; Vref: 1.2 V; Force analog part Enable; Speed selection 100 kHz + RC OSC 2MHz; First Clock predivider by 16; Sample rate 7.81 kHz	207.59	229.92	267.06	µA
ADC; Single-end mode; Vref: 1.2 V; Force analog part Enable; Speed selection 100 kHz + RC OSC 2MHz; First Clock predivider by 1; Sample rate 125.00 kHz	214.75	247.22	297.04	µA
ADC; Single-end mode; Vref: 1.2 V; Force analog part Enable; Speed selection 100 kHz + Ring OSC; First Clock predivider by 16; Sample rate 106.45 kHz	271.72	349.02	460.02	µA
ADC; Single-end mode; Vref: 1.2 V; Force analog part Enable; Speed selection 100 kHz + Ring OSC; First Clock predivider by 1; Sample rate 1.70 MHz	306.18	431.52	868.35	µA

5.7 OSC Specifications

5.7.1 25 kHz RC Oscillator

Table 3. 25 kHz RC OSC frequency limits

Power Supply Range (VDD) V	Temperature Range					
	+25 °C		0 °C ... +85 °C		-40 °C ... +85 °C	
	Minimum Value, kHz	Maximum Value, kHz	Minimum Value, kHz	Maximum Value, kHz	Minimum Value, kHz	Maximum Value, kHz
1.8 V ±5%	24.182	25.836	23.503	26.544	21.862	28.504
3.3 V ±10%	24.829	25.185	24.113	25.974	23.435	26.331
5 V ±10%	24.631	25.533	24.026	26.065	23.323	26.321
2.5 V - 4.5 V	24.564	25.445	24.014	26.032	23.279	26.544
1.71 V….5.5 V	22.544	27.226	21.967	27.910	20.573	29.504

Table 4. 25 kHz RC OSC frequency error (error calculated relative to nominal value)

Power Supply Range (VDD) V	Temperature Range					
	+25 °C		0 °C ... +85 °C		-40 °C ... +85 °C	
	Error (% at Minimum)	Error (% at Maximum)	Error (% at Minimum)	Error (% at Maximum)	Error (% at Minimum)	Error (% at Maximum)
1.8 V ±5%	-3.27%	3.34%	-5.99%	6.18%	-12.55%	14.01%
3.3 V ±10%	-0.68%	0.74%	-3.55%	3.90%	-6.26%	5.33%
5 V ±10%	-1.48%	2.13%	-3.90%	4.26%	-6.71%	5.29%
2.5 V - 4.5 V	-1.74%	1.78%	-3.94%	4.13%	-6.88%	6.18%
1.71 V….5.5 V	-9.82%	8.90%	-12.13%	11.64%	-17.71%	18.02%

5.7.2 2 MHz RC Oscillator

Table 5. 2 MHz RC OSC frequency limits

Power Supply Range (VDD) V	Temperature Range					
	+25 °C		0 °C ... +85 °C		-40 °C ... +85 °C	
	Minimum Value, MHz	Maximum Value, MHz	Minimum Value, MHz	Maximum Value, MHz	Minimum Value, MHz	Maximum Value, MHz
1.8 V ±5%	1.952	2.034	1.897	2.059	1.897	2.114
3.3 V ±10%	1.963	2.034	1.878	2.060	1.878	2.106
5 V ±10%	1.966	2.121	1.872	2.132	1.872	2.157
2.5 V - 4.5 V	1.900	2.081	1.825	2.097	1.825	2.121
1.71 V….5.5 V	1.753	2.118	1.744	2.136	1.736	2.154

Table 6. 2 MHz RC OSC frequency error (error calculated relative to nominal value)

Power Supply Range (VDD) V	Temperature Range					
	+25 °C		0 °C ... +85 °C		-40 °C ... +85 °C	
	Error (% at Minimum)	Error (% at Maximum)	Error (% at Minimum)	Error (% at Maximum)	Error (% at Minimum)	Error (% at Maximum)
1.8 V ±5%	-2.40%	1.70%	-5.15%	2.95%	-5.15%	5.71%
3.3 V ±10%	-1.84%	1.69%	-6.09%	3.01%	-6.09%	5.31%
5 V ±10%	-1.68%	6.05%	-6.39%	6.58%	-6.39%	7.87%
2.5 V - 4.5 V	-4.98%	4.05%	-8.76%	4.84%	-8.76%	6.07%
1.71 V….5.5 V	-12.37%	5.89%	-12.80%	6.81%	-13.22%	7.72%

5.7.3 27 MHz Ring Oscillator

Table 7. 27 MHz Ring OSC frequency limits

Power Supply Range (VDD) V	Temperature Range					
	+25 °C		0 °C ... +85 °C		-40 °C ... +85 °C	
	Minimum Value, MHz	Maximum Value, MHz	Minimum Value, MHz	Maximum Value, MHz	Minimum Value, MHz	Maximum Value, MHz
1.8 V ±5%	24.755	29.120	23.641	29.164	23.641	29.164
3.3 V ±10%	25.534	29.111	25.320	29.111	24.558	29.111
5 V ±10%	25.551	29.110	25.262	29.110	24.634	29.110
2.5 V - 4.5 V	25.532	29.111	25.299	29.111	24.558	29.111
1.71 V….5.5 V	24.771	29.111	23.641	29.128	23.641	29.128

Table 8. 27 MHz Ring OSC frequency error (error calculated relative to nominal value)

Power Supply Range (VDD) V	Temperature Range					
	+25 °C		0 °C ... +85 °C		-40 °C ... +85 °C	
	Error (% at Minimum)	Error (% at Maximum)	Error (% at Minimum)	Error (% at Maximum)	Error (% at Minimum)	Error (% at Maximum)
1.8 V ±5%	-8.32%	7.85%	-12.44%	8.02%	-12.44%	8.02%
3.3 V ±10%	-5.43%	7.82%	-6.22%	7.82%	-9.04%	7.82%
5 V ±10%	-5.37%	7.81%	-6.44%	7.81%	-8.76%	7.81%
2.5 V - 4.5 V	-5.44%	7.82%	-6.30%	7.82%	-9.04%	7.82%
1.71 V….5.5 V	-8.26%	7.82%	-12.44%	7.88%	-12.44%	7.88%

5.7.4 1.73 kHz LF Oscillator

Table 9. 1.73 kHz LF OSC frequency limits

Power Supply Range (VDD) V	Temperature Range					
	+25 °C		0 °C ... +85 °C		-40 °C ... +85 °C	
	Minimum Value, kHz	Maximum Value, kHz	Minimum Value, kHz	Maximum Value, kHz	Minimum Value, kHz	Maximum Value, kHz
1.8 V ±5%	1.453	1.981	1.431	2.003	1.368	2.027
3.3 V ±10%	1.465	1.988	1.444	2.008	1.384	2.027
5 V ±10%	1.491	2.114	1.471	2.130	1.411	2.140
2.5 V - 4.5 V	1.461	2.003	1.440	2.022	1.379	2.040
1.71 V….5.5 V	1.453	2.114	1.431	2.130	1.368	2.140

Table 10. 1.73 kHz LF OSC frequency error (error calculated relative to nominal value)

Power Supply Range (VDD) V	Temperature Range					
	+25 °C		0 °C ... +85 °C		-40 °C ... +85 °C	
	Error (% at Minimum)	Error (% at Maximum)	Error (% at Minimum)	Error (% at Maximum)	Error (% at Minimum)	Error (% at Maximum)
1.8 V ±5%	-16.00%	14.53%	-17.26%	15.80%	-20.93%	17.15%
3.3 V ±10%	-15.32%	14.89%	-16.53%	16.05%	-20.03%	17.18%
5 V ±10%	-13.84%	22.19%	-14.96%	23.11%	-18.42%	23.68%
2.5 V - 4.5 V	-15.57%	15.79%	-16.76%	16.89%	-20.27%	17.95%
1.71 V….5.5 V	-16.00%	22.19%	-17.26%	23.11%	-20.93%	23.68%

5.7.5 OSC Power On delay

Table 11. Oscillators Power On delay at room temperature; RC OSC power setting: "Auto Power On", RC osc clock to matrix input: “Enable”

Power Supply Range (VDD) V	LF OSC		RC OSC 2 MHz		RC OSC 25 kHz		RING OSC	
	Typical Value, µs	Maximum Value, µs	Typical Value, ns	Maximum Value, ns	Typical Value, µs	Maximum Value, µs	Typical Value, ns	Maximum Value, ns
1.71	562.8	639.2	929.8	1100.2	41.29	43.48	179.4	238.9
1.80	561.9	638.0	898.2	1054.6	41.21	42.75	161.8	188.9
1.89	561.1	637.2	873.1	1021.5	41.09	42.33	154.0	243.5
2.50	557.1	631.1	761.4	871.5	40.58	41.32	111.5	123.3
2.70	556.0	630.8	737.7	833.7	40.50	41.18	105.0	116.0
3.00	554.6	628.4	710.1	793.9	40.39	40.94	90.0	98.6
3.30	553.0	625.7	688.7	768.5	40.33	40.92	85.0	92.6
3.60	551.4	624.1	671.9	752.6	40.30	40.87	81.3	88.4
4.20	546.6	617.4	645.9	727.3	40.25	40.90	75.9	82.3
4.50	542.5	611.8	634.8	716.3	40.20	40.86	73.9	80.2
5.00	529.2	593.7	615.4	694.8	40.12	41.07	71.2	76.9
5.50	505.4	562.8	590.5	667.4	39.90	41.43	69.1	74.3

5.8 ACMP Specifications

Table 12. ACMP Specifications

Symbol	Parameter	Description/Note	Conditions	Min.	Typ.	Max.	Unit
V_{ACMP}	ACMP Input Voltage Range	Positive Input	VDD = 1.8 V ± 5 %	0	--	V_{DD}	V
		Negative Input		0	--	1.1	V
		Positive Input	VDD = 3.3 V ± 10 %	0	--	V_{DD}	V
		Negative Input		0	--	1.2	V
		Positive Input	VDD = 5.0 V ± 10 %	0	--	V_{DD}	V
		Negative Input		0	--	1.2	V
V_{offset}	ACMP Input Offset Voltage	Low Bandwidth - Enable, Vhys = 0 mV, Gain = 1, Vref = (50..1200) mV, VDD = (1.71..5.5) V	T = 25°C	-7.4	--	6.9	mV
			T = (-40..85)°C	-11.1	--	11.7	mV
		Low Bandwidth - Disable, Vhys = 0 mV, Gain =1, Vref = (50..1200) mV, VDD = (1.71..5.5) V	T = 25°C	-6.8	--	6.1	mV
			T = (-40..85)°C	-8.0	--	6.9	mV
t_{start}	ACMP Start Time	ACMP Power On delay, Minimal required wake time for the “Wake and Sleep function”, Regulator and Charge Pump set to automatic ON/OFF	BG = 550 µs, T = 25°C VDD = (1.71..5.5) V	--	396.3	1127.0	µS
			BG = 550 µs, T = (-40..85)°C VDD = (1.71..5.5) V	--	512.4	1901.7	µS
			BG = 100 µs, T = 25°C VDD = 2.7..5.5 V	--	85.5	218.2	µS
			BG = 100 µs, T = (-40..85)°C VDD = 2.7..5.5 V	--	106.7	397.0	µS

Symbol	Parameter	Description/Note	Conditions	Min.	Typ.	Max.	Unit
V_{HYS}	Built-in Hysteresis	V_{HYS} = 25 mV $V_{IL} = V_{REF} - V_{HYS}/2$ $V_{IH} = V_{REF} + V_{HYS}/2$	LB - Enabled, T = 25°C	--	--	30.9	mV
			LB - Disabled, T = 25°C	13.2	--	32.8	mV
		V_{HYS} = 50 mV $V_{IL} = V_{REF} - V_{HYS}$ $V_{IH} = V_{REF}$	LB - Enabled, T = 25°C	43.2	--	58.3	mV
			LB - Disabled, T = 25°C	45.7	--	54.8	mV
		V_{HYS} = 200 mV $V_{IL} = V_{REF} - V_{HYS}$ V_{IH} = Vin	LB - Enabled, T = 25°C	193.6	--	209.8	mV
			LB - Disabled, T = 25°C	194.9	--	206.9	mV
		V_{HYS} = 25 mV $V_{IL} = V_{REF} - V_{HYS}/2$ $V_{IH} = V_{REF} + V_{HYS}/2$	LB - Enabled, T = (-40…+85)°C	--	--	35.5	mV
			LB - Disabled, T = (-40…+85)°C	6.2	--	33.5	mV
		V_{HYS} = 50 mV $V_{IL} = V_{REF} - V_{HYS}$ $V_{IH} = V_{REF}$	LB - Enabled, T = (-40…+85)°C	39.0	--	64.0	mV
			LB - Disabled, T = (-40…+85)°C	42.7	--	58.3	mV
		V_{HYS} = 200 mV $V_{IL} = V_{REF} - V_{HYS}$ V_{IH} = Vin	LB - Enabled, T = (-40…+85)°C	189.4	--	215.2	mV
			LB - Disabled, T = (-40…+85)°C	192.2	--	209.9	mV
R_{sin}	Series Input Resistance	Gain = 1x		--	100.0	--	MΩ
		Gain = 0.5x		--	1.0	--	MΩ
		Gain = 0.33x		--	0.8	--	MΩ
		Gain = 0.25x		--	1.0	--	MΩ
PROP	Propagation Delay, Response Time for ACMP 0 to ACMP 4	Low Bandwidth - Enable, Gain = 1, VDD = (1.71..5.5) V, Overdrive = 5 mV	Low to High, T = (-40…+85)°C	--	32.81	380.26	µS
			High to Low, T = (-40…+85)°C	--	33.81	406.54	µS
		Low Bandwidth - Disable, Gain = 1, VDD = (1.71..5.5) V, Overdrive = 5 mV	Low to High, T = (-40…+85)°C	--	1.60	4.17	µS
			High to Low, T = (-40…+85)°C	--	1.43	3.30	µS
	Propagation Delay, Response Time for ACMP 5	Low Bandwidth - Enable, Gain = 1, T = (-40…+85)°C, VDD = (1.71..5.5) V, Overdrive = 5 mV	Low to High, T = (-40…+85)°C	--	56.02	482.64	µS
			High to Low, T = (-40…+85)°C	--	56.62	510.40	µS
		Low Bandwidth - Disable, Gain = 1, VDD = (1.71..5.5) V, Overdrive = 5 mV	Low to High, T = (-40…+85)°C	--	5.85	8.66	µS
			High to Low, T = (-40…+85)°C	--	4.34	6.70	µS

Symbol	Parameter	Description/Note	Conditions	Min.	Typ.	Max.	Unit
G	Gain error (including threshold and internal Vref error), T = (-40…+85)°C	G = 1, VDD = 1.71 V	Vref = 50…1200 mV	--	1	--	
		G = 1, VDD = 3.3 V	Vref = 50…1200 mV	--	1	--	
		G = 1, VDD = 5.5 V	Vref = 50…1200 mV	--	1	--	
		G = 0.5, VDD = 1.71 V	Vref = 100 mV	-0.55%	--	1.80%	
			Vref = 600 mV	-1.00%	--	1.26%	
			Vref = 1200 mV	-1.20%	--	1.24%	
		G = 0.5, VDD = 3.3 V	Vref = 100 mV	-0.87%	--	2.82%	
			Vref = 600 mV	-0.98%	--	1.26%	
			Vref = 1200 mV	-1.09%	--	1.21%	
		G = 0.5, VDD = 5.5 V	Vref = 100 mV	-1.88%	--	4.15%	
			Vref = 600 mV	-1.05%	--	1.35%	
			Vref = 1200 mV	-1.02%	--	1.27%	
		G = 0.33, VDD = 1.71V	Vref = 100 mV	-1.28%	--	2.40%	
			Vref = 600 mV	-1.13%	--	2.00%	
			Vref = 1200 mV	-1.21%	--	2.07%	
		G = 0.33, VDD = 3.3 V	Vref = 100 mV	-1.46%	--	4.00%	
			Vref = 600 mV	-1.40%	--	1.72%	
			Vref = 1200 mV	-1.63%	--	1.53%	
		G = 0.33, VDD = 5.5 V	Vref = 100 mV	-1.28%	--	2.40%	
			Vref = 600 mV	-1.46%	--	4.00%	
			Vref = 1200 mV	-1.55%	--	4.15%	
		G = 0.25, VDD = 1.71V	Vref = 100 mV	-1.21%	--	2.56%	
			Vref = 600 mV	-1.29%	--	2.25%	
			Vref = 1200 mV	-1.37%	--	2.30%	
		G = 0.25, VDD = 3.3 V	Vref = 100 mV	-1.36%	--	3.97%	
			Vref = 600 mV	-1.45%	--	1.84%	
			Vref = 1200 mV	-1.84%	--	1.82%	
		G = 0.25, VDD = 5.5 V	Vref = 100 mV	-2.09%	--	4.63%	
			Vref = 600 mV	-1.48%	--	1.94%	
			Vref = 1200 mV	-1.47%	--	1.87%	
Vref	Internal Vref error, Vref = 1200 mV	VDD = 1.8 V ± 5 %	T = 25°C	-0.96%	--	0.95%	
			T = (-40…+85)°C	-1.30%	--	1.12%	
		VDD = 3.3 V ± 10 %	T = 25°C	-1.02%	--	1.03%	
			T = (-40…+85)°C	-1.34%	--	1.14%	
		VDD = 5.0 V ± 10 %	T = 25°C	-1.20%	--	1.15%	
			T = (-40…+85)°C	-1.58%	--	1.48%	

5.9 ADC Specifications (Including PGA)

Note: PGA input voltage should not exceed values given in Section 5.1 Absolute Maximum Conditions.

Table 13. Single-Ended ADC Operation, T = (-40 to +85)°C, VDD = (1.71 to 5.5)V, unless otherwise specified

Symbol	Parameter	Description/Note	Conditions	Min.	Max.	Unit
V_{inp}	Input Voltage Range (bit 0 to bit 255), relative to GND	G = 0.25	VDD = 5V ±10%	120	4120	mV
		G = 0.5	VDD = 2.5 to 5.5 V	60	2060	mV
		G = 1		30	1030	mV
		G = 2		20	520	mV
		G = 4		15	265	mV
		G = 8		12	137	mV
ZE	Offset Zero Error	G = 0.25	T = 25°C, VDD = 5V ±10%	--	±1.7	LSB
		G = 0.5	T = 25°C, VDD = 2.5 to 5.5 V	--	±2.6	LSB
		G = 1	T = 25°C	--	±3	LSB
		G = 2		--	±2.6	LSB
		G = 4		--	±3.3	LSB
		G = 8		--	±4.6	LSB
dZE/dT	Offset Zero Error Temperature Drift	G = 0.25	VDD = 5V ±10%	--	±0.008	%/°C
		G = 0.5	VDD = 2.5 to 5.5 V	--	±0.009	%/°C
		G = 1		--	±0.01	%/°C
		G = 2		--	±0.014	%/°C
		G = 4		--	±0.025	%/°C
		G = 8		--	±0.048	%/°C
GE	Gain Error	G = 0.25	T = 25°C, VDD = 5V ±10%	--	±1.5	LSB
		G = 0.5	T = 25°C, VDD = 2.5 to 5.5 V	--	±1.3	LSB
		G = 1	T = 25°C	--	±1.5	LSB
		G = 2		--	±1.7	LSB
		G = 4		--	±1.3	LSB
		G = 8		--	±1.2	LSB
dGE/dT	Gain Error Temperature Coefficient	G = 0.25	VDD = 5V ±10%	--	±0.007	%/°C
		G = 0.5	VDD = 2.5 to 5.5 V	--	±0.008	%/°C
		G = 1		--	±0.007	%/°C
		G = 2		--	±0.009	%/°C
		G = 4		--	±0.008	%/°C
		G = 8		--	±0.008	%/°C