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SX1212 Transceiver
Ultra-Low Power Integrated 300-510MHz Transceiver

General Description

The SX1212 is a low cost single-chip transceiver operating in the frequency ranges from 300MHz to 510MHz. The SX1212 is optimized for very low power consumption (3mA in receiver mode). It incorporates a baseband modem with data rates up to 150 kb/s. Data handling features include a sixty-four byte FIFO, packet handling, automatic CRC generation and data whitening. Its highly integrated architecture allows for minimum external component count whilst maintaining design flexibility. All major RF communication parameters are programmable and most of them may be dynamically set. It complies with European (ETSI EN 300-220 V2.1.1) and North American (FCC part 15.247 and 15.249) regulatory standards.

Ordering Information

Table 1: Ordering Information

Part number	Delivery	Minimum Order Quantity / Multiple
SX1212IWLTRT	Tape & Reel	3000 pieces

- TQFN-32 package – Operating range [-40;+85°C]
- T refers to Lead Free packaging
- This device is WEEE and RoHS compliant

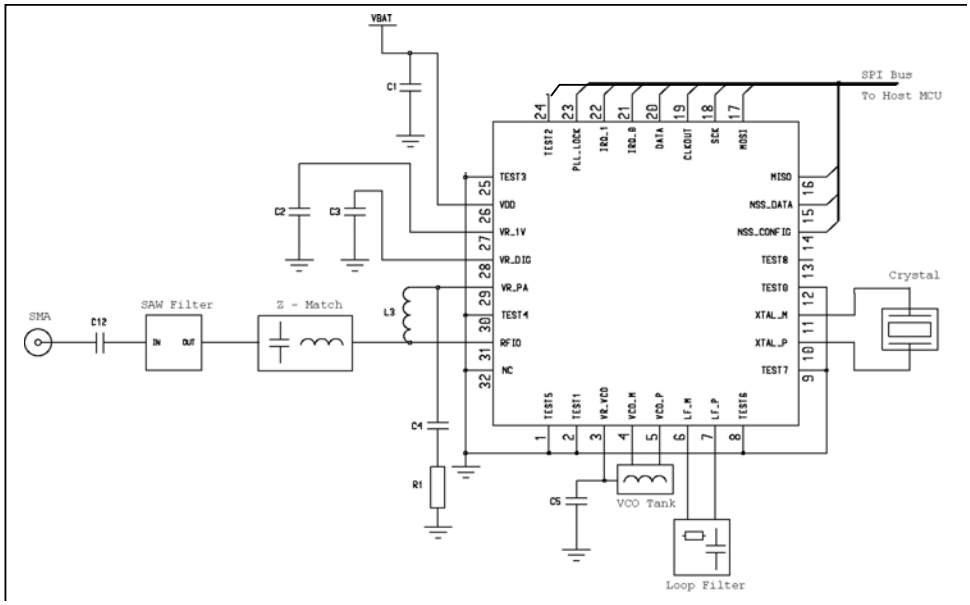
Features

- Low Rx power consumption: 3mA
- Low Tx power consumption: 25 mA @ +10 dBm
- Good reception sensitivity: down to -104 dBm at 25 kb/s in FSK, -110 dBm at 2kb/s in OOK
- Programmable RF output power: up to +12.5 dBm in 8 steps
- Packet handling feature with data whitening and automatic CRC generation
- RSSI (Received Signal Strength Indicator)
- Bit rates up to 150 kb/s, NRZ coding
- On-chip frequency synthesizer
- FSK and OOK modulation
- Incoming sync word recognition
- Built-in Bit-Synchronizer for incoming data and clock synchronization and recovery
- 5 x 5 mm TQFN package
- Optimized Circuit Configuration for Low-cost applications

Applications

- Wireless alarm and security systems
- Wireless sensor networks
- Automated Meter Reading
- Home and building automation
- Industrial monitoring and control
- Remote Wireless Control
- Active RFID PHY

Application Circuit Schematic



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Acronyms

BOM	Bill Of Materials
BR	Bit Rate
BW	Bandwidth
CCITT	Comité Consultatif International Téléphonique et Télégraphique - ITU
CP	Charge Pump
CRC	Cyclic Redundancy Check
DAC	Digital to Analog Converter
DDS	Direct Digital Synthesis
DLL	Dynamically Linked Library
ERP	Equivalent Radiated Power
ETSI	European Telecommunications Standards Institute
FCC	Federal Communications Commission
Fdev	Frequency Deviation
FIFO	First In First Out
FS	Frequency Synthesizer
FSK	Frequency Shift Keying
GUI	Graphical User Interface
IC	Integrated Circuit
ID	IDentificator
IF	Intermediate Frequency
IRQ	Interrupt ReQuest
ITU	International Telecommunication Union
LFSR	Linear Feedback Shift Register
LNA	Low Noise Amplifier
LO	Local Oscillator
LSB	Least Significant Bit
MSB	Most Significant Bit
NRZ	Non Return to Zero
NZIF	Near Zero Intermediate Frequency
OOK	On Off Keying
PA	Power Amplifier
PCB	Printed Circuit Board
PFD	Phase Frequency Detector
PLL	Phase-Locked Loop
POR	Power On Reset
RBW	Resolution BandWidth
RF	Radio Frequency
RSSI	Received Signal Strength Indicator
Rx	Receiver
SAW	Surface Acoustic Wave
SPI	Serial Peripheral Interface
SR	Shift Register
Stby	Standby
Tx	Transmitter
uC	Microcontroller
VCO	Voltage Controlled Oscillator
XO	Crystal Oscillator
XOR	eXclusive OR

This product datasheet contains a detailed description of the SX1212 performance and functionality. Please consult the Semtech website for the latest updates or errata.

1. General Description

The SX1212 is a single chip FSK and OOK transceiver capable of operation in the 300 to 510MHz license free ISM frequency bands. It complies with both the relevant European and North American standards, EN 300-220 V2.1.1 (June 2006 release) and FCC Part 15 (10-1-2006 edition). A unique feature of this circuit is its extremely low current consumption in receiver mode of only 3mA (typ).
The SX1212 comes in a 5x5 mm TQFN-32 package.

1.1. Simplified Block Diagram

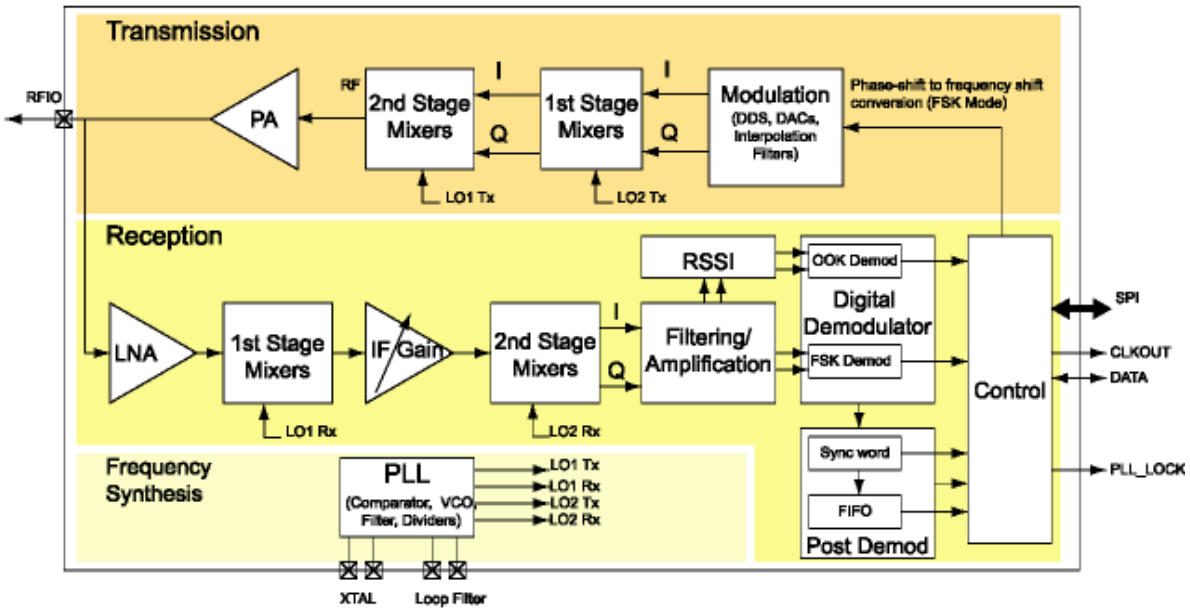

Figure 1: SX1212 Simplified Block Diagram

1.2. Pin Diagram

The following diagram shows the pins arrangement of the QFN package, top view.

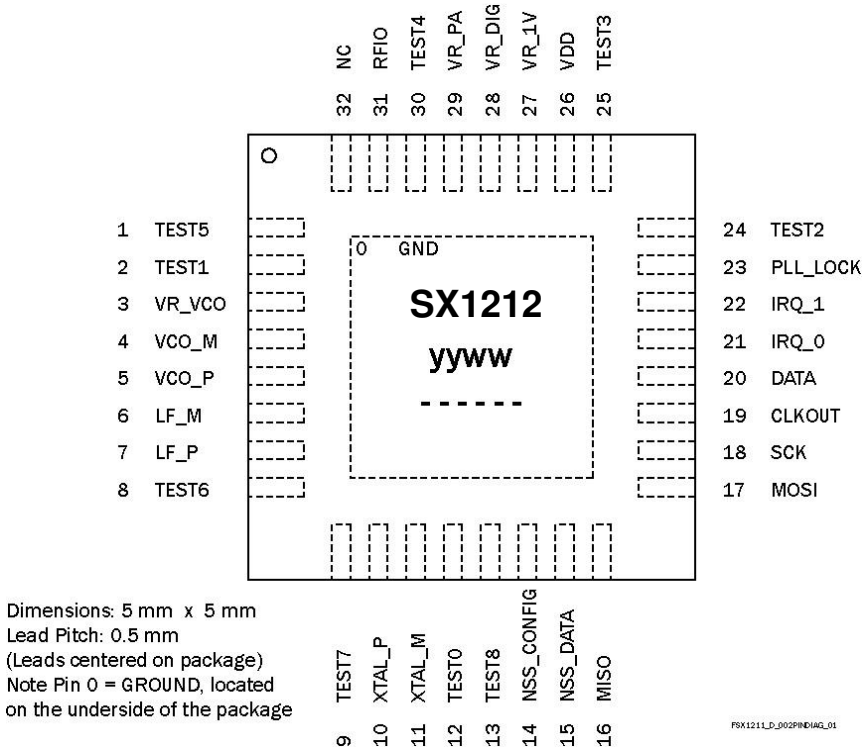

Figure 2: SX1212 Pin Diagram

Notes:
- yyww refers to the date code
- ------ refers to the lot number

1.3. Pin Description

Table 2: SX1212 Pinouts

Number	Name	Type	Description
0	GND	I	Exposed ground pad
1	TEST5	I/O	Connect to GND
2	TEST1	I/O	Connect to GND
3	VR_VCO	O	Regulated supply of the VCO
4	VCO_M	I/O	VCO tank
5	VCO_P	I/O	VCO tank
6	LF_M	I/O	PLL loop filter
7	LF_P	I/O	PLL loop filter
8	TEST6	I/O	Connect to GND
9	TEST7	I/O	Connect to GND
10	XTAL_P	I/O	Crystal connection
11	XTAL_M	I/O	Crystal connection
12	TEST0	I	Connect to GND
13	TEST8	I/O	POR. Do not connect if unused
14	NSS_CONFIG	I	SPI CONFIG enable
15	NSS_DATA	I	SPI DATA enable
16	MISO	O	SPI data output
17	MOSI	I	SPI data input
18	SCK	I	SPI clock input
19	CLKOUT	O	Clock output
20	DATA	I/O	NRZ data input and output (Continuous mode)
21	IRQ_0	O	Interrupt output
22	IRQ_1	O	Interrupt output
23	PLL_LOCK	O	PLL lock detection output
24	TEST2	O	No connect
25	TEST3	I/O	Connect to GND
26	VDD	I	Supply voltage
27	VR_1V	O	Regulated supply of the analog circuitry
28	VR_DIG	O	Regulated supply of digital circuitry
29	VR_PA	O	Regulated supply of the PA
30	TEST4	I/O	Connect to GND
31	RFIO	I/O	RF input/output
32	NC	-	Connect to GND

Note: pin 13 (Test 8) can be used as a manual reset trigger. See section 7.4.2 for details on its use.

2. Electrical Characteristics

2.1. ESD Notice

The SX1212 is a high performance radio frequency device. It satisfies:

- Class 2 of the JEDEC standard JESD22-A114-B (Human Body Model), except on pins 3-4-5-27-28-29-31 where it satisfies Class 1A.
- Class III of the JEDEC standard JESD22-C101C (Charged Device Model) on all pins. It should thus be handled with all the necessary ESD precautions to avoid any permanent damage.

2.2. Absolute Maximum Ratings

Stresses above the values listed below may cause permanent device failure. Exposure to absolute maximum ratings for extended periods may affect device reliability.

Table 3: Absolute Maximum Ratings

Symbol	Description	Min	Max	Unit
VDDmr	Supply voltage	-0.3	3.7	V
Tmr	Storage temperature	-55	125	°C
Pmr	Input level	-	0	dBm

2.3. Operating Range

Table 4: Operating Range

Symbol	Description	Min	Max	Unit
VDDop	Supply Voltage	2.1	3.6	V
Trop	Temperature	-40	+85	°C
ML	Input Level	-	0	dBm

2.4. Chip Specification

Conditions: Temp = 25 °C, VDD = 3.3 V, crystal frequency = 12.8 MHz, carrier frequency = 434 MHz, modulation FSK, data rate = 25 kb/s, Fdev = 50 kHz, fc = 100 kHz, unless otherwise specified.

2.4.1. Power Consumption

Table 5: Power Consumption Specification

Symbol	Description	Conditions	Min	Typ	Max	Unit
IDDSL	Supply current in sleep mode		-	0.1	2	µA
IDDST	Supply current in standby mode, CLKOUT disabled	Crystal oscillator running	-	65	85	µA
IDDFS	Supply current in FS mode	Frequency synthesizer running	-	1.3	1.7	mA
IDDR	Supply current in receiver mode		-	3.0	3.5	mA
IDDT	Supply current in transmitter mode	Output power = +10 dBm Output power = 1dBm(1)	- -	25 16	30 21	mA mA

(1) Guaranteed by design and characterization

2.4.2. Frequency Synthesis

Table 6: Frequency Synthesizer Specification

Symbol	Description	Conditions	Min	Typ	Max	Unit
FR	Frequency ranges	Programmable , (may require specific BOM)	300 320 350 390 430 470	- - - - - -	330 350 390 430 470 510	MHz MHz MHz MHz MHz MHz
BR_F	Bit rate (FSK)	NRZ	0.78	-	150	Kb/s
BR_O	Bit rate (OOK)	NRZ	0.78	-	32	Kb/s
FDA	Frequency deviation (FSK)		33	50	200	kHz
XTAL	Crystal oscillator frequency		9	12.8	15	MHz
FSTEP	Frequency synthesizer step	Variable, depending on the frequency.	-	2	-	kHz
TS_OSC	Oscillator wake-up time	From Sleep mode(1)	-	1.5	5	ms
TS_FS	Frequency synthesizer wake-up time at most 10 kHz away from the target	From Stby mode	-	500	800	µs
TS_HOP	Frequency synthesizer hop time at most 10 kHz away from the target	200 kHz step	-	180	-	µs
		1 MHz step	-	200	-	µs
		5 MHz step	-	250	-	µs
		7 MHz step	-	260	-	µs
		12 MHz step	-	290	-	µs
		20 MHz step	-	320	-	µs
		27 MHz step	-	340	-	µs

(1) Guaranteed by design and characterization

2.4.3. Transmitter

Table 7: Transmitter Specification

Symbol	Description	Conditions	Min	Typ	Max	Unit
RFOP	RF output power, programmable with 8 steps of typ. 3dB	Maximum power setting	-	+12.5	-	dBm
		Minimum power setting	-	-8.5	-	dBm
PN	Phase noise	Measured with a 600 kHz offset, at the transmitter output.	-	-112	-	dBc/Hz
SPT	Transmitted spurious	At any offset between 200 kHz and 600 kHz, unmodulated carrier, Fdev = 50 kHz.	-	-	-47	dBc
TS_TR(1)	Transmitter wake-up time	From FS to Tx ready.	-	120	500	µs
TS_TR2(1)	Transmitter wake-up time	From Stby to Tx ready.	-	600	900	µs

(1) Guaranteed by design and characterization

2.4.4. Receiver

On the following table, fc and fo describe the bandwidth of the active channel filters as described in section 3.4.4.2. All sensitivities are measured receiving a PN15 sequence, for a BER of 0.1.%

Table 8: Receiver Specification

Symbol	Description	Conditions	Min	Typ	Max	Unit
RFS_F	Sensitivity (FSK)	434 MHz, BR=25 kb/s, Fdev =50 kHz, fc=100 kHz	-	-104	-	dBm
			-	-	-	
			-	-	-	
			-	-	-	
RFS_O	Sensitivity (OOK)	434 MHz, 2kb/s NRZ fc-fo=50 kHz, fo=50 kHz	-	-110	-	dBm
			-	-	-	
			-	-	-	
			-	-	-	
CCR	Co-channel rejection	Modulation as wanted signal	-	-12	-	dBc
ACR	Adjacent channel rejection	Offset = 300 kHz	-	-	-	dB
		Offset = 600 kHz	-	42	-	dB
		Offset = 1.2 MHz	-	53	-	dB
BI	Blocking immunity	Offset = 1 MHz, unmodulated	-	53	-	dBc
		Offset = 2 MHz, unmodulated, no SAW	-	-	-	
		Offset = 10 MHz, unmodulated, no SAW	-	-	-	
RXBW_F(1,2)	Receiver bandwidth in FSK mode	Single side BW Polyphase Off	50	-	250	kHz
RXBW_O(1,2)	Receiver bandwidth in OOK mode	Single side BW Polyphase On	50	-	400	kHz
IIP3	Input 3rd order intercept point	Interferers at 1MHz and 1.950 MHz offset	-	-28	-	dBm
TS_RE(1)	Receiver wake-up time	From FS to Rx ready	-	280	500	µs
TS_RE2(1)	Receiver wake-up time	From Stby to Rx ready	-	600	900	µs
TS_RE_HOP	Receiver hop time from Rx ready to Rx ready with a frequency hop	200 kHz step	-	400	-	µs
		1MHz step	-	400	-	µs
		5MHz step	-	460	-	µs
		7MHz step	-	480	-	µs
		12MHz step	-	520	-	µs
		20MHz step	-	550	-	µs
		27MHz step	-	600	-	µs
TS_RSSI	RSSI sampling time	From Rx ready	-	-	1/Fdev	s
DR_RSSI	RSSI dynamic Range	Ranging from sensitivity	-	70	-	dB

(1) Information from design and characterization
(2) This reflects the whole receiver bandwidth, as described in sections 3.4.4.1 and 3.4.4.2

2.4.5. Digital Specification

Conditions: Temp = 25 °C, VDD = 3.3 V, crystal frequency = 12.8 MHz, unless otherwise specified.

Table 9: Digital Specification

Symbol	Description	Conditions	Min	Typ	Max	Unit
VIH	Digital input level high		0.8*VDD	-	-	V
VIL	Digital input level low		-	-	0.2*VDD	V
VOH	Digital output level high	Imax=1mA	0.9*VDD	-	-	V
VOL	Digital output level low	Imax=-1mA	-	-	0.1*VDD	V
SCK_CONFIG	SPI Config. clock frequency		-	-	6	MHz
SCK_DATA	SPI data clock frequency		-	-	1	MHz
T_DATA	DATA hold and setup time		2	-	-	µs
T_MOSI_C	MOSI setup time for SPI Config.		250	-	-	ns
T_MOSI_D	MOSI setup time for SPI Data.		312	-	-	ns
T_NSSC_L	NSS_CONFIG low to SCK rising edge. SCK falling edge to NSS_CONFIG high.		500	-	-	ns
T_NSSD_L	NSS_DATA low to SCK rising edge. SCK falling edge to NSS_DATA high.		625	-	-	ns
T_NSSC_H	NSS_CONFIG rising to falling edge.		500	-	-	ns
T_NSSD_H	NSS_DATA rising to falling edge.		625	-	-	ns

Note: on pin 10 (XTAL_P) and 11 (XTAL_N), maximum voltages of 1.8V can be applied.

3. Architecture Description

This section describes in depth the architecture of this ultra low-power transceiver:

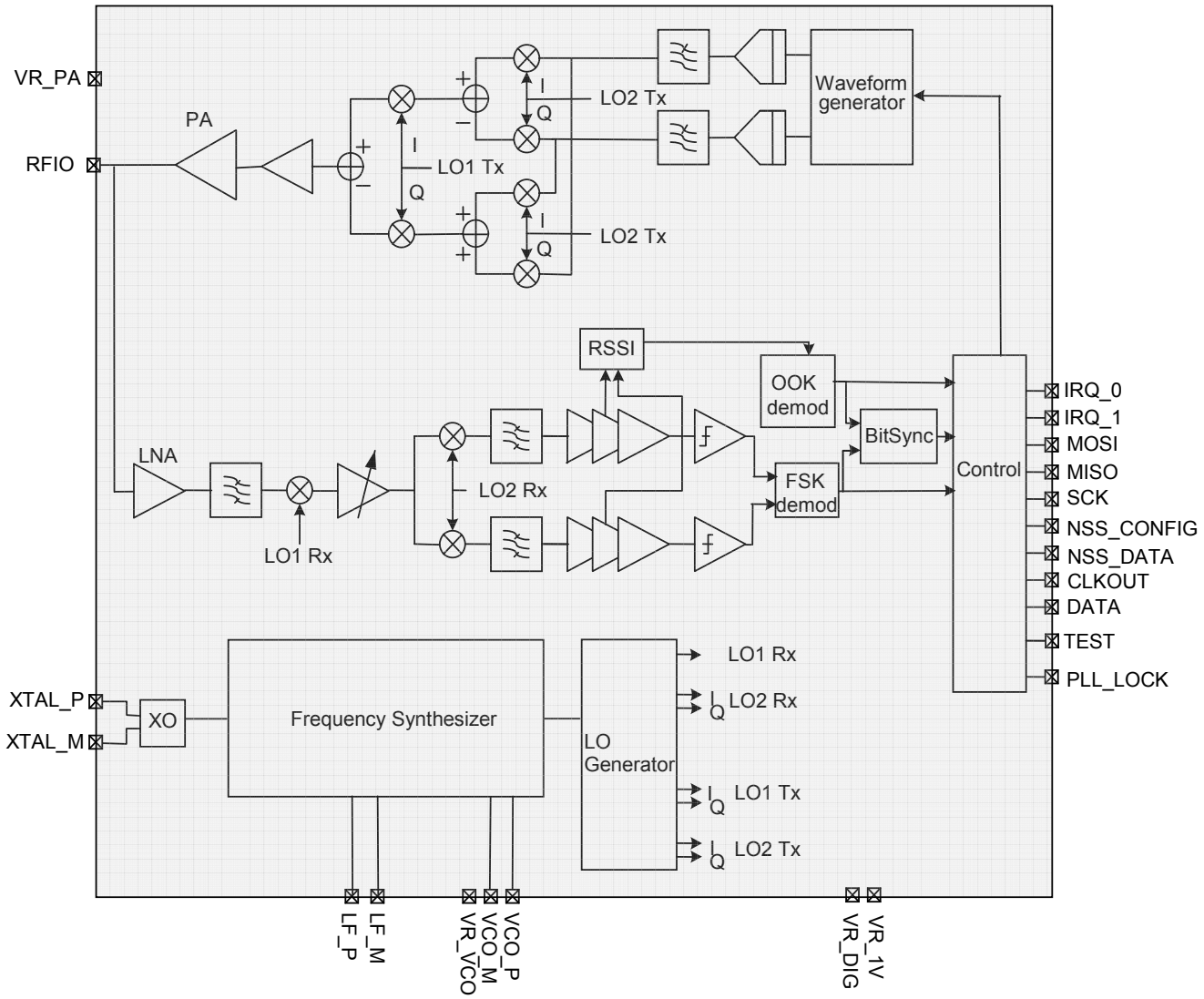

Figure 3: SX1212 Detailed Block Diagram

3.1. Power Supply Strategy

To provide stable sensitivity and linearity characteristics over a wide supply range, the SX1212 is internally regulated. This internal regulated power supply structure is described below:

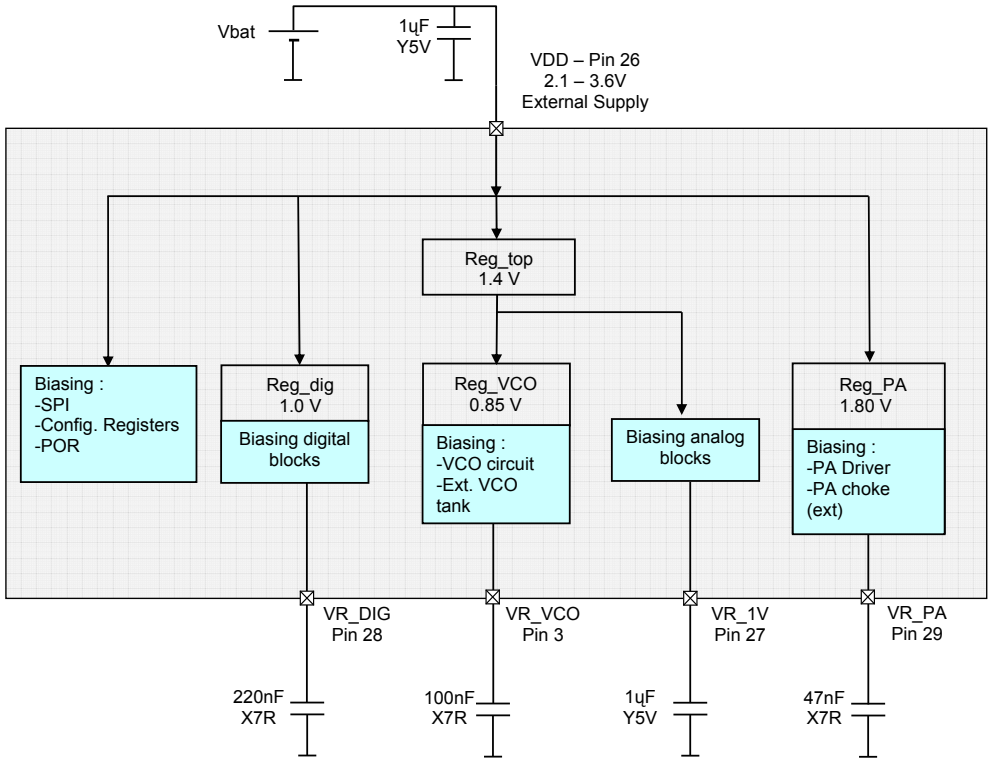

Figure 4: Power Supply Breakdown

To ensure correct operation of the regulator circuit, the decoupling capacitor connection shown in Figure 4 is required. These decoupling components are recommended for any design.

3.2. Frequency Synthesis Description

The frequency synthesizer of the SX1212 is a fully integrated integer-N type PLL. The PLL circuit requires only five external components for the PLL loop filter and the VCO tank circuit.

3.2.1. Reference Oscillator

The SX1212 embeds a crystal oscillator, which provides the reference frequency for the PLL. The recommended crystal specification is given in section 7.1.

3.2.2. CLKOUT Output

The reference frequency, or a sub-multiple of it, can be provided on CLKOUT (pin 19) by activating the bit OSCParam_Clkout_on. The division ratio is programmed through bits OSCParam_Clkout_freq. The two applications of the CLKOUT output are:

- To provide a clock output for a companion uC, thus saving the cost of an additional oscillator. CLKOUT can be made available in any operation mode, except Sleep mode, and is automatically enabled at power-up.
- To provide an oscillator reference output. Measurement of the CLKOUT signal enables simple software trimming of the initial crystal tolerance.

Note: To minimize the current consumption of the SX1212, ensure that the CLKOUT signal is disabled when unused.

3.2.3. PLL Architecture

The crystal oscillator (XO) forms the reference oscillator of an Integer-N Phase Locked Loop (PLL), whose operation is discussed in the following section. Figure 5 shows a block schematic of the SX1212 PLL. Here the crystal reference frequency and the software controlled dividers R, P and S determine the output frequency of the PLL.

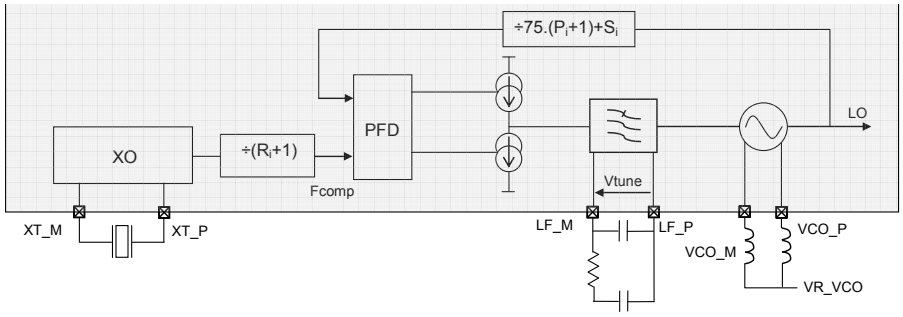

Figure 5: Frequency Synthesizer Description

The VCO tank inductors are connected on an external differential input. Similarly, the loop filter is also located externally. However, there is an internal 8pF capacitance at VCO input that should be subtracted from the desired loop filter capacitance.

The output signal of the VCO is used as the input to the local oscillator (LO) generator stage, illustrated in Figure 6. The VCO frequency is subdivided and used in a series of up (down) conversions for transmission (reception).

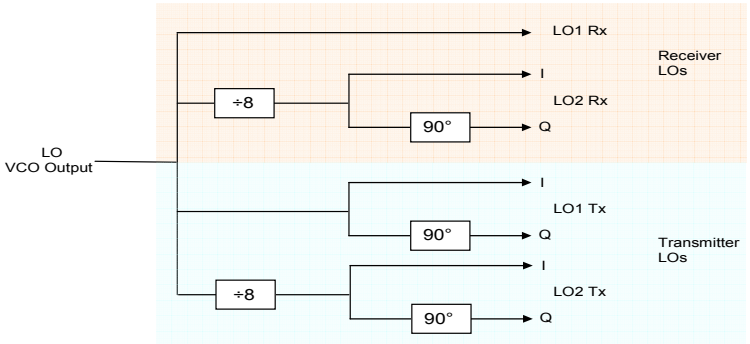

Figure 6: LO Generator

3.2.4. PLL Tradeoffs

With an integer-N PLL architecture, the following criterion must be met to ensure correct operation:

- The comparison frequency, Fcomp, of the Phase Frequency Detector (PFD) input must remain higher than six times the PLL bandwidth (PLLBW) to guarantee loop stability and to reject harmonics of the comparison frequency Fcomp. This is expressed in the inequality:

$$PLLBW \leq \frac{Fcomp}{6}$$

- However the PLLBW has to be sufficiently high to allow adequate PLL lock times
- Because the divider ration R determines Fcomp, it should be set close to 119, leading to Fcomp≈100 kHz which will ensure suitable PLL stability and speed.

With the recommended Bill Of Materials (BOM) of the reference design of section 7.5.3, the PLL prototype is the following:

- 64 ≤ R ≤ 169
- S < P+1
- PLLBW = 15 kHz nominal
- Startup times and reference frequency spurs as specified.

3.2.5. Voltage Controlled Oscillator

The integrated VCO requires only two external tank circuit inductors. As the input is differential, the two inductors should have the same nominal value. The performance of these components is important for both the phase noise and the power consumption of the PLL. It is recommended that a pair of high Q factor inductors is selected. These should be mounted orthogonally to other inductors (in particular the PA choke) to reduce spurious coupling between the PA and VCO. In addition, such measures may reduce radiated pulling effects and undesirable transient behavior, thus minimizing spectral occupancy. Note that ensuring a symmetrical layout of the VCO inductors will further improve PLL spectral purity.

For best performance wound type inductors, with tight tolerance, should be used as described in section 7.5.3.

3.2.5.1. SW Settings of the VCO

To guarantee the optimum operation of the VCO over the SX1212's frequency and temperature ranges, the following settings should be programmed into the SX1212:

Target channel (MHz)	300-330	320-350	350-390	390-430	430-470	470-510
Freq_band	000	001	010	011	100	101

Table 10: MCParam_Freq_band Setting

3.2.5.2. Trimming the VCO Tank by Hardware and Software

To ensure that the frequency band of operation may be accurately addressed by the R, P and S dividers of the synthesizer, it is necessary to ensure that the VCO is correctly centered. Note that for the reference design (see section 7.5) no centering is necessary. However, any deviation from the reference design may require the optimization procedure, outlined below, to be implemented. This procedure is simplified thanks to the built-in VCO trimming feature which is controlled over the SPI interface. This tuning does not require any RF test equipment, and can be achieved by simply measuring Vtune, the voltage between pins 6 (LFM) and 7 (LFP).

The VCO is centered if the voltage is within the range:

$$100 \le Vtune(mV) \le 200$$

Note that this measurement should be conducted when in transmit mode at the center frequency of the desired band (for example ~315 MHz in the 300-330 MHz band), with the appropriate MCParam_Freq_band setting.

If this inequality is not satisfied then adjust the MCParam_VCO_trim bits from 00 whilst monitoring Vtune. This allows the VCO voltage to be trimmed in + 60 mV increments. Should the desired voltage range be inaccessible, the voltage may be adjusted further by changing the tank circuit inductance value. Note that an increase in inductance will result in an increase Vtune.

Note for mass production: The VCO capacitance is piece to piece dependant. As such, the optimization proposed above should be verified on several prototypes, to ensure that the population is centered on 150 mV.

3.2.6. PLL Loop Filter

To adequately reject spurious components arising from the comparison frequency Fcomp, an external 2nd order loop filter is employed.

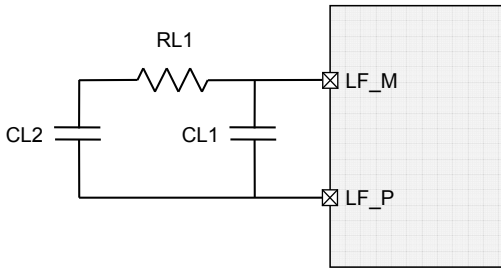

Figure 7: Loop Filter

Following the recommendations made in section 3.2.4, the loop filter proposed in the reference design's bill of material on section 7.5.3 should be used. The loop filter settings are frequency band independent and are hence relevant to all implementations of the SX1212.

3.2.7. PLL Lock Detection Indicator

The SX1212 also features a PLL lock detect indicator. This is useful for optimizing power consumption, by adjusting the synthesizer wake up time (TS_FS), since the PLL startup time is lower than specified under nominal conditions. The lock status can be read on bit IRQParam_PLL_lock, and must be cleared by writing a "1" to this same register. In addition, the lock status can be reflected in pin 23 PLL_LOCK, by setting the bit IRQParam_Enable_lock_detect.

3.2.8. Frequency Calculation

As shown in Figure 5 the PLL structure comprises three different dividers, R, P and S, which set the output frequency through the LO. A second set of dividers is also available to allow rapid switching between a pair of frequencies: R1/P1/S1 and R2/P2/S2. These six dividers are programmed by six bytes of the register MCParam from addresses 6 to 11.

3.2.8.1. FSK Mode

The following formula gives the relationship between the local oscillator, and R, P and S values, when using FSK modulation.

$$Frf, fsk = \frac{9}{8} Flo$$

$$Frf, fsk = \frac{9}{8} \frac{Fxtal}{R+1} \left[75(P+1) + S\right]$$

3.2.8.2. OOK Mode

Due to the manner in which the baseband OOK symbols are generated, the signal is always offset by the FSK frequency deviation (Fdev - as programmed in MCParam_Freq_dev). Hence, the center of the transmitted OOK signal is:

$$Frf,ook,tx = \frac{9}{8}Flo - Fdev$$

$$Frf,ook,tx = \frac{9}{8}\frac{Fxtal}{R+1}\left[75(P+1)+S\right] - Fdev$$

Consequently, in receive mode, due to the low intermediate frequency (Low-IF) architecture of the SX1212 the frequency should be configured so as to ensure the correct low-IF receiver baseband center frequency, IF2.

$$Frf,ook,rx = \frac{9}{8}Flo - IF2$$

$$Frf,ook,rx = \frac{9}{8}\frac{Fxtal}{R+1}\left[75(P+1)+S\right] - IF2$$

Note that from Section 3.4.4, it is recommended that IF2 be set to 100 kHz.

3.3. Transmitter Description

The SX1212 is set to transmit mode when MCParam_Chip_mode = 100.

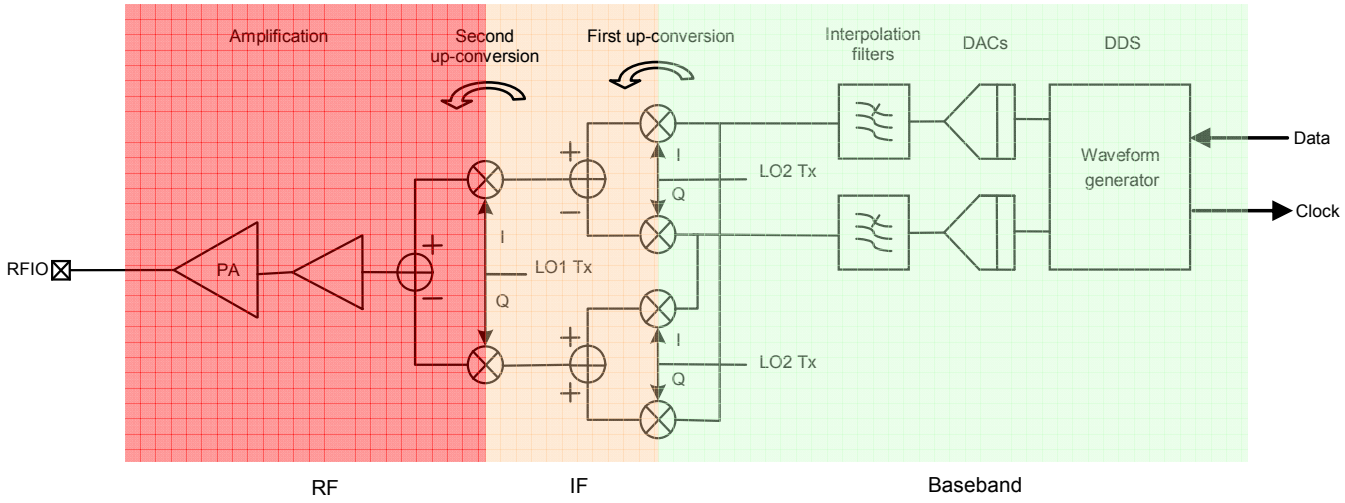

Figure 8: Transmitter Architecture

3.3.1. Architecture Description

The baseband I and Q signals are digitally generated by a DDS whose digital to analog converters (DAC) followed by two anti-aliasing low-pass filters transform the digital signal into analog in-phase (I) and quadrature (Q) components whose frequency is the selected frequency deviation (Fdev).

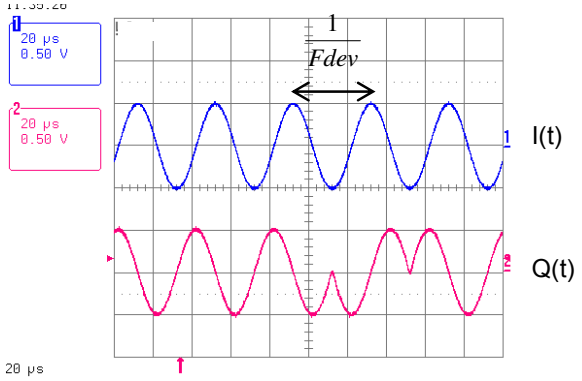

Figure 9: I(t), Q(t) Overview

In FSK mode, the relative phase of I and Q is switched by the input data between -90° and +90° with continuous phase. The modulation is therefore performed at this initial stage, since the information contained in the phase difference will be converted into a frequency shift when the I and Q signals are up-converted in the first mixer stage. This first up-conversion stage is duplicated to enhance image rejection. The FSK convention is such that:

$$DATA = ''1'' \Rightarrow Frf + Fdev$$
$$DATA = ''0'' \Rightarrow Frf - Fdev$$

In OOK mode, the phase difference between the I and Q channels is kept constant (independent of the transmitted data). Thus, the first stage of up-conversion creates a fixed frequency signal at the low IF = Fdev (This explains why the transmitted OOK spectrum is offset by Fdev).
OOK Modulation is accomplished by switching on and off the PA and PA regulator stages. By convention:

$$DATA = ''1'' \Rightarrow PAon$$
$$DATA = ''0'' \Rightarrow PAoff$$

After the interpolation filters, a set of four mixers combines the I and Q signals and converts them into a pair of complex signals at the second intermediate frequency, equal to 1/8 of the LO frequency, or 1/9 of the RF frequency. These two new I and Q signals are then combined and up-converted to the final RF frequency by two quadrature mixers fed by the LO signal. The signal is pre-amplified, and then the transmitter output is driven by a final power amplifier stage.

3.3.2. Bit Rate Setting

In Continuous transmit mode, setting the Bit Rate is useful to determine the frequency of DCLK. As explained in section 5.3.2, DCLK will trigger an interrupt on the uC each time a new bit has to be transmitted.

$$BR = \frac{F_{XTAL}}{2 * \left[1 + val(MCParam\_BR\_C)\right] * \left[1 + val(MCParam\_BR\_D)\right]}$$

3.3.3. Alternative Settings

Bit rate, frequency deviation and TX interpolation filter settings are a function of the reference oscillator crystal frequency, F_{XTAL}. Settings other than those programmable with a 12.8 MHz crystal can be obtained by selection of the correct reference oscillator frequency. Please contact your local Semtech representative for further details.

3.3.4. Fdev Setting in FSK Mode

The frequency deviation, Fdev, of the FSK transmitter is programmed through bits MCParam_Freq_dev:

$$Fdev = \frac{F_{XTAL}}{32 * \left[1 + val(MCParam\_Freq\_dev)\right]}$$

For correct operation the modulation index ß should be such that:

$$\beta = 2 * \frac{Fdev}{BR} \geq 2$$

It should be noted that for communications between a pair of SX1212s, that Fdev should be at least 33 kHz to ensure a correct operation on the receiver side.

3.3.5. Fdev Setting in OOK Mode

Fdev has no physical meaning in OOK transmit mode. However, as has been shown - due to the DDS baseband signal generation, the OOK signal is always offset by “-Fdev” (see formulas is section 3.2.8). It is suggested that Fdev retains its default value of 100 kHz in OOK mode.

3.3.6. Interpolation Filter

After digital to analog conversion, both I and Q signals are smoothed by interpolation filters. This block low-pass filters the digitally generated signal, and prevents the alias signals from entering the modulators. Its bandwidth can be programmed with the register RXParam_InterpFiltTx, and should be set to:

$$BW \cong 3 * \left[Fdev + \frac{BR}{2} \right]$$

Where Fdev is the programmed frequency deviation as set in MCParam_Freq_dev, and BR is the physical Bit Rate of transmission.
Notes:

- Low interpolation filter bandwidth will attenuate the baseband I/Q signals thus reducing the power of the FSK signal. Conversely, excessive bandwidth will degrade spectral purity.
- For the wideband FSK modulation, for example when operating in DTS mode, the recommended filter setting can not be reached. However, the impact upon spectral purity will be negligible, due to the already wideband channel.

3.3.7. Power Amplifier

The Power Amplifier (PA) integrated in the SX1212 operates under a regulated voltage supply of 1.8 V. The external PA choke inductor is biased by an internal regulator output made available on pin 29 (VR_PA). Thanks to these features, the PA output power is consistent over the power supply range. This is important for mobile applications where this allows both predictable RF performance and battery life.

3.3.7.1. Rise and Fall Times Control

In OOK mode, the PA ramp times can be accurately controlled through the MCParam_PA_ramp register. Those bits directly control the slew rate of VR_PA output (pin 29).

Table 11: PA Rise/Fall Times

MCParam_PA_ramp	t_{VR_PA}	t_{PA_OUT} (rise / fall)
00	3 us	2.5 / 2 us
01	8.5 us	5 / 3 us
10	15 us	10 / 6 us
11	23 us	20 / 10 us

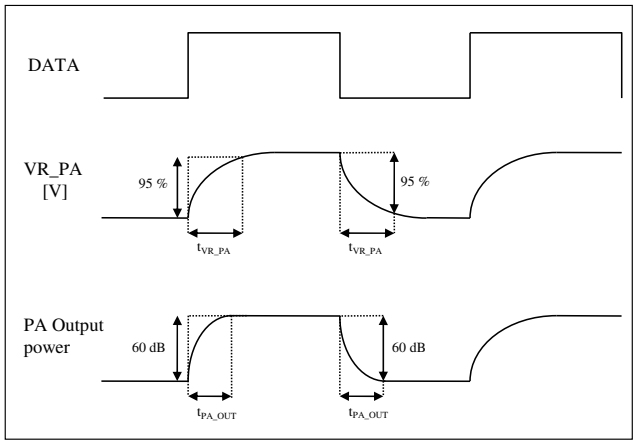

Figure 10: PA Control

3.3.7.2. Optimum Load Impedance (value to confirm)

As the PA and the LNA front-ends in the SX1212 share the same Input/Output pin, they are internally matched to approximately 50 Ω.

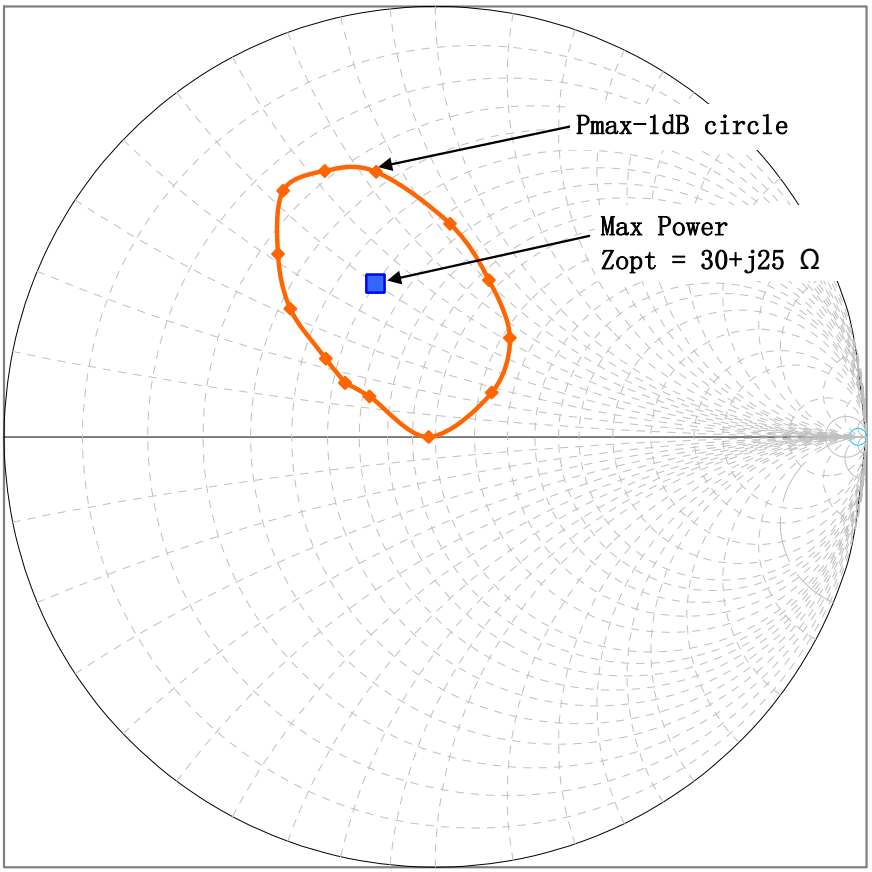

Figure 11: Optimal Load Impedance Chart

Please refer to the reference design section for an optimized PA load setting.

3.3.7.3. Suggested PA Biasing and Matching

The recommended PA bias and matching circuit is illustrated below:

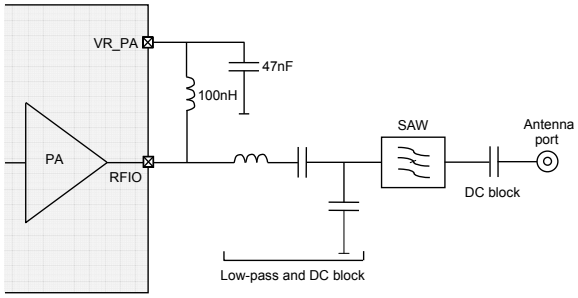

Figure 12: Recommended PA Biasing and Output Matching

Please refer to section 7.5.3 of this document for the optimized matching arrangement for each frequency band.

3.3.8. Common Input and Output Front-End

The receiver and the transmitter share the same RFIO pin (pin 31). Figure 13 below shows the configuration of the common RF front-end.

- In transmit mode, the PA and the PA regulator are active, with the voltage on the VR_PA pin equal to the nominal voltage of the regulator (1.8 V). The external inductance is used to bias the PA.
- In receive mode, both PA and PA regulator are off and VR_PA is tied to ground. The external inductance LT1 is then used to bias the LNA.

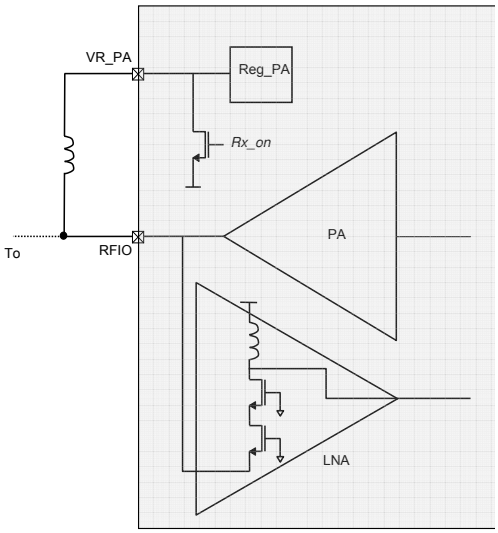

Figure 13: Front-end Description

3.4. Receiver Description

The SX1212 is set to receive mode when MCParam_Chip_mode = 011.

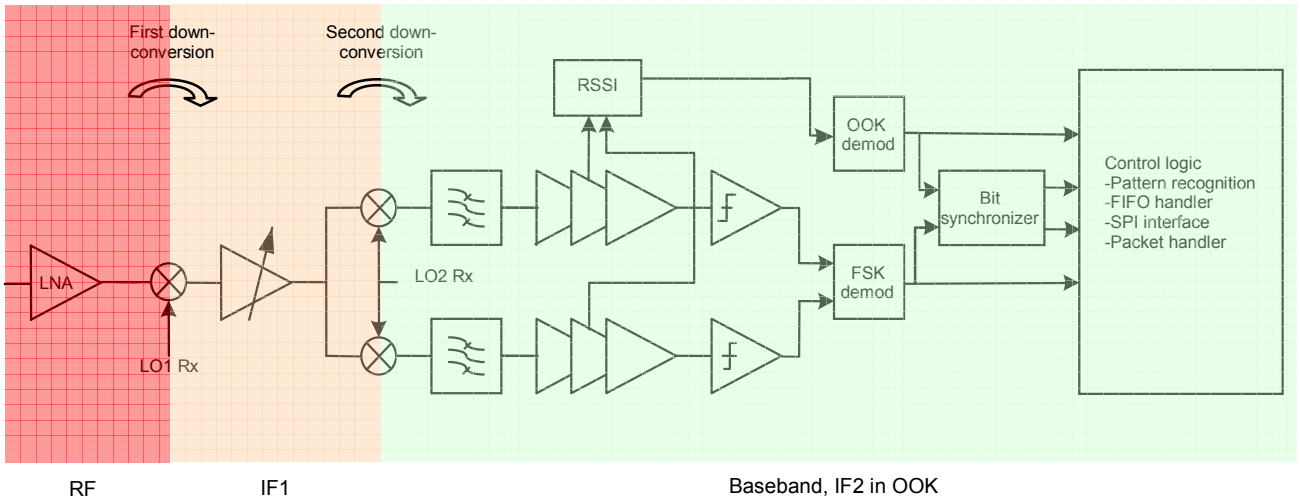

Figure 14: Receiver Architecture

3.4.1. Architecture

The SX1212 receiver employs a super-heterodyne architecture. Here, the first IF is 1/9th of the RF frequency (approximately 100MHz). The second down-conversion down-converts the I and Q signals to base band in the case of the FSK receiver (Zero IF) and to a low-IF (IF2) for the OOK receiver.

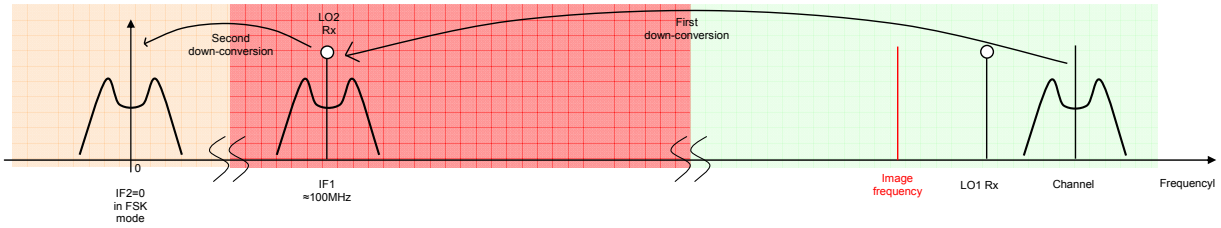

Figure 15: FSK Receiver Setting

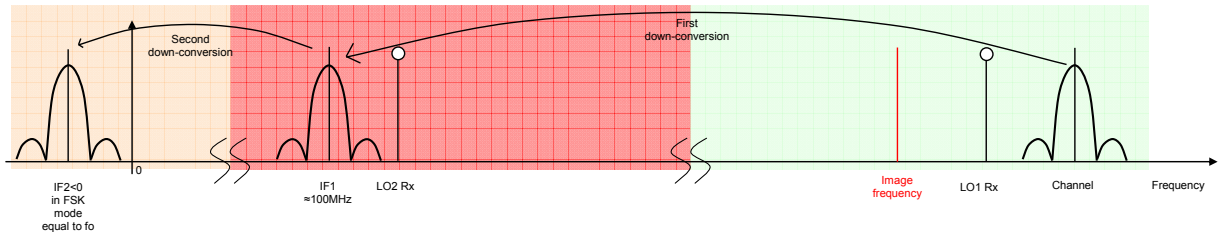

Figure 16: OOK Receiver Setting

After the second down-conversion stage, the received signal is channel-select filtered and amplified to a level adequate for demodulation. Both FSK and OOK demodulation are available. Finally, an optional Bit Synchronizer (BitSync) is provided, to be supply a synchronous clock and data stream to a companion uC in Continuous mode,

or to fill the FIFO buffers with glitch-free data in Buffered mode. The operation of the receiver is now described in detail.

Note: Image rejection is achieved by the SAW filter.

3.4.2. LNA and First Mixer

In receive mode, the RFIO pin is connected to a fixed gain, common-gate, Low Noise Amplifier (LNA). The performance of this amplifier is such that the Noise Figure (NF) of the receiver can be estimated to be ≈7 dB.

3.4.3. IF Gain and Second I/Q Mixer

Following the LNA and first down-conversion, there is an IF amplifier whose gain can be programmed from -13.5 dB to 0 dB in 4.5 dB steps, via the register MCParam_IF_gain. The default setting corresponds to 0 dB gain, but lower values can be used to increase the RSSI dynamic range. Refer to section 3.4.7 for additional information.

3.4.4. Channel Filters

The second mixer stages are followed by the channel select filters. The channel select filters have a strong influence on the noise bandwidth and selectivity of the receiver and hence its sensitivity. Each filter comprises a passive and active section.

3.4.4.1. Passive Filter

Each channel select filter features a passive second-order RC filter, with a bandwidth programmable through the bits RXParam_PassiveFilt. As the wider of the two filters, its effect on the sensitivity is negligible, but its bandwidth has to be setup instead to optimize blocking immunity. The value entered into this register sets the single side bandwidth of this filter. For optimum performance it should be set to 3 to 4 times the cutoff frequency of the active Butterworth (or polyphase) filter described in the next section.

$$3 * Fc_{ButterfFilt} \leq BW_{passive,filter} \leq 4 * Fc_{ButterFilt}$$

3.4.4.2. Active Filter

The 'fine' channel selection is performed by an active, third-order, Butterworth filter, which acts as a low-pass filter for the zero-IF configuration (FSK), or a complex polyphase filter for the Low-IF (OOK) configuration. The RXParam_PolypFilt_on bit enables/disables the polyphase filter.

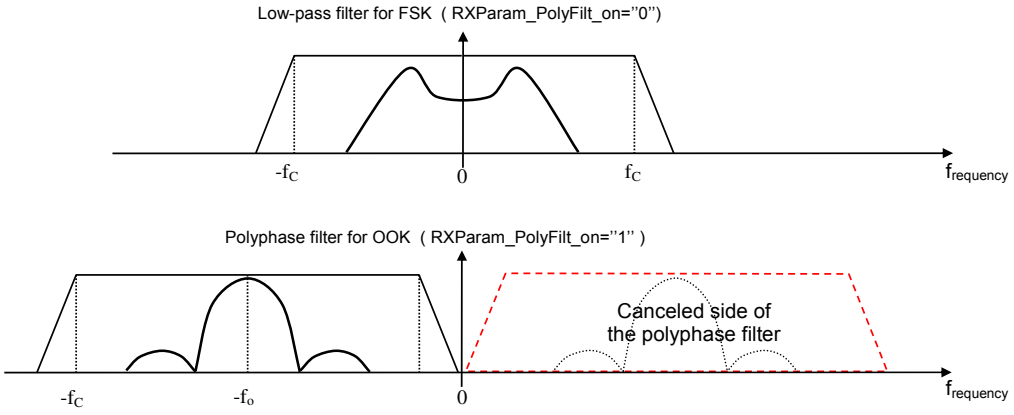

Figure 17: Active Channel Filter Description

As can be seen from Figure 17, the required bandwidth of this filter varies between the two demodulation modes.

- FSK mode: The 99% energy bandwidth of an FSK modulated signal is approximated to be:

$$BW_{99\%,FSK} = 2 * \left[Fdev + \frac{BR}{2} \right]$$

The bits RXParam_ButterFilt set fc, the cutoff frequency of the filter. As we are in a Zero-IF configuration, the FSK lobes are centered around the virtual “DC” frequency. The choice of fc should be such that the modulated signal falls in the filter bandwidth, anticipating the Local Oscillator frequency drift over the operating temperature and aging of the device:

$$2 * fc > BW_{99\%,FSK} + LO_{drifts}$$

Please refer to the charts in section 3.4.5 for an accurate overview of the filter bandwidth vs. setting.

- OOK mode: The 99% energy bandwidth of an OOK modulated signal is approximated to be:

$$BW_{99\%,OOK} = \frac{2}{Tbit} = 2.BR$$

The bits RXParam_PolypFilt_center set fo, the center frequency of the polyphase filter when activated. fo should always be chosen to be equal to the low Intermediate Frequency of the receiver (IF2). This is why, in the GUI described in section 7.2.1 of this document, the low IF frequency of the OOK receiver denoted IF2 has been replaced by fo.

The following setting is recommended:

$$fo = 100kHz$$
$$RXParam\_PolypFilt = "0011"$$

The value stored in RXParam_ButterFilt determines fc, the filter cut-off frequency. So the user should set fc according to:

$$2 * (fc - fo) > BW_{99\%,OOK} + LO_{drifts}$$

Again, fc as a function of RXParam_ButterFilt is given in the section 3.4.6.

3.4.5. Channel Filters Setting in FSK Mode

Fc, the 3dB cutoff frequency of the Butterworth filter used in FSK reception, is programmed through the bit RXParam_ButterFilt. However, the whole receiver chain influences this cutoff frequency. Thus the channel select and resultant filter bandwidths are summarized in the following chart: