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Features

- Core
  - ARM® Cortex®-M3 revision 2.0 running at up to 48 MHz
  - Thumb®-2 instruction
  - 24-bit SysTick Counter
  - Nested Vector Interrupt Controller
- Pin-to-pin compatible with SAM7S legacy products (48- and 64-pin versions) and SAM3S (48-, 64- and 100-pin versions)
- Memories
  - From 16 to 256 Kbytes embedded Flash, 128-bit wide access, memory accelerator, single plane
  - From 4 to 24 Kbytes embedded SRAM
  - 16 Kbytes ROM with embedded bootloader routines (UART) and IAP routines
- System
  - Embedded voltage regulator for single supply operation
  - Power-on-Reset (POR), Brown-out Detector (BOD) and Watchdog for safe operation
  - Quartz or ceramic resonator oscillators: 3 to 20 MHz main power with Failure Detection and optional low power 32.768 kHz for RTC or device clock
  - High precision 8/12 MHz factory trimmed internal RC oscillator with 4 MHz default frequency for device startup. In-application trimming access for frequency adjustment
  - Slow Clock Internal RC oscillator as permanent low-power mode device clock
  - One PLL up to 130 MHz for device clock
  - Up to 10 peripheral DMA (PDC) channels
- Low Power Modes
  - Sleep and Backup modes, down to 3 µA in Backup mode
  - Ultra low power RTC
- Peripherals
  - Up to 2 USARTs with RS-485 and SPI mode support. One USART (USART0) has ISO7816, IrDA® and PDC support in addition
  - Two 2-wire UARTs
  - 2 Two Wire Interface (I2C compatible), 1 SPI
  - Up to 6 Three-Channel 16-bit Timer/Counter with capture, waveform, compare and PWM mode. Quadrature Decoder Logic and 2-bit Gray Up/Down Counter for Stepper Motor
  - 4-channel 16-bit PWM
  - 32-bit Real-time Timer and RTC with calendar and alarm features
  - Up to 16 channels, 384 KSPS 10-bit ADC
  - One 500 KSPS 10-bit DAC
- I/O
  - Up to 79 I/O lines with external interrupt capability (edge or level sensitivity), debouncing, glitch filtering and on-die Series Resistor Termination
  - Three 32-bit Parallel Input/Output Controllers
- Packages
  - 100-lead LQFP, 14 x 14 mm, pitch 0.5 mm/100-ball TFBGA, 9 x 9 mm, pitch 0.8 mm
  - 64-lead LQFP, 10 x 10 mm, pitch 0.5 mm/64-pad QFN 9x9 mm, pitch 0.5 mm
  - 48-lead LQFP, 7 x 7 mm, pitch 0.5 mm/48-pad QFN 7x7 mm, pitch 0.5 mm

AT91SAM ARM-based Flash MCU

SAM3N Series

Summary

11011BS–ATARM–22-Feb-12

1. SAM3N Description

Atmel's SAM3N series is a member of a family of Flash microcontrollers based on the high performance 32-bit ARM Cortex-M3 RISC processor. It operates at a maximum speed of 48 MHz and features up to 256 Kbytes of Flash and up to 24 Kbytes of SRAM. The peripheral set includes 2x USARTs, 2x UARTs, 2x TWIs, 3x SPI, as well as 1 PWM timer, 6x general purpose 16-bit timers, an RTC, a 10-bit ADC and a 10-bit DAC.

The SAM3N series is ready for capacitive touch thanks to the QTouch library, offering an easy way to implement buttons, wheels and sliders.

The SAM3N device is an entry-level general purpose microcontroller. That makes the SAM3N the ideal starting point to move from 8- /16-bit to 32-bit microcontrollers.

It operates from 1.62V to 3.6V and is available in 48-pin, 64-pin and 100-pin QFP, 48-pin and 64-pin QFN, and 100-pin BGA packages.

The SAM3N series is the ideal migration path from the SAM3S for applications that require a reduced BOM cost. The SAM3N series is pin-to-pin compatible with the SAM3S series. Its aggressive price point and high level of integration pushes its scope of use far into cost-sensitive, high-volume applications.

1.1 Configuration Summary

The SAM3N4/2/1/0/00 differ in memory size, package and features list. Table 1-1 summarizes the configurations of the 9 devices.

Table 1-1. Configuration Summary

Device	Flash	SRAM	Package	Number of PIOs	ADC	Timer	PDC Channels	USART	DAC
SAM3N4A	256 Kbytes	24 Kbytes	LQFP48 QFN48	34	8 channels	6(1)	8	1	_
SAM3N4B	256 Kbytes	24 Kbytes	LQFP64 QFN64	47	10 channels	6(2)	10	2	1
SAM3N4C	256 Kbytes	24 Kbytes	LQFP100 BGA100	79	16 channels	6	10	2	1
SAM3N2A	128 Kbytes	16 Kbytes	LQFP48 QFN48	34	8 channels	6(1)	8	1	_
SAM3N2B	128 Kbytes	16 Kbytes	LQFP64 QFN64	47	10 channels	6((2)	10	2	1
SAM3N2C	128 Kbytes	16 Kbytes	LQFP100 BGA100	79	16 channels	6	10	2	1
SAM3N1A	64 Kbytes	8 Kbytes	LQFP48 QFN48	34	8 channels	6(1)	8	1	_
SAM3N1B	64 Kbytes	8 Kbytes	LQFP64 QFN64	47	10 channels	6(2)	10	2	1
SAM3N1C	64 Kbytes	8 Kbytes	LQFP100 BGA100	79	16 channels	6	10	2	1
SAM3N0A	32 Kbytes	8 Kbytes	LQFP48 QFN48	34	8 channels	6(1)	8	1	_
SAM3N0B	32 Kbytes	8 Kbytes	LQFP64 QFN64	47	10 channels	6(2)	10	2	1
SAM3N0C	32 Kbytes	8 Kbytes	LQFP100 BGA100	79	16 channels	6	10	2	1
SAM3N00A	16 Kbytes	4 KBytes	LQFP48 QFN48	34	8 channels	6(1)	8	1	_
SAM3N00B	16 Kbytes	4 KBytes	LQFP64 QFN64	47	10 channels	6(2)	10	2	1

Notes: 1. Only two TC channels are accessible through the PIO.
2. Only three TC channels are accessible through the PIO.

2. SAM3N Block Diagram

Figure 2-1. SAM3N 100-pin version Block Diagram

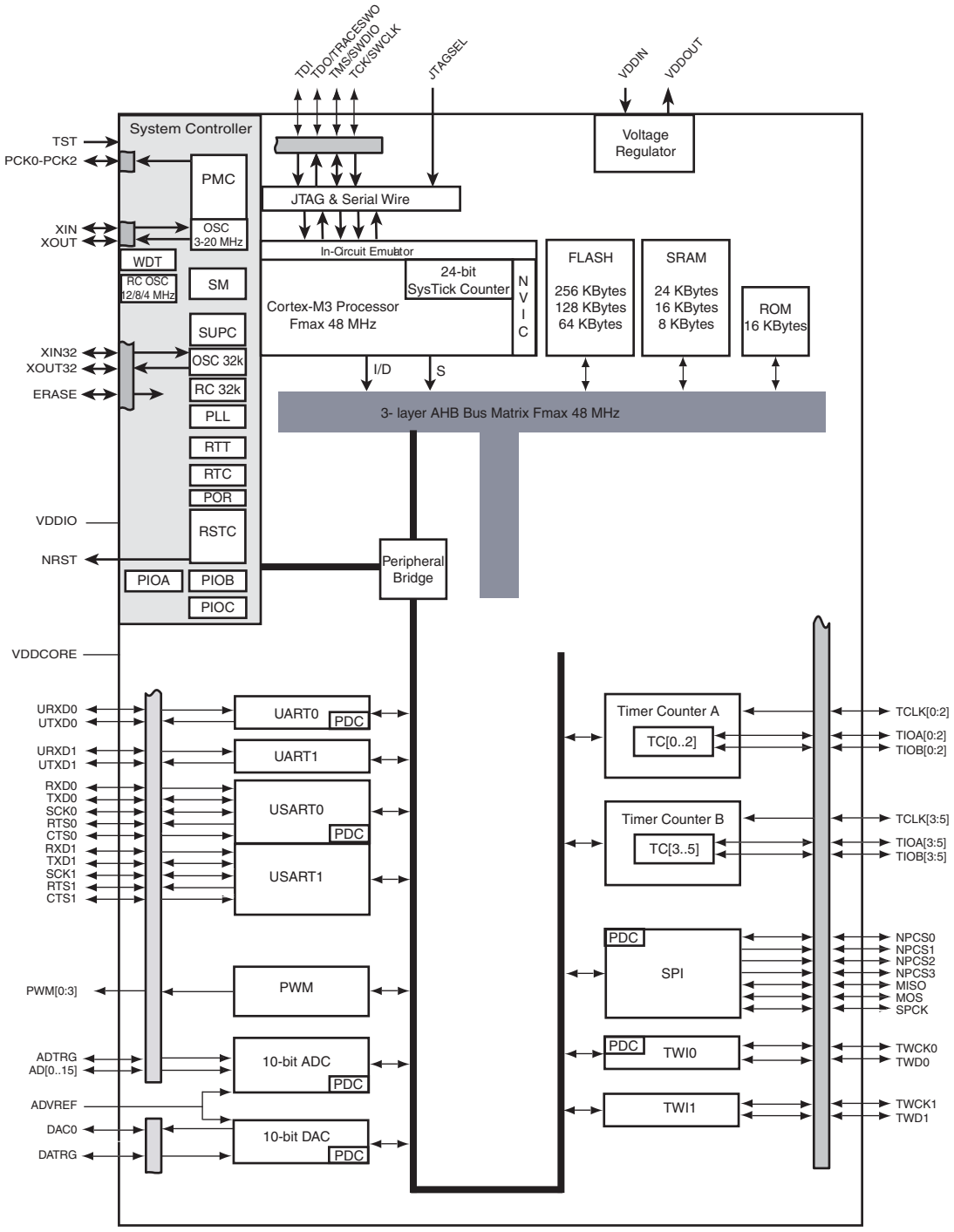


Figure 2-2. SAM3N 64-pin version Block Diagram

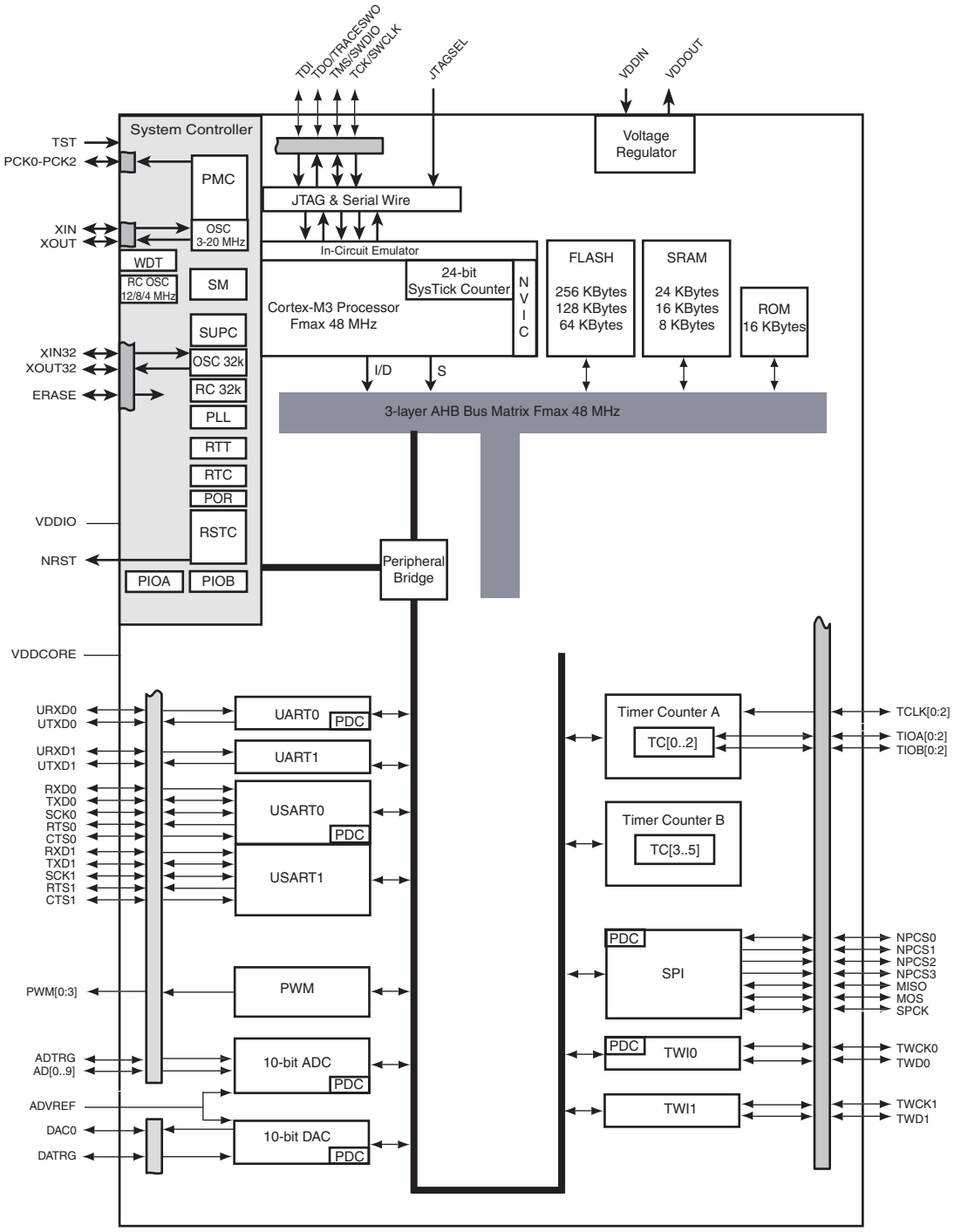
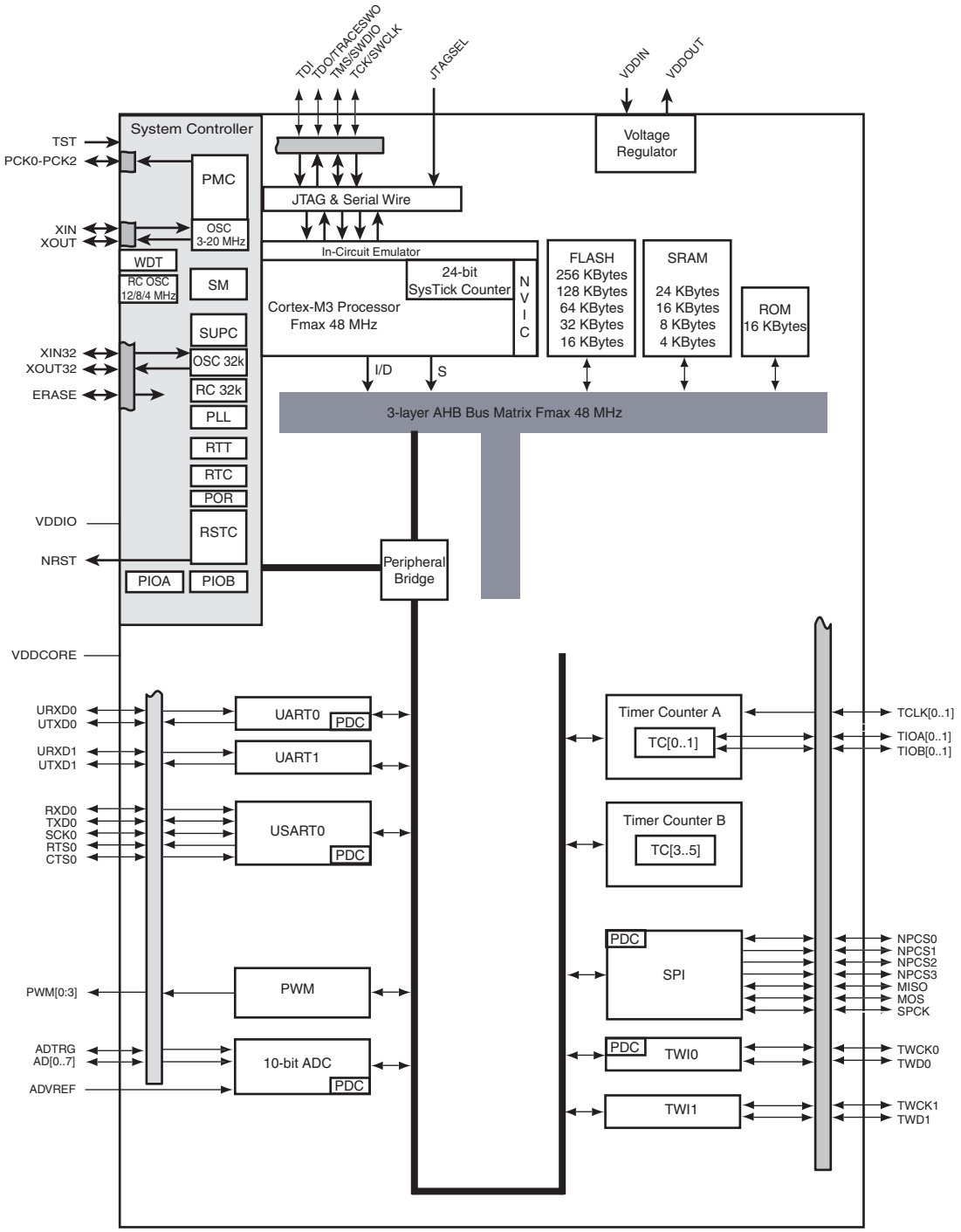


Figure 2-3. SAM3N 48-pin version Block Diagramz



3. Signal Description

Table 3-1 gives details on the signal name classified by peripheral.

Table 3-1. Signal Description List

Signal Name	Function	Type	Active Level	Voltage Reference	Comments
Power Supplies					
VDDIO	Peripherals I/O Lines Power Supply	Power			1.62V to 3.6V
VDDIN	Voltage Regulator, ADC and DAC Power Supply	Power			1.8V to 3.6V(3)
VDDOUT	Voltage Regulator Output	Power			1.8V Output
VDDPLL	Oscillator and PLL Power Supply	Power			1.65 V to 1.95V
VDDCORE	Power the core, the embedded memories and the peripherals	Power			1.65V to 1.95V Connected externally to VDDOUT
GND	Ground	Ground			
Clocks, Oscillators and PLLs					
XIN	Main Oscillator Input	Input		VDDIO	Reset State: - PIO Input - Internal Pull-up disabled - Schmitt Trigger enabled(1)
XOUT	Main Oscillator Output	Output			
XIN32	Slow Clock Oscillator Input	Input			
XOUT32	Slow Clock Oscillator Output	Output			
PCK0 - PCK2	Programmable Clock Output	Output			Reset State: - PIO Input - Internal Pull-up enabled - Schmitt Trigger enabled(1)
ICE and JTAG					
TCK/SWCLK	Test Clock/Serial Wire Clock	Input		VDDIO	Reset State: - SWJ-DP Mode - Internal pull-up disabled - Schmitt Trigger enabled(1)
TDI	Test Data In	Input			
TDO/TRACESWO	Test Data Out/Trace Asynchronous Data Out	Output			
TMS/SWDIO	Test Mode Select /Serial Wire Input/Output	Input / I/O			
JTAGSEL	JTAG Selection	Input	High		Permanent Internal pull-down

Table 3-1. Signal Description List (Continued)

Signal Name	Function	Type	Active Level	Voltage Reference	Comments
Flash Memory					
ERASE	Flash and NVM Configuration Bits Erase Command	Input	High	VDDIO	Reset State: - Erase Input - Internal pull-down enabled - Schmitt Trigger enabled(1)
Reset/Test					
NRST	Microcontroller Reset	I/O	Low	VDDIO	Permanent Internal pull-up
TST	Test Mode Select	Input		VDDIO	Permanent Internal pull-down
Universal Asynchronous Receiver Transceiver - UARTx					
URXDx	UART Receive Data	Input			
UTXDx	UART Transmit Data	Output			
PIO Controller - PIOA - PIOB - PIOC					
PA0 - PA31	Parallel IO Controller A	I/O		VDDIO	Reset State: - PIO or System IOs(2) - Internal pull-up enabled - Schmitt Trigger enabled(1)
PB0 - PB14	Parallel IO Controller B	I/O			
PC0 - PC31	Parallel IO Controller C	I/O			
Universal Synchronous Asynchronous Receiver Transmitter USARTx					
SCKx	USARTx Serial Clock	I/O			
TXDx	USARTx Transmit Data	I/O			
RXDx	USARTx Receive Data	Input			
RTSx	USARTx Request To Send	Output			
CTSx	USARTx Clear To Send	Input			
Timer/Counter - TC					
TCLKx	TC Channel x External Clock Input	Input			
TIOAx	TC Channel x I/O Line A	I/O			
TIOBx	TC Channel x I/O Line B	I/O			
Pulse Width Modulation Controller- PWMC					
PWMx	PWM Waveform Output for channel x	Output			

Table 3-1. Signal Description List (Continued)

Signal Name	Function	Type	Active Level	Voltage Reference	Comments
Serial Peripheral Interface - SPI					
MISO	Master In Slave Out	I/O			
MOSI	Master Out Slave In	I/O			
SPCK	SPI Serial Clock	I/O			
SPI_NPCS0	SPI Peripheral Chip Select 0	I/O	Low		
SPI_NPCS1 - SPI_NPCS3	SPI Peripheral Chip Select	Output	Low		
Two-Wire Interface- TWIx					
TWDx	TWIx Two-wire Serial Data	I/O			
TWCKx	TWIx Two-wire Serial Clock	I/O			
Analog					
ADVREF	ADC and DAC Reference	Analog			
10-bit Analog-to-Digital Converter - ADC					
AD0 - AD15	Analog Inputs	Analog			
ADTRG	ADC Trigger	Input		VDDIO	
Digital-to-Analog Converter Controller- DACC					
DAC0	DACC channel analog output	Analog			
DATRG	DACC Trigger	Input		VDDIO	
Fast Flash Programming Interface					
PGMEN0-PGMEN2	Programming Enabling	Input		VDDIO	
PGMM0-PGMM3	Programming Mode	Input			
PGMD0-PGMD15	Programming Data	I/O			
PGMRDY	Programming Ready	Output	High		
PGMNVALID	Data Direction	Output	Low		
PGMNOE	Programming Read	Input	Low		
PGMCK	Programming Clock	Input			
PGMNCMD	Programming Command	Input	Low		

Notes: 1. Schmitt Triggers can be disabled through PIO registers.
2. Some PIO lines are shared with System IOs.
3. See Section 5.3 “Typical Powering Schematics” for restriction on voltage range of Analog Cells.

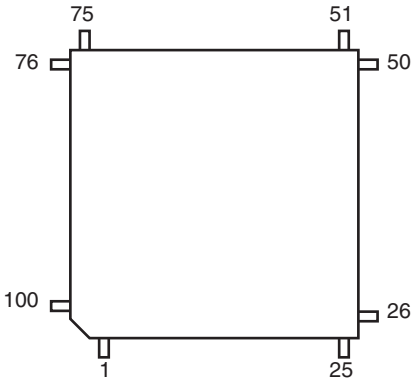
4. Package and Pinout

SAM3N4/2/1/0/00 series is pin-to-pin compatible with SAM3S products. Furthermore SAM3N4/2/1/0/00 devices have new functionalities referenced in italic inTable 4-1, Table 4-3 and Table 4-4.

4.1 SAM3N4/2/1/0/00C Package and Pinout

4.1.1 100-lead LQFP Package Outline

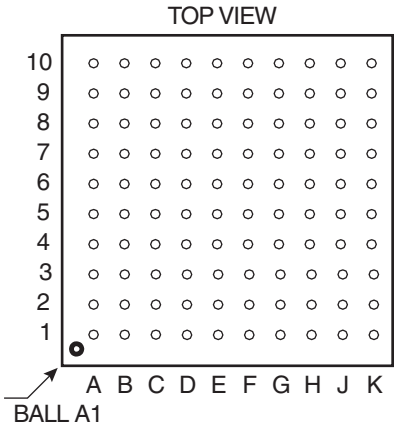
Figure 4-1. Orientation of the 100-lead LQFP Package



4.1.2 100-ball TFBGA Package Outline

The 100-Ball TFBGA package has a 0.8 mm ball pitch and respects Green Standards. Its dimensions are 9 x 9 x 1.1 mm.

Figure 4-2. Orientation of the 100-ball TFBGA Package



4.1.3 100-Lead LQFP Pinout

Table 4-1. 100-lead LQFP SAM3N4/2/1/0/00C Pinout

1	ADVREF	26	GND	51	TDI/PB4	76	TDO/TRACESWO/PB5
2	GND	27	VDDIO	52	PA6/PGMNOE	77	JTAGSEL
3	PB0/AD4	28	PA16/PGMD4	53	PA5/PGMRDY	78	PC18
4	PC29/AD13	29	PC7	54	PC28	79	TMS/SWDIO/PB6
5	PB1/AD5	30	PA15/PGMD3	55	PA4/PGMNCMD	80	PC19
6	PC30/AD14	31	PA14/PGMD2	56	VDDCORE	81	PA31
7	PB2/AD6	32	PC6	57	PA27	82	PC20
8	PC31/AD15	33	PA13/PGMD1	58	PC8	83	TCK/SWCLK/PB7
9	PB3/AD7	34	PA24	59	PA28	84	PC21
10	VDDIN	35	PC5	60	NRST	85	VDDCORE
11	VDDOUT	36	VDDCORE	61	TST	86	PC22
12	PA17/PGMD5/AD0	37	PC4	62	PC9	87	ERASE/PB12
13	PC26	38	PA25	63	PA29	88	PB10
14	PA18/PGMD6/AD1	39	PA26	64	PA30	89	PB11
15	PA21/AD8	40	PC3	65	PC10	90	PC23
16	VDDCORE	41	PA12/PGMD0	66	PA3	91	VDDIO
17	PC27	42	PA11/PGMM3	67	PA2/PGMEN2	92	PC24
18	PA19/PGMD7/AD2	43	PC2	68	PC11	93	PB13/DAC0
19	PC15/AD11	44	PA10/PGMM2	69	VDDIO	94	PC25
20	PA22/AD9	45	GND	70	GND	95	GND
21	PC13/AD10	46	PA9/PGMM1	71	PC14	96	PB8/XOUT
22	PA23	47	PC1	72	PA1/PGMEN1	97	PB9/*PGMCK/XIN*
23	PC12/AD12	48	PA8/XOUT32/ PGMM0	73	PC16	98	VDDIO
24	PA20/AD3	49	PA7/XIN32/ PGMNVALID	74	PA0/PGMEN0	99	PB14
25	PC0	50	VDDIO	75	PC17	100	VDDPLL

4.1.4 100-ball TFBGA Pinout

Table 4-2. 100-ball TFBGA SAM3N4/2/1/0/00C Pinout

A1	PB1	C6	PB7	F1	PA18	H6	PC4
A2	PC29	C7	PC16	F2	PC26	H7	PA11
A3	VDDIO	C8	PA1	F3	VDDOUT	H8	PC1
A4	PB9	C9	PC17	F4	GND	H9	PA6
A5	PB8	C10	PA0	F5	VDDIO	H10	PB4
A6	PB13	D1	PB3	F6	PA27	J1	PC15
A7	PB11	D2	PB0	F7	PC8	J2	PC0
A8	PB10	D3	PC24	F8	PA28	J3	PA16
A9	PB6	D4	PC22	F9	TST	J4	PC6
A10	JTAGSEL	D5	GND	F10	PC9	J5	PA24
B1	PC30	D6	GND	G1	PA21	J6	PA25
B2	ADVREF	D7	VDDCORE	G2	PC27	J7	PA10
B3	GNDANA	D8	PA2	G3	PA15	J8	GND
B4	PB14	D9	PC11	G4	VDDCORE	J9	VDDCORE
B5	PC21	D10	PC14	G5	VDDCORE	J10	VDDIO
B6	PC20	E1	PA17	G6	PA26	K1	PA22
B7	PA31	E2	PC31	G7	PA12	K2	PC13
B8	PC19	E3	VDDIN	G8	PC28	K3	PC12
B9	PC18	E4	GND	G9	PA4	K4	PA20
B10	PB5	E5	GND	G10	PA5	K5	PC5
C1	PB2	E6	NRST	H1	PA19	K6	PC3
C2	VDDPLL	E7	PA29	H2	PA23	K7	PC2
C3	PC25	E8	PA30	H3	PC7	K8	PA9
C4	PC23	E9	PC10	H4	PA14	K9	PA8
C5	PB12	E10	PA3	H5	PA13	K10	PA7

4.2 SAM3N4/2/1/0/00B Package and Pinout

Figure 4-3. Orientation of the 64-pad QFN Package

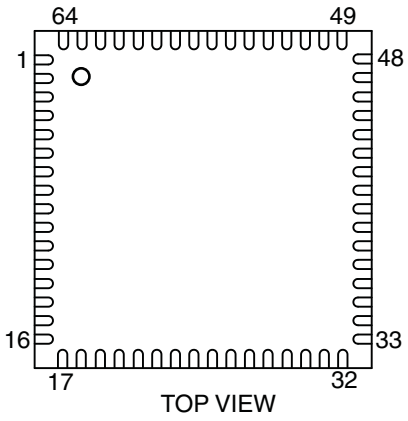
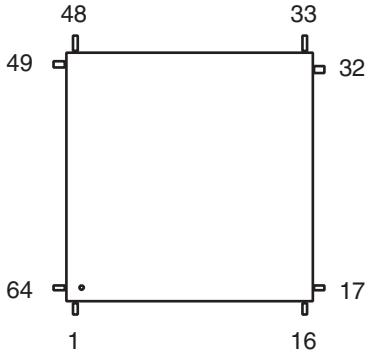


Figure 4-4. Orientation of the 64-lead LQFP Package



4.2.1 64-Lead LQFP and QFN Pinout

64-pin version SAM3N devices are pin-to-pin compatible with SAM3S products. Furthermore, SAM3N products have new functionalities shown in italic in Table 4-3.

Table 4-3. 64-pin SAM3N4/2/1/0/00B Pinout

1	ADVREF	17	GND	33	*TDI/PB4*	49	*TDO/TRACESWO/PB5*
2	GND	18	VDDIO	34	PA6/PGMNOE	50	JTAGSEL
3	*PB0/AD4*	19	PA16/PGMD4	35	PA5/PGMRDY	51	*TMS/SWDIO/PB6*
4	*PB1AD5*	20	PA15/PGMD3	36	PA4/PGMNCMD	52	PA31
5	*PB2/AD6*	21	PA14/PGMD2	37	PA27/PGMD15	53	*TCK/SWCLK/PB7*
6	*PB3/AD7*	22	PA13/PGMD1	38	PA28	54	VDDCORE
7	VDDIN	23	PA24/PGMD12	39	NRST	55	*ERASE/PB12*
8	VDDOUT	24	VDDCORE	40	TST	56	*PB10*
9	PA17/PGMD5/AD0	25	PA25/PGMD13	41	PA29	57	*PB11*
10	PA18/PGMD6/AD1	26	PA26/PGMD14	42	PA30	58	VDDIO
11	PA21/PGMD9/AD8	27	PA12/PGMD0	43	PA3	59	*PB13/DAC0*
12	VDDCORE	28	PA11/PGMM3	44	PA2/PGMEN2	60	GND
13	PA19/PGMD7/AD2	29	PA10/PGMM2	45	VDDIO	61	*XOUT/PB8*
14	PA22/PGMD10/AD9	30	PA9/PGMM1	46	GND	62	*XIN/PGMCK/PB9*
15	PA23/PGMD11	31	PA8/XOUT32/PGMM0	47	PA1/PGMEN1	63	*PB14*
16	PA20/PGMD8/AD3	32	PA7/XIN32/XOUT32/PGMNVALID	48	PA0/PGMEN0	64	VDDPLL

Note: The bottom pad of the QFN package must be connected to ground.

4.3 SAM3N4/2/1/0/00A Package and Pinout

Figure 4-5. Orientation of the 48-pad QFN Package

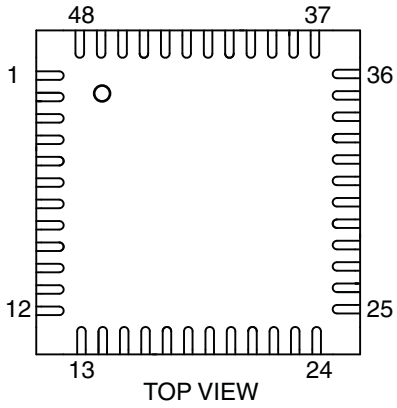
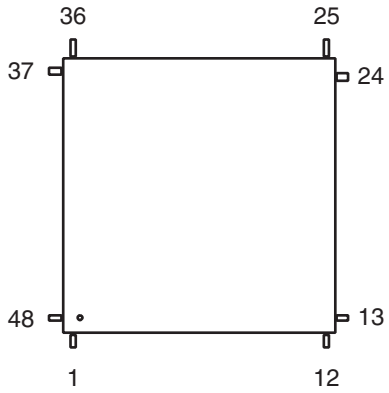


Figure 4-6. Orientation of the 48-lead LQFP Package



4.3.1 48-Lead LQFP and QFN Pinout

Table 4-4. 48-pin SAM3N4/2/1/0/00A Pinout

1	ADVREF	13	VDDIO	25	*TDI/PB4*	37	*TDO/TRACESWO/ PB5*
2	GND	14	PA16/PGMD4	26	PA6/PGMNOE	38	JTAGSEL
3	*PB0/AD4*	15	PA15/PGMD3	27	PA5/PGMRDY	39	*TMS/SWDIO/PB6*
4	*PB1/AD5*	16	PA14/PGMD2	28	PA4/PGMNCMD	40	*TCK/SWCLK/PB7*
5	*PB2/AD6*	17	PA13/PGMD1	29	NRST	41	VDDCORE
6	*PB3/AD7*	18	VDDCORE	30	TST	42	*ERASE/PB12*
7	VDDIN	19	PA12/PGMD0	31	PA3	43	*PB10*
8	VDDOUT	20	PA11/PGMM3	32	PA2/PGMEN2	44	*PB11*
9	PA17/PGMD5/AD0	21	PA10/PGMM2	33	VDDIO	45	*XOUT/PB8*
10	PA18/PGMD6/AD1	22	PA9/PGMM1	34	GND	46	*XIN/P/PB9/GMCK*
11	PA19/PGMD7/AD2	23	PA8/XOUT32/PG MM0	35	PA1/PGMEN1	47	VDDIO
12	PA20/AD3	24	PA7/XIN32/PGMN VALID	36	PA0/PGMEN0	48	VDDPLL

Note: The bottom pad of the QFN package must be connected to ground.

5. Power Considerations

5.1 Power Supplies

The SAM3N product has several types of power supply pins:

- VDDCORE pins: Power the core, including the processor, the embedded memories and the peripherals. Voltage ranges from 1.62V and 1.95V.
- VDDIO pins: Power the Peripherals I/O lines, Backup part, 32 kHz crystal oscillator and oscillator pads. Voltage ranges from 1.62V and 3.6V
- VDDIN pin: Voltage Regulator, ADC and DAC Power Supply. Voltage ranges from 1.8V to 3.6V for the Voltage Regulator
- VDDPLL pin: Powers the PLL, the Fast RC and the 3 to 20 MHz oscillators. Voltage ranges from 1.62V and 1.95V.

5.2 Voltage Regulator

The SAM3N embeds a voltage regulator that is managed by the Supply Controller.

This internal regulator is intended to supply the internal core of SAM3N. It features two different operating modes:

- In Normal mode, the voltage regulator consumes less than 700 µA static current and draws 60 mA of output current. Internal adaptive biasing adjusts the regulator quiescent current depending on the required load current. In Wait Mode quiescent current is only 7 µA.
- In Backup mode, the voltage regulator consumes less than 1 µA while its output (VDDOUT) is driven internally to GND. The default output voltage is 1.80V and the start-up time to reach Normal mode is less than100 µs.

For adequate input and output power supply decoupling/bypassing, refer to the Voltage Regulator section in the Electrical Characteristics section of the datasheet.

5.3 Typical Powering Schematics

The SAM3N supports a 1.62V-3.6V single supply mode. The internal regulator input connected to the source and its output feeds VDDCORE. Figure 5-1 shows the power schematics.

As VDDIN powers the voltage regulator and the ADC/DAC, when the user does not want to use the embedded voltage regulator, it can be disabled by software via the SUPC (note that it is different from Backup mode).

Figure 5-1. Single Supply

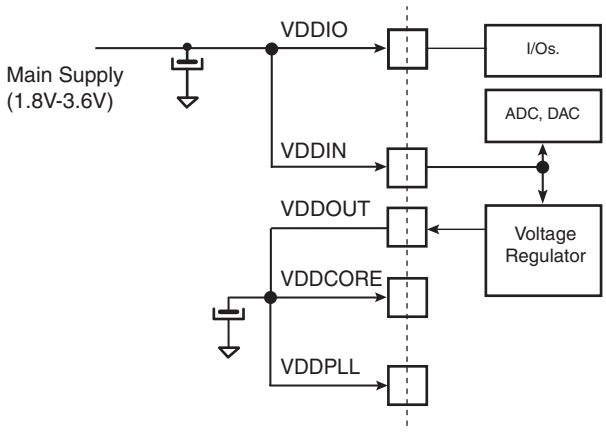
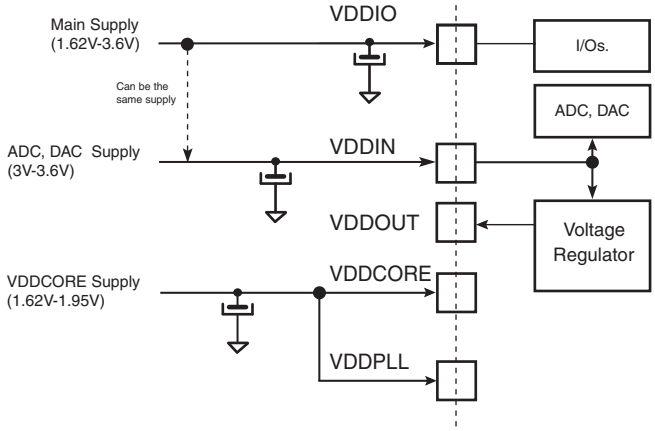


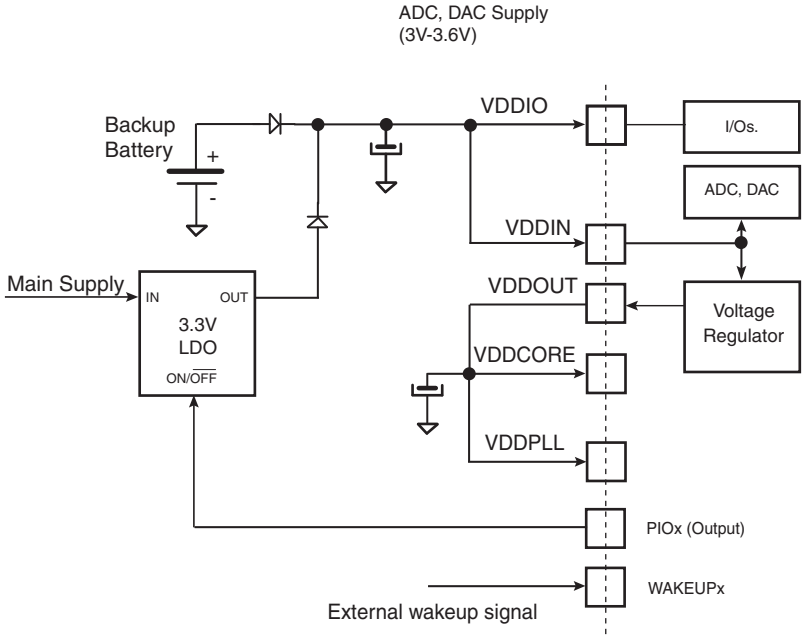
Figure 5-2. Core Externally Supplied



Note: Restrictions
With Main Supply < 3V, ADC and DAC are not usable.
With Main Supply >= 3V, all peripherals are usable.

Figure 5-3 below provides an example of the powering scheme when using a backup battery. Since the PIO state is preserved when in backup mode, any free PIO line can be used to switch off the external regulator by driving the PIO line at low level (PIO is input, pull-up enabled after backup reset). External wake-up of the system can be from a push button or any signal. See Section 5.6 “Wake-up Sources” for further details.TFBGA

Figure 5-3. Core Externally Supplied (backup battery)



Note: The two diodes provide a "switchover circuit" (for illustration purpose) between the backup battery and the main supply when the system is put in backup mode.

5.4 Active Mode

Active mode is the normal running mode with the core clock running from the fast RC oscillator, the main crystal oscillator or the PLL. The power management controller can be used to adapt the frequency and to disable the peripheral clocks.

5.5 Low Power Modes

The various low-power modes of the SAM3N are described below:

5.5.1 Backup Mode

The purpose of backup mode is to achieve the lowest power consumption possible in a system that is performing periodic wakeups to carry out tasks but not requiring fast startup time (<0.1ms). Total current consumption is 3 µA typical.

The Supply Controller, zero-power power-on reset, RTT, RTC, Backup registers and 32 kHz oscillator (RC or crystal oscillator selected by software in the Supply Controller) are running. The regulator and the core supply are off.

Backup mode is based on the Cortex-M3 deep sleep mode with the voltage regulator disabled.

The SAM3N can be awakened from this mode through WUP0-15 pins, the supply monitor (SM), the RTT or RTC wake-up event.

Backup mode is entered by using WFE instructions with the SLEEPDEEP bit in the System Control Register of the Cortex-M3 set to 1. (See the Power management description in The ARM Cortex M3 Processor section of the product datasheet).

Exit from Backup mode happens if one of the following enable wake-up events occurs:

- WKUPEN0-15 pins (level transition, configurable debouncing)

- Supply Monitor alarm
- RTC alarm
- RTT alarm

5.5.2 Wait Mode

The purpose of the wait mode is to achieve very low power consumption while maintaining the whole device in a powered state for a startup time of less than 10 µs. Current Consumption in Wait mode is typically 15 µA (total current consumption) if the internal voltage regulator is used or 8 µA if an external regulator is used.

In this mode, the clocks of the core, peripherals and memories are stopped. However, the core, peripherals and memories power supplies are still powered. From this mode, a fast start up is available.

This mode is entered via Wait for Event (WFE) instructions with LPM = 1 (Low Power Mode bit in PMC_FSMR). The Cortex-M3 is able to handle external or internal events in order to wake up the core (WFE). By configuring the WUP0-15 external lines as fast startup wake-up pins (refer to Section 5.7 “Fast Start-Up”). RTC or RTT Alarm wake-up events can be used to wake up the CPU (exit from WFE).

Entering Wait Mode:

- Select the 4/8/12 MHz fast RC oscillator as Main Clock
- Set the LPM bit in the PMC Fast Startup Mode Register (PMC_FSMR)
- Execute the Wait-For-Event (WFE) instruction of the processor

Note: Internal Main clock resynchronization cycles are necessary between the writing of MOSCRCEN bit and the effective entry in Wait mode. Depending on the user application, Waiting for MOSCRCEN bit to be cleared is recommended to ensure that the core will not execute undesired instructions.

5.5.3 Sleep Mode

The purpose of sleep mode is to optimize power consumption of the device versus response time. In this mode, only the core clock is stopped. The peripheral clocks can be enabled. The current consumption in this mode is application dependent.

This mode is entered via Wait for Interrupt (WFI) or Wait for Event (WFE) instructions with LPM = 0 in PMC_FSMR.

The processor can be woke up from an interrupt if WFI instruction of the Cortex M3 is used, or from an event if the WFE instruction is used to enter this mode.

5.5.4 Low Power Mode Summary Table

The modes detailed above are the main low power modes. Each part can be set to on or off separately and wake up sources can be individually configured. Table 5-1 below shows a summary of the configurations of the low power modes.

Table 5-1. Low Power Mode Configuration Summary

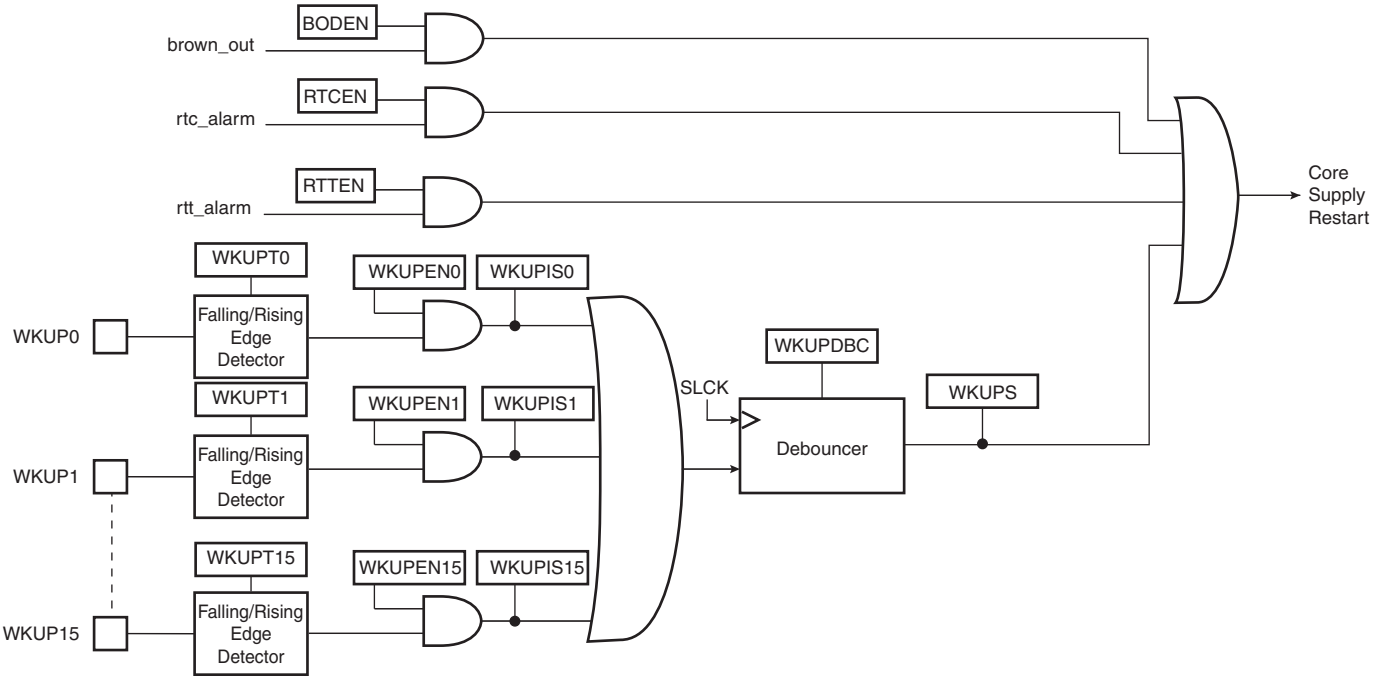
Mode	SUPC, 32 kHz Oscillator RTC RTT Backup Registers, POR (Backup Region)	Regulator	Core Memory Peripherals	Mode Entry	Potential Wake Up Sources	Core at Wake Up	PIO State while in Low Power Mode	PIO State at Wake Up	Consumption (2) (3)	Wake Up Time(1)
Backup Mode	ON	OFF	OFF (Not powered)	WFE +SLEEPDEEP bit = 1	WUP0-15 pins BOD alarm RTC alarm RTT alarm	Reset	Previous state saved	PIOA & PIOB & PIOC Inputs with pull ups	3 µA typ(4)	< 0.1 ms
Wait Mode	ON	ON	Powered (Not clocked)	WFE +SLEEPDEEP bit = 0 +LPM bit = 1	Any Event from: Fast startup through WUP0-15 pins RTC alarm RTT alarm	Clocked back	Previous state saved	Unchanged	5 µA/15 µA (5)	< 10 µs
Sleep Mode	ON	ON	Powered(7) (Not clocked)	WFE or WFI +SLEEPDEEP bit = 0 +LPM bit = 0	Entry mode = WFI Interrupt Only; Entry mode = WFE Any Enabled Interrupt and/or Any Event from: Fast start-up through WUP0-15 pins RTC alarm RTT alarm	Clocked back	Previous state saved	Unchanged	(6)	(6)

Notes:
1. When considering wake-up time, the time required to start the PLL is not taken into account. Once started, the device works with the 4/8/12 MHz Fast RC oscillator. The user has to add the PLL start-up time if it is needed in the system. The wake-up time is defined as the time taken for wake up until the first instruction is fetched.
2. The external loads on PIOs are not taken into account in the calculation.
3. Supply Monitor current consumption is not included.
4. Total Current consumption.
5. 5 µA on VDDCORE, 15 µA for total current consumption (using internal voltage regulator), 8 µA for total current consumption (without using internal voltage regulator).
6. Depends on MCK frequency.
7. In this mode the core is supplied and not clocked but some peripherals can be clocked.

5.6 Wake-up Sources

The wake-up events allow the device to exit backup mode. When a wake-up event is detected, the Supply Controller performs a sequence which automatically reenables the core power supply and the SRAM power supply, if they are not already enabled.

Figure 5-4. Wake-up Source

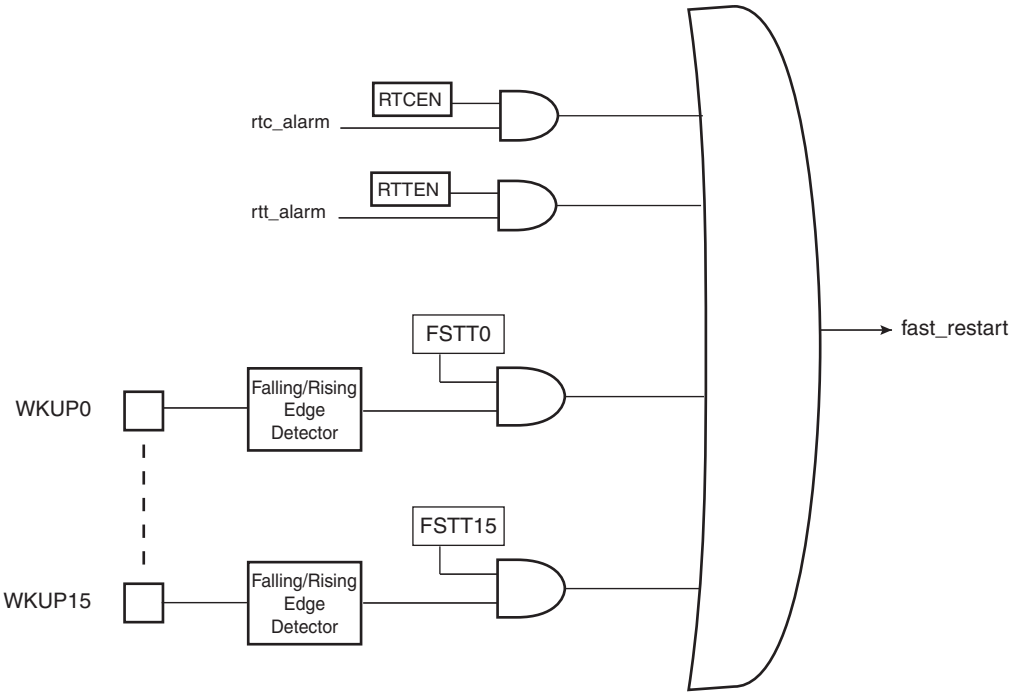


5.7 Fast Start-Up

The SAM3N allows the processor to restart in a few microseconds while the processor is in wait mode. A fast start up can occur upon detection of a low level on one of the 19 wake-up inputs (WKUP0 to 15 + SM + RTC + RTT).

The fast restart circuitry, as shown in Figure 5-5, is fully asynchronous and provides a fast start-up signal to the Power Management Controller. As soon as the fast start-up signal is asserted, the PMC automatically restarts the embedded 4 MHz fast RC oscillator, switches the master clock on this 4 MHz clock and reenables the processor clock.

Figure 5-5. Fast Start-Up Sources



6. Input/Output Lines

The SAM3N has several kinds of input/output (I/O) lines such as general purpose I/Os (GPIO) and system I/Os. GPIOs can have alternate functionality due to multiplexing capabilities of the PIO controllers. The same PIO line can be used whether in IO mode or by the multiplexed peripheral. System I/Os include pins such as test pins, oscillators, erase or analog inputs.

6.1 General Purpose I/O Lines

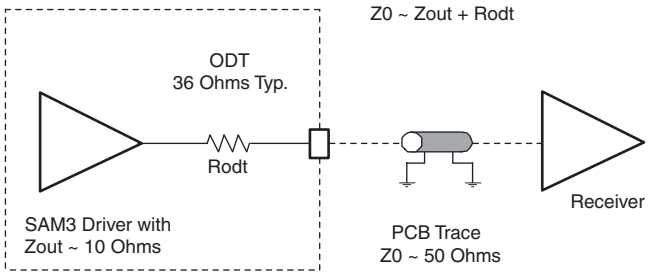
GPIO Lines are managed by PIO Controllers. All I/Os have several input or output modes such as pull-up or pull-down, input Schmitt triggers, multi-drive (open-drain), glitch filters, debouncing or input change interrupt. Programming of these modes is performed independently for each I/O line through the PIO controller user interface. For more details, refer to the product PIO controller section.

The input output buffers of the PIO lines are supplied through VDDIO power supply rail.

The SAM3N embeds high speed pads able to handle up to 45 MHz for SPI clock lines and 35 MHz on other lines. See AC Characteristics Section in the Electrical Characteristics Section of the datasheet for more details. Typical pull-up and pull-down value is 100 kΩ for all I/Os.

Each I/O line also embeds an ODT (On-Die Termination), (see Figure 6-1). It consists of an internal series resistor termination scheme for impedance matching between the driver output (SAM3N) and the PCB trace impedance preventing signal reflection. The series resistor helps to reduce I/O switching current (di/dt) thereby reducing in turn, EMI. It also decreases overshoot and undershoot (ringing) due to inductance of interconnect between devices or between boards. In conclusion ODT helps diminish signal integrity issues.

Figure 6-1. On-Die Termination



6.2 System I/O Lines

System I/O lines are pins used by oscillators, test mode, reset and JTAG to name but a few. Described below are the SAM3N system I/O lines shared with PIO lines:

These pins are software configurable as general purpose I/O or system pins. At startup the default function of these pins is always used.

Table 6-1. System I/O Configuration Pin List.

SYSTEM_IO bit number	Default function after reset	Other function	Constraints for normal start	Configuration
12	ERASE	PB12	Low Level at startup(1)	In Matrix User Interface Registers (Refer to the System I/O Configuration Register in the Bus Matrix section of the product datasheet.)
7	TCK/SWCLK	PB7	-	
6	TMS/SWDIO	PB6	-	
5	TDO/TRACESWO	PB5	-	
4	TDI	PB4	-	
-	PA7	XIN32	-	See footnote (2) below
-	PA8	XOUT32	-	
-	PB9	XIN	-	See footnote (3) below
-	PB8	XOUT	-	

Notes:
1. If PB12 is used as PIO input in user applications, a low level must be ensured at startup to prevent Flash erase before the user application sets PB12 into PIO mode.
2. In the product Datasheet Refer to: Slow Clock Generator of the Supply Controller section.
3. In the product Datasheet Refer to: 3 to 20 MHZ Crystal Oscillator information in the PMC section.

6.2.1 Serial Wire JTAG Debug Port (SWJ-DP) Pins

The SWJ-DP pins are TCK/SWCLK, TMS/SWDIO, TDO/SWO, TDI and commonly provided on a standard 20-pin JTAG connector defined by ARM. For more details about voltage reference and reset state, refer to Table 3-1 on page 7.

At startup, SWJ-DP pins are configured in SWJ-DP mode to allow connection with debugging probe. Please refer to the Debug and Test Section of the product datasheet.

SWJ-DP pins can be used as standard I/Os to provide users more general input/output pins when the debug port is not needed in the end application. Mode selection between SWJ-DP mode (System IO mode) and general IO mode is performed through the AHB Matrix Special Function Registers (MATRIX_SFR). Configuration of the pad for pull-up, triggers, debouncing and glitch filters is possible regardless of the mode.

The JTAGSEL pin is used to select the JTAG boundary scan when asserted at a high level. It integrates a permanent pull-down resistor of about 15 kΩ to GND, so that it can be left unconnected for normal operations.

By default, the JTAG Debug Port is active. If the debugger host wants to switch to the Serial Wire Debug Port, it must provide a dedicated JTAG sequence on TMS/SWDIO and TCK/SWCLK which disables the JTAG-DP and enables the SW-DP. When the Serial Wire Debug Port is active, TDO/TRACESWO can be used for trace.

The asynchronous TRACE output (TRACESWO) is multiplexed with TDO. So the asynchronous trace can only be used with SW-DP, not JTAG-DP. For more information about SW-DP and JTAG-DP switching, please refer to the Debug and Test Section.