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SM802104

ClockWorks™ Fibre Channel (106.25MHz, 212.5MHz), Ultra-Low Jitter, LVPECL Frequency Synthesizer

General Description

The SM802104 is a member of the ClockWorks™ family of devices from Micrel and provides an extremely low-noise timing solution for Fibre Channel clock signals. It is based upon a unique, patented RotaryWave® architecture that provides very low phase noise.

The device operates from a 3.3V or 2.5V power supply and synthesizes LVPECL output clocks at 106.25MHz or 212.5MHz. There are normally two clock outputs, but one output can be achieved by powering down the second output with the OE pin. The SM802104 accepts a 26.5625MHz crystal or LVCMOS reference clock.

Data sheets and support documentation can be found on Micrel's web site at: www.micrel.com.

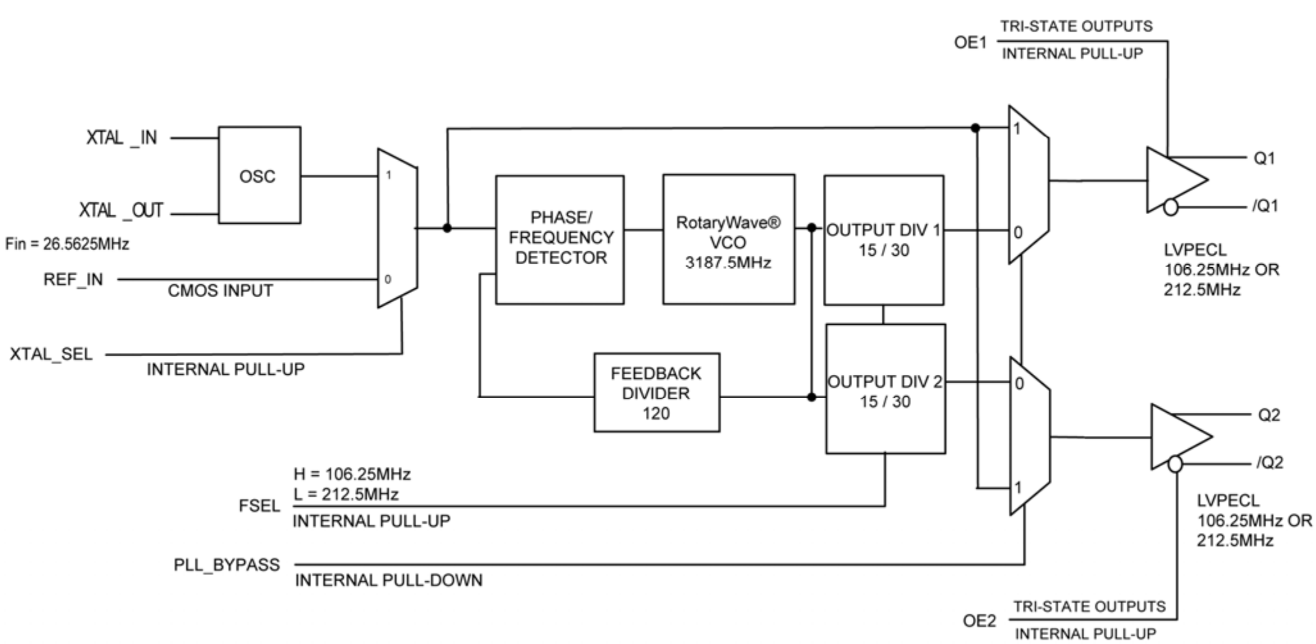
Features

- Generates one or two LVPECL clock outputs at 106.25MHz or 212.5MHz
- 2.5V or 3.3V operating range
- Typical phase jitter @ 106.25MHz (637kHz to 10MHz): 200fs
- Industrial temperature range
- Green, RoHS, and PFOS compliant
- Available in 24-pin 4mm × 4mm QFN package

Applications

- Fibre Channel
- Storage Networking (SAN, NAS)

Block Diagram



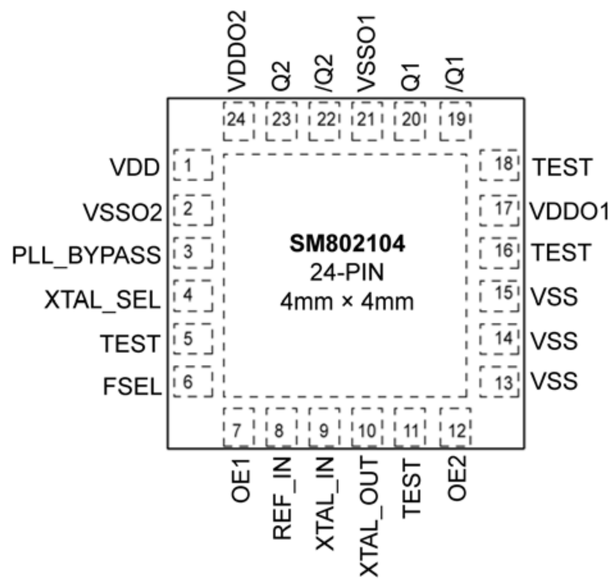
Ordering Information

Part Number	Marking	Shipping	Junction Temperature Range[1]	Package
SM802104UMG	802104	Tube	-40°C to +85°C	24-Pin QFN
SM802104UMGR	802104	Tape and Reel	-40°C to +85°C	24-Pin QFN

Note:

1. Devices are Green, RoHS, and PFOS compliant.

Pin Configuration



24-Pin QFN (code)
(Top View)

Pin Description

Pin Number	Pin Name	Pin Type	Pin Level	Pin Function
19, 20	/Q1, Q1	O, (DIF)	LVPECL	Differential Clock Output from Bank 1 106.25MHz or 212.5MHz
22, 23	/Q2, Q2	O, (DIF)	LVPECL	Differential Clock Output from Bank 2 106.25MHz or 212.5MHz
24	VDDO2	PWR		Power Supply for Output Bank 2
2	VSSO2	PWR		Power Supply Ground for Output Bank 2
3	PLL_BYPASS	I, (SE)	LVCMOS	PLL Bypass, Selects Output Source 0 = Normal PLL Operation 1 = Output from Input Reference Clock or Crystal 45KΩ pull-down
4	XTAL_SEL	I, (SE)	LVCMOS	Selects PLL Input Reference Source 0 = REF_IN, 1 = XTAL, 45KΩ pull-up

Pin Description (Continued)

Pin Number	Pin Name	Pin Type	Pin Level	Pin Function
5, 11, 16, 18	TEST			Factory Test pins, Do not connect anything to these pins.
1	VDD	PWR		Core Power Supply
13, 14, 15	VSS	PWR		Core Power Supply Ground
17	VDDO1	PWR		Power Supply for Output Bank 1
21	VSSO1	PWR		Power Supply Ground for Output Bank 1
8	REF_IN	I, (SE)	LVCMOS	Reference Clock Input
9	XTAL_IN	I, (SE)	12pF crystal	Crystal Reference Input, no load caps needed. See Fig. 5.
10	XTAL_OUT	O, (SE)	12pF crystal	Crystal Reference Output, no load caps needed. See Fig. 5.
6	FSEL	I, (SE)	LVCMOS	Frequency Select, 1 = 106.25MHz, 0 = 212.5MHz, 45KΩ pull-up
7	OE1	I, (SE)	LVCMOS	Output Enable, Q1 disables to tri-state, 0 = Disabled, 1 = Enabled, 45KΩ pull-up
12	OE2	I, (SE)	LVCMOS	Output Enable, Q2 disables to tri-state, 0 = Disabled, 1 = Enabled, 45KΩ pull-up

Application Information

Input Reference

When operating with a crystal input reference, do not apply a switching signal to REF_IN.

Crystal Layout

Keep the layers under the crystal as open as possible.

Do not place switching signals or noisy supplies under the crystal.

Truth Tables

PLL_BYPASS	XTAL_SEL	INPUT	OUTPUT
0	–	–	PLL
1	–	–	XTAL/REF_IN
–	0	REF_IN	–
–	1	XTAL	–

FSEL	Output Frequency (MHz)
0	212.5
1	106.25

Absolute Maximum Ratings[1]

Supply Voltage (V_{DD}, V_{DDOx}) ....+4.6V
Input Voltage (V_{IN}) .... -0.50V to V_{DD} + 0.5V
Lead Temperature (soldering, 20s)............................ 260°C
Case Temperature .... 115°C
Storage Temperature (T_s) ....-65°C to +150°C

Operating Ratings[2]

Supply Voltage (V_{DD}, V_{DDOx})................. +2.375V to +3.465V
Ambient Temperature (T_A)........................... -40°C to +85°C
Junction Thermal Resistance[3]
QFN (θ_{JA})
Still-Air... 50°C/W
QFN (ψ_{JB})
Junction-to-Board .... 30°C/W

DC Electrical Characteristics[4]

V_{DD} = $V_{DDO1/2}$ = 3.3V ±5% or 2.5V ±5%

V_{DD} = 3.3V ±5%, $V_{DDO1/2}$ = 3.3V ±5% or 2.5V ±5%

T_A = -40°C to +85°C.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
V_{DD}, V_{DDOx}	2.5V Operating Voltage		2.375	2.5	2.625	V
V_{DD}, V_{DDOx}	3.3V Operating Voltage		3.135	3.3	3.465	V
I_{DD} REF_IN	Supply current V_{DD} + V_{DDO} XTAL_SEL = 0 Outputs open	106.25MHz - 1 output		82	105	mA
		106.25MHz - 2 outputs		98	127	
		212.5MHz - 1 output		92	119	
		212.5MHz - 2 outputs		111	145	
I_{DD} XTAL	Supply current V_{DD} + V_{DDO} XTAL_SEL = 1 Outputs open	106.25MHz - 1 output		93	120	mA
		106.25MHz - 2 outputs		109	142	
		212.5MHz - 1 output		103	134	
		212.5MHz - 2 outputs		122	159	

LVPECL DC Electrical Characteristics[4]

V_{DD} = $V_{DDO1/2}$ = 3.3V ±5% or 2.5V ±5%

V_{DD} = 3.3V ±5%, $V_{DDO1/2}$ = 3.3V ±5% or 2.5V ±5%

T_A = -40°C to +85°C. R_L = 50Ω to V_{DDO} - 2V

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
V_{OH}	Output High Voltage		V_{DDO} – 1.145	V_{DDO} – 0.97	V_{DDO} – 0.845	V
V_{OL}	Output Low Voltage		V_{DDO} – 1.945	V_{DDO} – 1.77	V_{DDO} – 1.645	V
V_{SWING}	Output Voltage Swing		0.6	0.8	1.0	V

Notes:

1. Permanent device damage may occur if absolute maximum ratings are exceeded. This is a stress rating only and functional operation is not implied at conditions other than those detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
2. The data sheet limits are not guaranteed if the device is operated beyond the operating ratings.
3. Package thermal resistance assumes exposed pad is soldered (or equivalent) to the device's most negative potential on the PCB.
4. The circuit is designed to meet the AC and DC specifications shown in the above table(s) after thermal equilibrium has been established.

LVCMOS (PLL_BYPASS, XTAL_SEL, OE1/2, FSEL) DC Electrical Characteristics(4)

V_{DD} = 3.3V ±5%, or 2.5V ±5%, T_A = -40°C to +85°C.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
V_{IH}	Input High Voltage		2		V_{DD} + 0.3	V
V_{IL}	Input Low Voltage		-0.3		0.8	V
I_{IH}	Input High Current	V_{DD} = V_{IN} = 3.465V			150	µA
I_{IL}	Input Low Current	V_{DD} = 3.465V, V_{IN} = 0V	-150			µA

REF_IN DC Electrical Characteristics(4)

V_{DD} = 3.3V ±5%, or 2.5V ±5%, T_A = -40°C to +85°C.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
V_{IH}	Input High Voltage		1.1		V_{DD} + 0.3	V
V_{IL}	Input Low Voltage		-0.3		0.6	V
I_{IN}	Input Current	XTAL_SEL = V_{IL}, V_{IN} = 0V to V_{DD}	-5		5	µA
		XTAL_SEL = V_{IH}, V_{IN} = V_{DD}		20		µA

Crystal Characteristics

NDK NX2520SA

Parameter	Condition	Min.	Typ.	Max.	Units
Mode of Oscillation	12pF Load	**Fundamental, Parallel Resonant**			
Frequency			26.5625		MHz
Equivalent Series Resistance (ESR)				50	Ω
Shunt Capacitor, C0			3	7	pF
Correlation Drive Level			100	300	uW

AC Electrical Characteristics[4, 5]

$V_{DD} = V_{DDO1/2}$ = 3.3V ±5% or 2.5V ±5%

V_{DD} = 3.3V ±5%, $V_{DDO1/2}$ = 3.3V ±5% or 2.5V ±5%

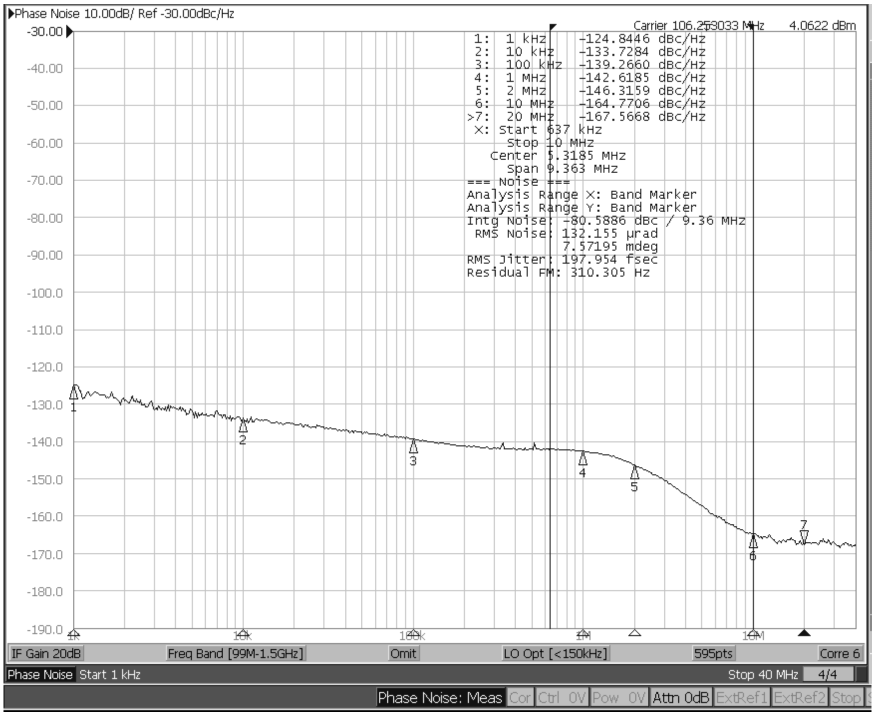
T_A = -40°C to +85°C. R_L = 50Ω to V_{DDO} - 2V

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
F_{OUT1}	Output Frequency 1	FSEL=1		106.25		MHz
F_{OUT2}	Output Frequency 2	FSEL=0		212.5		MHz
Ppm	Output ppm Variation	Crystal reference. Note 6	-50		50	ppm
F_{REF}	Reference Input Frequency			26.5625		MHz
T_R/T_F	LVPECL Output Rise/Fall Time	20% – 80%	80	175	350	ps
ODC	Output Duty Cycle		48	50	52	%
T_{SKEW}	Output-to-Output Skew	Within bank. Note 7			45	ps
T_{LOCK}	PLL Lock Time				20	ms
$T_{jit}(\varnothing)$	RMS Phase Jitter[8]	106.25MHz Integration Range (637kHz – 10MHz) Integration Range (12kHz – 20MHz) 212.5MHz Integration Range (637kHz – 10MHz) Integration Range (12kHz – 20MHz)		 200 250 200 250		fs
	Spurious Noise Components	26.5625MHz using 106.25MHz 26.5625MHz using 212.5MHz		-80 -85		dBc

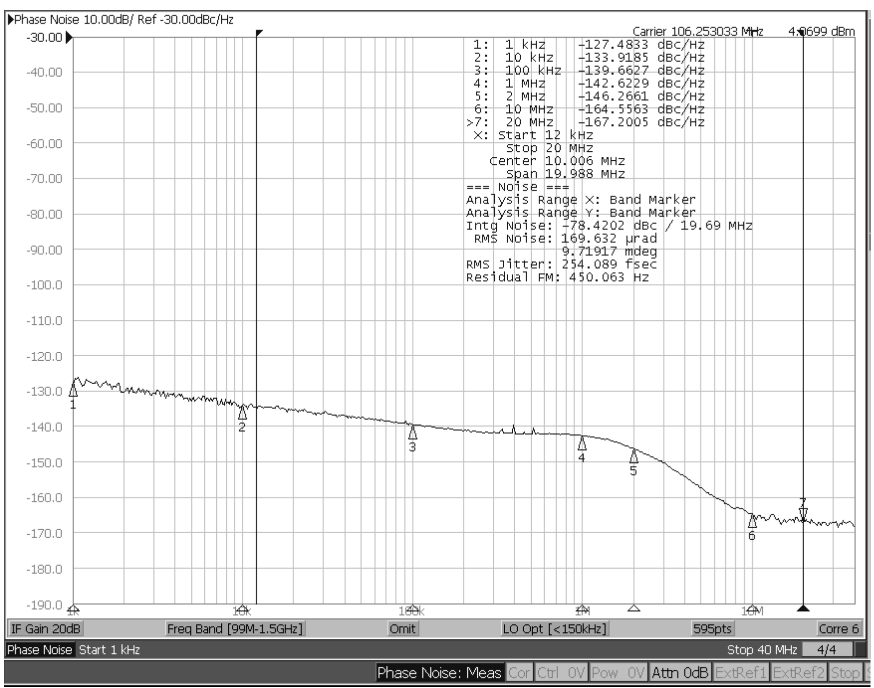
Notes:

5. All phase noise measurements were taken with an Agilent 5052B phase noise system.
6. Crystal tolerance at room less than ± 15ppm, over temp less than ±20ppm.
7. Defined as skew between outputs at the same supply voltage and with equal load conditions and same frequency; Measured at the output differential crossing points.
8. Measured using 26.5625MHz crystal as the input reference source. If using an external reference input, use a low phase noise source. With an external reference, the phase noise will follow the input source phase noise up to about 1MHz.

Phase Noise Plots

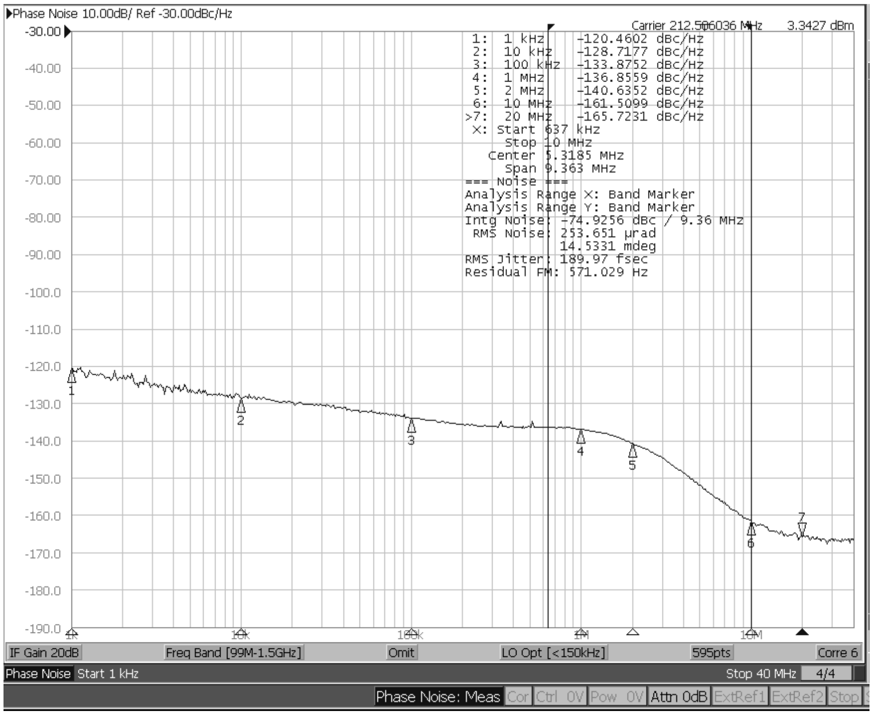


Phase Noise Plot: 106.25MHz, 637kHz – 10MHz 198fS

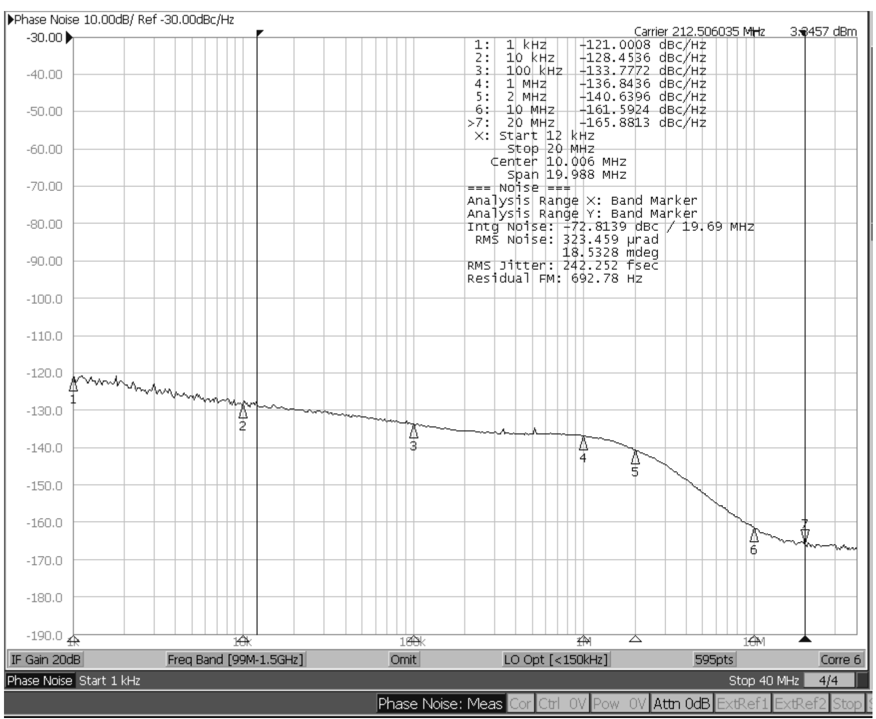


Phase Noise Plot: 106.25MHz, 12kHz – 20MHz 254fS

Phase Noise Plots (Continued)



Phase Noise Plot: 212.5MHz, 637kHz – 10MHz 190fS



Phase Noise Plot: 212.5MHz, 12kHz – 20MHz 242fS

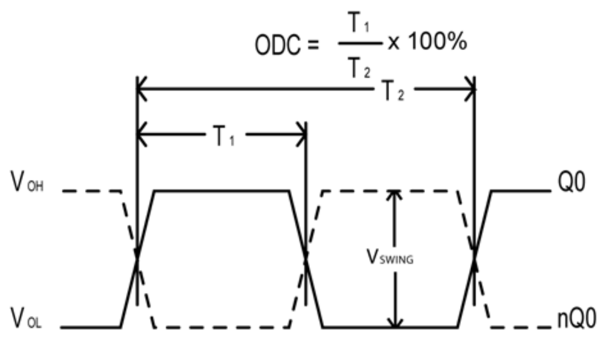


Figure 1. Duty Cycle Timing

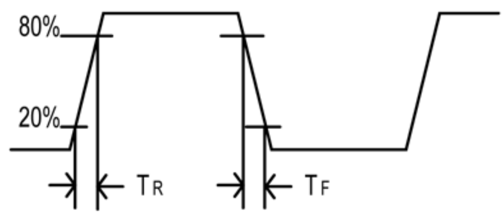


Figure 2. All outputs Rise/Fall Time

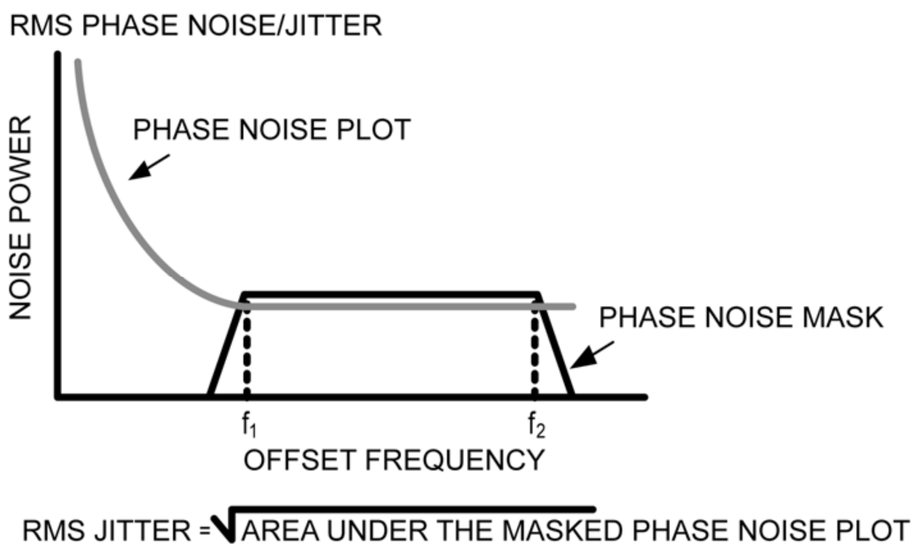


Figure 3. RMS Phase/Noise Jitter

hbwhelp@micrel.com or (408) 955-1690

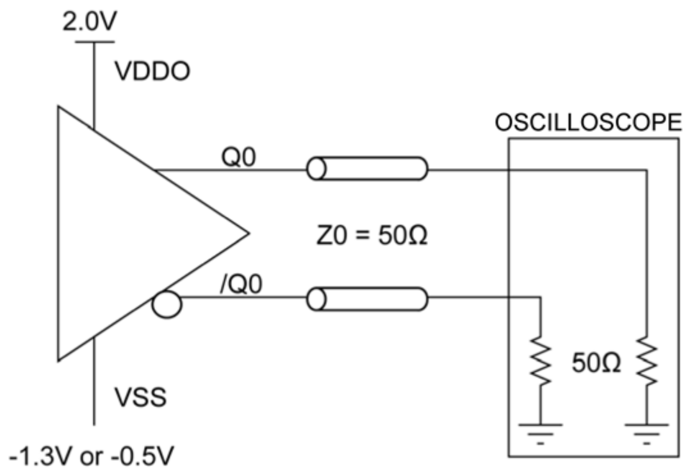


Figure 4. LVPECL Output Load and Test Circuit

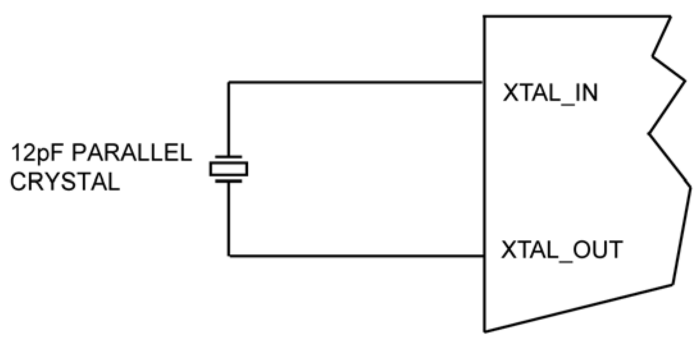
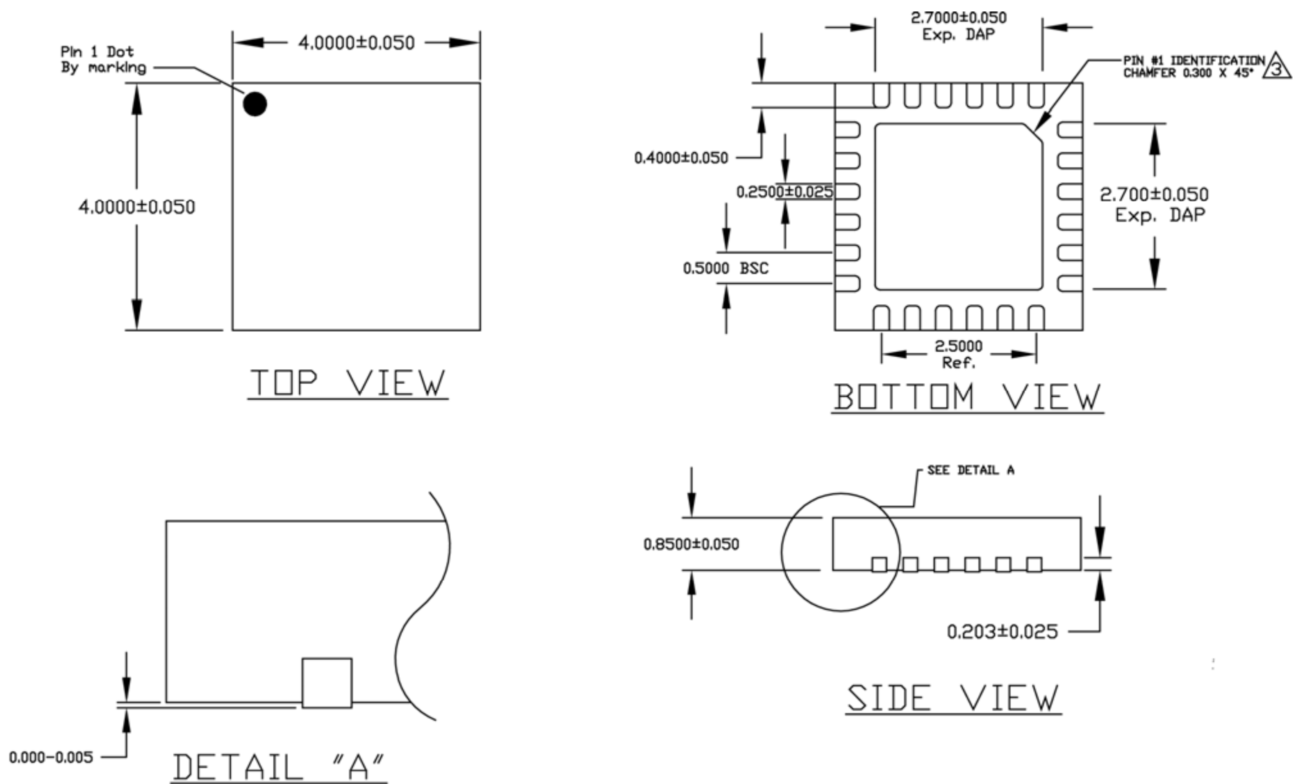


Figure 5. Crystal Input Interface

Package Information



NOTE:
1. ALL DIMENSIONS ARE IN MILLIMETERS (mm).
2. THE PIN#1 IDENTIFIER MUST EXIST ON THE TOP SURFACE OF PACKAGE BY USING IDENTIFICATION MARK OR OTHER FEATURE OF PACKAGE BODY.
3. CHAMFER STYLE PIN 1 IDENTIFIER ON BOTTOM SIDE

(4mm x 4mm) QFN

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