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SM840002

ClockWorks™ Dual 10-Gigabit/Gigabit Ethernet 62.5MHz, 125MHz, or 156.25MHz, Ultra-Low Jitter LVCMOS Clock Frequency Synthesizer

General Description

The SM840002 is a dual 10-Gigabit Ethernet and Gigabit Ethernet, 62.5MHz, 125MHz, or 156.25MHz LVCMOS clock frequency synthesizer and a member of the ClockWorks™ family of devices from Micrel. It provides a low-noise timing solution for high-speed, high-accuracy synthesis of clock signals. It includes a patented RotaryWave® architecture that provides a very stable clock with very-low noise.

Power supplies of either 2.5V or 3.3V are supported, with superior jitter and phase-noise performance. The device synthesizes a 62.5MHz, 125MHz, or 156.25MHz, low-noise LVCMOS output pair for Ethernet applications. The crystal reference frequency is 25MHz.

The SM840002 is an excellent replacement for IDT FemtoClocks®, with improved waveform integrity, and jitter.

Data sheets and support documentation can be found on Micrel's web site at: www.micrel.com.

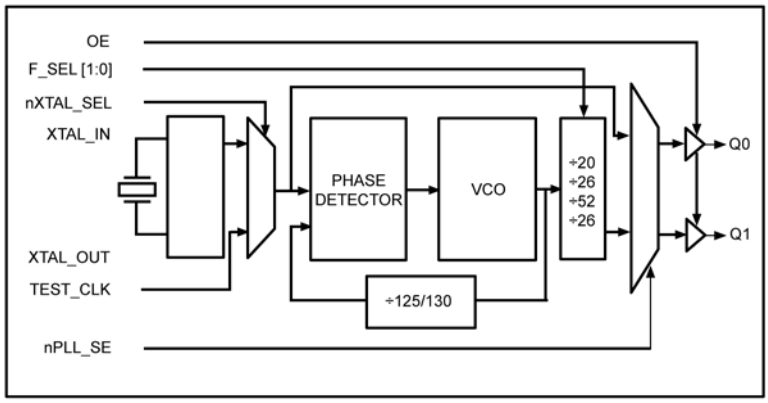
Features

- Generates two LVCMOS outputs
- Operating supply modes:
  - Core/Output
  - 3.3V/3.3V, 2.5V/2.5V
- Typical phase jitter @156.25MHz~64 fs (1.875MHz – 20MHz)
- Crystal frequency: 25MHz
- 62.5MHz, 125MHz, or 156.25MHz output frequency
- Output Skew: 12ps (maximum)
- Phase Noise @ 156.25MHz:
  - 1KHz: –126dBc/Hz
  - 10KHz: –130dBc/Hz
  - 100KHz: –126dBc/Hz
  - 1MHz: –139dBc/Hz
  - 10MHz: –165dBc/Hz
  - 20MHz: –166/dBc/Hz
- Temperature range: –40°C to +75°C
- Green-, RoHS-, and PFOS-compliant
- Available in 16-pin TSSOP

Applications

- Gigabit Ethernet
- 10-Gigabit Ethernet

Block Diagram



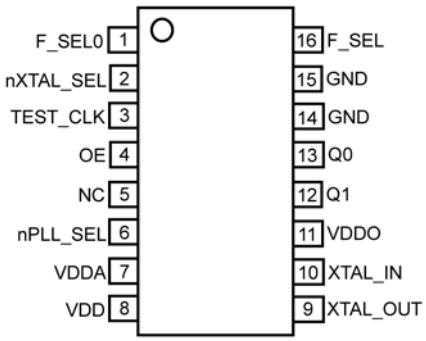
Ordering Information[1]

Part Number	Package Type	Operating Range	Package Marking
SM840002KA	K-16	–40°C to +75°C	840002
SM840002KA TR[2]	K-16	–40°C to +75°C	840002

Notes:

1. Devices are Green-, RoHS-, and PFOS-compliant.
2. Tape and Reel.

Pin Configuration



16-Pin TSSOP (K-16)

Pin Description

Pin Number	Pin Name	Type	Level	Pin Function
1	F_SEL0	I	Pull-Up	Frequency Select Pin. LVCMOS interface levels.
2	nXTAL_SEL	I	Pull-Down	Selects between XTAL and TEST_CLK Reference Input. When HIGH, selects TEST_CLK. When LOW, selects XTAL inputs. LVCMOS interface levels.
3	TEST_CLK	I	Pull-Down	Single-Ended LVCMOS Clock Input.
4	OE	I	Pull-Up	Output Enable. When HIGH, the outputs are active. When LOW, the outputs are in a high impedance state. LVCMOS interface levels.
5	NC			No Connect.
6	nPLL_SEL	I	Pull-Down	Selects between the VCO reference and the VCO Output. When LOW, the output is driven from the VCO output. When HIGH, the PLL is bypassed.
7	V_{DDA}	P		2.5V or 3.3V Output Power Supply. No filter resistor needed.
8	V_{DD}	P		2.5V or 3.3V Output Power Supply.
9	XTAL_OUT	O	12pF Crystal	Crystal Reference Output, no load caps needed.
10	XTAL_IN	I	12pF Crystal	Crystal Reference Input, no load caps needed.
11	V_{DDO}	P		2.5V or 3.3V Output Power Supply.
12	Q1	O	LVCMOS	Single-Ended Output Clock.
13	Q0	O	LVCMOS	Single-Ended Output Clock.
14	GND	P		Ground.
15	GND	P		Ground.
16	F_SEL1	I	Pull-up	Frequency Select Pin. LVCMOS interface levels.

Configuring the SM840002

Xtal Frequency (MHz)	F_SEL1	F_SEL0	M Divider	N Divider	Output Frequency (MHz)
25	0	0	125	20	156.25
25	0	1	130	26	125
25	1	0	130	52	62.5
25	1	1	130	26	125

Absolute Maximum Ratings[1]

Supply Voltage (V_{DD}) ..... +4.6V
Input Voltage (V_{IN}) ..... –0.50V to V_{DD}+0.5V
Output Voltage (V_{OUT}) ..... –0.50V to V_{DD}+0.5V
Lead Temperature (soldering, 20sec.) ..... 260°C
Storage Temperature (T_s) ..... –65°C to +150°C

Operating Ratings[2]

Supply Voltage (V_{DDO}) ..... +2.375V to +3.465V
Supply Voltage ($V_{DD,}$ V_{DDA}) ..... +2.375V to +3.465V
Ambient Temperature (T_A) ..... –40°C to +75°C
Junction Thermal Resistance
TSSOP (θ_{JA})(Still Air) ..... 127°C/W

DC Electrical Characteristics[3]

V_{DDA} = V_{DD} = 2.5V ±5%, V_{DDO} = 2.5V ±5%, T_A = –40°C to +75°C, unless noted.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
V_{DD}	Core Supply Voltage		2.375	2.50	2.625	V
V_{DDA}	Analog Supply Voltage		2.375	2.50	2.625	V
V_{DDO}	Output Supply Voltage		2.375	2.50	2.625	V
I_{DD}	Core Supply Current			0.1	1	mA
I_{DDA}	Analog Supply Current			48	55	mA
I_{DDO}	Output Supply Current	No Load		15	23	mA

V_{DDA} = V_{DD} = 3.3V ±5%, V_{DDO} = 3.3V ±5%, T_A = –40°C to +75°C, unless noted.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
V_{DD}	Core Supply Voltage		3.135	3.30	3.465	V
V_{DDA}	Analog Supply Voltage		3.135	3.30	3.465	V
V_{DDO}	Output Supply Voltage		3.135	3.30	3.465	V
I_{DD}	Core Supply Current			0.1	1	
I_{DDA}	Analog Supply Current			49	55	mA
I_{DDO}	Power Supply Current	No Load		25	32	mA

Notes:

1. Permanent device damage may occur if absolute maximum ratings are exceeded. This is a stress rating only and functional operation is not implied at conditions other than those detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
2. The data sheet limits are not guaranteed if the device is operated beyond the operating ratings.
3. The circuit is designed to meet the DC specifications shown in the above table after thermal equilibrium has been established.

LVCMOS DC Electrical Characteristics[3]

V_{DDA} = V_{DD} =2.5V or 3.3V ±5%, V_{DDO} = 2.5V or 3.3V ±5%, T_A = –40°C to +75°C, unless noted.

Symbol	Parameter		Condition	Min.	Typ.	Max.	Units
V_{IH}	Input HIGH Voltage			2		V_{DD} + 0.3	V
V_{IL}	Input LOW Voltage			–0.30		0.80	V
I_{IH}	Input HIGH Current	OE, F_SEL0, F_SEL1	V_{DD} = V_{IN} =3.465V or 2.625V			5	µA
		nPLL_SEL, MR, nXTAL_SEL, TEST_CLK	V_{DD} = V_{IN} =3.465V or 2.625V			150	µA
I_{IL}	Input LOW Current	OE, F_SEL0, F_SEL1	V_{DD} = 3.465V or 2.625V V_{IN} = 0V	–150			µA
		nPLL_SEL, MR, nXTAL_SEL, TEST_CLK	V_{DD} = 3.465V or 2.625V V_{IN} = 0V	–5			µA
V_{OH}	Output HIGH Voltage[4]		V_{DDO} = 3.3V ±5%	2.6			V
			V_{DDO} = 2.5V ±5%	1.8			V
V_{OL}	Output LOW Voltage[4]		V_{DDO} = 3.3V ±5% or 2.5V ±5%			0.5	V

AC Electrical Characteristics[5]

V_{DDA} = V_{DD} =2.5V or 3.3V ±5%, V_{DDO} = 2.5V or 3.3V ±5%, T_A = –40°C to +75°C, unless noted.

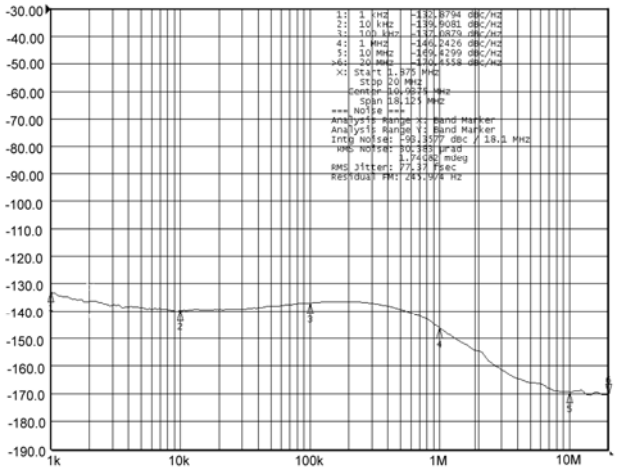
Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
F_{OUT}	Output Frequency	F_SEL[1:0] = 00		156.25		MHz
F_{OUT}	Output Frequency	F_SEL[1:0] = 01		125		MHz
F_{OUT}	Output Frequency	F_SEL[1:0] = 10		62.5		MHz
F_{OUT}	Output Frequency	F_SEL[1:0] = 11		125		MHz
t_{SKEW}	Output Skew[6]				12	ps
t_{JITTER}	RMS Phase Jitter	156.25MHz		0.064		ps
t_{JITTER}	RMS Phase Jitter	125MHz		0.065		ps
t_{JITTER}	RMS Phase Jitter	62.5MHz		0.077		ps
t_R/t_F	Output Rise/ Fall Time	20% to 80%	100		350	ps
O_{DC}	Output Duty Cycle		48	50	52	%

Notes:

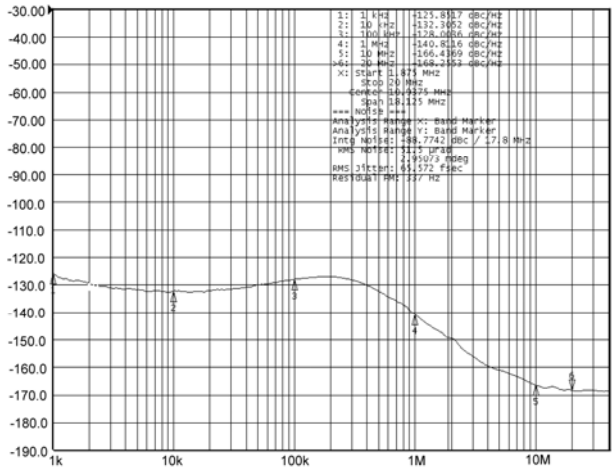
4. Outputs terminated with 50Ω to V_{DD}/2. See Parameters measurements 3.3V load test circuit.
5. The circuit is designed to meet the AC specifications shown in the above table(s) after thermal equilibrium has been established.
6. Defined as skew between outputs at the same supply voltage and with equal load conditions; Measured at the output differential crossing points.

Crystal Characteristics

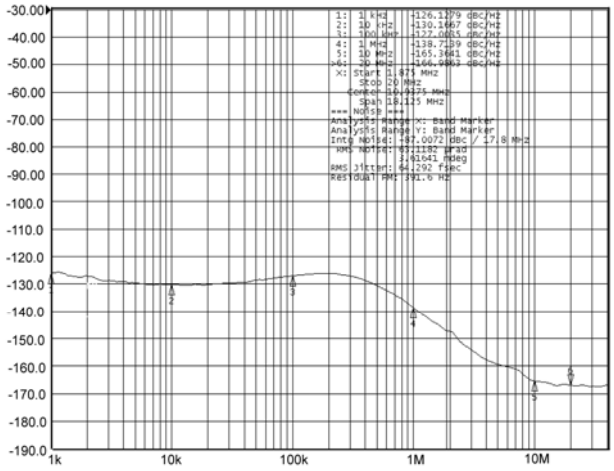
Parameter	Condition	Min.	Typ.	Max.	Units
Mode of Oscillation	12pF Load		Fundamental, Parallel Resonant		
Frequency			25		MHz
Equivalent Series Resistance (ESR)				50	Ω
Shunt Capacitor, C0			3	7	pF
Correlation Drive Level			100	300	uW



Phase Noise Plot: 62.5MHz @ 3.3V



Phase Noise Plot: 125MHz @ 3.3V



Phase Noise Plot: 156.25MHz @ 3.3V

hbwhelp@micrel.com or (408) 955-1690

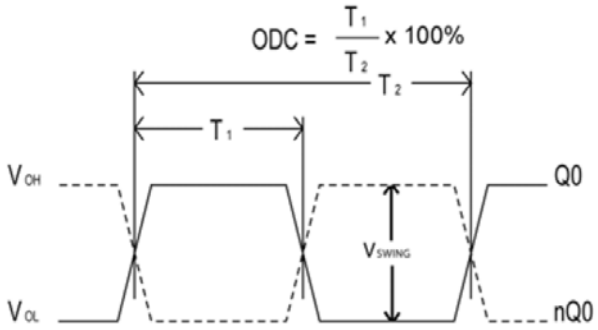


Figure 1. Duty Cycle Timing

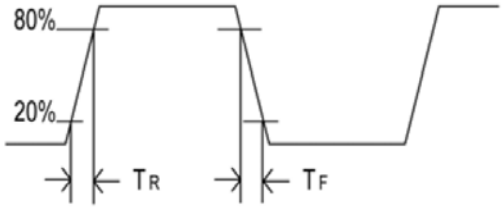


Figure 2. All Outputs Rise/Fall Time

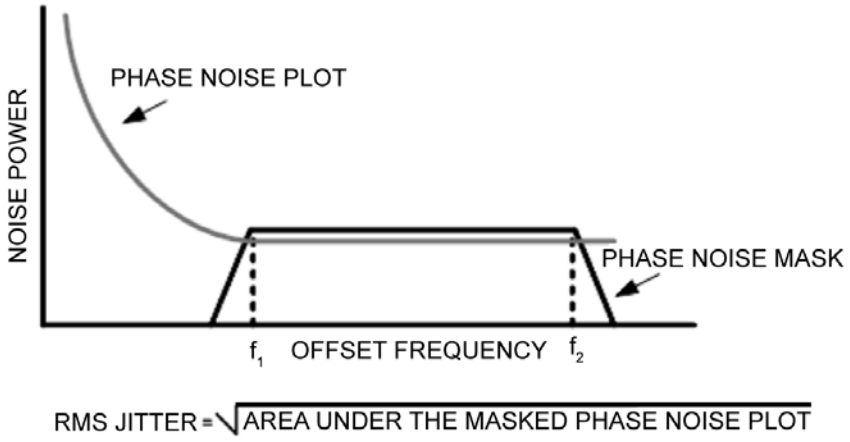


Figure 3. RMS Phase Noise/Jitter

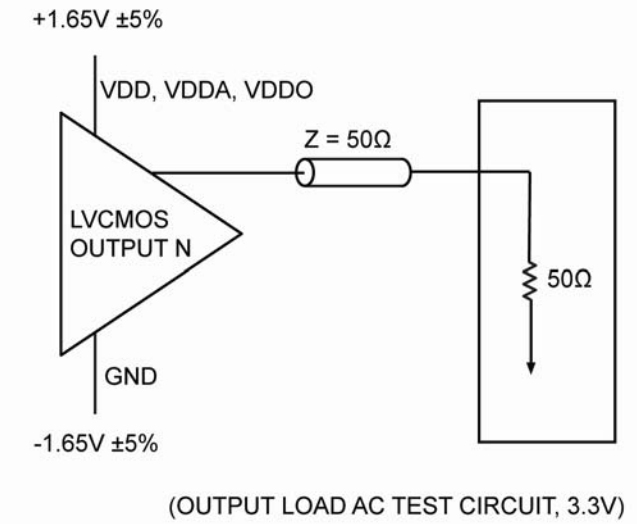


Figure 4. LVCMOS Output Load and Test Circuit

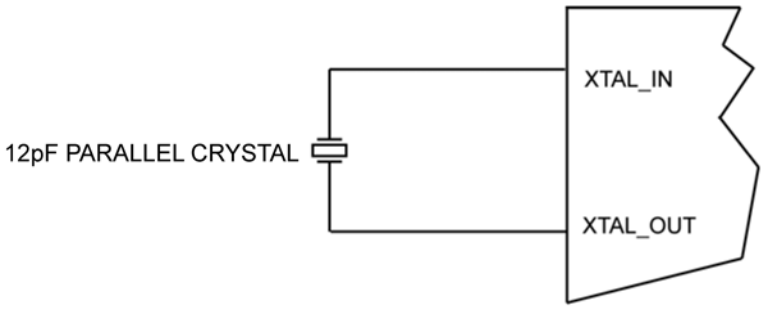
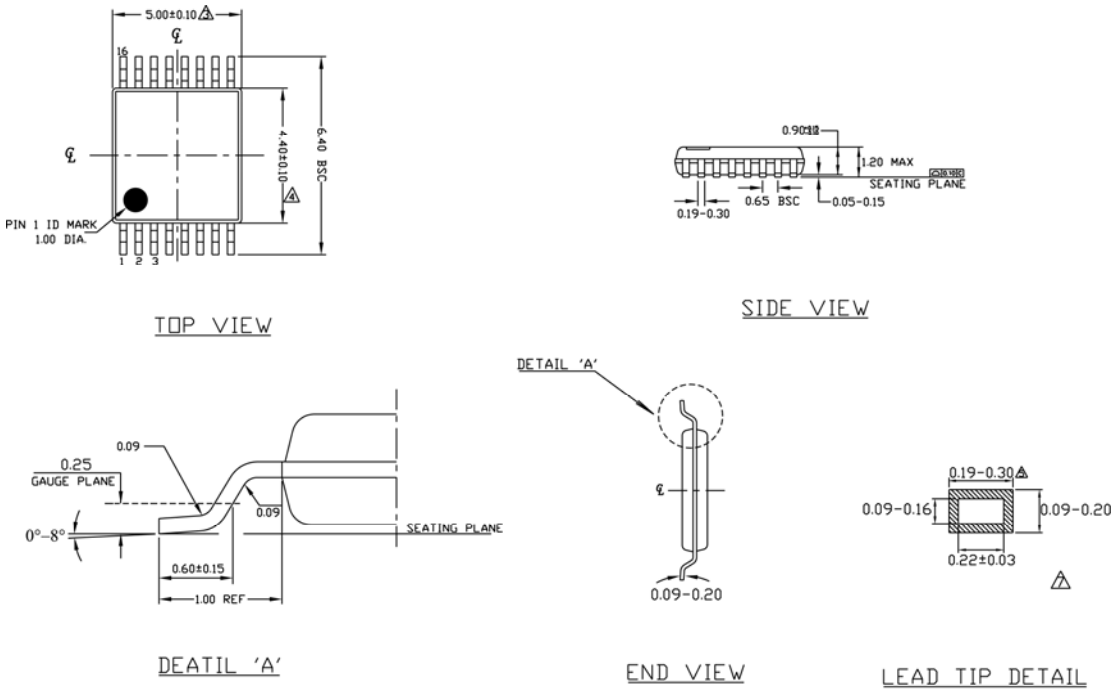


Figure 5. Crystal Input Interface

Package Information



Notes

1. All dimensions are in millimeters (angles in degrees).
2. Dimensioning and tolerancing per ANSI Y14.5M-1994.
3. Dimension does not include mold flash ,protrusions or gate burrs.
4. Dimension does not include internal flash or protrusion.
5. Dimension does not include dambar protrusion.
6. Cross section to be determined at 0.10 to 0.25mm from the lead tip.

16-Pin TSSOP (K-16)

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