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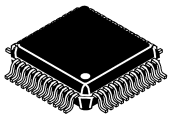
Document Number: S/MM912F634
Rev. 9.2, 5/2017

Integrated S12 Based Relay Driver with LIN

S/MM912F634



48-PIN LQFP
98ASH00962A
7.0 mm x 7.0 mm
AP SUFFIX: Non-exposed Pad

48-PIN LQFP-EP
98ASA00173D
7.0 mm x 7.0 mm
AE SUFFIX: Exposed Pad

The S/MM912F634 is an integrated single package solution integrating an HCS12 microcontroller with a SMARTMOS analog control IC. The Die to Die Interface (D2D) controlled analog die combines system base chip and application specific functions, including a LIN transceiver.

Features

- 16-Bit S12 CPU, 32 kByte FLASH, 2.0 kByte RAM
- Background debug (BDM) & debug module (DBG)
- Die to die bus interface for transparent memory mapping
- On-chip oscillator & two independent watchdogs
- LIN 2.1 physical layer interface with integrated SCI
- Six digital MCU GPIOs shared with SPI (PA5…0)
- 10-Bit, 15 channel - analog to digital converter (ADC)
- 16-Bit, four channel - timer module (TIM16B4C)
- 8-Bit, two channel - pulse width modulation module (PWM)
- Six high-voltage / wake-up inputs (L5.0)
- Three low-voltage GPIOs (PB2.0)
- Low-power modes with cyclic sense & forced wake-up
- Current sense module with selectable gain
- Reverse battery protected voltage sense module
- Two protected low-side outputs to drive inductive loads
- Two protected high-side outputs
- Chip temperature sensor
- Hall sensor supply
- Integrated voltage regulator(s)

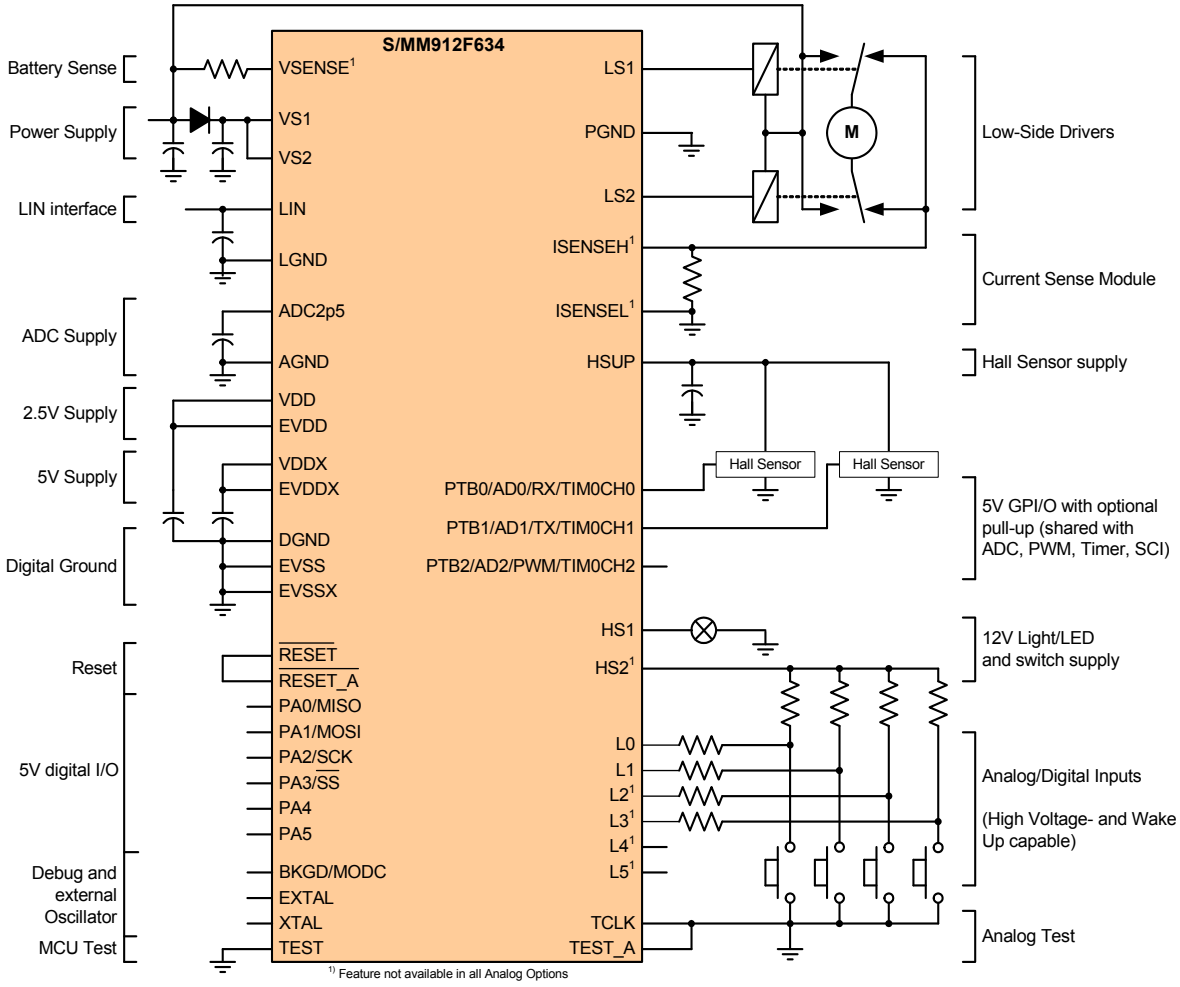


Figure 1. Simplified Application Diagram

1 Ordering Information

Table 1. Ordering Information

Device [2]	Temperature Range (T_A)	Package	Max. Bus Frequency (MHz) (f_{BUSMAX})	Flash (kB)	RAM (kB)	Analog Option [1]
MM912F634DV1AE	-40 to 105 °C	98ASA00173D, 48-PIN LQFP-EP	20	32	2	1
MM912F634DV2AE						2
MM912F634DV2AP		98ASH00962A, 48-PIN LQFP	16	32		
SM912F634DV1AE	-40 to 105 °C	98ASA00173D, 48-PIN LQFP-EP	20	32	2	1
SM912F634DV2AE						2
SM912F634DV2AP		98ASH00962A, 48-PIN LQFP	16	32		

Note:
1. See Table 2.
2. For Tape and Reel orders add R2 to the part suffix

NOTE

For the SM912F634DVxxx parts, by factory default the SLPBG_LOCK bit is set to 0 in the MCU IFR while in the MM912F634DVxxx parts by default the SLPBG_LOCK bit is set to 1.

Table 2. Analog Options[3]

Feature	Option 1	Option 2
Current Sense Module	YES	NO
Wake-up Inputs (Lx)	L0…L5	L0…L3

Note:
3. This table only highlights the analog die differences between the derivatives. See Section 4.2.3, “Analog Die Options" for detailed information.

The device part number follows the standard scheme below:

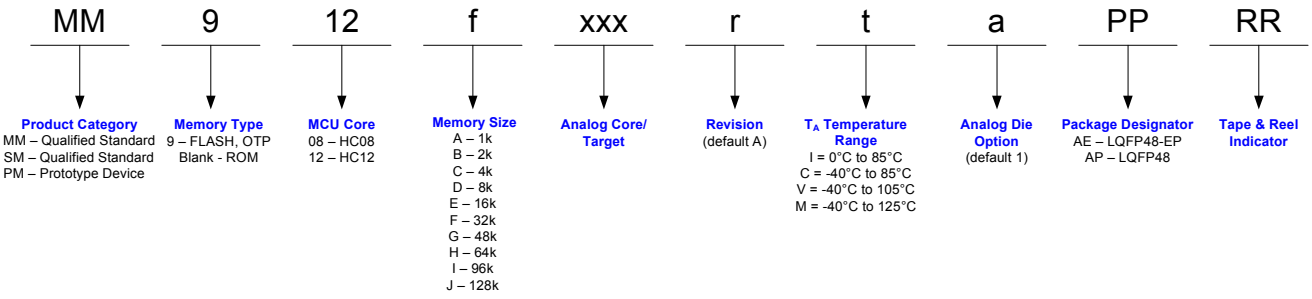


Figure 2. Part Number Scheme

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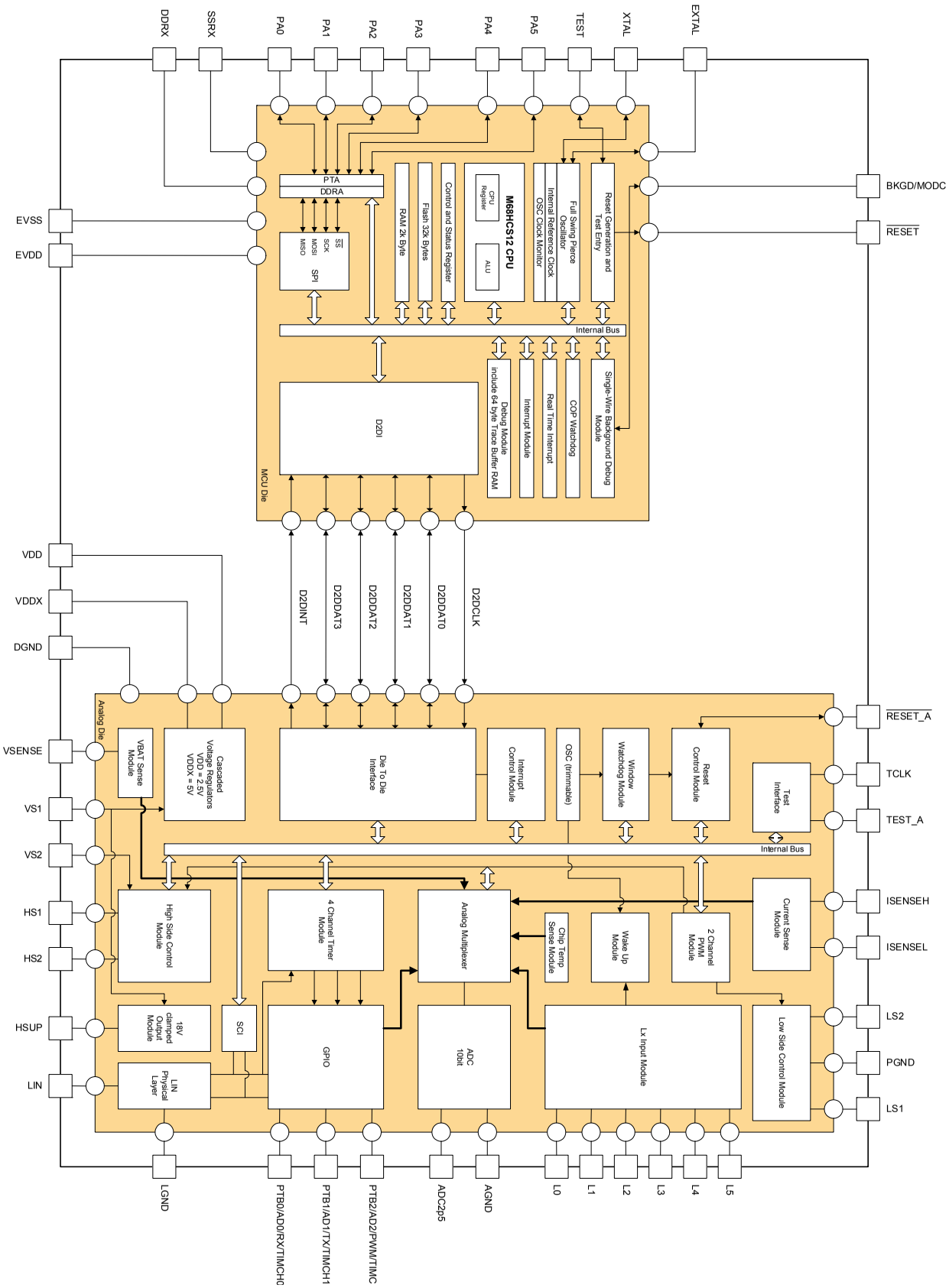


Figure 3. Device Block Diagram

2 Pin Assignment

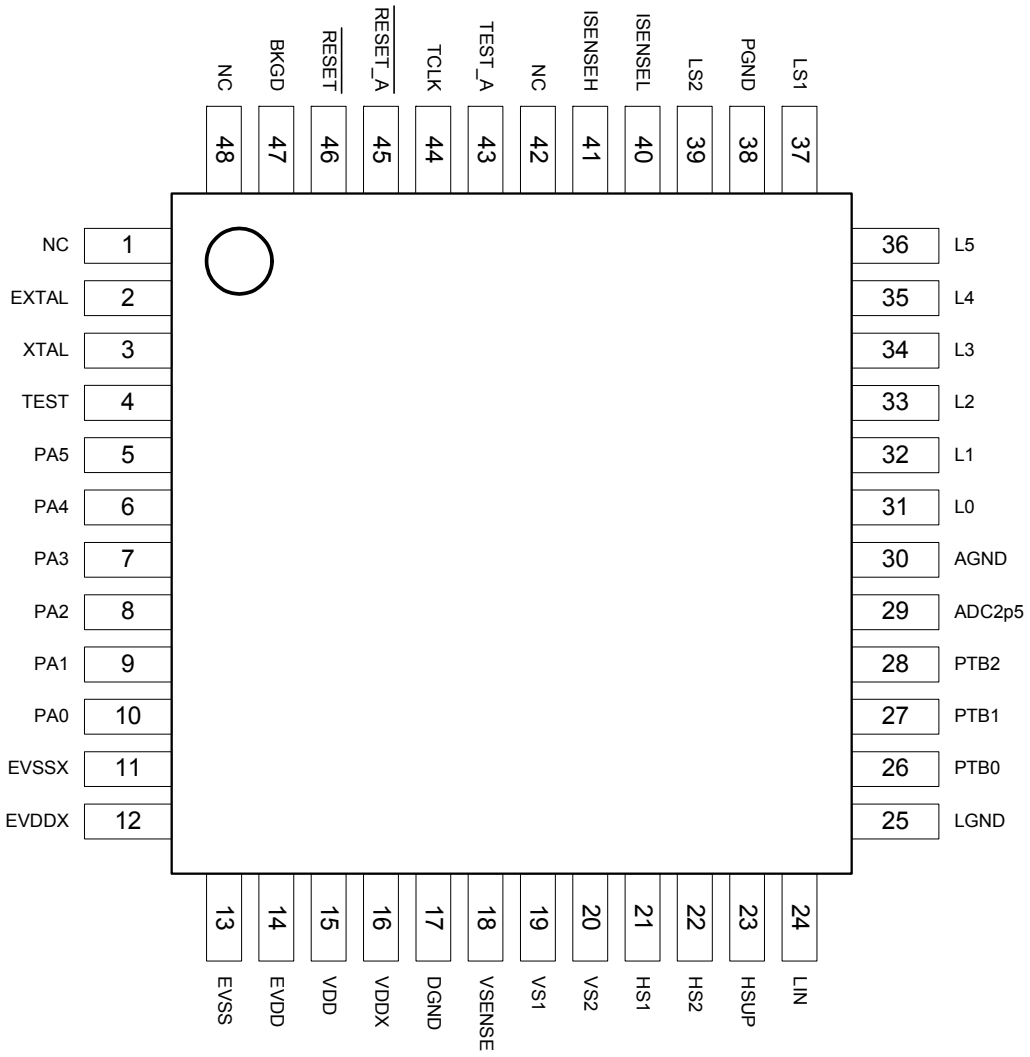


Figure 4. S/MM912F634 Pin Out

NOTE

The device exposed pad (package option AE only) is recommended to be connected to GND.

Not all pins are available for analog die option 2. See Section 4.2.3, “Analog Die Options" for details.

2.1 S/MM912F634 Pin Description

The following table gives a brief description of all available pins on the S/MM912F634 package. Refer to the highlighted chapter for detailed information.

Table 3. S/MM912F634 Pin Description

Pin #	Pin Name	Formal Name	Description
1	NC	Not connected Pin	This pin is reserved for alternative function and should be left floating or connected to GND.
2	EXTAL	MCU Oscillator Pin	EXTAL is one of the optional crystal/resonator driver and external clock pins. On reset, all the device clocks are derived from the Internal Reference Clock. See Section 4.33, “External Oscillator (S12SOSCFPV1)".

Table 3. S/MM912F634 Pin Description (continued)

Pin #	Pin Name	Formal Name	Description
3	XTAL	MCU Oscillator Pin	XTAL is one of the optional crystal/resonator driver and external clock pins. On reset, all the device clocks are derived from the Internal Reference Clock. See Section 4.33, “External Oscillator (S12SOSCFPV1)".
4	TEST	MCU Test Pin	This input only pin is reserved for test. This pin has a pull-down device. The TEST pin must be tied to EVSS in user mode.
5	PA5	MCU PA5 Pin	General purpose port A input or output pin 5. See Section 4.27, “Port Integration Module (9S12I32PIMV1)".
6	PA4	MCU PA4 Pin	General purpose port A input or output pin 4. See Section 4.27, “Port Integration Module (9S12I32PIMV1)".
7	PA3	MCU PA3 / $\overline{SS}$ Pin	General purpose port A input or output pin 3, shared with the $\overline{SS}$ signal of the integrated SPI Interface. See Section 4.27, “Port Integration Module (9S12I32PIMV1)".
8	PA2	MCU PA2 / SCK Pin	General purpose port A input or output pin 2, shared with the SCLK signal of the integrated SPI Interface. See Section 4.27, “Port Integration Module (9S12I32PIMV1)".
9	PA1	MCU PA1 / MOSI Pin	General purpose port A input or output pin 1, shared with the MOSI signal of the integrated SPI Interface. See Section 4.27, “Port Integration Module (9S12I32PIMV1)".
10	PA0	MCU PA0 / MISO Pin	General-purpose port A input or output pin 0, shared with the MISO signal of the integrated SPI Interface. See Section 4.27, “Port Integration Module (9S12I32PIMV1)".
11	EVSSX	MCU 5.0 V Ground Pin	Ground for the MCU 5.0 V power supply.
12	EVDDX	MCU 5.0 V Supply Pin	MCU 5.0 V - I/O buffer supply. See Section 4.26, “S/MM912F634 - MCU Die Overview".
13	EVSS	MCU 2.5 V Ground Pin	Ground for the MCU 2.5 V power supply.
14	EVDD	MCU 2.5 V Supply Pin	MCU 2.5 V - MCU Core- and Flash power supply. See Section 4.26, “S/MM912F634 - MCU Die Overview".
15	VDD	Voltage Regulator Output 2.5 V	+2.5 V main voltage regulator output pin. External capacitor (C_{VDD}) needed. See Section 4.4, “Power Supply".
16	VDDX	Voltage Regulator Output 5.0 V	+5.0 V main voltage regulator output pin. External capacitor (C_{VDDX}) needed. See Section 4.4, “Power Supply".
17	DGND	Digital Ground Pin	This pin is the device digital ground connection for the 5.0 V and 2.5 V logic. DGND, LGND, and AGND are internally connected to PGND via a back to back diode.
18	VSENSE	Voltage Sense Pin	Battery voltage sense input. This pin can be connected directly to the battery line for voltage measurements. The voltage present at this input is scaled down by an internal voltage divider, and can be routed to the internal ADC via the analog multiplexer.The pin is self-protected against reverse battery connections. An external resistor (R_{VSENSE}) is needed for protection[4]. See Section 4.22, “Supply Voltage Sense - VSENSE".
19	VS1	Power Supply Pin 1	This pin is the device power supply pin 1. VS1 is primarily supplying the VDDX Voltage regulator and the Hall Sensor Supply Regulator (HSUP). VS1 can be sensed via a voltage divider through the AD converter. Reverse battery protection diode is required. See Section 4.4, “Power Supply"
20	VS2	Power Supply Pin 2	This pin is the device power supply pin 2. VS2 supplies the High-side Drivers (HSx). Reverse battery protection diode required. See Section 4.4, “Power Supply"
21	HS1	High-side Output 1	This pin is the first High-side output. It is supplied through the VS2 pin. It is designed to drive small resistive loads with optional PWM. In cyclic sense mode, this output activates periodically during low power mode. See Section 4.11, “High-side Drivers - HS".
22	HS2	High-side Output 2	This pin is the second High-side output. It is supplied through the VS2 pin. It is designed to drive small resistive loads with optional PWM. In cyclic sense mode, this output activates periodically during low power mode. See Section 4.11, “High-side Drivers - HS".
23	HSUP	Hall Sensor Supply Output	This pin is designed as an 18 V Regulator to drive Hall Sensor Elements. It is supplied through the VS1 pin. An external capacitor (C_{HSUP}) is needed. See Section 4.10, “Hall Sensor Supply Output - HSUP".
24	LIN	LIN Bus I/O	This pin represents the single-wire bus transmitter and receiver. See Section 4.14, “LIN Physical Layer Interface - LIN".
25	LGND	LIN Ground Pin	This pin is the device LIN Ground connection. DGND, LGND, and AGND are internally connected to PGND via a back to back diode.

Table 3. S/MM912F634 Pin Description (continued)

Pin #	Pin Name	Formal Name	Description
26	PTB0	General Purpose I/O 0	This is the General Purpose I/O pin 0 based on VDDX with the following shared functions: • PTB0 - Bidirectional 5.0 V (VDDX) digital port I/O with selectable internal pull-up resistor. • AD0 - Analog Input Channel 0, 0…2.5 V (ADC2p5) analog input • TIM0CH0 - Timer Channel 0 Input/Output • Rx - Selectable connection to LIN / SCI See Section 4.17, “General Purpose I/O - PTB[0…2]".
27	PTB1	General Purpose I/O 1	This is the General Purpose I/O pin 1 based on VDDX with the following shared functions: • PTB1 - Bidirectional 5.0 V (VDDX) digital port I/O with selectable internal pull-up resistor. • AD1 - Analog Input Channel 1, 0…2.5 V (ADC2p5) analog input • TIM0CH1 - Timer Channel 1 Input/Output • Tx - Selectable connection to LIN / SCI See Section 4.17, “General Purpose I/O - PTB[0…2]".
28	PTB2	General Purpose I/O 2	This is the General Purpose I/O pin 2 based on VDDX with the following shared functions: • PTB2 - Bidirectional 5.0 V (VDDX) digital port I/O with selectable internal pull-up resistor. • AD2 - Analog Input Channel 2, 0…2.5 V (ADC2p5) analog input • TIM0CH2 - Timer Channel 2 Input/Output • PWM - Selectable connection to PWM Channel 0 or 1 See Section 4.17, “General Purpose I/O - PTB[0…2]".
29	ADC2p5	ADC Reference Voltage	This pin represents the ADC reference voltage and has to be connected to a filter capacitor. See Section 4.19, “Analog Digital Converter - ADC"
30	AGND	Analog Ground Pin	This pin is the device Analog to Digital Converter ground connection. DGND, LGND and AGND are internally connected to PGND via a back to back diode.
31	L0	High Voltage Input 0	This pins is the High Voltage Input 0 with the following shared functions: • L0 - Digital High Voltage Input 0. When used as digital input, a series resistor (R_{Lx}) must be used to protect against automotive transients.(5) • AD3 - Analog Input 3 with selectable divider for 0…5.0 V and 0…18 V measurement range. • WU0 - Selectable Wake-up input 0 for wake up and cyclic sense during low power mode. See Section 4.16, “High Voltage Inputs - Lx"
32	L1	High Voltage Input 1	This pins is the High Voltage Input 1 with the following shared functions: • L1 - Digital High Voltage Input 1. When used as digital input, a series resistor (R_{Lx}) must be used to protect against automotive transients.(5) • AD4 - Analog Input 4 with selectable divider for 0…5.0 V and 0…18 V measurement range. • WU1 - Selectable Wake-up input 1 for wake-up and cyclic sense during low power mode. See Section 4.16, “High Voltage Inputs - Lx".
33	L2	High Voltage Input 2	This pins is the High Voltage Input 2 with the following shared functions: • L2 - Digital High Voltage Input 2. When used as digital input, a series resistor (R_{Lx}) must be used to protect against automotive transients.(5) • AD5 - Analog Input 5 with selectable divider for 0…5.0 V and 0…18 V measurement range. • WU2 - Selectable Wake-up input 2 for wake-up and cyclic sense during low power mode. See Section 4.16, “High Voltage Inputs - Lx".
34	L3	High Voltage Input 3	This pins is the High Voltage Input 3 with the following shared functions: • L3 - Digital High Voltage Input 3. When used as digital input, a series resistor (R_{Lx}) must be used to protect against automotive transients.(5) • AD6 - Analog Input 6 with selectable divider for 0…5.0 V and 0…18 V measurement range. • WU3 - Selectable Wake-up input 3 for wake-up and cyclic sense during low power mode. See Section 4.16, “High Voltage Inputs - Lx".
35	L4	High Voltage Input 4	This pins is the High Voltage Input 4 with the following shared functions: • L4 - Digital High Voltage Input 4. When used as digital input, a series resistor (R_{Lx}) must be used to protect against automotive transients.(5) • AD7 - Analog Input 7 with selectable divider for 0…5.0 V and 0…18 V measurement range. • WU4 - Selectable Wake-up input 4 for wake-up and cyclic sense during low power mode. See Section 4.16, “High Voltage Inputs - Lx". Note: This pin function is not available on all device configurations.

Table 3. S/MM912F634 Pin Description (continued)

Pin #	Pin Name	Formal Name	Description
36	L5	High Voltage Input 5	This pins is the High Voltage Input 5 with the following shared functions: • L5 - Digital High Voltage Input 5. When used as digital input, a series resistor (R_{Lx}) must be used to protect against automotive transients.(5) • AD8 - Analog Input 8 with selectable divider for 0…5.0 V and 0…18 V measurement range. • WU5 - Selectable Wake-up input 5 for wake-up and cyclic sense during low power mode. See Section 4.16, “High Voltage Inputs - Lx". Note: This pin function is not available on all device configurations.
37	LS1	Low-side Output 1	Low-side output 1 used to drive small inductive loads like relays. The output is short-circuit protected, includes active clamp circuitry and can be also controlled by the PWM module. See Section 4.12, “Low-side Drivers - LSx".
38	PGND	Power Ground Pin	This pin is the device Low-side Ground connection. DGND, LGND and AGND are internally connected to PGND via a back to back diode.
39	LS2	Low-side Output 2	Low-side output 2 used to drive small inductive loads like relays. The output is short-circuit protected, includes active clamp circuitry and can be also controlled by the PWM module. See Section 4.12, “Low-side Drivers - LSx".
40	ISENSEL	Current Sense Pins L	Current Sense differential input “Low”. This pin is used in combination with ISENSEH to measure the voltage drop across a shunt resistor. See Section 4.20, “Current Sense Module - ISENSE". Note: This pin function is not available on all device configurations.
41	ISENSEH	Current Sense Pins H	Current Sense differential input “High”. This pin is used in combination with ISENSEL to measure the voltage drop across a shunt resistor. Section 4.20, “Current Sense Module - ISENSE". Note: This pin function is not available on all device configurations.
42	NC	Not connected Pin	This pin is reserved for alternative function and should be left floating.
43	TEST_A	Test Mode Pin	Analog die Test Mode pin for Test Mode only. This pin must be grounded in user mode.
44	TCLK	Test Clock Input	Test Mode Clock Input pin for Test Mode only. The pin can be used to disable the internal watchdog for development purpose in user mode. See Section 4.9, “Window Watchdog". The pin is recommended to be grounded in user mode.
45	$\overline{\text{RESET\_A}}$	Reset I/O	Bidirectional Reset I/O pin of the analog die. Active low signal. Internal pull-up. V_{DDX} based. See Section 4.7, “Resets". To be externally connected to the $\overline{\text{RESET}}$ pin.
46	$\overline{\text{RESET}}$	MCU Reset Pin	The $\overline{\text{RESET}}$ pin is an active low bidirectional control signal. It acts as an input to initialize the MCU to a known start-up state, and an output when an internal MCU function causes a reset. The $\overline{\text{RESET}}$ pin has an internal pull-up device to EVDDX.
47	BKGD	MCU Background Debug and Mode Pin	The BKGD/MODC pin is used as a pseudo-open-drain pin for the background debug communication. It is used as MCU operating mode select pin during reset. The state of this pin is latched to the MODC bit at the rising edge of $\overline{\text{RESET}}$. The BKGD pin has a pull-up device.
48	NC	Not connected Pin	This pin is reserved for alternative function and should be left floating or connected to GND.

Note:

4. An optional filter capacitor C_{VSENSE} is recommended to be placed between the board connector and R_{VSENSE} to GND for increased ESD performance.
5. An optional filter capacitor C_{Lx} is recommended to be placed between the board connector and R_{Lx} to GND for increased ESD performance.

2.2 MCU Die Signal Properties

This section describes the external MCU signals. It includes a table of signal properties.

Table 4. Signal Properties Summary

Pin Name Function 1	Pin Name Function 2	Power Supply	Internal Pull Resistor		Description
			CTRL	Reset State	
EXTAL	—	V_{DD}	NA	NA	Oscillator pins
XTAL	—	V_{DD}	NA	NA	
$\overline{\text{RESET}}$	—	V_{DDX}	Pull-up		External reset

Table 4. Signal Properties Summary (continued)

Pin Name Function 1	Pin Name Function 2	Power Supply	Internal Pull Resistor		Description
			CTRL	Reset State	
TEST	—	N.A.	$\overline{\text{RESET}}$ pin	Down	Test input
BKGD	MODC	V_{DDX}	Always on	UP	Background debug
PA5	—	V_{DDX}	NA	NA	Port A I/O
PA4	—	V_{DDX}	NA	NA	Port A I/O
PA3	SS	V_{DDX}	NA	NA	Port A I/O, SPI
PA2	SCK	V_{DDX}	NA	NA	Port A I/O, SPI
PA1	MOSI	V_{DDX}	NA	NA	Port A I/O, SPI
PA0	MISO	V_{DDX}	NA	NA	Port A I/O, SPI

3 Electrical Characteristics

3.1 General

This supplement contains electrical information for the embedded MC9S12I32 microcontroller die, as well as the S/MM912F634 analog die.

3.2 Absolute Maximum Ratings

Absolute maximum ratings are stress ratings only. A functional operation under or outside those maxima is not guaranteed. Stress beyond those limits may affect the reliability or cause permanent damage of the device.

This device contains circuitry protecting against damage due to high static voltage or electrical fields. However, it is advised that normal precautions be taken to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate voltage level. All voltages are with respect to ground unless otherwise noted.

Table 5. Absolute Maximum Electrical Ratings - Analog Die

Ratings	Symbol	Value	Unit
Supply Voltage at VS1 and VS2 Normal Operation (DC) Transient Conditions (load dump) Transient input voltage with external component (according to LIN Conformance Test Specification / ISO7637-2)	$V_{SUP(SS)}$ $V_{SUP(PK)}$ $V_{SUP(TR)}$	-0.3 to 27 -0.3 to 40 see Section 3.9, “Additional Test Information ISO7637-2"	V
L0…L5 - Pin Voltage Normal Operation with a series R_{LX} resistor (DC) Transient input voltage with external component (according to LIN Conformance Test Specification / ISO7637-2)	V_{LxDC} V_{LxTR}	-27 to 40 see Section 3.9, “Additional Test Information ISO7637-2"	V
LIN Pin Voltage Normal Operation (DC) Transient input voltage with external component (according to LIN Conformance Test Specification / ISO7637-2)	V_{BUSDC} V_{BUSTR}	-33 to 40 see Section 3.9, “Additional Test Information ISO7637-2"	V
Supply Voltage at VDDX	V_{DDX}	-0.3 to 5.5	V
Supply Voltage at VDD (6)	V_{DD}	-0.3 to 2.75	V
VDD output current	I_{VDD}	Internally Limited	A
VDDX output current	I_{VDDX}	Internally Limited	A
TCLK Pin Voltage	V_{TCLK}	-0.3 to 10	V
$\overline{\text{RESET\_A}}$ Pin Voltage	V_{IN}	-0.3 to V_{DDx}+0.3	V
Input / Output Pins PTB[0:2] Voltage	V_{IN}	-0.3 to V_{DDx}+0.3	V
HS1 and HS2 Pin Voltage (DC)	V_{HS}	-0.3 to VS2+0.3	V
LS1 and LS2 Pin Voltage (DC)	V_{LS}	-0.3 to 45	V
ISENSEH and ISENSEL Pin Voltage (DC)	V_{ISENSE}	-0.3 to 40	V
HSUP Pin Voltage (DC)	V_{HSUP}	-0.3 to VS1+0.3	V
VSENSE Pin Voltage (DC)	V_{VSENSE}	-27 to 40	V

Note:

6. Caution: As this pin is adjacent to the VDDX pin, care should be taken to avoid a short between VDD and VDDX, for example, during the soldering process. A short-circuit between these pins might lead to permanent damage.

Table 6. Maximum Electrical Ratings - MCU Die

Ratings	Symbol	Value	Unit
5.0 V Supply Voltage	V_{EDDX}	-0.3 to 6.0	V
2.5 V Supply Voltage	V_{EDD}	-0.3 to 2.75	V
Digital I/O input voltage (PA0...PA7, PE0, PE1)	V_{IN}	-0.3 to 6.0	V
EXTAL, XTAL	V_{ILV}	-0.3 to 2.16	V
TEST input	V_{TEST}	-0.3 to 10.0	V
Instantaneous maximum current Single pin limit for all digital I/O pins	I_D	-25 to 25	mA
Instantaneous maximum current Single pin limit for EXTAL, XTAL	I_{DL}	-25 to 25	mA

Table 7. Maximum Thermal Ratings

Ratings	Symbol	Value	Unit
Storage Temperature	T_{STG}	-55 to 150	°C
Package Thermal Resistance - LQFP48-EP Four layer board (JEDEC 2s2p) Junction to Ambient Natural Convection (7) Junction to Board (9) Two layer board (JEDEC 1s) Junction to Ambient Natural Convection (7), (8)	 $R_{\theta JA}$ $R_{\theta JB}$ $R_{\theta JA}$	 39 16 91	°C/W
Package Thermal Resistance - LQFP48 Four layer board (JEDEC 2s2p) Junction to Ambient Natural Convection (7) Junction to Board (9) Two layer board (JEDEC 1s) Junction to Ambient Natural Convection (7), (8)	 $R_{\theta JA}$ $R_{\theta JB}$ $R_{\theta JA}$	 59 31 96	°C/W
Peak Package Reflow Temperature During Reflow (10),(11)	T_{PPRT}	300	°C

Notes

7. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
8. Per JEDEC JESD51-6 with the board (JESD51-7) horizontal.
9. Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
10. Pin soldering temperature limit is for 10 seconds maximum duration. Not designed for immersion soldering. Exceeding these limits may cause malfunction or permanent damage to the device.
11. NXP's Package Reflow capability meets Pb-free requirements for JEDEC standard J-STD-020C. For Peak Package Reflow Temperature and Moisture Sensitivity Levels (MSL), Go to www.NXP.com, search by part number [e.g. remove prefixes/suffixes and enter the core ID to view all orderable parts. (i.e. MC34xxxD enter 34xxx), and review parametrics.

3.3 Operating Conditions

This section describes the operating conditions of the device. Unless otherwise noted those conditions apply to all the following data.

Table 8. Operating Conditions

Ratings	Symbol	Value	Unit
Analog Die Nominal Operating Voltage	V_{SUP}	5.5 to 18	V
Analog Die Functional Operating Voltage - Device is fully functional. All features are operating.	V_{SUPOP}	5.5 to 27	V
MCU I/O and supply voltage(12)	V_{EDDX}	4.5 to 5.5	V

Table 8. Operating Conditions (continued)

Ratings	Symbol	Value	Unit
MCU Digital logic supply voltage[12]	V_{EDD}	2.25 to 2.75	V
MCU External Oscillator	f_{OSC}	4.0 to 16	MHz
MCU Bus frequency	f_{BUS}	f_{BUSMAX}[13]	MHz
Operating Ambient Temperature, MM912x634xVxxx	T_A	-40 to 105	°C
Operating Junction Temperature - Analog Die	T_{J_A}	-40 to 150	°C
Operating Junction Temperature - MCU Die	T_{J_M}	-40 to 140	°C

Note:
12. During power up and power down sequence always $V_{DD} < V_{DDX}$
13. f_{BUSMAX} frequency ratings differ by device and is specified in Table 1

3.4 Supply Currents

This section describes the current consumption characteristics of the device as well as the conditions for the measurements.

3.4.1 Measurement Conditions

All measurements are without output loads. Unless otherwise noted, the currents are measured in MCU special single chip mode and the CPU code is executed from RAM.

Table 9. Supply Currents

Ratings	Symbol	Min	Typ[14]	Max	Unit
Normal Mode analog die only, excluding external loads, LIN Recessive State (5.5 V ≤ V_{SUP} ≤ 18 V, 2.25 V ≤ E_{VDD} ≤ 2.75 V, 4.5 V ≤ E_{VDDX} ≤ 5.5 V, -40 °C ≤ T_{J_A} ≤ 150 °C).	I_{RUN_A}	-	5.0	8.0	mA
Normal Mode MCU die only (T_{J_M} = 140 °C; V_{DD} = 2.75 V, V_{DDX} = 5.5 V, f_{OSC} = 4.0 MHz, f_{BUS} = f_{BUSMAX}[18])[15]	I_{RUN_M}	-	12.5	15	mA
Stop Mode internal analog die only, excluding external loads, LIN Recessive State, Lx enabled, measured at VS1+VS2 (5.5 V ≤ V_{SUP} ≤ 18 V, 2.25 V ≤ E_{VDD} ≤ 2.75 V, 4.5 V ≤ E_{VDDX} ≤ 5.5 V) -40 °C ≤ T_{J_A} ≤ 125 °C 125 °C < T_{J_A} ≤ 140 °C	I_{STOP_A}	 - -	 20 -	 40 50	µA
Stop Mode MCU die only (V_{DD} = 2.75 V, V_{DDX} = 5.5 V, f_{OSC} = 4.0 MHz, f_{BUS} = f_{BUSMAX}[18]; MCU in STOP; RTI and COP off)[16] T_{J_M} = 140 °C T_{J_M} = 105 °C T_{J_M} = 25 °C	I_{STOP_M}	 - - -	 0.135 0.035 0.010	 0.400 0.200 0.030	mA
Stop Mode MCU die only (V_{DD} = 2.75 V, V_{DDX} = 5.5 V, f_{OSC} = 4.0 MHz, f_{BUS} = f_{BUSMAX}[18]; MCU in STOP; RTI and COP on)[16] T_{J_M} = 140 °C T_{J_M} = 105 °C T_{J_M} = 25 °C	I_{STOP_M}	 - - -	 0.205 0.104 0.079	 0.500 0.300 0.110	mA
Wait Mode MCU die only (T_{J_M} = 140 °C; V_{DD} = 2.75 V, V_{DDX} = 5.5 V, f_{OSC} = 4.0 MHz, f_{BUS} = f_{BUSMAX}[18]; All modules except RTI disabled)[17]	I_{WAIT_M}	-	7.0	12	mA
Sleep Mode (VDD = VDDX = OFF; 5.5 V ≤ V_{SUP} ≤ 18 V; -40 °C ≤ T_{J_A} ≤ 150 °C; 3.0 V < L_X < 1.0 V).	I_{SLEEP}	-	15	28	µA
Cyclic Sense Supply Current Adder (5.0 ms Cycle)	I_{CS}	-	15	20	µA

Note:
14. Typical values noted reflect the approximate parameter mean at T_A = 25 °C
15. I_{RUN_M} denotes the sum of the currents flowing into VDD and VDDX.
16. I_{STOP_M} denotes the sum of the currents flowing into VDD and VDDX.
17. I_{WAIT_M} denotes the sum of the currents flowing into VDD and VDDX.
18. f_{BUSMAX} frequency ratings differ by device and is specified in Table 1.

3.5 Static Electrical Characteristics

Static electrical characteristics noted under conditions 5.5V ≤ VSUP ≤ 18 V, -40 °C ≤ T_A ≤ 105 °C, unless otherwise noted. Typical values noted reflect the approximate parameter mean at T_A = 25 °C under nominal conditions unless otherwise noted.

3.5.1 Static Electrical Characteristics Analog Die

Table 10. Static Electrical Characteristics - Power Supply

Ratings	Symbol	Min	Typ	Max	Unit
Power-On Reset (POR) Threshold (measured on VS1)	V_{POR}	1.5	-	3.5	V
Low Voltage Warning (LVI) Threshold (measured on VS1, falling edge) Hysteresis (measured on VS1)	 V_{LVI} V_{LVI_H}	 5.55 -	 6.0 1.0	 6.6 -	V
High Voltage Warning (HVI) Threshold (measured on VS2, rising edge) Hysteresis (measured on VS2)	 V_{HVI} V_{HVI_H}	 18 -	 19.25 1.0	 20.5 -	V
Low Battery Warning (LBI) Threshold (measured on VSENSE, falling edge) Hysteresis (measured on VSENSE)	 V_{LBI} V_{LBI_H}	 5.55 -	 6.0 1.0	 6.6 -	V
J2602 Undervoltage threshold	$V_{J2602UV}$	5.5	5.7	6.2	V
Low VDDX Voltage (LVRX) Threshold	V_{LVRX}	2.7	3.0	3.3	V
Low VDD Voltage Reset (LVR) Threshold Normal Mode	V_{LVR}	2.30	2.35	2.4	V
Low VDD Voltage Reset (LVR) Threshold Stop Mode (19)	V_{LVRS}	1.6	1.85	2.1	V
VDD Overvoltage Threshold (VROV)	V_{VDDOV}	2.575	2.7875	3.0	V
VDDX Overvoltage Threshold (VROVX)	V_{VDDXOV}	5.25	5.675	6.1	V

Note:
19. See MM912F634ER, MM912F634 , Silicon Analog Mask (M91W) / Digital Mask (M33G) Errata

Table 11. Static Electrical Characteristics - Resets

Ratings	Symbol	Min	Typ	Max	Unit
Low-state Output Voltage I_{OUT} = 2.0 mA	V_{OL}	-	-	0.8	V
Pull-up Resistor	R_{RPU}	25	-	50	kΩ
Low-state Input Voltage	V_{IL}	-	-	$0.3V_{DDX}$	V
High-state Input Voltage	V_{IH}	$0.7V_{DDX}$	-	-	V
Reset Release Voltage (VDDX)	V_{RSTRV}	-	1.5	-	V
RESET_A pin Current Limitation		5.0	7.5	10	mA

Table 12. Static Electrical Characteristics - Window Watchdog

Ratings	Symbol	Min	Typ	Max	Unit
Watchdog Disable Voltage (fixed voltage)	V_{TST}	7.0	-	10	V
Watchdog Enable Voltage (fixed voltage)	V_{TSTEN}	-	-	5.5	V

Table 13. Static Electrical Characteristics - Voltage Regulator 5V (VDDX)

Ratings	Symbol	Min	Typ	Max	Unit
Normal Mode Output Voltage 1.0 mA < I_{VDDX} + $I_{VDDXINTERNAL}$ < 80 mA; 5.5 V < V_{SUP} < 27 V (20)	V_{DDXRUN}	4.75	5.00	5.25	V
Normal Mode Output Current Limitation (I_{VDDX})	$I_{VDDXLIMRUN}$	80	130	200	mA
Stop Mode Output Voltage (I_{VDDX} + $I_{VDDXINTERNAL}$ < 500 µA for $T_J \geq$ 25 °C; I_{VDDX} + $I_{VDDXINTERNAL}$ < 400 µA for T_J < 25 °C) (20)	$V_{DDXSTOP}$	-	5.0	5.5	V
Stop Mode Output Current Limitation (I_{VDDX})	$I_{VDDXLIMSTOP}$	-	-	20	mA
Line Regulation Normal Mode, I_{VDDX} = 80 mA Stop Mode, I_{VDDX} = 500 µA	LR_{XRUN} LR_{XSTOP}	- -	20 -	25 200	mV
Load Regulation Normal Mode, 1.0 mA < I_{VDDX} < 80 mA Normal Mode, V_{SUP} = 3.6 V, 1.0 mA < I_{VDDX} < 40 mA Stop Mode, 100 µA < I_{VDDX} < 500 µA	LD_{XRUN} LD_{XCRK} LD_{XSTOP}	- - -	15 - -	80 200 250	mV
External Capacitor	C_{VDDX}	1.0	-	10	µF
External Capacitor ESR	C_{VDDX_R}	-	-	10	Ω

Note:
20. $I_{VDDXINTERNAL}$ includes internal consumption from both analog and MCU die.

Table 14. Static Electrical Characteristics - Voltage Regulator 2.5 V (VDD)

Ratings	Symbol	Min	Typ	Max	Unit
Normal Mode Output Voltage 1.0 mA < I_{VDD} + $I_{VDDINTERNAL}$ ≤ 45 mA; 5.5 V < V_{SUP} < 27 V (21)	V_{DDRUN}	2,425	2.5	2,575	V
Normal Mode Output Current Limitation (I_{VDD}) T_J < 25 °C $T_J \geq$ 25 °C	$I_{VDDLIMRUN}$	- -	80 80	120 143	mA
Stop Mode Output Voltage´ (I_{VDD} + $I_{VDDINTERNAL}$ < 500 µA for $T_J \geq$ 25 °C; I_{VDD} + $I_{VDDINTERNAL}$ < 400 µA for T_J < 25 °C) (21)	V_{DDSTOP}	2.25	2.5	2.75	V
Stop Mode Output Current Limitation (I_{VDD})	$I_{VDDLIMSTOP}$	-	-	10	mA
Line Regulation Normal Mode, I_{VDD} = 45 mA Stop Mode, I_{VDD} = 1.0 mA	LR_{RUN} LR_{STOP}	- -	10 -	12.5 200	mV
Load Regulation Normal Mode, 1.0 mA < I_{VDD} < 45 mA Normal Mode, V_{SUP} = 3.6 V, 1.0 mA < I_{VDD} < 30 mA Stop Mode, 100 µA < I_{VDD} < 500 µA	LD_{RUN} LD_{CRK} LD_{STOP}	- - -	7.5 - -	40 40 200	mV
External Capacitor	C_{VDD}	1.0	-	10	µF
External Capacitor ESR	C_{VDD_R}	-	-	10	Ω

Note:
21. $I_{VDDINTERNAL}$ includes internal consumption from both analog and MCU die.

Table 15. Static Electrical Characteristics - Hall Sensor Supply Output - HSUP

Ratings	Symbol	Min	Typ	Max	Unit
Current Limitation (3.7 V ≤ V_{SUP} ≤ 18 V)	I_{HSUP}	40	70	90	mA
Output Drain-to-Source On resistance T_J = 150 °C, I_{LOAD} = 30 mA; 5.5 V ≤ V_{SUP} ≤ 16 V T_J = 150 °C, I_{LOAD} = 30 mA; 3.7 V ≤ V_{SUP} < 5.5 V	$R_{DS(on)}$	 - -	 - -	 10 13	Ω
Output Voltage: (18 V ≤ V_{SUP} ≤ 27 V)	$VHSUP_{MAX}$	16	17.5	18	V
Load Regulation (1.0 mA < I_{HSUP} < 30 mA; V_{SUP} > 18 V)	LD_{HSUP}	-	-	500	mV
Hall Supply Capacitor Range	C_{HSUP}	0.22	-	10	µF
External Capacitor ESR	C_{HSUP_R}	-	-	10	Ω

Table 16. Static Electrical Characteristics - High-side Drivers - HS

Ratings	Symbol	Min	Typ	Max	Unit
Output Drain-to-Source On resistance T_J = 25 °C, I_{LOAD} = 50 mA; V_{SUP} > 9.0 V T_J = 150 °C, I_{LOAD} = 50 mA; V_{SUP} > 9.0 V T_J = 150 °C, I_{LOAD} = 30 mA; 5.5V < V_{SUP} < 9.0 V	$R_{DS(ON)}$	 - - -	 - - -	 7.0 10 14	Ω
Output Current Limitation (0 V < V_{OUT} < V_{SUP} - 2.0 V)	I_{LIMHSX}	60	110	250	mA
Open Load Current Detection	I_{OLHSX}	-	5.0	7.5	mA
Leakage Current (-0.2 V < V_{HSx} < V_{S2} + 0.2 V)	I_{LEAK}	-	-	10	µA
Current Limitation Flag Threshold (5.5 V < V_{SUP} < 27 V)	V_{THSC}	V_{SUP} -2	-	-	V

Table 17. Static Electrical Characteristics - Low-side Drivers - LS

Ratings	Symbol	Min	Typ	Max	Unit
Output Drain-to-Source On resistance T_J = 25 °C, I_{LOAD} = 150 mA, V_{SUP} > 9.0 V T_J = 150 °C, I_{LOAD} = 150 mA, V_{SUP} > 9.0 V T_J = 150 °C, I_{LOAD} = 120 mA, 5.5 V < V_{SUP} < 9.0 V	$R_{DS(ON)}$	 – – –	 – – –	 2.5 4.5 10	Ω
Output Current Limitation (2.0 V < V_{OUT} < V_{SUP})	I_{LIMLSX}	180	275	380	mA
Open Load Current Detection	I_{OLLSX}	-	8.0	12	mA
Leakage Current (-0.2 V < V_{OUT} < VS1)	I_{LEAK}	-	-	10	µA
Active Output Energy Clamp (I_{OUT} = 150 mA)	V_{CLAMP}	40	-	45	V
Coil Series Resistance (I_{OUT} = 150 mA)	R_{COIL}	120	-		Ω
Coil Inductance (I_{OUT} = 150 mA)	R_{COIL}	-	-	400	mH
Current Limitation Flag Threshold (5.5 V < V_{SUP} < 27 V)	V_{THSC}	2.0	-	-	V

Table 18. Static Electrical Characteristics - LIN Physical Layer Interface - LIN

Ratings	Symbol	Min	Typ	Max	Unit
Current Limitation for Driver dominant state. V_{BUS} = 18 V	I_{BUSLIM}	40	120	200	mA
Input Leakage Current at the Receiver incl. Pull-up Resistor RSLAVE; Driver OFF; VBUS = 0 V; VBAT = 12 V	$I_{BUS\_PAS\_DOM}$	-1.0	-	-	mA
Input Leakage Current at the Receiver incl. Pull-up Resistor RSLAVE; Driver OFF; 8.0 V < VBAT < 18 V; 8.0 V < VBUS < 18 V; VBUS ≥ VBAT	$I_{BUS\_PAS\_REC}$	-	-	20	µA

Table 18. Static Electrical Characteristics - LIN Physical Layer Interface - LIN (continued)

Ratings	Symbol	Min	Typ	Max	Unit
Input Leakage Current; GND Disconnected; GNDDEVICE = VSUP; 0 < VBUS < 18 V; VBAT = 12 V	$I_{BUS\_NO\_GND}$	-1.0	-	1.0	mA
Input Leakage Current; VBAT disconnected; VSUP_DEVICE = GND; 0 < VBUS < 18 V	$I_{BUS\_NO\_BAT}$	-	-	100	µA
Receiver Input Voltage; Receiver Dominant State	V_{BUSDOM}	-	-	0.4	V_{SUP}
Receiver Input Voltage; Receiver Recessive State	V_{BUSREC}	0.6	-	-	V_{SUP}
Receiver Threshold Center (V_{TH_DOM} + V_{TH_REC})/2	V_{BUS_CNT}	0.475	0.5	0.525	V_{SUP}
Receiver Threshold Hysteresis (V_{TH_REC} - V_{TH_DOM})	V_{BUS_HYS}	-	-	0.175	V_{SUP}
Voltage Drop at the serial Diode	D_{SER_INT}	0.4	0.7	1.0	V
LIN Pull-up Resistor	R_{SLAVE}	20	30	60	kΩ
Bus Wake-up Threshold from Stop or Sleep[22]	V_{WUP}	4.5	5.0	6.0	V
Bus Dominant Voltage	V_{DOM}	-	-	2.5	V

Note:
22. Considering drop from VBAT to LIN, at very low VBAT level, the internal logic detects a dominant as the threshold does not decrease with VSUP.

Table 19. Static Electrical Characteristics - High Voltage Inputs - Lx

Ratings	Symbol	Min	Typ	Max	Unit
Low Detection Threshold 7.0 V ≤ V_{SUP} ≤ 27 V 5.5 V ≤ V_{SUP} ≤ 7 V	V_{THL}	 2.2 1.5	 2.5 2.5	 3.4 4.0	V
High Detection Threshold 7.0 V ≤ V_{SUP} ≤ 27 V 5.5 V ≤ V_{SUP} ≤ 7 V	V_{THH}	 2.6 2.0	 3.0 3.0	 3.7 4.5	V
Hysteresis 5.5 V ≤ V_{SUP} ≤ 27 V	V_{HYS}	0.25	0.45	1.0	V
Input Current Lx (-0.2 V < V_{IN} < VS1)	I_{IN}	-10	-	10	µA
Analog Input Impedance Lx	R_{LxIN}	-	-	1.2	MΩ
Lx Series Resistor	R_{Lx}	9.5	10	10.5	kΩ
Lx Capacitor (optional)[23]	C_{Lx}	-	100	-	nF
Analog Input Divider Ratio ($RATIO_{Lx}$ = V_{Lx} / V_{ADOUT0}) LXDS (Lx Divider Select) = 0 LXDS (Lx Divider Select) = 1	$RATIO_{Lx}$	 - -	 2.0 7.2	 - -	
Analog Input Divider Ratio Accuracy	$RATIO_{LX}$	-5.5	-	5.5	%
Analog Inputs Channel Ratio - Mismatch LXDS (Lx Divider Select) = 0 LXDS (Lx Divider Select) = 1	Lx_{MATCH}	 - -	 - -	 5.0 5.0	%

Note:
23. The ESD behavior specified in Section 3.8, “ESD Protection and Latch-up Immunity" are guaranteed without the optional capacitor.

Table 20. Static Electrical Characteristics - General Purpose I/O - PTB[0…2]

Ratings	Symbol	Min	Typ	Max	Unit
Input high voltage	V_{IH}	$0.7V_{DDX}$	-	V_{DDX}+0.3	V
Input low voltage	V_{IL}	V_{SS}-0.3	-	$0.35V_{DDX}$	V
Input hysteresis	V_{HYS}	-	140	-	mV
Input high voltage (VS1 = 3.7 V)	$V_{IH3.7}$	2.1	-	V_{DDX}+0.3	V

Table 20. Static Electrical Characteristics - General Purpose I/O - PTB[0…2] (continued)

Ratings	Symbol	Min	Typ	Max	Unit
Input low voltage (VS1 = 3.7 V)	$V_{IL3.7}$	V_{SS}-0.3	-	1.4	V
Input hysteresis (VS1 = 3.7 V)	$V_{HYS3.7}$	100	200	300	mV
Input leakage current (pins in high-impedance input mode) (V_{IN} = V_{DDX} or V_{SSX})	I_{IN}	-1.0	-	1.0	µA
Output high voltage (pins in output mode) Full drive I_{OH} = –10 mA	V_{OH}	V_{DDX}-0.8	-	-	V
Output low voltage (pins in output mode) Full drive I_{OL} = +10 mA	V_{OL}	-	-	0.8	V
Internal pull-up resistance (V_{IH} min > Input voltage > V_{IL} max)	R_{PUL}	26.25	37.5	48.75	kΩ
Input capacitance	C_{IN}	-	6.0	-	pF
Clamp Voltage when selected as analog input	V_{CL_AIN}	VDD	-	-	V
Analog Input impedance = 10 kΩ max, Capacitance = 12 pF	R_{AIN}	-	-	10	kΩ
Analog Input Capacitance = 12 pF	C_{AIN}	-	12	-	pF
Maximum current all PTB combined (VDDX capability)	I_{BMAX}	-15	-	15	mA
Output Drive strength at 10 MHz	C_{OUT}	-	-	100	pF

Table 21. Static Electrical Characteristics - Analog Digital Converter - ADC(24)

Ratings	Symbol	Min	Typ	Max	Unit
ADC2p5 Reference Voltage 5.5 V < V_{SUP} < 27 V	$V_{ADC2p5RUN}$	2,45	2.5	2,55	V
ADC2p5 Reference Stop Mode Output Voltage	$V_{ADC2p5STOP}$	-	-	100	mV
Line Regulation, Normal Mode	LR_{RUNA}	-	10	12.5	mV
External Capacitor	C_{ADC2p5}	0.1	-	1.0	µF
External Capacitor ESR	C_{VDD_R}	-	-	10	W
Scale Factor Error	E_{SCALE}	-1	-	1	LSB
Differential Linearity Error	E_{DNL}	-1.5	-	1.5	LSB
Integral Linearity Error	E_{INL}	-1.5	-	1.5	LSB
Zero Offset Error	E_{OFF}	-2.0	-	2.0	LSB
Quantization Error	E_Q	-0.5	-	0.5	LSB
Total Error with offset compensation	TE	-5.0	-	5.0	LSB
Bandgap measurement Channel (CH14) Valid Result Range (including ±7.0% bg1p25 sleep accuracy + high-impedance measurement error of ±5.0% at f_{ADC})(25)	AD_{CH14}	1.1	1.25	1.4	V

Note:
24. No external load allowed on the ADC2p5 pin.
25. Reduced ADC frequency lowers measurement error.

Table 22. Static Electrical Characteristics - Current Sense Module - ISENSE

Ratings	Symbol	Min	Typ	Max	Unit
Gain	G				
CSGS (Current Sense Gain Select) = 000		-	7.0	-	
CSGS (Current Sense Gain Select) = 001		-	9.0	-	
CSGS (Current Sense Gain Select) = 010		-	10	-	
CSGS (Current Sense Gain Select) = 011		-	12	-	
CSGS (Current Sense Gain Select) = 100		-	14	-	
CSGS (Current Sense Gain Select) = 101		-	18	-	
CSGS (Current Sense Gain Select) = 110		-	24	-	
CSGS (Current Sense Gain Select) = 111		-	36	-	
Gain Accuracy		-3.0	-	3.0	%
Offset		-1.5	-	1.5	%
Resolution[26]	RES	-	51	-	mA/LSB
ISENSEH, ISENSEL Input Common Mode Voltage Range	V_{IN}	-0.2	-	3.0	V
Current Sense Module - Normal Mode Current Consumption Adder (CSE = 1)	I_{ISENSE}	-	600	-	µA

Note:
26. RES = 2.44 mV/(GAIN*R_{SHUNT})

Table 23. Static Electrical Characteristics - Temperature Sensor - TSENSE

Ratings	Symbol	Min	Typ	Max	Unit
Internal Chip Temperature Sense Gain[27]	TS_G	-	9.17	-	mV/k
Internal Chip Temperature Sense Error at the end of conversion[27]	TS_{ERR}	–5.0	-	5.0	°C
Temperature represented by a ADC_{IN} Voltage of 0.150 V[27]	$T_{0.15V}$	-55	-50	-45	°C
Temperature represented by a ADC_{IN} Voltage of 1.984 V[27]	$T_{1.984V}$	145	150	155	°C

Note:
27. Guaranteed by design and characterization.

Table 24. Static Electrical Characteristics - Supply Voltage Sense - VSENSE and VS1SENSE

Ratings	Symbol	Min	Typ	Max	Unit
VSENSE Input Divider Ratio ($RATIO_{VSENSE}$ = V_{VSENSE} / ADCIN) 5.5 V < V_{SUP} < 27 V	$RATIO_{VSENSE}$		10.8		
VSENSE error - whole path (VSENSE pin to Digital value)	ER_{VSENSE}	-	-	5.0	%
VS1SENSE Input Divider Ratio ($RATIO_{VS1SENSE}$ = $V_{VS1SENSE}$ / ADCIN) 5.5 V < V_{SUP} < 27 V	$RATIO_{VS1SENSE}$		10.8		
VS1SENSE error - whole path (VS1 pin to Digital value)	$ER_{VS1SENSE}$	-	-	5.0	%
VSENSE Series Resistor	R_{VSENSE}	9.5	10	10.5	kΩ
VSENSE Capacitor (optional)[28]	C_{VSENSE}	-	100	-	nF

Note:
28. The ESD behavior specified in Section 3.8, “ESD Protection and Latch-up Immunity" is guaranteed without the optional capacitor.

3.5.2 Static Electrical Characteristics MCU Die

3.5.2.1 I/O Characteristics

This section describes the characteristics of all I/O pins except EXTAL, XTAL, TEST and supply pins.

Table 25. 5.0 V I/O Characteristics for PTA, $\overline{\text{RESET}}$ and BKGD Pins

Ratings	Symbol	Min	Typ	Max	Unit
Input high voltage	V_{IH}	0.65*V_{DD}	-	-	V
Input high voltage	V_{IH}	-	-	V_{DD} + 0.3	V
Input low voltage	V_{IL}	-	-	0.35*V_{DD}	V
Input low voltage	V_{IL}	V_{SS} - 0.3	-	-	V
Input hysteresis	V_{HYS}	-	250	-	mV
Input leakage current (pins in high-impedance input mode) V_{in} = V_{DDX} or V_{SSX}	I_{IN}	-1.0	-	1.0	µA
Output high voltage (pins in output mode) Partial Drive I_{OH} = -2.0 mA	V_{OH}	V_{DD} – 0.8	-	-	V
Output high voltage (pins in output mode) Full Drive I_{OH} = -10 mA	V_{OH}	V_{DD} – 0.8	-	-	V
Output low voltage (pins in output mode) Partial drive I_{OL} = +2.0 mA	V_{OL}	-	-	0.8	V
Output low voltage (pins in output mode) Full Drive I_{OL} = +10 mA	V_{OL}	-	-	0.8	V
Internal pull-up resistance (V_{IH}min > input voltage > V_{IL}max)	R_{PUL}	25	-	50	kΩ
Internal pull-down resistance (V_{IH}min > input voltage > V_{IL}max)	R_{PDH}	25	-	50	kΩ
Input capacitance	C_{in}	-	6.0	-	pF
Injection current[29] Single pin limit Total device Limit, sum of all injected currents	 I_{ICS} I_{ICP}	 -2.5 -25	 - -	 2.5 25	mA

Note:
29. Refer to Section 3.8, “ESD Protection and Latch-up Immunity" for more details.

3.6 Dynamic Electrical Characteristics

Dynamic electrical characteristics noted under conditions 5.5V ≤ VSUP ≤ 18 V, -40 °C ≤ T_A ≤ 105 °C, unless otherwise noted. Typical values noted reflect the approximate parameter mean at T_A = 25 °C under nominal conditions unless otherwise noted.

3.6.1 Dynamic Electrical Characteristics Analog Die

Table 26. Dynamic Electrical Characteristics - Modes of Operation

Ratings	Symbol	Min	Typ	Max	Unit
VDD Short Timeout	t_{VTO}	110	150	205	ms
Analog Base Clock	f_{BASE}	-	100	-	kHz
Reset Delay	t_{RST}	140	200	280	µs

Table 27. Dynamic Electrical Characteristics - Power Supply

Ratings	Symbol	Min	Typ	Max	Unit
Glitch Filter Low Battery Warning (LBI)[30]	t_{LB}	-	2.0	-	µs
Glitch Filter Low Voltage Warning (LVI)[30]	t_{LV}	-	2.0	-	µs

Table 27. Dynamic Electrical Characteristics - Power Supply (continued)

Ratings	Symbol	Min	Typ	Max	Unit
Glitch Filter High Voltage Warning (HVI)[30]	t_{HV}	-	2.0	-	µs

Note:
30. Guaranteed by design.

Table 28. Dynamic Electrical Characteristics - Die to Die Interface - D2D

Ratings	Symbol	Min	Typ	Max	Unit
Operating Frequency (D2DCLK, D2D[0:3])	f_{D2D}	$f_{ADC(MIN)}$	-	f_{BUSMAX}[31]	MHz

Note:
31. f_{BUSMAX} frequency ratings differ by device and is specified in Table 1

Table 29. Dynamic Electrical Characteristics - Resets

Ratings	Symbol	Min	Typ	Max	Unit
Reset Deglitch Filter Time	t_{RSTDF}	1.2	2.0	3.0	µs
Reset Low Level Duration	t_{RSTLOW}	140	200	280	µs

Table 30. Dynamic Electrical Characteristics - Wake-up / Cyclic Sense

Ratings	Symbol	Min	Typ	Max	Unit
Lx Wake-up Filter Time	t_{WUF}	-	20		µs
Cyclic Sense / Forced Wake-up Timing Accuracy - not trimmed	CS_{AC}	-35	-	35	%
Cyclic Sense / Forced Wake-up Timing Accuracy - trimmed[32]	CS_{ACT}	-5.0	-	5.0	%
Time between HSx on and Lx sense during cyclic sense	t_S	same as t_{HSON} / t_{HSONT}			-
HSx ON duration during Cyclic Sense	t_{HSON}	140	200	280	µs
HSx ON duration during Cyclic Sense - trimmed[32]	t_{HSONT}	180	200	220	µs

Note:
32. Trimming parameters are not available in Sleep mode.

Table 31. Dynamic Electrical Characteristics - Window Watchdog

Ratings	Symbol	Min	Typ	Max	Unit
Initial Non-window Watchdog Timeout	t_{IWDTO}	110	150	190	ms
Watchdog Timeout Accuracy - not trimmed	WD_{AC}	-35	-	35	%
Watchdog Timeout Accuracy - trimmed	WD_{ACT}	-5.0	-	5.0	%

Table 32. Dynamic Electrical Characteristics - High-side Drivers - HS

Ratings	Symbol	Min	Typ	Max	Unit
High-side Operating Frequency[33], Load Condition: $C_{LOAD} \leq 2.2$ nF; $R_{LOAD} \geq 500\ \Omega$	f_{HS}	-	-	50	kHz

Note:
33. Guaranteed by design.

Table 33. Dynamic Electrical Characteristics - Low-side Drivers - LS

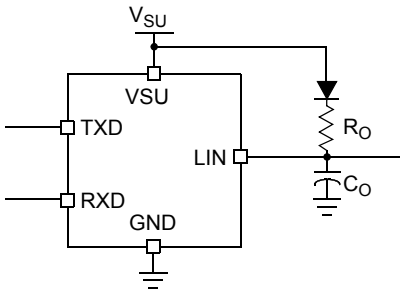
Ratings	Symbol	Min	Typ	Max	Unit
Low-side Operating Frequency[34], Load Condition: $C_{LOAD} \leq 2.2$ nF; $R_{LOAD} \geq 500\ \Omega$	f_{HS}	-	-	50	kHz

Note:
34. Guaranteed by design.

Table 34. Dynamic Electrical Characteristics - LIN Physical Layer Interface - LIN

Ratings	Symbol	Min	Typ	Max	Unit
Bus Wake-up Deglitcher (Sleep and Stop Mode)	t_{PROPWL}	60	80	100	µs
Fast Bit Rate (Programming Mode)	BR_{FAST}	-	-	100	kBit/s
Propagation Delay of Receiver, t_{REC_PD} = MAX (t_{REC_PDR}, t_{REC_PDF})[35]	t_{REC_PD}	-	-	6.0	µs
Symmetry of Receiver Propagation Delay, t_{REC_PDF} - t_{REC_PDR}	t_{REC_SYM}	-2.0	-	2.0	µs
LIN Driver - 20.0 kBit/s; Bus load conditions (C_{BUS}; R_{BUS}): 1.0 nF; 1.0 kΩ / 6,8 nF;660 Ω / 10 nF;500 Ω. Measurement thresholds: 50% of TXD signal to LIN signal threshold defined at each parameter. See Figure 5 and Figure 6.					
Duty Cycle 1: $TH_{REC(MAX)}$ = 0.744 x V_{SUP}, $TH_{DOM(MAX)}$ = 0.581 x V_{SUP}, 7.0 V ≤ V_{SUP} ≤ 18 V; t_{Bit} = 50 µs;, D1 = $t_{BUS\_REC(MIN)}$/(2 x t_{Bit})	D1	0.396	-	-	
Duty Cycle 2: $TH_{REC(MIN)}$ = 0.422 x V_{SUP}, $TH_{DOM(MIN)}$ = 0.284 x V_{SUP}, 7.6 V ≤ V_{SUP} ≤ 18 V; t_{BIT} = 50 µs, D2 = $t_{BUS\_REC(MAX)}$/(2 x t_{BIT})	D2	-	-	0.581	
LIN Driver - 10.0 kBit/s; Bus load conditions (C_{BUS}; R_{BUS}): 1.0 nF; 1.0 kΩ / 6,8 nF;660 Ω / 10 nF;500 Ω. Measurement thresholds: 50% of TXD signal to LIN signal threshold defined at each parameter. See Figure 5 and Figure 7.					
Duty Cycle 3: $TH_{REC(MAX)}$ = 0.778 x V_{SUP}, $TH_{DOM(MAX)}$ = 0.616 x V_{SUP}, 7.0 V ≤ V_{SUP} ≤ 18 V; t_{BIT} = 96 µs, D3 = $T_{BUS\_REC(MIN)}$/(2 x t_{BIT})	D3	0.417	-	-	
Duty Cycle 4: $TH_{REC(MIN)}$ = 0.389 x V_{SUP}, $TH_{DOM(MIN)}$ = 0.251 x V_{SUP}, 7.6 V ≤ V_{SUP} ≤ 18 V; t_{BIT} = 96 µs, D4 = $t_{BUS\_REC(MAX)}$/(2 x t_{BIT})	D4	-	-	0.590	
Transmitter Symmetry t_{TRAN_SYM} < MAX(t_{TRAN_SYM}60%, t_{TRAN_SYM}40%) tran_sym60% = ttran_pdf60% - ttran_pdr60% tran_sym40% = ttran_pdf40% - ttran_pdr40%	t_{TRAN_SYM}	-7.25	0	7.25	µs

Note:
35. V_{SUP} from 7.0 to 18 V, bus load R_{BUS} and C_{BUS} 1.0 nF / 1.0 kΩ, 6.8 nF / 660 Ω, 10 nF / 500 Ω. Measurement thresholds: 50% of TXD signal to LIN signal threshold defined at each parameter. See Figure 5 and Figure 8.
36. LIN Transmitter Timing, (V_{SUP} from 7.0 to 18 V) - See Figure 9



Note: Rn and Cn: 1.0kΩ/1.0nF, 660Ω/6.8

Figure 5. Test Circuit for Timing Measurements

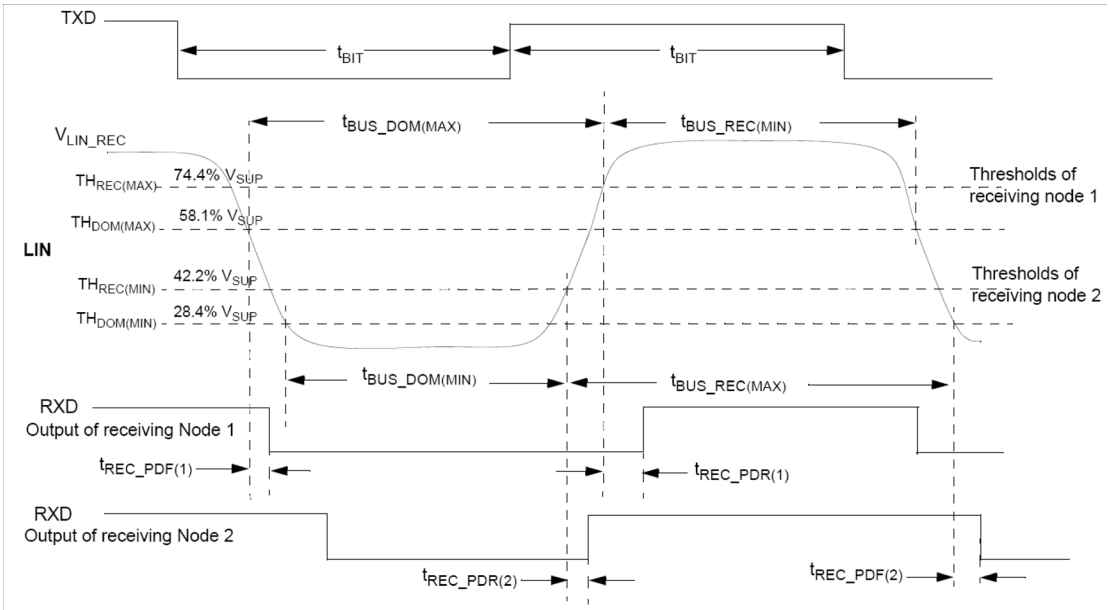


Figure 6. LIN Timing Measurements for Normal Baud Rate

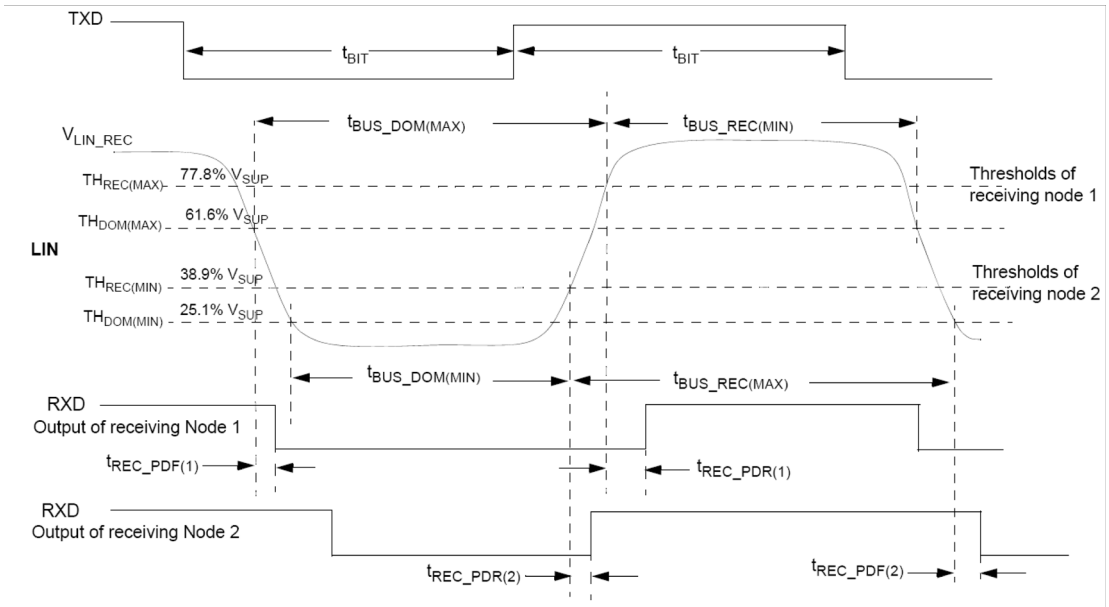


Figure 7. LIN Timing Measurements for Slow Baud Rate

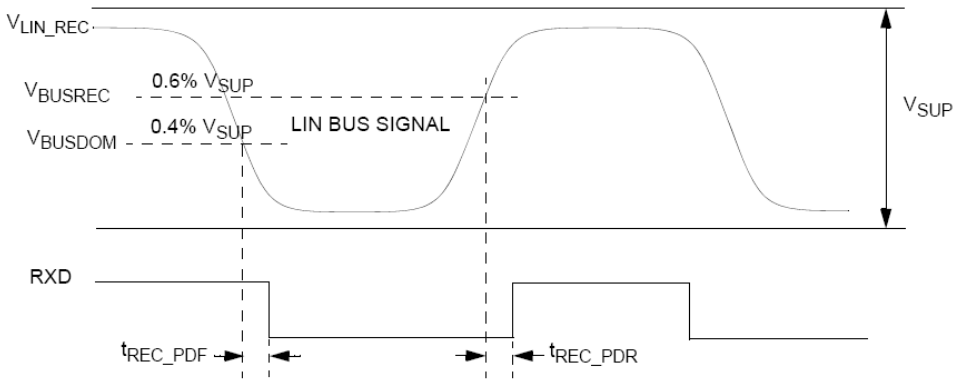


Figure 8. LIN Receiver Timing

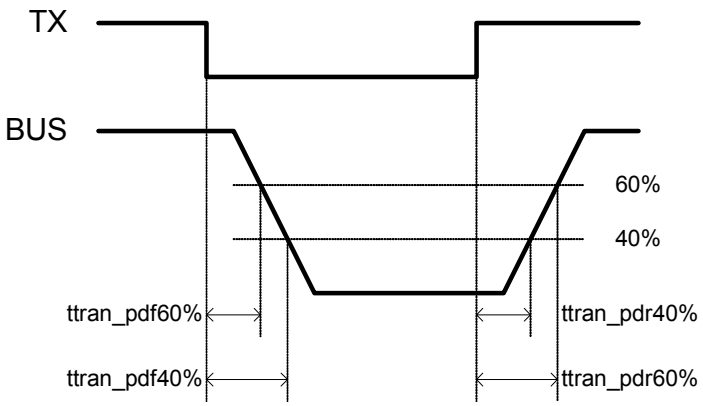


Figure 9. LIN Transmitter Timing

Table 35. Dynamic Electrical Characteristics - General Purpose I/O - PTB[0…2]

Ratings	Symbol	Min	Typ	Max	Unit
GPIO Digital Frequency[37]	f_{PTB}	-	-	10	MHz
Propagation Delay - Rising Edge[37], [38]	t_{PDR}	-	-	20	ns
Rise Time - Rising Edge[37]	t_{RISE}	-	-	17.5	ns
Propagation Delay - Falling Edge[37]	t_{PDF}	-	-	20	ns
Rise Time - Falling Edge[37]	t_{FALL}	-	-	17.5	ns

Note:
37. Guaranteed by design.
38. Load PTBx = 100 pF.

Table 36. Dynamic Electrical Characteristics - Analog Digital Converter - ADC

Ratings	Symbol	Min	Typ	Max	Unit
ADC Operating Frequency[39]	f_{ADC}	1.6	2.0	2.4	MHz
Conversion Time (from ACCR write to CC Flag)[39]	t_{CONV}		26		clk
Sample Frequency Channel 14 (Bandgap)[39]	f_{CH14}	-	-	2.5	kHz

Note:
39. Guaranteed by design.

3.6.2 Dynamic Electrical Characteristics MCU Die

3.6.2.1 NVM Timing

The time base for all NVM program or erase operations is derived from the bus block. A minimum bus frequency f_{NVMBUS} is required for performing program or erase operations. The NVM module do not has any means to monitor the frequency and does not prevent a program or erase operation at frequencies above or below the specified minimum. Attempting to program or erase the NVM modules at a lower frequency, a full program, or erase transition is not assured.

The Flash program and erase operations are timed using a clock derived from the bus clock using the FCLKDIV and register. The frequency of this clock must be set within the limits specified as f_{NVMOP}.

The minimum program and erase times shown in Table 37 are calculated for maximum f_{NVMOP} and maximum f_{BUS}. The maximum times are calculated for minimum f_{NVMOP} and a f_{BUS} of 2.0 MHz.

3.6.2.1.1 Single Word Programming

The programming time for single word programming is dependant on the bus frequency as a well as on the frequency f_{NVMOP}, and can be calculated according to the following formula.

$$t_{swpgm} = 9 \cdot \frac{1}{f_{NVMOP}} + 25 \cdot \frac{1}{f_{bus}}$$

3.6.2.1.2 Burst Programming

This applies only to the Flash, where up to 64 words in a row can be programmed consecutively, using burst programming by keeping the command pipeline filled. The time to program a consecutive word can be calculated as:

$$t_{bwpgm} = 4 \cdot \frac{1}{f_{NVMOP}} + 9 \cdot \frac{1}{f_{bus}}$$

The time to program a whole row is:

$$t_{brpgm} = t_{swpgm} + 63 \cdot t_{bwpgm}$$

Burst programming is more than 2 times faster than single word programming.

3.6.2.1.3 Sector Erase

NOTE

The sector erase cycle is divided into 16 individual erase pulses to achieve faster system response during the erase flow. The given erase time (t_{ERA}) specifies the time considering consecutive pulses.

Erasing a 512-byte Flash sector takes:

$$t_{era} \approx 4000 \cdot \frac{1}{f_{NVMOP}}$$

The setup time can be ignored for this operation.

3.6.2.1.4 Mass Erase

Erasing a NVM block takes:

$$t_{mass} \approx 20000 \text{ Þ } \frac{1}{f_{NVMOP}}$$

The setup time can be ignored for this operation.

3.6.2.1.5 Blank Check

The time it takes to perform a blank check on the Flash is dependant on the location of the first non-blank word, starting at relative address zero. It takes one bus cycle per word to verify plus a setup of the command.

$$t_{check} \text{ a location Þ } t_{cyc} + 10 \text{ Þ } t_{cyc}$$

Table 37. NVM Timing Characteristics

Rating	Symbol	Min	Typ	Max	Unit
Bus frequency for programming or erase operations	f_{NVMBUS}	1.0	-	-	MHz
Operating frequency	f_{NVMOP}	150	-	200	kHz
Single word programming time	t_{SWPGM}	46(40)	-	74.5(40)	µs
Flash burst programming consecutive word	t_{BWPGM}	20.4(40)	-	31(41)	µs
Flash burst programming time for 64 words(43)	t_{BRPGM}	1331.2(40)	-	2027.5(41)	µs
Sector erase time(41)	t_{ERA}	20(42)	-	26.7(41)	ms
Mass erase time	t_{MASS}	100(44)	-	133(41)	ms
Blank check time Flash per block	t_{CHECK}	11(43)	-	65546(44)	t_{CYC}

Note:
40. Minimum programming times are achieved under maximum NVM operating frequency f_{NVMOP} and maximum bus frequency f_{BUS}.
41. The sector erase cycle is divided into 16 individual erase pulses to achieve faster system response during the erase flow. The given erase time (t_{ERA}) specifies the time considering consecutive pulses.
42. Minimum erase times are achieved under maximum NVM operating frequency, f_{NVMOP}.
43. Minimum time, if first word in the array is not blank.
44. Maximum time to complete check on an erased block.