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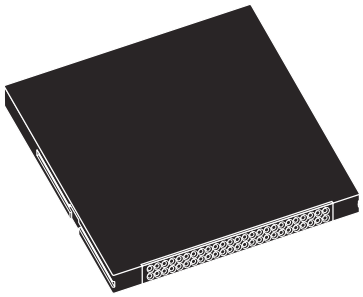
SMCxxxBF

32-Mbyte, 64-Mbyte, 128-Mbyte, 256-Mbyte, 512-Mbyte, 1-Gbyte, 2-Gbyte and 4-Gbyte 3.3/5 V supply CompactFlash™ card

Preliminary Data

Features

- Custom-designed, highly-integrated memory controller
  - Fully compliant with CompactFlash™ specification 3.0
  - Fully compatible with PCMCIA specification
  - PC Card ATA interface supported
  - True IDE mode compatible
  - Up to PIO mode 6 supported
  - Up to 4 multi-word DMA supported
  - Hardware RS-code ECC (4-byte/528-byte correction)
- Small form factor
  - 36.4 mm x 42.8 mm x 3.3 mm
- Low-power CMOS technology
- 3.3 V / 5.0 V power supply
- Power saving mode (with automatic wake-up)
- High reliability
  - MTBF > 3,000,000 hours
  - Data reliability: < 1 non-recoverable error per 10^{14} bits read
  - Endurance: > 2,000,000 erase/program cycles
  - Number of card insertions/removals: >10,000



CompactFlash™

- Hot swappable
- High performance
  - Up to 23.8 Mbyte/s transfer rate
  - Sustained write performance (host to card): 15 Mbyte/s
  - Sustained read performance (host to card: 22.5 Mbyte/s)
- Available densities (formatted)
  - 32 Mbytes to 4 Gbytes
- Operating system support
  - Standard software drivers operation

Table 1. Product list

Reference	Part number	Package form factor	Operating voltage range
SMCxxxBF	SMC032BF	CF type I	3.3 V + 5%, 5 V + 10%
	SMC064BF		
	SMC128BF		
	SMC256BF		
	SMC512BF		
	SMC01GBF		
	SMC02GBF		
	SMC04GBF		

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1 Description

The CompactFlash is a small form factor non-volatile memory card which provides high capacity data storage. Its aim is to capture, retain and transport data, audio and images, facilitating the transfer of all types of digital information between a large variety of digital systems.

The card operates in three basic modes:

- PCMCIA I/O mode
- PCMCIA memory mode
- True IDE mode

The CompactFlash also supports advanced timing modes. Advanced timing modes are PCMCIA style I/O modes that are 100 ns or faster, PCMCIA memory modes that are 100 ns or faster, true IDE PIO modes 5,6 and multi-word DMA modes 3,4.

It conforms to the PC card specification when operating in the PCMCIA I/O mode, and in the PCMCIA memory mode (personal computer memory card international association standard, JEIDA in Japan), and to the ATA specification when operating in true IDE mode. CompactFlash cards can be used with passive adapters in a PC-card type II or type III socket.

The card has an internal intelligent controller which manages interface protocols, data storage and retrieval as well as hardware RS-code error correction code (ECC), defect handling, diagnostics and clock control. Once the card has been configured by the host, it behaves as a standard ATA (IDE) disk drive. The hardware RS-code ECC allows to detect and correct 4 bytes per 528 bytes.

The specification has been realized and approved by the CompactFlash association (CFA). This non-proprietary specification enables users to develop CF products that function correctly and are compatible with future CF design.

The system highlights are shown in *Table 2*, *Table 3*, *Table 4*, *Table 5*, *Table 6* and *Table 7*.

Related documentation

- PCMCIA PC card standard, 1995
- PCMCIA PC card ATA specification, 1995
- AT attachment interface document, american national standards institute, X3.221-1994
- CF+ and CompactFlash specification revision 3.0.

Table 2. System performance

System performance		Max	Unit
Sleep to write		0.05	ms
Sleep to read		0.15	ms
Power-up to ready		480	ms
Data transfer rate (burst)		23.8 (162X)(1)	Mbyte/s
Sustained read		22.5 (150X)(1)	Mbyte/s
Sustained write		15 (100X)(1)	Mbyte/s
Command to DRQ	Read	135	µs
	Write	50	

1. 162X, 130X and 85X, speed grade markings where 1X = 150 Kbytes/s. All values are measured for an ambient temperature of 25 °C. They refer to the 1-Gbyte CompactFlash card in PIO mode 6, cycle time 80 ns, File size = 20 Mbytes sequential; sector count = 256.

Table 3. Current consumption(1)

Current consumption (typ)	3.3 V	5 V	Unit
Read	23	30	mA
Write	40	45	mA
Standby	1.0	2.0	mA
Sleep mode	1.0	2.0	mA

1. All values are typical at 25 °C and nominal supply voltage and refer to 1-Gbyte CompactFlash card, operating in PIO mode.

Table 4. Environmental specifications

Environmental specifications	Operating	Non-operating
Temperature	–40 to 85 °C	–50 to 100 °C
Humidity (non-condensing)	N/A	85% RH, at 85 °C
Salt water spray	N/A	3% NaCl at 35 °C(1)
Vibration (peak -to-peak)	N/A	30Gmax.
Shock	N/A	3,000Gmax.

1. MIL STD METHOD 1009.

Table 5. Physical dimensions

Physical dimensions		Unit
Width	42.8	mm
Height	36.4	mm
Thickness	3.3	mm
Weight (typ.)	10	g

2 Capacity specification

This section *Table 6* shows the specific capacity for the various CF models and the default number of heads, sector/tracks and cylinders.

Table 6. CF capacity specification

Part number	Capacity	Default_cylinders	Default_ heads	Default_sectors _track	Sectors_card	Total addressable capacity (byte)
SMC032BF	32 Mbytes	490	4	32	62,720	32,112,640
SMC064BF	64 Mbytes	490	8	32	125,440	64,225,280
SMC128BF	128 Mbytes	980	8	32	250,880	128,450,560
SMC256BF	256 Mbytes	980	16	32	501,760	256,901,120
SMC512BF	512 Mbytes	993	16	63	1,000,944	512,483,328
SMC01GBF	1 Gbyte	1,986	16	63	2,001,888	1,024,966,656
SMC02GBF	2 Gbytes	3,970	16	63	4,001,760	2,048,901,120
SMC04GBF	4 Gbytes	7,964	16	63	8,027,712	4,110,188,544

Table 7. System reliability and maintenance

MTBF (at 25 °C)	> 3,000,000 hours
Insertions/removals	> 10,000
Preventive maintenance	None
Data reliability	< 1 non-recoverable error per 10^{14} bits read
Endurance	0 +70 °C > 2,000,000 erase/program cycles(1)
	-40 +85 °C > 600,000 erase/program cycles(1)

1. Dependent on final system qualification data.

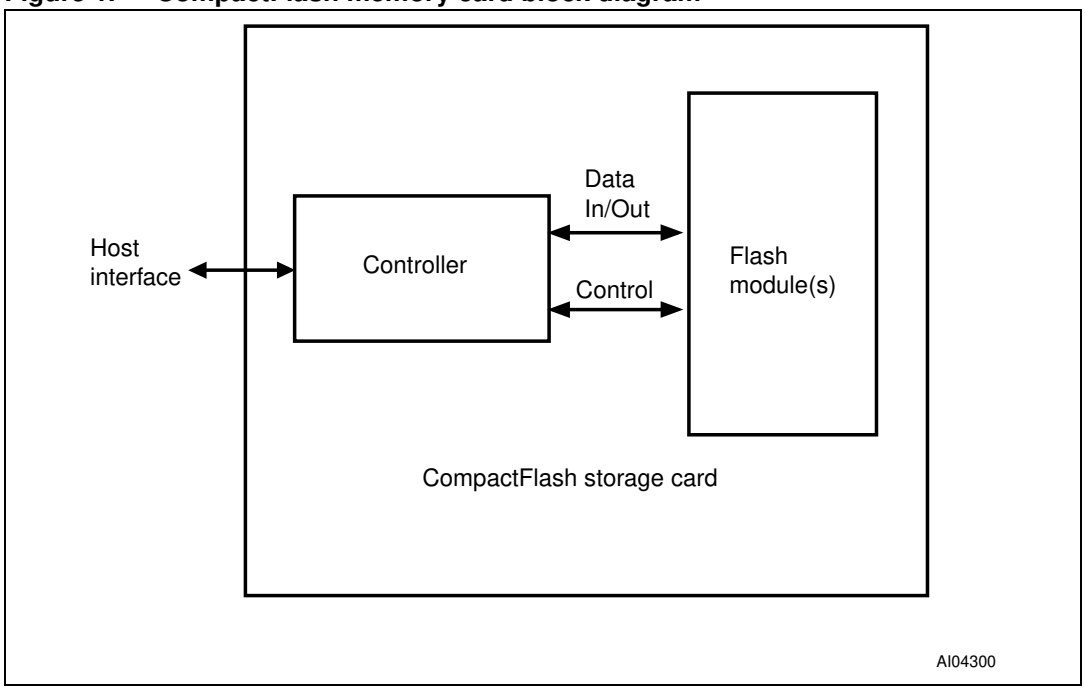
3 Card physical

3.1 Physical description

The CompactFlash memory card contains a single chip controller and flash memory module(s). The controller interfaces with a host system allowing data to be written to and read from the flash memory module(s). *Figure 1* shows the block diagram of the CompactFlash memory card.

The card is offered in a type I package with a 50-pin connector consisting of two rows of 25 female contacts on 50 mil (1.27 mm) centers. *Figure 10* shows type I card dimensions.

Figure 1. CompactFlash memory card block diagram



4 Electrical interface

4.1 Electrical description

The CompactFlash memory card operates in three basic modes:

- PC card ATA using I/O mode
- PC card ATA using memory mode
- True IDE mode, which is compatible with most disk drives.

The signal/pin assignments are listed in *Table 8* Low active signals have a '–' prefix. Pin types are input, output or input/output.

The configuration of the card is controlled using the standard PCMCIA configuration registers starting at address 200h in the attribute memory space of the memory card.

Table 9 describes the I/O signals. Inputs are signals sourced from the host while outputs are signals sourced from the card. The signals are described for each of the three operating modes.

All outputs from the card are totem pole except the data bus signals that are bi-directional tri-state. Refer to the *Section 4.2: Electrical specification* for definitions of input and output type.

Table 8. Pin assignment and pin type

Pin Num	PC card memory mode			PC card I/O mode			True IDE mode		
	Signal name	Pin type	In, Out type	Signal name	Pin type	In, Out type	Signal name	Pin type	In, Out type
1	GND		Ground	GND		Ground	GND		Ground
2	D03	I/O	I1Z,OZ3	D03	I/O	I1Z,OZ3	D03	I/O	I1Z,OZ3
3	D04	I/O	I1Z,OZ3	D04	I/O	I1Z,OZ3	D04	I/O	I1Z,OZ3
4	D05	I/O	I1Z,OZ3	D05	I/O	I1Z,OZ3	D05	I/O	I1Z,OZ3
5	D06	I/O	I1Z,OZ3	D06	I/O	I1Z,OZ3	D06	I/O	I1Z,OZ3
6	D07	I/O	I1Z,OZ3	D07	I/O	I1Z,OZ3	D07	I/O	I1Z,OZ3
7	–CE1	I	I3U	–CE1	I	I3U	–CS0	I	I3Z
8	A10	I	I1Z	A10	I	I1Z	A10(2)	I	I1Z
9(1)	–OE	I	I3U	–OE	I	I3U	–ATASEL	I	I3U
10	A09	I	I1Z	A09	I	I1Z	A09(2)	I	I1Z
11	A08	I	I1Z	A08	I	I1Z	A08(2)	I	I1Z
12	A07	I	I1Z	A07	I	I1Z	A07(2)	I	I1Z
13	V_{CC}		Power	V_{CC}		Power	V_{CC}		Power
14	A06	I	I1Z	A06	I	I1Z	A06(2)	I	I1Z
15	A05	I	I1Z	A05	I	I1Z	A05(2)	I	I1Z
16	A04	I	I1Z	A04	I	I1Z	A04(2)	I	I1Z

Table 8. Pin assignment and pin type (continued)

Pin Num	PC card memory mode			PC card I/O mode			True IDE mode		
	Signal name	Pin type	In, Out type	Signal name	Pin type	In, Out type	Signal name	Pin type	In, Out type
17	A03	I	I1Z	A03	I	I1Z	A03(2)	I	I1Z
18	A02	I	I1Z	A02	I	I1Z	A02	I	I1Z
19	A01	I	I1Z	A01	I	I1Z	A01	I	I1Z
20	A00	I	I1Z	A00	I	I1Z	A00	I	I1Z
21	D00	I/O	I1Z,OZ3	D00	I/O	I1Z,OZ3	D00	I/O	I1Z,OZ3
22	D01	I/O	I1Z,OZ3	D01	I/O	I1Z,OZ3	D01	I/O	I1Z,OZ3
23	D02	I/O	I1Z,OZ3	D02	I/O	I1Z,OZ3	D02	I/O	I1Z,OZ3
24	WP	O	OT3	–IOIS16	O	OT3	–IOIS16	O	ON3
25	–CD2	O	Ground	–CD2	O	Ground	–CD2	O	Ground
26	–CD1	O	Ground	–CD1	O	Ground	–CD1	O	Ground
27	D11(3)	I/O	I1Z,OZ3	D11(3)	I/O	I1Z,OZ3	D11(3)	I/O	I1Z,OZ3
28	D12(3)	I/O	I1Z,OZ3	D12(3)	I/O	I1Z,OZ3	D12(3)	I/O	I1Z,OZ3
29	D13(3)	I/O	I1Z,OZ3	D13(3)	I/O	I1Z,OZ3	D13(3)	I/O	I1Z,OZ3
30	D14(3)	I/O	I1Z,OZ3	D14(3)	I/O	I1Z,OZ3	D14(3)	I/O	I1Z,OZ3
31	D15(3)	I/O	I1Z,OZ3	D15(3)	I/O	I1Z,OZ3	D15(3)	I/O	I1Z,OZ3
32	–CE2(3)	I	I3U	–CE2(3)	I	I3U	–CS1(3)	I	I3Z
33	–VS1	O	Ground	–VS1	O	Ground	–VS1	O	Ground
34	–IORD	I	I3U	–IORD	I	I3U	–IORD	I	I3Z
35	–IOWR	I	I3U	–IOWR	I	I3U	–IOWR	I	I3Z
36	–WE	I	I3U	–WE	I	I3U	–WE(4)	I	I3U
37	READY	O	OT1	-IREQ	O	OT1	INTRQ	O	OZ1
38	V_{CC}		Power	V_{CC}		Power	V_{CC}		Power
39	–CSEL(5)(3)	I	I2Z	–CSEL(5)	I	I2Z	–CSEL(5)	I	I2U
40	–VS2	O	OPEN	–VS2	O	OPEN	–VS2	O	OPEN
41	RESET	I	I2Z	RESET	I	I2Z	-RESET	I	I2Z
42	–WAIT	O	OT1	–WAIT	O	OT1	IORDY	O	ON1
43	–INPACK	O	OT1	–INPACK	O	OT1	DMARQ	O	OZ1
44	–REG	I	I3U	–REG	I	I3U	-DMACK(6)	I	I3U
45	BVD2	I/O	I1U,OT1	–SPKR	I/O	I1U,OT1	–DASP	I/O	I1U,ON1
46	BVD1	I/O	I1U,OT1	–STSCHG	I/O	I1U,OT1	–PDIAG	I/O	I1U,ON1
47	D08(3)	I/O	I1Z,OZ3	D08(3)	I/O	I1Z,OZ3	D08(3)	I/O	I1Z,OZ3
48	D09(3)	I/O	I1Z,OZ3	D09(3)	I/O	I1Z,OZ3	D09(3)	I/O	I1Z,OZ3

Table 8. Pin assignment and pin type (continued)

Pin Num	PC card memory mode			PC card I/O mode			True IDE mode		
	Signal name	Pin type	In, Out type	Signal name	Pin type	In, Out type	Signal name	Pin type	In, Out type
49	D10(3)	I/O	I1Z,OZ3	D10(3)	I/O	I1Z,OZ3	D10(3)	I/O	I1Z,OZ3
50	GND		Ground	GND		Ground	GND		Ground

1. For True IDE mode, pin 9 is grounded.
2. The signal should be grounded by the host.
3. These signals are required only for 16-bit accesses and not required when installed in 8-bit systems. Devices should allow for 3-state signals not to consume current.
4. The signal should be tied to V_{CC} by the host.
5. The -CSEL signal is ignored by the card in PC card modes. However, because it is not pulled up on the card in these modes it should not be left floating by the host in PC card modes. In these modes, the pin is normally connected by the host to PC card A25 or grounded by the host.
6. When the device does not operate in DMA mode, the signal should be held High or tied to V_{CC} by the host. To ensure proper operation with older hosts when DMA mode is disabled, the card should ignore the –DMACK signal.

Table 9. Signal descriptions

Signal name	Dir.	Pin	Description
A10 to A0 (PC card memory mode)	I	8,10,11,12, 14,15,16,17, 18,19,20	Used (with –REG) to select: the I/O port address registers, the memory mapped port address registers, a byte in the card information structure and its configuration control and status registers.
A10 to A0 (PC card I/O mode)			Same as PC card memory mode
A2 to A0 (True IDE mode)			Only A2 to A0 are used to select the one of eight registers in the task file, the remaining lines should be grounded.
BVD1 (PC card memory mode)	I/O	46	The battery voltage status of the card, as no battery is required it is asserted High.
–STSCHG (PC card I/O mode)			Alerts the host to changes in the ready and write protect states. Its use is controlled by the card configuration and status register.
–PDIAG (True IDE mode)			The Pass Diagnostic signal in the master/slave handshake protocol.
BVD2 (PC card memory mode)	I/O	45	The battery voltage status of the card, as no battery is required it is asserted High.
–SPKR (PC card I/O mode)			The Binary Audio output from the card. It is asserted High as audio functions are not supported.
–DASP (True IDE mode)			This input/output is the Disk Active/Slave Present signal in the master/slave handshake protocol.

Table 9. Signal descriptions (continued)

Signal name	Dir.	Pin	Description
D15-D00 (PC card memory mode)	I/O	31,30,29,28, 27,49,48,47, 6,5,4,3,2, 23,22,21	Carry the data, commands and status information between the host and the controller. D00 is the LSB of the even byte of the word. D08 is the LSB of the odd byte of the word.
D15-D00 (PC card I/O mode)			Same as PC card memory mode.
D15-D00 (True IDE mode)			All task file operations occur in byte mode on D00 to D07 while all data transfers are 16 bits using D00 to D15.
GND (PC card memory mode)		1,50	Ground.
GND (PC card I/O mode)			Same for all modes.
GND (True IDE mode)			Same for all modes.
–INPACK (PC card memory mode)	O	43	Not used, should not be connected to the host.
–INPACK (PC card I/O mode)			The input acknowledge is asserted when the card is selected and responding to an I/O read cycle at the current address on the bus. It is used by the host to control the enable of any input data buffers between the card and CPU.
DMARQ (True IDE mode)			The DMARQ input signal is used to request a DMA data transfer between the host and the card. It is asserted to notify that the card is ready to transfer data to or from the host. For multi-word DMA transfers, the direction of data transfer is controlled by -IORD and -IOWR. DMARQ is used in conjunction with –DMACK to perform handshaking: the card waits until –DMACK has been asserted by the host to de-assert DMARQ, and re-assert it again if there is still data to be transferred (see *Section 10.10*). DMARQ is not driven when the card is not selected. If the host does not support DMA mode, DMARQ should be left unconnected.
–IORD (PC card memory mode)	I	34	Not used.
–IORD (PC card I/O mode)			I/O read strobe generated by the host. It gates I/O data onto the bus.
–IORD (True IDE mode)			Same as PC card I/O mode.

Table 9. Signal descriptions (continued)

Signal name	Dir.	Pin	Description
–CD1, –CD2 (PC card memory mode)	O	26,25	These are connected to ground on the card. They are used by the host to determine that the card is fully inserted into its socket.
–CD1, –CD2 (PC card I/O mode)			Same for all modes.
–CD1, –CD2 (True IDE mode)			Same for all modes.
–CE1, –CE2 (PC card memory mode)	I	7,32	Used to select the card and to indicate whether a byte or a word operation is being performed. –CE2 accesses the odd Byte, –CE1 accesses the even byte or the odd byte depending on A0 and –CE2. A multiplexing scheme based on A0, –CE1, –CE2 allows 8-bit hosts to access all data on D0 to D7.
–CE1, –CE2 (PC card I/O mode)			Same as PC card memory mode.
–CS0, –CS1 (True IDE mode)			–CS0 is the chip select for the task file registers, while –CS1 selects the alternate status register and the device control register. When –DMACK is asserted, -CS0 and –CS1 must be de-asserted and data width is 16 bits.
–CSEL (PC card memory mode)			Not used.
–CSEL (PC card I/O mode)	I	39	Not used.
–CSEL (True IDE mode)			This internally pulled up signal is used to configure the card as a master or slave. When grounded it is configured as a master, when open it is configured as a slave.
–IOWR (PC card memory mode)	I	35	Not used.
–IOWR (PC card I/O mode)			The I/O write strobe pulse is used to clock I/O data on the bus into the card controller registers. Clocking occurs on the rising edge.
–IOWR (True IDE mode)			Same as PC card I/O mode.
–OE (PC card memory mode)	I	9	This is an Output Enable strobe generated by the host interface. It reads data and the CIS and configuration registers.
–OE (PC card I/O mode)			Reads the CIS and configuration registers.
–ATASEL (True IDE mode)			This input signal must be driven Low to enable true IDE mode.

Table 9. Signal descriptions (continued)

Signal name	Dir.	Pin	Description
READY (PC card memory mode)	O	37	Indicates whether the card is busy (Low), or ready to accept a new data transfer operation (High). The host socket must provide a pull-up resistor. At power-up and reset, the Ready signal is held Low until the commands are completed. No access should be made during this time. The Ready signal is held High whenever the card has been powered up with Reset continuously disconnected or asserted.
–IREQ (PC card I/O mode)			Interrupt request. It is strobed Low to generate a pulse mode interrupt or held Low for a level mode interrupt.
INTRQ (True IDE mode)			Active High interrupt request to the host.
–REG (PC card memory mode)	I	44	Used to distinguish between common memory and register (attribute) memory accesses. High for common memory, Low for attribute memory.
–REG (PC card I/O mode)			Must be Low during I/O cycles when the I/O address is on the bus.
–DMACK (True IDE mode)			The –DMACK input signal is used to acknowledge DMA transfers. It is asserted by the host in response to DMARQ to initiate the transfer. When DMA mode is disabled, the card should ignore the -DMACK signal. If the host does not support DMA mode, but only True IDE mode, this signal should be driven High or tied to V_{CC} by the host.
RESET (PC card memory mode)	I	41	Resets the card (active High). The card is reset at power-up only if this pin is left High or unconnected.
RESET (PC card I/O mode)			Same as PC card memory mode.
–RESET (True IDE mode)			Hardware reset from the host (active Low).
V_{CC} (PC card memory mode)		13,38	+5 V, +3.3 V power.
V_{CC} (PC card I/O mode)			Same for all modes.
V_{CC} (True IDE mode)			Same for all modes.
–VS1, –VS2 (PC card memory mode)	O	33,40	Voltage sense signals.–VS1 is grounded so that the CIS can be read at 3.3 volts and –VS2 is reserved by PCMCIA for a secondary voltage.
–VS1, –VS2 (PC card I/O mode)			Same for all modes.
–VS1, –VS2 (True IDE mode)			Same for all modes.

Table 9. Signal descriptions (continued)

Signal name	Dir.	Pin	Description
–WAIT (PC card memory mode)	O	42	Numonyx CF does not assert the WAIT (IORDY) signal
–WAIT (PC card I/O mode)			
IORDY (True IDE mode)			
–WE (PC card memory mode)	I	36	Driven by the host to strobe memory write data to the registers.
–WE (PC card I/O mode)			Used for writing to the configuration registers.
–WE (True IDE mode)			Not used, should be connected to V_{CC} by the host.
WP (PC card memory mode)	O	24	No write protect switch available. It is held Low after the completion of the reset initialization sequence.
–IOIS16 (PC card I/O mode)			Used for the 16-bit port (–IOIS16) function. Low indicates that a 16-bit or odd byte only operation can be performed at the addressed port.
–IOCS16 (True IDE mode)			Asserted Low when the card is expecting a word data transfer cycle.

4.2 Electrical specification

Table 10 defines the DC characteristics for the CompactFlash memory card. Unless otherwise stated, conditions are:

- V_{CC} = 5 V ± 10%
- V_{CC} = 3.3 V ± 5%
- -40 °C to 85 °C.

Table 11 shows that the card operates correctly in both the voltage ranges and that the current requirements must not exceed the maximum limit shown.

Table 10. Absolute maximum conditions

Parameter	Symbol	Conditions
Input power	V_{CC}	– 0.3 V to 6.5 V
Voltage on any pin except V_{CC} with respect to GND	V	– 0.5 V to V_{CC} + 0.5 V

Table 11. Input power

Voltage	Maximum average RMS current	Measurement conditions
3.3 V ± 5%	85	– 40 + 85 °C
5 V ± 10%	100	– 40 + 85 °C

4.3 Current measurement

The current is measured by connecting an amp meter in series with the V_{CC} supply. The meter should be set to the 2A scale range, and have a fast current probe with an RC filter with a time constant of 0.1 ms. Current measurements are taken while looping on a data transfer command with a sector count of 128. Current consumption values for both read and write commands are not to exceed the maximum average RMS current specified in *Table 11*. *Table 12* shows the input leakage current, *Table 13* the input characteristics, *Table 14* the output drive type and *Table 15* the output drive characteristics.

Table 12. Input leakage current(1)

Type	Parameter	Symbol	Conditions	Min	Typ	Max	Units
IxZ	Input leakage current	IL	$V_{IH} = V_{CC}$ V_{IL} = GND	– 1		1	µA
IxU	Pull up resistor	RPU1	V_{CC} = 5.0 V	50		500	kΩ
IxD	Pull down resistor	RPD1	V_{CC} = 5.0 V	50		500	kΩ

1. x refers to the characteristics described in *Table 13*. For example, I1U indicates a pull up resistor with a type 1 input characteristic.

Table 13. Input characteristics

Type	Parameter	Symbol	Min	Typ	Max	Min	Typ	Max	Units
			V_{CC} = 3.3 V			V_{CC} = 5.0 V			
1	Input voltage CMOS	V_{IH}	2.4			3.3			V
		V_{IL}			0.6			0.8	
2	Input voltage CMOS	V_{IH}	1.5			2.0			V
		V_{IL}			0.6			0.8	
3	Input voltage CMOS Schmitt Trigger	V_{TH}		1.8			2.8		V
		V_{TL}		1.0			2.0		

Table 14. Output drive type(1)

Type	Output type	Valid conditions
OTx	Totempole	I_{OH} & I_{OL}
OZx	Tri-state N-P channel	I_{OH} & I_{OL}
OPx	P-channel only	I_{OH} only
ONx	N-channel only	I_{OL} only

1. x refers to the characteristics described in *Table 15*. For example, OT3 refers to totem pole output with a type 3 output drive characteristic.

Table 15. Output drive characteristics

Type	Parameter	Symbol	Conditions	Min	Typ	Max	Units
1	Output voltage	V_{OH}	I_{OH} = -4 mA	V_{CC} – 0.8 V			V
		V_{OL}	I_{OL} = 4 mA			Gnd + 0.4 V	
2	Output voltage	V_{OH}	I_{OH} = -4 mA	V_{CC} – 0.8 V			V
		V_{OL}	I_{OL} = 4 mA			Gnd + 0.4 V	
3	Output voltage	V_{OH}	I_{OH} = -4 mA	V_{CC} – 0.8 V			V
		V_{OL}	I_{OL} = 4 mA			Gnd + 0.4 V	
X	Tri-state leakage current	I_{OZ}	V_{OL} = Gnd	–10		10	µA
			V_{OH} = V_{CC}				

4.4 Additional requirements for CompactFlash advanced timing mode

When operating in a CompactFlash advanced timing mode, the following conditions must be respected:

- Only one CompactFlash card must be connected to the CompactFlash bus
- The load capacitance (cable included) for all signals must be lower than 40 pF
- The cable length must be lower than 0.15 m (6 inches). The cable length is measured from the card connector to the host controller. 0.46 m (18 inches) cables are not supported.

5 Command interface

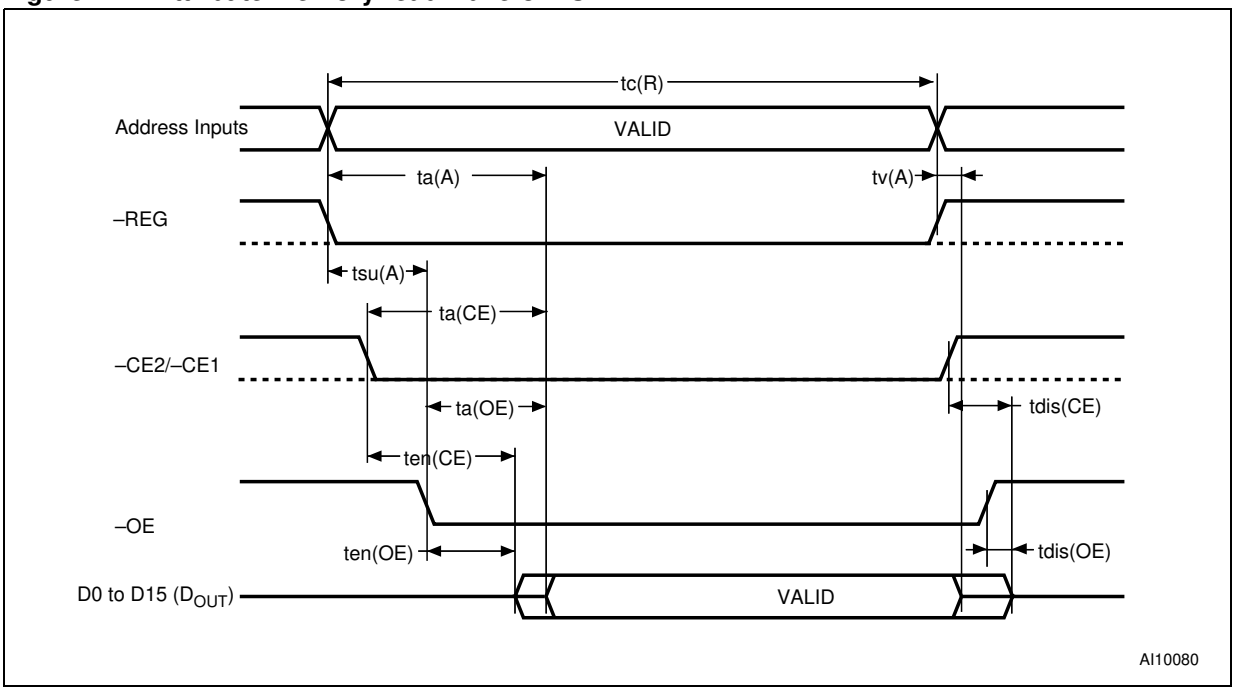
There are two types of bus cycles and timing sequences that occur in the PCMCIA type interface, direct mapped I/O transfer and memory access. Two types of bus cycles are also available in true IDE interface type: PIO transfer and multi-word DMA transfer.

Table 16, *Table 17*, *Table 18*, *Table 19*, *Table 20*, *Table 21* and *Table 22* show the read and write timing parameters. *Figure 2*, *Figure 3*, *Figure 4*, *Figure 5*, *Figure 6*, *Figure 7* and *Figure 8* show the read and write timing diagrams.

In order to set the card mode, the -OE (-ATASEL) signal must be set and kept stable before applying V_{CC} until the reset phase is completed. To place the card in memory mode or I/O mode, -OE(-ATASEL) must be driven High, while it must be driven Low to place the card in true IDE mode.

5.1 Attribute memory read and write

Figure 2. Attribute memory read waveforms

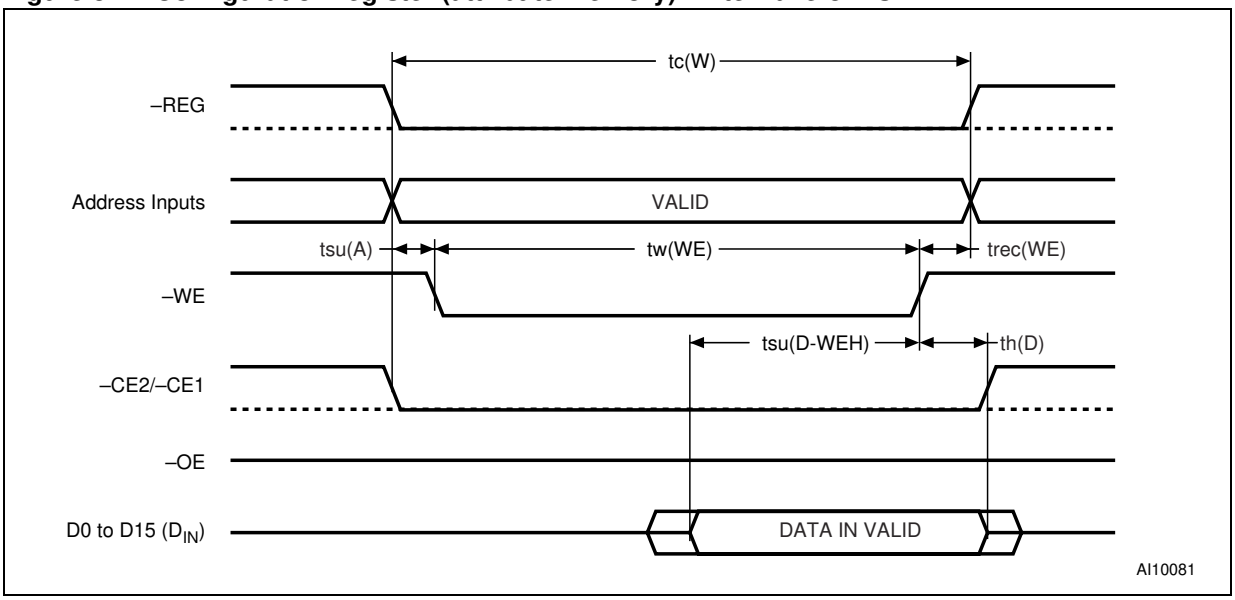


1. D_{OUT} signifies data provided by the CompactFlash memory card to the system. The -CE signal or both the -OE signal and the -WE signal must be de-asserted between consecutive cycle operations.

Table 16. Attribute memory read timing

Speed version			300 ns		
Symbol	**IEEE symbol**	**Parameter**	**Min**	**Max**	**Unit**
tc(R)	t_{AVAV}	Read cycle time	300		ns
ta(A)	t_{AVQV}	Address access time		300	ns
ta(CE)	t_{ELQV}	CE access time		300	ns
ta(OE)	t_{GLQV}	OE access time		150	ns
tdis(CE)	t_{EHQZ}	Output disable time from CE		100	ns
tdis(OE)	t_{GHQZ}	Output disable time from OE		100	ns
ten(CE)	t_{ELQNZ}	Output enable time from CE	5		ns
ten(OE)	t_{GLQNZ}	Output enable time from OE	5		ns
tv(A)	t_{AXQX}	Data valid from address change	0		ns
tsu(A)	t_{AVGL}	Address setup time	30		ns

Figure 3. Configuration register (attribute memory) write waveforms



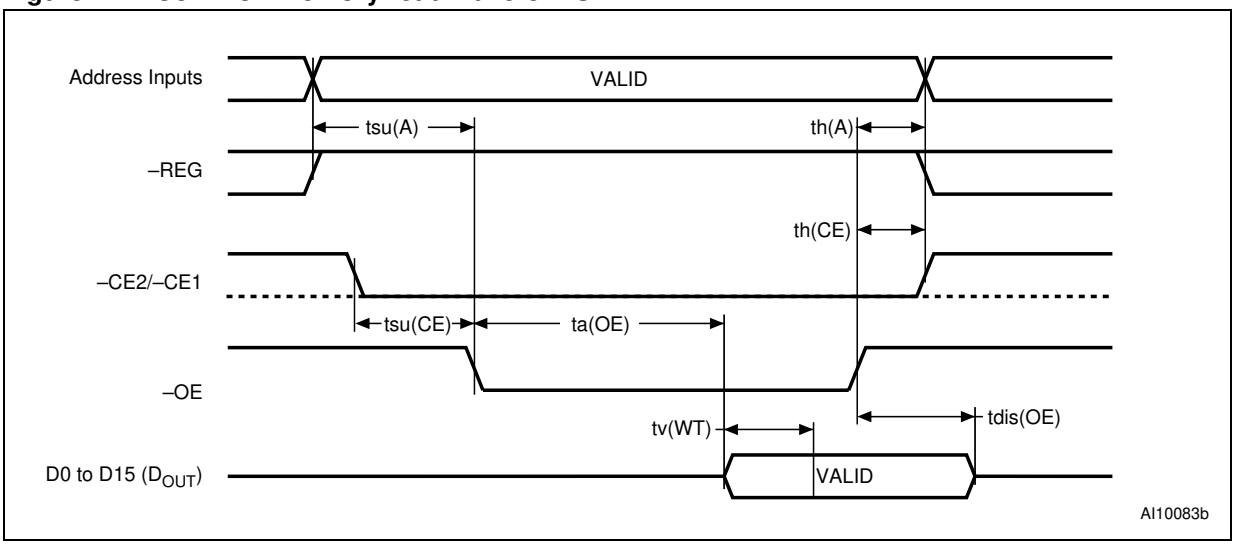
1. D_{IN} signifies data provided by the system to the CompactFlash card.

Table 17. Configuration register (attribute memory) write timing

Speed version			250 ns		
Symbol	**IEEE symbol**	**Parameter**	**Min**	**Max**	**Unit**
tc(W)	t_{AVAV}	Write cycle time	250		ns
tw(WE)	t_{WLWH}	Write pulse width	150		ns
tsu(A)	t_{AVWL}	Address setup time	30		ns
tsu(D-WEH)	t_{DVWH}	Data setup time from WE	80		ns
th(D)	t_{WMDX}	Data hold time	30		ns
trec(WE)	t_{WMAX}	Write recovery time	30		ns

5.2 Common memory read and write

Figure 4. Common memory read waveforms



1. D_{OUT} means data provided by the CompactFlash memory card to the system.

Table 18. Common memory read timing(1)

Cycle time mode			250 ns		120 ns		100 ns		80 ns		Unit
Symbol	IEEE Symbol	Parameter	Min	Max	Min	Max	Min	Max	Min	Max	
ta(OE)	t_{GLQV}	Output enable access time		125		60		50		45	ns
tdis(OE)	t_{GHQZ}	Output disable time from OE		100		60		50		45	ns
tsu(A)	t_{AVGL}	Address setup time	30		15		10		10		ns
th(A)	t_{GHAX}	Address hold time	20		15		15		10		ns
tsu(CE)	t_{ELGL}	CE setup time	0		0		0		0		ns
th(CE)	t_{GHEH}	CE hold time	20		15		15		10		ns

1. Numonyx CF does not assert the WAIT signal.