Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

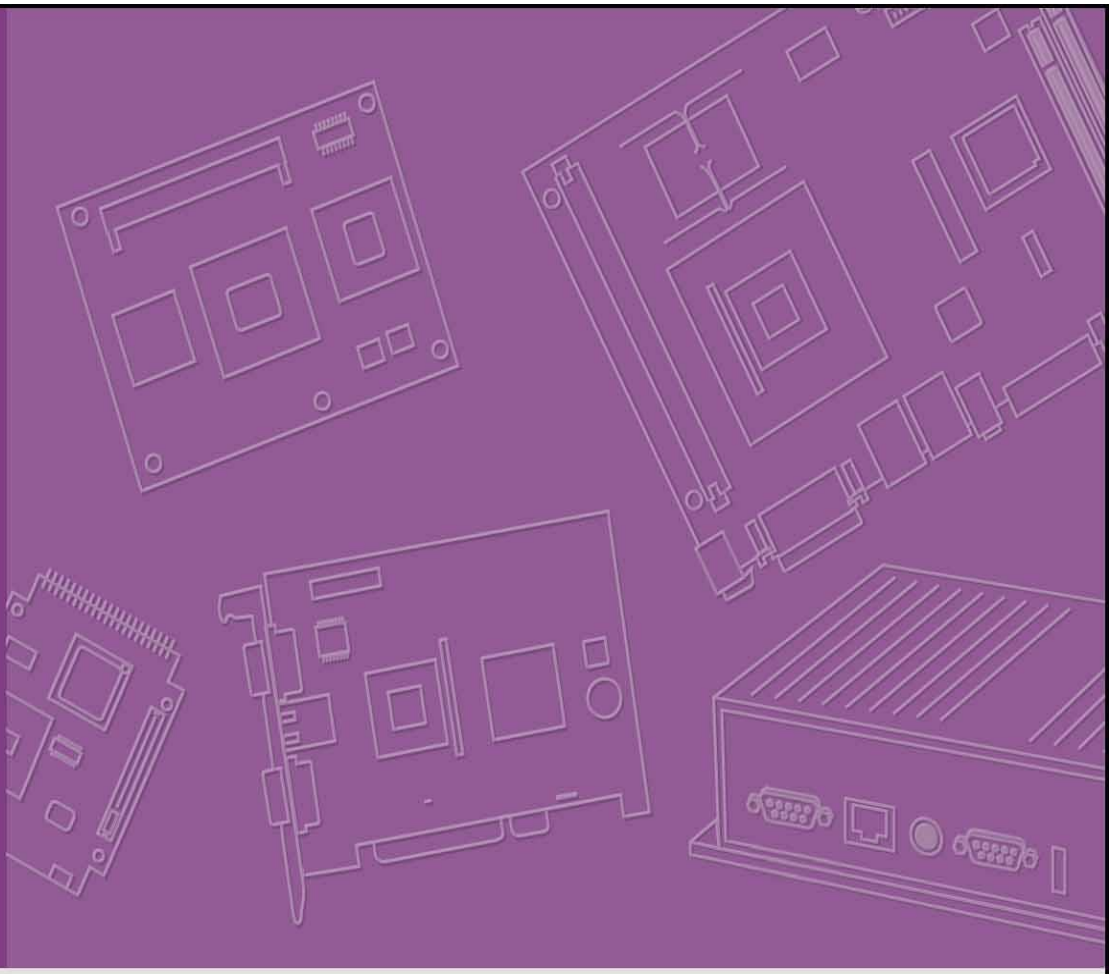
With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!


## Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

ADVANTECH EmbCore



CarrierBoard
Design Guide

# SOM-6868

R120 2016'10'27

## Contents

# 1. Introduction

## 1.1. About This Document

This design guide provides information for designing a custom system Carrier Board for COM Express Type 6 Module. It includes Signal Descriptions, Routing Guidelines and Trace Length Guidelines. The main purpose is designing Carrier Board for helping customers fast and easy using the module of Advantech to be designed.

## 1.2. Signal Table Terminology

Table 1 below describes the terminology used in this section for the Signal Description tables.

The "#" symbol at the end of the signal name indicates that the active or asserted state occurs when the signal is at a low voltage level. When "#" is not present, the signal is asserted when at a high voltage level.

The terms "Input" and "Output" and their abbreviations in Table 1 below refer to the Module's view, i.e. an input is an input for the Module and not for the Carrier-Board.

Table 1: Signal Table Terminology Descriptions

| *Term* | *Description* |
|---|---|
| I/O 3.3V | Bi-directional signal 3.3V tolerant |
| I/O 5V | Bi-directional signal 5V tolerant |
| I 3.3V | Input 3.3V tolerant |
| I 5V | Input 5V tolerant |
| I/O 3V3_SBY | Bi-directional 3.3V tolerant active during Suspend and running state. |
| O 3.3V | Output 3.3V signal level |
| O 5V | Output 5V signal level |
| OD | Open drain output |
| P | Power input/output |
| *_S0 | Signal active during running state. |
| PCIE | In compliance with PCI Express Base Specification |
| USB | In compliance with the Universal Serial Bus Specification |
| GbE | In compliance with IEEE 802.3ab 1000BASE-T Gigabit Ethernet |
| SATA | In compliance with Serial ATA specification |
| REF | Reference voltage output. May be sourced from a Module power plane. |
| PDS | Pull-down strap. A Module output pin that is either tied to GND or is not connected. Used to signal Module capabilities (pin-out type) to the Carrier Board. |

## 1.3. Terminology

Table 2: Conventions and Terminology

| *Terminology* | *Description* |
|---|---|
| AC ‘97 / HDA | Audio CODEC '97/High Definition Audio |
| ACPI | Advanced Configuration Power Interface – standard to implement power saving modes in PCAT systems |
| ADD2 | Advanced Digital Display, 2nd Generation |
| ADD2/MEC | Advanced Digital Display, 2nd Generation, Media Expansion Card |
| Basic Module | COM Express® 125mm x 95mm Module form factor. |
| BIOS | Basic Input Output System – firmware in PC-AT system that is used to initialize system components before handing control over to the operating system. |
| CAN | Controller-area network (CAN or CAN-bus) is a vehicle bus standard designed to allow microcontrollers to communicate with each other within a vehicle without a host computer. |
| Carrier Board | An application specific circuit board that accepts a COM Express® Module. |
| Compact Module | COM Express® 95mm x 95mm Module form factor |
| CRT | Cathode Ray Tube |
| DAC | Digital Analog Converter |
| DDC | Display Data Control – VESA (Video Electronics Standards Association) standard to allow identification of the capabilities of a VGA monitor |
| DDI | Digital Display Interface– containing DisplayPort, HDMI/DVI and SDVO |
| DNI | Do Not Install |
| DP | DisplayPort is a digital display interface standard put forth by the Video Electronics Standards Association (VESA). It defines a new license free, royalty free, digital audio/video interconnect, intended to be used primarily between a computer and its display monitor. |
| DP | DisplayPort is a digital display interface standard put forth by the Video Electronics Standards Association (VESA). It defines a new license free, royalty free, digital audio/video interconnect, intended to be used primarily between a computer and its display monitor. |
| DVI | Digital Visual Interface - a Digital Display Working Group (DDWG) standard that defines a standard video interface supporting both digital and analog video signals. The digital signals use TMDS. |

| *Terminology* | *Description* |
|---|---|
| EAPI | Embedded Application Programming Interface<br>Software interface for COM Express® specific industrial functions<br>• System information<br>• Watchdog timer<br>• I2C Bus<br>• Flat Panel brightness control<br>• User storage area<br>• GPIO |
| EDID | Extended Display Identification Data |
| EDP | Embedded DisplayPort (eDP) is a digital display interface standard produced by the Video Electronics Standards Association (VESA) for digital interconnect of Audio and Video. |
| EEPROM | Electrically Erasable Programmable Read-Only Memory |
| EFT | Electrical Fast Transient |
| EMI | Electromagnetic Interference |
| ESD | Electrostatic Discharge |
| Express Card | A PCMCIA standard built on the latest USB 2.0 and PCI Express buses. |
| Extended Module | COM Express® 155mm x 110mm Module form factor. |
| FR4 | A type of fiber-glass laminate commonly used for printed circuit boards. |
| Gb | Gigabit |
| GbE | Gigabit Ethernet |
| GPI | General Purpose Input |
| GPIO | General Purpose Input Output |
| GPO | General Purpose Output |
| HDA | Intel High Definition Audio (HD Audio) refers to the specification released by Intel in 2004 for delivering high definition audio that is capable of playing back more channels at higher quality than AC97. |
| HDMI | High Definition Multimedia Interface |
| I2C | Inter Integrated Circuit – 2 wire (clock and data) signaling scheme allowing communication between integrated circuits, primarily used to read and load register values. |
| DE | Integrated Device Electronics – parallel interface for hard disk drives – also known as PATA |
| Legacy Device | Relics from the PC-AT computer that are not in use in contemporary PC systems: primarily the ISA bus, UART-based serial ports, parallel printer ports, PS-2 keyboards, and mice.<br>Definitions vary as to what constitutes a legacy device. Some definitions |

| | |
|---|---|
| | include IDE as a legacy device. |
| *Terminology* | *Description* |
| LAN | Local Area Network |
| LPC | Low Pin-Count Interface: a low speed interface used for peripheral circuits such as Super I/O controllers, which typically combine legacy-device support into a single IC. |
| LS | Least Significant |
| LVDS | Low-Voltage Differential Signaling – widely used as a physical interface for TFT flat panels.<br>LVDS can be used for many high-speed signaling applications. In this document, it refers only to TFT flat-panel applications. |
| MEC | Media Expansion Card |
| Mini Module | COM Express® 84x55mm Module form factor |
| MS | Most Significant |
| NA | Not available |
| NC | Not connected |
| OBD-II | On-Board Diagnostics 2nd generation |
| OEM | Original Equipment Manufacturer |
| PATA | Parallel AT Attachment – parallel interface standard for hard-disk drives – also known as IDE,AT Attachment, and as ATA |
| PC-AT | "Personal Computer – Advanced Technology" – an IBM trademark term used to refer to Intel x86 based personal computers in the 1990s |
| PCB | Printed Circuit Board |
| PCI | Peripheral Component Interface |
| PCI Express (PCIe) | Peripheral Component Interface Express – next-generation high speed Serialized I/O bus |
| PCI Express Lane | One PCI Express Lane is a set of 4 signals that contains two differential lines for Transmitter and two differential lines for Receiver. Clocking information is embedded into the data stream. |
| PD | Pull Down |
| PEG | PCI Express Graphics |
| PHY | Ethernet controller physical layer device |
| Pin-out Type | A reference to one of seven COM Express® definitions for the signals that appear on the COM Express® Module connector pins. |
| PS2<br>PS2 Keyboard<br>PS2 Mouse | "Personal System 2" - an IBM trademark term used to refer to Intel x86 based personal computers in the 1990s. The term survives as a reference to the style of mouse and keyboard interface that were introduced with the PS2 system. |

| *Terminology* | *Description* |
|---|---|
| PU | Pull Up |
| ROM | Read Only Memory – a legacy term – often the device referred to as a ROM can actually be written to, in a special mode. Such writable ROMs are sometimes called Flash ROMs. BIOS is stored in ROM or Flash ROM. |
| RTC | Real Time Clock – battery backed circuit in PC-AT systems that keeps system time and date as well as certain system setup parameters |
| S0, S1, S2, S3, S4, S5 | Sleep States defined by the ACPI specificationS0 Full power, all devices powered<br>S1 Sleep State, all context maintained<br>S2 Sleep State, CPU and Cache context lost<br>S3 Suspend to RAM System context stored in RAM; RAM is in standby<br>S4 Suspend to Disk System context stored on disk<br>S5 Soft Off Main power rail off, only standby power rail present |
| SATA | Serial AT Attachment: serial-interface standard for hard disks |
| SDVO | Serialized Digital Video Out is a proprietary technology introduced by Intel® to add additional video signaling interfaces to a system. Being phased out |
| SMBus | System Management Bus |
| SO-DIMM | Small Outline Dual In-line Memory Module |
| SPI | Serial Peripheral Interface |
| TBD | To be determined |
| TMDS | Transition Minimized Differential Signaling - a digital signaling protocol between the graphics subsystem and display. TMDS is used for the DVI digital signals. DC coupled |
| TPM | Trusted Platform Module, chip to enhance the security features of a computer system. |
| UIM | User Identity Module |
| USB | Universal Serial Bus |
| VESA | Video Electronics Standards Association |
| WDT | Watch Dog Timer |

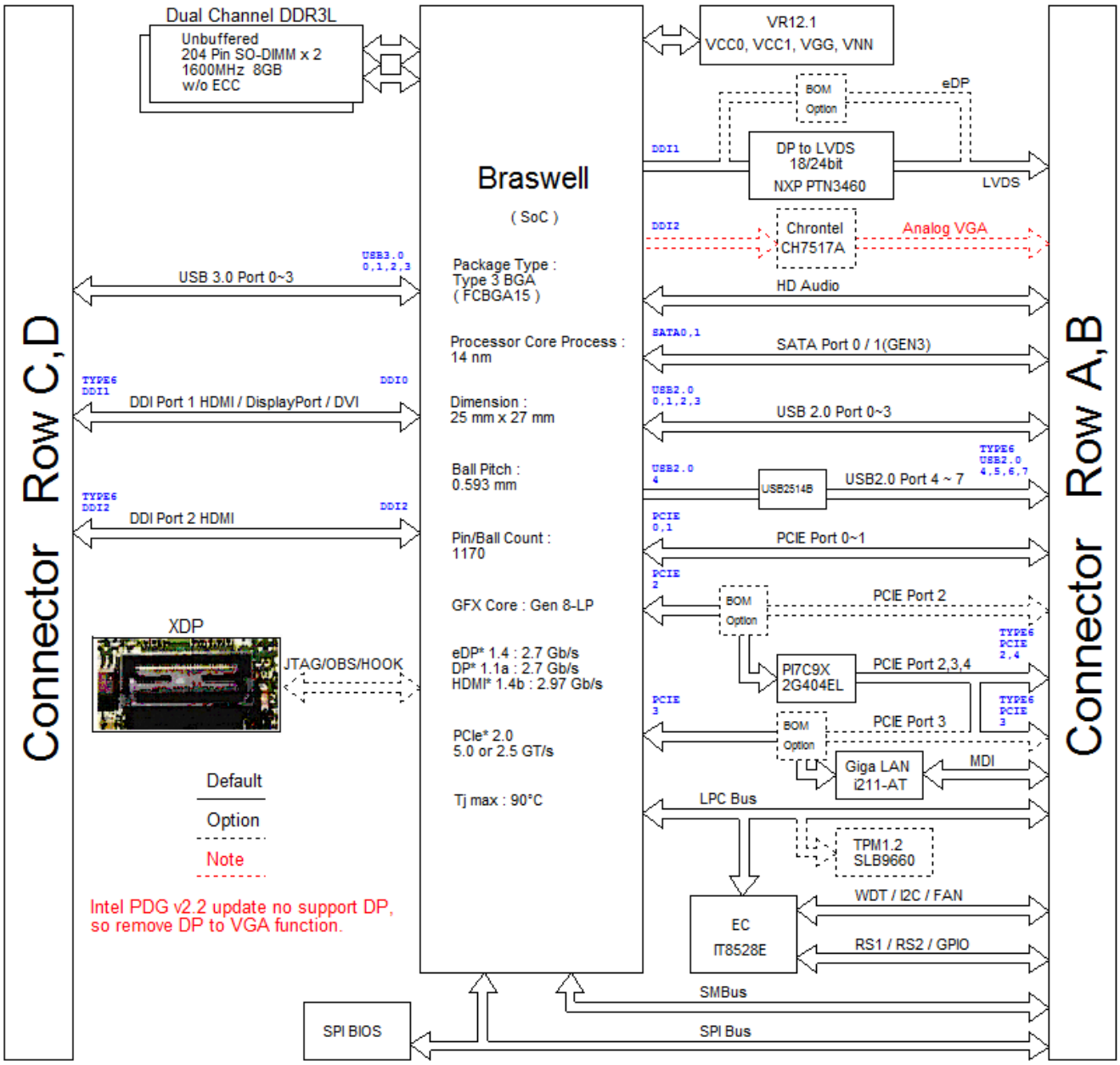
## 1.4. Reference Documents

| Document |
|---|
| COM Express Carrier Design Guide Rev. 2.0 |
| Intel EDS Document |
| Intel Layout Guide Document |
| ATX12V Power Supply Design Guide Rev. 2.01 |

## 1.5. Revision History

| Revision | Date | PCB Rev. | Changes |
|---|---|---|---|
| 1.00 | Jun 22, 2016 | A101-2 | |
| 1.20 | Oct. 27, 2016 | A101-2 | 1. Add SDIO in design guide, but SOM-6868 is not support.<br>2. Add eDP Max length |
| | | | |
| | | | |
| | | | |
| | | | |
| | | | |

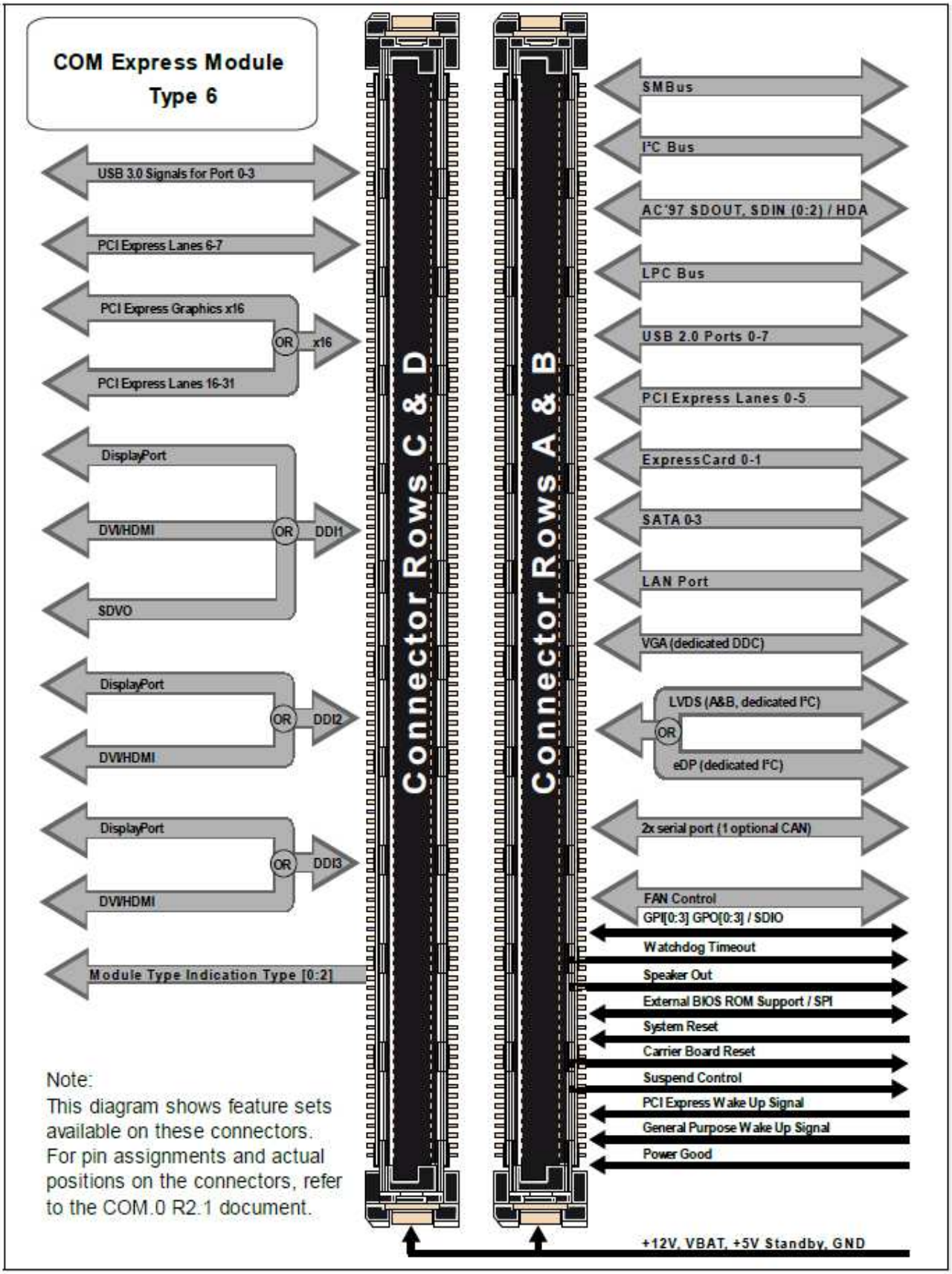
## 1.6. SOM-6868 Block Diagram



# 2. COM Express Type 6 Interfaces

## 2.1. COM Express Type 6 Connector Layout

Figure 1: COM Express Type6 Connector Layout



## 2.2. COM Express Type 6 Connector Pin-out

Table 3: COM Express Type6 Pin-out

**Connector Rows A and B**

| Pin# | Type 6 Description | Pin# | Type 6 Description |
|---|---|---|---|
| A1 | GND | B1 | GND |
| A2 | GBE0_MDI3- | B2 | GBE0_ACT# |
| A3 | GBE0_MDI3+ | B3 | LPC_FRAME# |
| A4 | GBE0_LINK100# | B4 | LPC_AD0 |
| A5 | GBE0_LINK1000# | B5 | LPC_AD1 |
| A6 | GBE0_MDI2- | B6 | LPC_AD2 |
| A7 | GBE0_MDI2+ | B7 | LPC_AD3 |
| A8 | GBE0_LINK# | B8 | LPC_DRQ0# |
| A9 | GBE0_MDI1- | B9 | LPC_DRQ1# |
| A10 | GBE0_MDI1+ | B10 | LPC_CLK |
| A11 | GND | B11 | GND |
| A12 | GBE0_MDI0- | B12 | PWRBTN# |
| A13 | GBE0_MDI0+ | B13 | SMB_CK |
| A14 | GBE0_CTREF | B14 | SMB_DAT |
| A15 | SUS_S3# | B15 | SMB_ALERT# |
| A16 | SATA0_TX+ | B16 | SATA1_TX+ |
| A17 | SATA0_TX | B17 | SATA1_TX |
| A18 | SUS_S4# | B18 | SUS_STAT# |
| A19 | SATA0_RX+ | B19 | SATA1_RX+ |
| A20 | SATA0_RX | B20 | SATA1_RX- |
| A21 | GND | B21 | GND |
| A22 | SATA2_TX+ | B22 | SATA3_TX+ |
| A23 | SATA2_TX | B23 | SATA3_TX- |
| A24 | SUS_S5# | B24 | PWR_OK |
| A25 | SATA2_RX+ | B25 | SATA3_RX+ |
| A26 | SATA2_RX | B26 | SATA3_RX- |
| A27 | BATLOW# | B27 | WDT |
| A28 | (S)ATA_ACT# | B28 | AC/HDA_SDIN2 |
| A29 | AC/HDA_SYNC | B29 | AC/HDA_SDIN1 |
| A30 | AC/HDA_RST# | B30 | AC/HDA_SDIN0 |
| A31 | GND | B31 | GND |
| A32 | AC/HDA_BITCLK | B32 | SPKR |

## Connector Rows A and B

| Pin# | Type 6 Description | Pin# | Type 6 Description |
|---|---|---|---|
| A33 | AC/HDA_SDOUT | B33 | I2C_CK |
| A34 | BIOS_DIS0# | B34 | I2C_DAT |
| A35 | THRMTRIP# | B35 | THRM# |
| A36 | USB6- | B36 | USB7- |
| A37 | USB6+ | B37 | USB7+ |
| A38 | USB_6_7_OC# | B38 | USB_4_5_OC# |
| A39 | USB4- | B39 | USB5- |
| A40 | USB4+ | B40 | USB5+ |
| A41 | GND | B41 | GND |
| A42 | USB2- | B42 | USB3- |
| A43 | USB2+ | B43 | USB3+ |
| A44 | USB_2_3_OC# | B44 | USB_0_1_OC# |
| A45 | USB0- | B45 | USB1- |
| A46 | USB0+ | B46 | USB1+ |
| A47 | VCC_RTC | B47 | EXCD1_PERST# |
| A48 | EXCD0_PERST# | B48 | EXCD1_CPPE# |
| A49 | EXCD0_CPPE# | B49 | SYS_RESET# |
| A50 | LPC_SERIRQ | B50 | CB_RESET# |
| A51 | GND | B51 | GND |
| A52 | PCIE_TX5+ | B52 | PCIE_RX5+ |
| A53 | PCIE_TX5- | B53 | PCIE_RX5- |
| A54 | GPI0 | B54 | GPO1 |
| A55 | PCIE_TX4+ | B55 | PCIE_RX4+ |
| A56 | PCIE_TX4- | B56 | PCIE_RX4- |
| A57 | GND | B57 | GPO2 |
| A58 | PCIE_TX3+ | B58 | PCIE_RX3+ |
| A59 | PCIE_TX3- | B59 | PCIE_RX3- |
| A60 | GND | B60 | GND |
| A61 | PCIE_TX2+ | B61 | PCIE_RX2+ |
| A62 | PCIE_TX2- | B62 | PCIE_RX2- |
| A63 | GPI1 | B63 | GPO3 |
| A64 | PCIE_TX1+ | B64 | PCIE_RX1+ |
| A65 | PCIE_TX1- | B65 | PCIE_RX1- |
| A66 | GND | B66 | WAKE0# |
| A67 | GPI2 | B67 | WAKE1# |

## Connector Rows A and B

| Pin# | Type 6 Description | Pin# | Type 6 Description |
|---|---|---|---|
| A68 | PCIE_TX0+ | B68 | PCIE_RX0+ |
| A69 | PCIE_TX0- | B69 | PCIE_RX0- |
| A70 | GND | B70 | GND |
| A71 | LVDS_A0+ | B71 | LVDS_B0+ |
| A72 | LVDS_A0- | B72 | LVDS_B0- |
| A73 | LVDS_A1+ | B73 | LVDS_B1+ |
| A74 | LVDS_A1- | B74 | LVDS_B1- |
| A75 | LVDS_A2+ | B75 | LVDS_B2+ |
| A76 | LVDS_A2- | B76 | LVDS_B2- |
| A77 | LVDS_VDD_EN | B77 | LVDS_B3+ |
| A78 | LVDS_A3+ | B78 | LVDS_B3- |
| A79 | LVDS_A3- | B79 | LVDS_BKLT_EN |
| A80 | GND | B80 | GND |
| A81 | LVDS_A_CK+ | B81 | LVDS_B_CK+ |
| A82 | LVDS_A_CK- | B82 | LVDS_B_CK- |
| A83 | LVDS_I2C_CK | B83 | LVDS_BKLT_CTRL |
| A84 | LVDS_I2C_DAT | B84 | VCC_5V_SBY |
| A85 | GPI3 | B85 | VCC_5V_SBY |
| A86 | RSVD | B86 | VCC_5V_SBY |
| A87 | eDP_HPD | B87 | VCC_5V_SBY |
| A88 | PCIE_CLK_REF+ | B88 | BIOS_DIS1# |
| A89 | PCIE_CLK_REF- | B89 | VGA_RED |
| A90 | GND | B90 | GND |
| A91 | SPI_POWER | B91 | VGA_GRN |
| A92 | SPI_MISO | B92 | VGA_BLU |
| A93 | GPO0 | B93 | VGA_HSYNC |
| A94 | SPI_CLK | B94 | VGA_VSYNC |
| A95 | SPI_MOSI | B95 | VGA_I2C_CK |
| A96 | TPM_PP | B96 | VGA_I2C_DAT |
| A97 | TYPE10# | B97 | SPI_CS# |
| A98 | SER0_TX | B98 | RSVD |
| A99 | SER0_RX | B99 | RSVD |
| A100 | GND | B100 | GND |
| A101 | SER1_TX | B101 | FAN_PWMOUT |
| A102 | SER1_RX | B102 | FAN_TACHIN |

## Connector Rows A and B

| Pin# | Type 6 Description | Pin# | Type 6 Description |
|---|---|---|---|
| A103 | LID# | B103 | SLEEP# |
| A104 | VCC_12V | B104 | VCC_12V |
| A105 | VCC_12V | B105 | VCC_12V |
| A106 | VCC_12V | B106 | VCC_12V |
| A107 | VCC_12V | B107 | VCC_12V |
| A108 | VCC_12V | B108 | VCC_12V |
| A109 | VCC_12V | B109 | VCC_12V |
| A110 | GND | B110 | GND |

Connector Rows C and D

| Pin# | Type 6 Description | Pin# | Type 6 Description |
|---|---|---|---|
| C1 | GND | D1 | GND |
| C2 | GND | D2 | GND |
| C3 | USB_SSRX0- | D3 | USB_SSTX0- |
| C4 | USB_SSRX0+ | D4 | USB_SSTX0+ |
| C5 | GND | D5 | GND |
| C6 | USB_SSRX1- | D6 | USB_SSTX1- |
| C7 | USB_SSRX1+ | D7 | USB_SSTX1+ |
| C8 | GND | D8 | GND |
| C9 | USB_SSRX2- | D9 | USB_SSTX2- |
| C10 | USB_SSRX2+ | D10 | USB_SSTX2+ |
| C11 | GND | D11 | GND |
| C12 | USB_SSRX3- | D12 | USB_SSTX3- |
| C13 | USB_SSRX3+ | D13 | USB_SSTX3+ |
| C14 | GND | D14 | GND |
| C15 | DDI1_PAIR6+ | D15 | DDI1_CTRLCLK_AUX+ |
| C16 | DDI1_PAIR6- | D16 | DDI1_CTRLCLK_AUX- |
| C17 | RSVD | D17 | RSVD |
| C18 | RSVD | D18 | RSVD |
| C19 | PCIE_RX6+ | D19 | PCIE_TX6+ |
| C20 | PCIE_RX6- | D20 | PCIE_TX6- |
| C21 | GND | D21 | GND |
| C22 | PCIE_RX7+ | D22 | PCIE_TX7+ |
| C23 | PCIE_RX7- | D23 | PCIE_TX7- |
| C24 | DDI1_HPD | D24 | RSVD |
| C25 | DDI1_PAIR4 + | D25 | RSVD |
| C26 | DDI1_PAIR4 - | D26 | DDI1_PAIR0+ |
| C27 | RSVD | D27 | DDI1_PAIR0- |
| C28 | RSVD | D28 | RSVD |
| C29 | DDI1_PAIR5+ | D29 | DDI1_PAIR1+ |
| C30 | DDI1_PAIR5- | D30 | DDI1_PAIR1- |
| C31 | GND | D31 | GND |
| C32 | DDI2_CTRLCLK_AUX+ | D32 | DDI1_PAIR2+ |
| C33 | DDI2_CTRLCLK_AUX- | D33 | DDI1_PAIR2- |
| C34 | DDI2_DDC_AUX_SEL | D34 | DDI1_DDC_AUX_SEL |
| C35 | RSVD | D35 | RSVD |
| C36 | DDI3_CTRLCLK_AUX+ | D36 | DDI1_PAIR3+ |

Connector Rows C and D

| Pin# | Type 6 Description | Pin# | Type 6 Description |
|---|---|---|---|
| C37 | DDI3_CTRLCLK_AUX- | D37 | DDI1_PAIR3- |
| C38 | DDI3_DDC_AUX_SEL | D38 | RSVD |
| C39 | DDI3_PAIR0+ | D39 | DDI2_PAIR0+ |
| C40 | DDI3_PAIR0- | D40 | DDI2_PAIR0- |
| C41 | GND | D41 | GND |
| C42 | DDI3_PAIR1+ | D42 | DDI2_PAIR1+ |
| C43 | DDI3_PAIR1- | D43 | DDI2_PAIR1- |
| C44 | DDI3_HPD | D44 | DDI2_HPD |
| C45 | RSVD | D45 | RSVD |
| C46 | DDI3_PAIR2+ | D46 | DDI2_PAIR2+ |
| C47 | DDI3_PAIR2- | D47 | DDI2_PAIR2- |
| C48 | RSVD | D48 | RSVD |
| C49 | DDI3_PAIR3+ | D49 | DDI2_PAIR3+ |
| C50 | DDI3_PAIR3- | D50 | DDI2_PAIR3- |
| C51 | GND | D51 | GND |
| C52 | PEG_RX0+ | D52 | PEG_TX0+ |
| C53 | PEG_RX0- | D53 | PEG_TX0- |
| C54 | TYPE0# | D54 | PEG_LANE_RV# |
| C55 | PEG_RX1+ | D55 | PEG_TX1+ |
| C56 | PEG_RX1- | D56 | PEG_TX1- |
| C57 | TYPE1# | D57 | TYPE2# |
| C58 | PEG_RX2+ | D58 | PEG_TX2+ |
| C59 | PEG_RX2- | D59 | PEG_TX2- |
| C60 | GND | D60 | GND |
| C61 | PEG_RX3+ | D61 | PEG_TX3+ |
| C62 | PEG_RX3- | D62 | PEG_TX3- |
| C63 | RSVD | D63 | RSVD |
| C64 | RSVD | D64 | RSVD |
| C65 | PEG_RX4+ | D65 | PEG_TX4+ |
| C66 | PEG_RX4- | D66 | PEG_TX4- |
| C67 | RSVD | D67 | GND |
| C68 | PEG_RX5+ | D68 | PEG_TX5+ |
| C69 | PEG_RX5- | D69 | PEG_TX5- |
| C70 | GND | D70 | GND |
| C71 | PEG_RX6+ | D71 | PEG_TX6+ |

Connector Rows C and D

| Pin# | Type 6 Description | Pin# | Type 6 Description |
|---|---|---|---|
| C72 | PEG_RX6- | D72 | PEG_TX6- |
| C73 | GND | D73 | GND |
| C74 | PEG_RX7+ | D74 | PEG_TX7+ |
| C75 | PEG_RX7- | D75 | PEG_TX7- |
| C76 | GND | D76 | GND |
| C77 | RSVD | D77 | RSVD |
| C78 | PEG_RX8+ | D78 | PEG_TX8+ |
| C79 | PEG_RX8- | D79 | PEG_TX8- |
| C80 | GND | D80 | GND |
| C81 | PEG_RX9+ | D81 | PEG_TX9+ |
| C82 | PEG_RX9- | D82 | PEG_TX9- |
| C83 | RSVD | D83 | RSVD |
| C84 | GND | D84 | GND |
| C85 | PEG_RX10+ | D85 | PEG_TX10+ |
| C86 | PEG_RX10- | D86 | PEG_TX10- |
| C87 | GND | D87 | GND |
| C88 | PEG_RX11+ | D88 | PEG_TX11+ |
| C89 | PEG_RX11- | D89 | PEG_TX11- |
| C90 | GND | D90 | GND |
| C91 | PEG_RX12+ | D91 | PEG_TX12+ |
| C92 | PEG_RX12- | D92 | PEG_TX12- |
| C93 | GND | D93 | GND |
| C94 | PEG_RX13+ | D94 | PEG_TX13+ |
| C95 | PEG_RX13- | D95 | PEG_TX13- |
| C96 | GND | D96 | GND |
| C97 | RSVD | D97 | RSVD |
| C98 | PEG_RX14+ | D98 | PEG_TX14+ |
| C99 | PEG_RX14- | D99 | PEG_TX14- |
| C100 | GND | D100 | GND |
| C101 | PEG_RX15+ | D101 | PEG_TX15+ |
| C102 | PEG_RX15- | D102 | PEG_TX15- |
| C103 | GND | D103 | GND |
| C104 | VCC_12V | D104 | VCC_12V |
| C105 | VCC_12V | D105 | VCC_12V |
| C106 | VCC_12V | D106 | VCC_12V |

Connector Rows C and D

| Pin# | Type 6 Description | Pin# | Type 6 Description |
|---|---|---|---|
| C107 | VCC_12V | D107 | VCC_12V |
| C108 | VCC_12V | D108 | VCC_12V |
| C109 | VCC_12V | D109 | VCC_12V |
| C110 | GND | D110 | GND |

## 2.3. PCI Express

### 2.3.1. COM Express A-B Connector and C-D Connector PCIe Groups

COM Express Type 6 Modules have two groups of PCIe lanes. There is a group of up to eight lanes; six are located on COM Express A-B connector and two on C-D connector that are intended for general purpose use, such as interfacing the COM Express Module to Carrier Board PCIe peripherals. A second group of PCIe lanes is defined on the COM Express C-D connector.

This group is intended primarily for the PCIe Graphics interfaces (also referred to as the PEG interface), and is typically 16 PCIe lanes wide. For some Modules, the PEG lanes may be used for general purpose PCIe lanes if the external graphics interface is not in use. This usage is Module and Module chipset dependent.

### 2.3.2. General Purpose PCIe Signal Definitions

The general purpose PCI Express interface of the COM Express Type 6 Module on the COM Express A-B connector consists of up to 6 lanes plus 2 lanes on connector C-D, each with a receive and transmit differential signal pair designated from PCIE_RX0 (+ and -) to PCIE_RX7 (+ and -) and correspondingly from PCIE_TX0 (+ and -) to PCIE_TX7 (+ and -). The 8 lanes may be grouped into various link widths as defined in the COM Express spec.

Table 4: General Purpose PCI Express Signal Descriptions

| Signal | Pin# | Description | I/O | Note |
|---|---|---|---|---|
| PCIE_RX0+<br>PCIE_RX0- | B68<br>B69 | PCIe channel 0. Receive Input differential pair.<br>Carrier Board:<br>Device - Connect AC Coupling cap 100nF near COME to PCIE0 x1 device PETp/n0.<br>Slot - Connect to PCIE0 x1 Conn pin A16, A17 PERp/n0.<br>N/C if not used. | I PCIE | |
| PCIE_TX0+<br>PCIE_TX0- | A68<br>A69 | PCIe channel 0. Transmit Output differential pair.<br>Module has integrated AC Coupling Capacitor.<br>Carrier Board:<br>Device - Connect to PCIE0 x1 device PERp/n0.<br>Slot - Connect to PCIE0 x1 Conn pin B14, B15 PETp/n0.<br>N/C if not used. | O PCIE | |

| Signal | Pin# | Description | I/O | Note |
|---|---|---|---|---|
| PCIE_RX1+<br>PCIE_RX1- | B64<br>B65 | PCIe channel 1. Receive Input differential pair.<br>Carrier Board:<br>Device - Connect AC Coupling cap 100nF near to PCIE1 x1 device PETp/n0.<br>Slot - Connect to PCIE1 x1 Conn pin A16, A17 PERp/n0.<br>N/C if not used. | I PCIE | |
| PCIE_TX1+<br>PCIE_TX1- | A64<br>A65 | PCIe channel 1. Transmit Output differential pair.<br>Module has integrated AC Coupling Capacitor.<br>Carrier Board:<br>Device - Connect to PCIE1 x1 device PERp/n0.<br>Slot - Connect to PCIE1 x1 Conn pin B14, B15 PETp/n0.<br>N/C if not used. | O PCIE | |
| PCIE_RX2+<br>PCIE_RX2- | B61<br>B62 | PCIe channel 2. Receive Input differential pair.<br>Carrier Board:<br>Device - Connect AC Coupling cap 100nF near COME to PCIE2 x1 device PETp/n0.<br>Slot - Connect to PCIE2 x1 Conn pin A16, A17 PERp/n0.<br>N/C if not used. | I PCIE | |
| PCIE_TX2+<br>PCIE_TX2- | A61<br>A62 | PCIe channel 2. Transmit Output differential pair.<br>Module has integrated AC Coupling Capacitor.<br>Carrier Board:<br>Device - Connect to PCIE2 x1 device PERp/n0.<br>Slot - Connect to PCIE2 x1 Conn pin B14, B15 PETp/n0.<br>N/C if not used. | O PCIE | |
| PCIE_RX3+<br>PCIE_RX3- | B58<br>B59 | PCIe channel 3. Receive Input differential pair.<br>Carrier Board:<br>Device - Connect AC Coupling cap 100nF near to PCIE3 x1 device PETp/n0.<br>Slot - Connect to PCIE3 x1 Conn pin A16, A17 PERp/n0.<br>N/C if not used. | I PCIE | |

| Signal | Pin# | Description | I/O | Note |
|---|---|---|---|---|
| PCIE_TX3+<br>PCIE_TX3- | A58<br>A59 | PCIe channel 3. Transmit Output differential pair.<br>Module has integrated AC Coupling Capacitor.<br>Carrier Board:<br>Device - Connect to PCIE3 x1 device PERp/n0.<br>Slot - Connect to PCIE3 x1 Conn pin B14, B15 PETp/n0.<br>N/C if not used. | O PCIE | |
| PCIE_RX4+<br>PCIE_RX4- | B55<br>B56 | PCIe channel 4. Receive Input differential pair.<br>Carrier Board:<br>Device - Connect AC Coupling cap 100nF near to PCIE4 x1 device PETp/n0.<br>Slot - Connect to PCIE4 x1 Conn pin A16, A17 PERp/n0.<br>N/C if not used. | I PCIE | |
| PCIE_TX4+<br>PCIE_TX4- | A55<br>A56 | PCIe channel 4. Transmit Output differential pair.<br>Module has integrated AC Coupling Capacitor.<br>Carrier Board:<br>Device - Connect to PCIE4 x1 device PERp/n0.<br>Slot - Connect to PCIE4 x1 Conn pin B14, B15 PETp/n0.<br>N/C if not used. | O PCIE | |
| PCIE_RX5+<br>PCIE_RX5- | B52<br>B53 | PCIe channel 5. Receive Input differential pair.<br>Carrier Board:<br>Device - Connect AC Coupling cap 100nF near to PCIE5 x1 device PETp/n0.<br>Slot - Connect to PCIE5 x1 Conn pin A16, A17 PERp/n0.<br>N/C if not used. | I PCIE | 1 |
| PCIE_TX5+<br>PCIE_TX5- | A52<br>A53 | PCIe channel 5. Transmit Output differential pair.<br>Module has integrated AC Coupling Capacitor.<br>Carrier Board:<br>Device - Connect to PCIE5 x1 device PERp/n0.<br>Slot - Connect to PCIE5 x1 Conn pin B14, B15 PETp/n0.<br>N/C if not used. | O PCIE | 1 |

| Signal | Pin# | Description | I/O | Note |
|---|---|---|---|---|
| PCIE_RX6+<br>PCIE_RX6- | C19<br>C20 | PCIe channel 6. Receive Input differential pair.<br>Carrier Board:<br>Device - Connect AC Coupling cap 100nF near to PCIE5 x1 device PETp/n0.<br>Slot - Connect to PCIE5 x1 Conn pin A16, A17 PERp/n0.<br>N/C if not used. | I PCIE | 1 |
| PCIE_TX6+<br>PCIE_TX6- | D19<br>D20 | PCIe channel 6. Transmit Output differential pair.<br>Module has integrated AC Coupling Capacitor.<br>Carrier Board:<br>Device - Connect to PCIE6 x1 device PERp/n0.<br>Slot - Connect to PCIE6 x1 Conn pin B14, B15 PETp/n0.<br>N/C if not used. | O PCIE | 1 |
| PCIE_RX7+<br>PCIE_RX7- | C22<br>C23 | PCIe channel 7. Receive Input differential pair.<br>Carrier Board:<br>Device - Connect AC Coupling cap 100nF near to PCIE6 x1 device PETp/n0.<br>Slot - Connect to PCIE6 x1 Conn pin A16, A17 PERp/n0.<br>N/C if not used. | I PCIE | 1 |
| PCIE_TX7+<br>PCIE_TX7- | D22<br>D23 | PCIe channel 7. Transmit Output differential pair.<br>Module has integrated AC Coupling Capacitor.<br>Carrier Board:<br>Device - Connect to PCIE7 x1 device PERp/n0.<br>Slot - Connect to PCIE7 x1 Conn pin B14, B15 PETp/n0.<br>N/C if not used. | O PCIE | 1 |
| PCIE_CLK_REF+<br>PCIE_CLK_REF- | A88<br>A89 | PCIe Reference Clock for all COM Express PCIe lanes, and for PEG lanes.<br>Carrier Board:<br>Connect 0Ω in series to<br>Device - PCIE device REFCLK+, REFCLK-.<br>Slot - PCIE Conn pin A13 REFCLK+, A14 REFCLK-.<br>*Connect to PCIE Clock Buffer input to provide PCIE clocks output for more than one PCIE devices or slots.<br>N/C if not used. | O PCIE | |