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SP2996B

2 Amp DDR Bus Termination Regulator

September 2010 Rev. 2.0.0

GENERAL DESCRIPTION

The SP2996B voltage regulator is designed to convert voltage supplies ranging from 1.6V to 6V into a desired output voltage which is adjusted by an external resistor divider.

The regulator is capable of sourcing or sinking up to 2A of Continuous current while regulating an output voltage to within 20mV. The SP2996B provides an excellent voltage source for active termination schemes of high speed transmission lines such as those seen in high speed memory buses and distributed backplane designs when used in conjunction with series termination resistors. The voltage output of the regulator can be used as a termination voltage for DDR SDRAM, and it meets the JEDEC SSTL-2 and SSTL-3 specifications. Current limits in both sourcing and sinking mode, plus on-chip thermal shutdown make the circuit tolerant of output fault conditions.

APPLICATIONS

- **DDR Memory Termination**
- **Active Bus Termination**
- **Supply Splitter**

FEATURES

- **Capable of Sourcing and sinking 2A Continuous Current**
- **Supports both DDR1 ($1.25V_{TT}$) and DDR2 ($0.9V_{TT}$) Requirements**
- **Low Output Voltage Offset, ± 20mV**
- **Thermal and Current Limit Protection**
- **Integrated Power MOSFETs**
- **Generates Termination for SSTL-2**
- **High Accuracy Output at Full Load**
- **Adjustable V_{OUT} by External Resistors**
- **Minimal External Components**
- **Available in 8-Pin NSOIC Package**

TYPICAL APPLICATION DIAGRAM

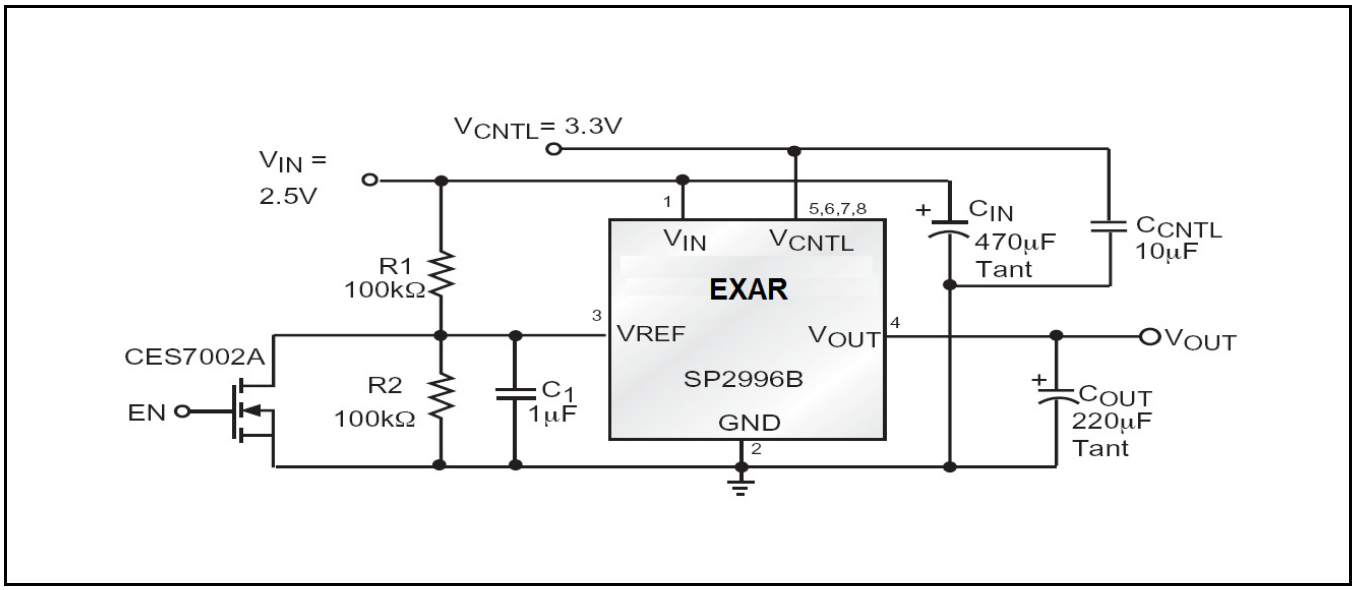


Fig. 1: SP2996B Application Diagram

ABSOLUTE MAXIMUM RATINGS

These are stress ratings only and functional operation of the device at these ratings or any other above those indicated in the operation sections of the specifications below is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

Supply Voltage ..... -0.3V to 7.0V
Junction Temperature Range ..... -40°C to +125°C
Storage Temperature ..... -65°C to 150°C

OPERATING RATINGS

Operating Temperature Range ..... -40°C to +85°C
Thermal Resistance θ_{JA} ..... 160°C/W
Thermal Resistance θ_{JC} ..... 40°C/W

ELECTRICAL SPECIFICATIONS

Specifications with standard type are for an Operating Ambient Temperature of T_A = 25°C only; limits applying over the full Operating Junction Temperature range are denoted by a "•". Minimum and Maximum limits are guaranteed through test, design, or statistical correlation. Typical values represent the most likely parametric norm at T_A = 25°C, and are provided for reference purposes only. Unless otherwise indicated, V_{IN} = 2.5V, V_{CNTL} = 3.3V, V_{REF} = 0.5xV_{IN}, C_{OUT} = 10µF (ceramic), T_A= 25°C.

Parameter	Min.	Typ.	Max.	Units		Conditions
Input Voltage Range (DDR 1/2) V_{IN}	1.6	2.5/1.8		V		(note 4) Keep $V_{CNTL} \geq V_{IN}$ on operation power on and power off sequences
Input Voltage Range (DDR 1/2) V_{CNTL}	3.0	3.3	3.6	V		(note 4) I_{OUT} = 0mA
Output Voltage V_{OUT}		V_{REF}		V		I_{OUT} = 0mA
Output Offset Voltage V_{OS}	-20		+20	mV		No load
Load Regulation (DDR 1/2) ΔV_{LOR}		10	25	mV		I_{OUT} = 0.1mA to +2A
		10	25	mV		I_{OUT} = 0.1mA to -2A
Quiescent Current I_Q		8	30	µA		V_{REF} < 0.2V, V_{OUT} = OFF
Operating Current of V_{CNTL}, I_{CNTL}		3	10	mA		No load
Bias Current of V_{REF}			1	µA		V_{REF} = 1.25V
Current Limit I_{IL}	2.2	3	4.5	A		(note 3)
Thermal Protection						
Thermal Shutdown Temperature T_{SD}	125	150		°C		(note 4) 3.3V ≤ V_{CNTL} ≤ 5V, guaranteed by design
Thermal Shutdown Hysteresis		30		°C		Guaranteed by design
Shutdown Specifications						
Shutdown Threshold $V_{TRIGGER}$	0.8			V		Output ON V_{REF} = 0V → 1.25V
			0.2			Output OFF V_{REF} = 1.25V → 0V

Note 1: V_{OS} offset is the voltage measurement defined as V_{OUT} subtracted from V_{REF}.
Note 2: Load regulation is measured at constant junction temperature, using pulse testing with a low ON time.
Note 3: Current limit is measured by pulsing a short time.
Note 4: In order to safely operate your system, V_{CNTL} must be > V_{IN}.

BLOCK DIAGRAM

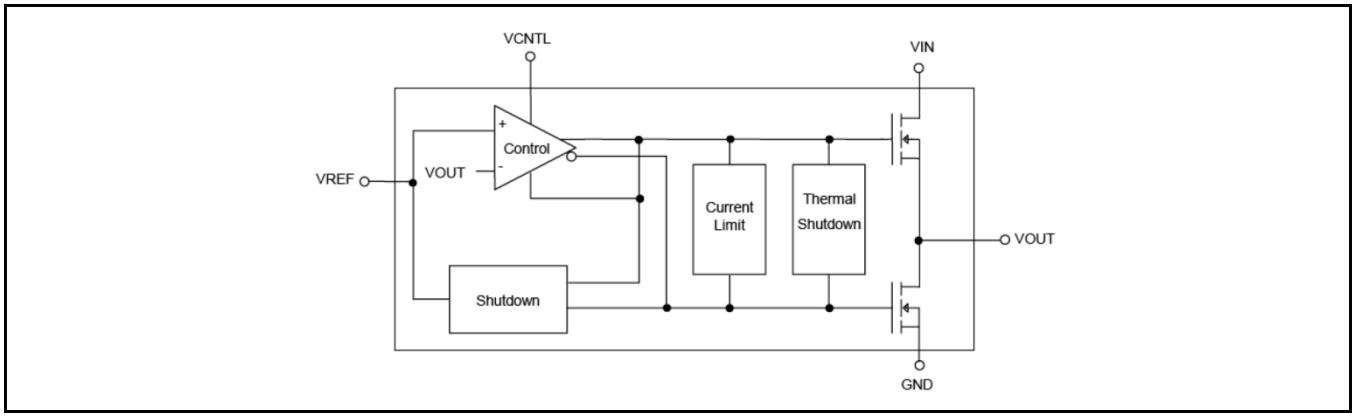


Fig. 2: SP2996B Block Diagram

PIN ASSIGNMENT

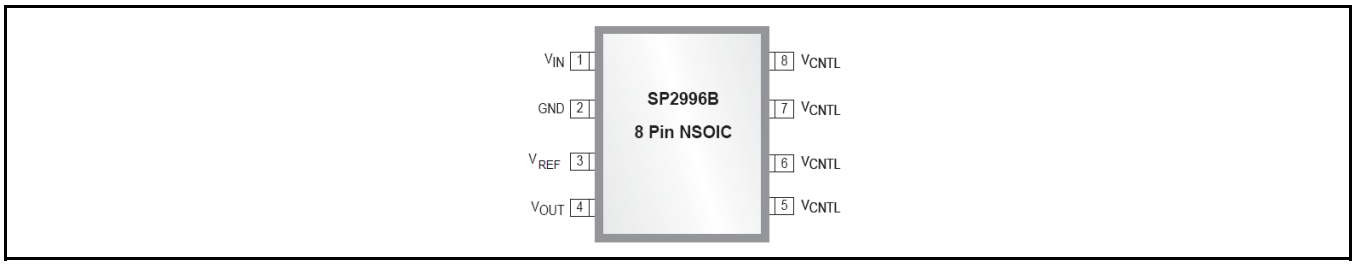


Fig. 3: SP2996B Pin Assignment

PIN DESCRIPTION

Name	Pin Number	Description
V_{IN}	1	Power Input Voltage
GND	2	Ground Signal
V_{REF}	3	Reference Input Voltage. This input can also be used as an enable signal. Refer to typical application circuit.
V_{OUT}	4	Output Voltage
V_{CNTL}	5	Voltage for the driver circuit and all analog blocks
V_{CNTL}	6	
V_{CNTL}	7	
V_{CNTL}	8	

ORDERING INFORMATION

Part Number	Temperature Range	Marking	Package	Packing Quantity	Note 1	Note 2
SP2996BEN-L	-40°C≤T_A≤+85°C	SP2996BE YYWWL X	SOIC-8	Bulk	Lead Free	
SP2996BEN-L/TR	-40°C≤T_A≤+85°C	SP2996BE YYWWL X	SOIC-8	2.5K/Tape & Reel	Lead Free	

"YY" = Year – "WW" = Work Week – "L" = Lead Free Indicator - "X" = Lot Number; when applicable.

TYPICAL PERFORMANCE CHARACTERISTICS

All data taken at V_{IN} = 2.5V, V_{CNTL} = 3.3V, V_{REF} = 0.5xV_{IN}, C_{OUT} = 10µF (ceramic), T_A= 25°C, unless otherwise specified - Schematic and BOM from Application Information section of this datasheet.

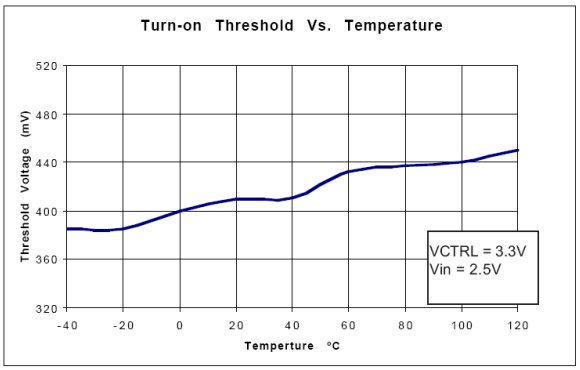


Fig. 4: Turn-on Threshold vs Temperature

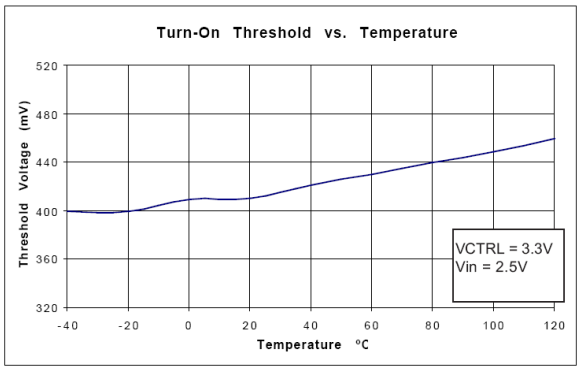


Fig. 5: Turn-on Threshold vs Temperature

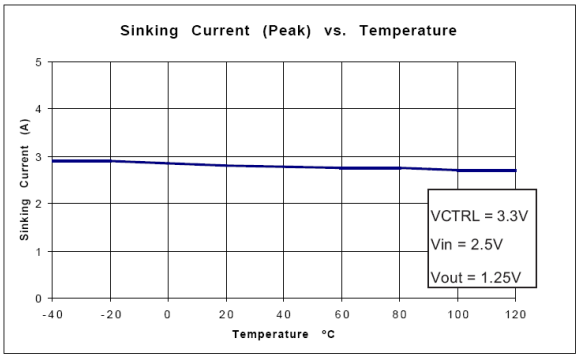


Fig. 6: Sinking Current (Peak) vs Temperature

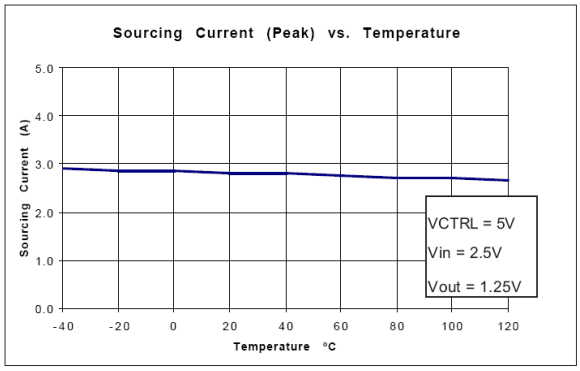


Fig. 7: Sourcing Current (Peak) vs Temperature

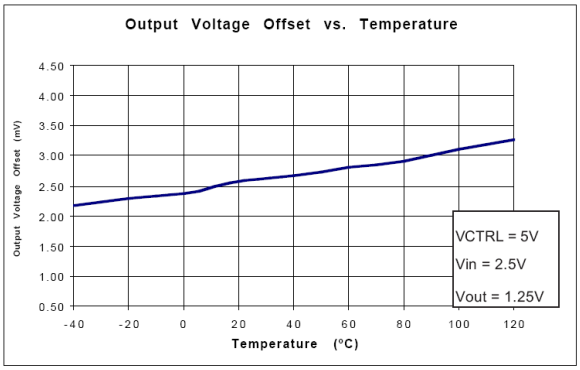


Fig. 8: Output Offset Voltage vs Temperature

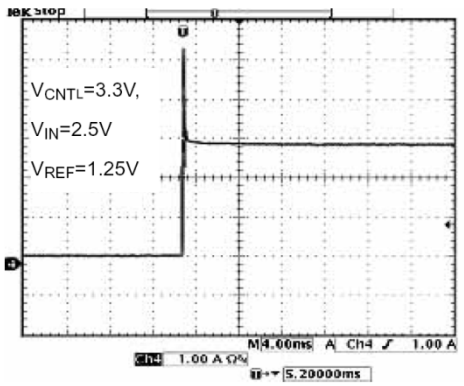


Fig. 9: Output Short Circuit (Sinking)

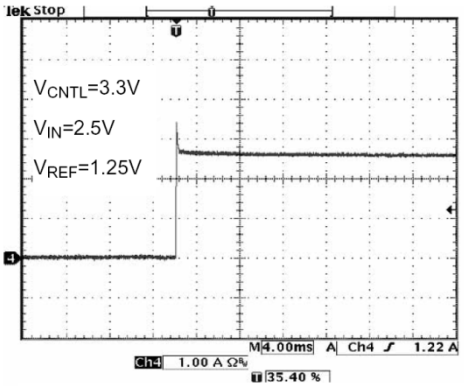


Fig. 10: Output Short Circuit (Sourcing)

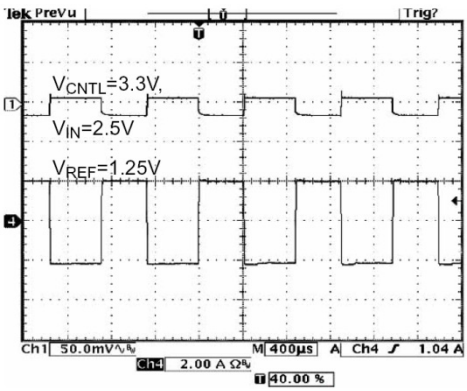


Fig. 11: Transient Response @ $1.25V_{TT}$/2A

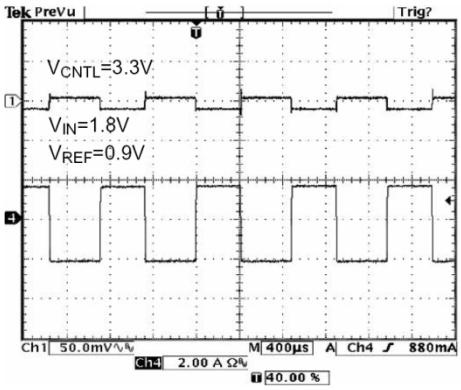


Fig. 12: Transient Response @ $1.25V_{TT}$/2A

APPLICATION INFORMATION

INTERNAL PARASITIC DIODE

Avoid forward-biasing the internal parasitic diode, V_{OUT} to V_{CNTL}, and V_{OUT} to V_{IN}. Positive voltage should not be applied to the output if V_{IN} and V_{CNTL} are not present.

CONSIDERATIONS FOR DESIGNING, RESISTANCE OF VOLTAGE DIVIDER

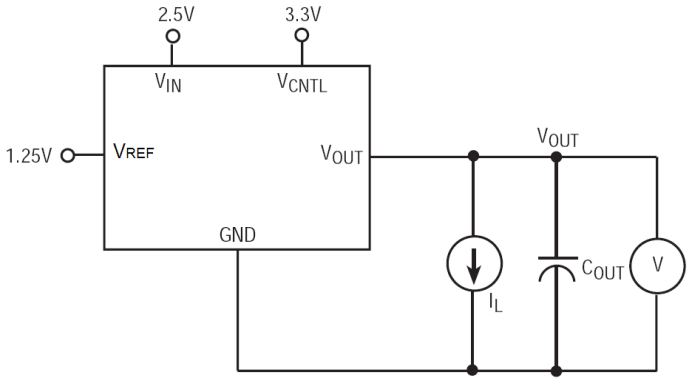
When the reference voltage is programmed below 0.2V the pulldown capability of the internal NMOS transistor is limited. It is recommened to place a filter capacitor from V_{REF} to ground in order to reduce sensitivity to noise and improve power up characteristics (soft start).

LAYOUT CONSIDERATIONS

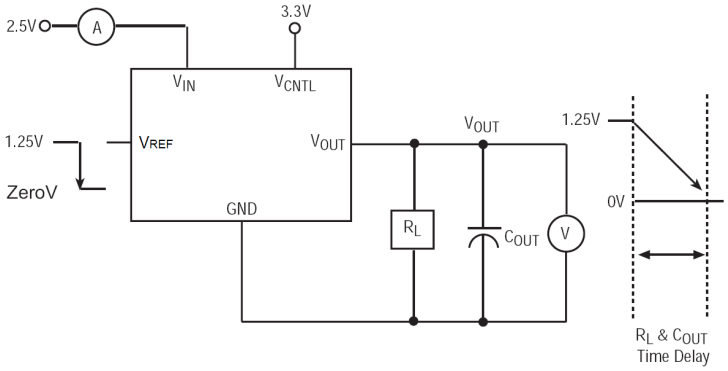
The SP2996B is offered in the NSOIC-8 package, resulting in attention needing to be paid to dissipating heat effectively when it operates in high current. In order to prevent maximum junction temperature from being exceeded, suitable copper area is necessary. The large copper area at VCNTL pins is available, and by taking advantage of this, much heat dissipation is attained. Use vias to direct heat into the bottom layer as the layout examples show below. All capacitors should be placed as close as possible to relative pins.

TEST CIRCUITS

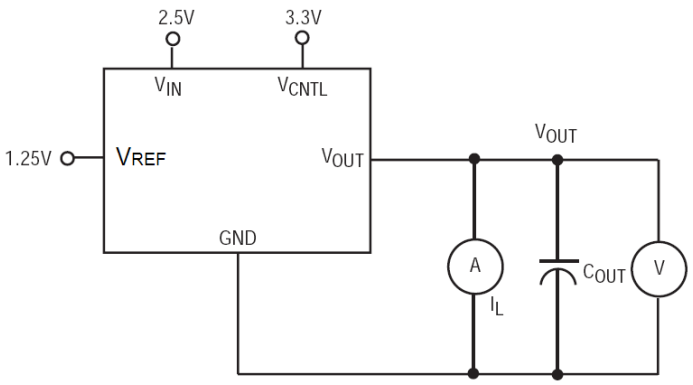
Testing Output Voltage Tolerance ΔV_{LOAD}



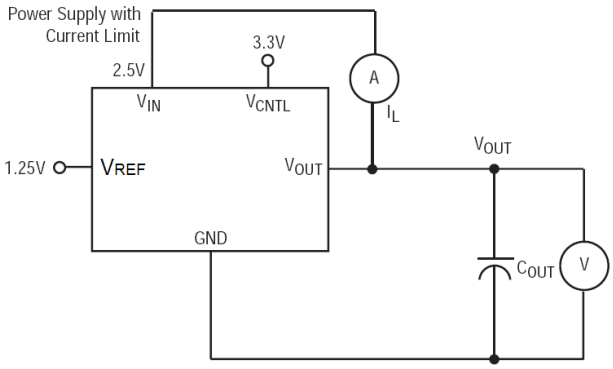
Testing Current in Shutdown Mode I_{SHDN}



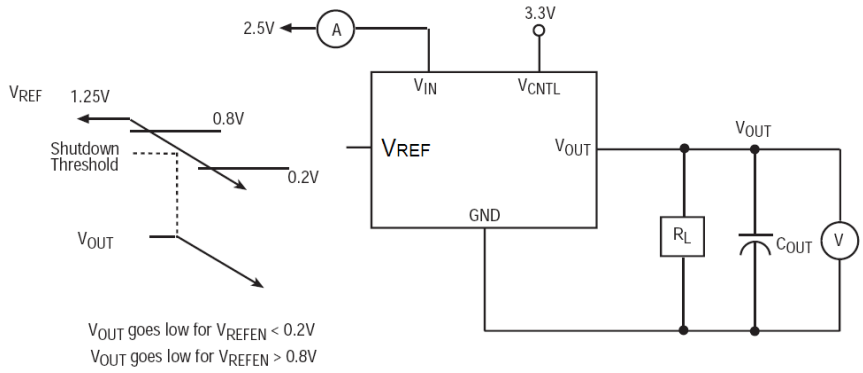
Testing Current Limit for High Side I_{LIMIT}



Testing Current Limit for Low Side I_{Limit}

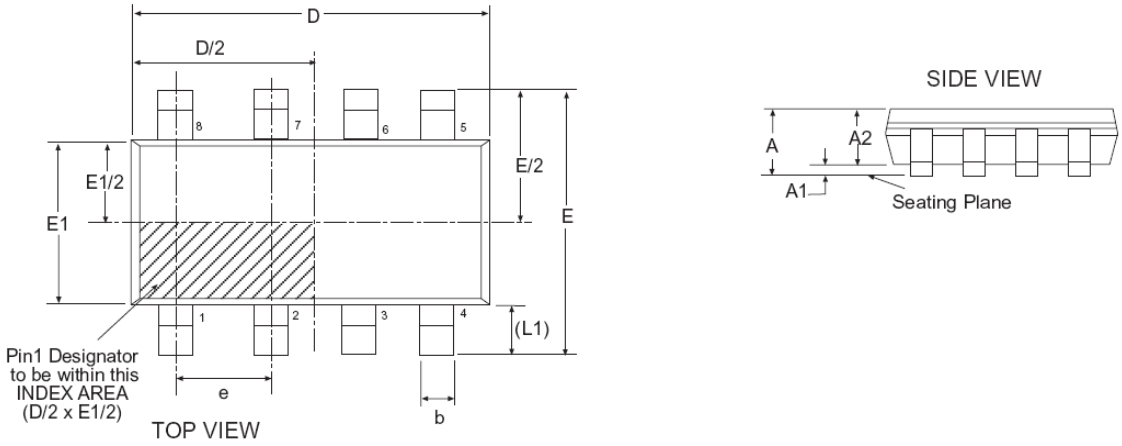


Testing V_{REF} Pin Shutdown Threshold $V_{TRIGGER}$



PACKAGE SPECIFICATION

8-PIN NSOIC



8 Pin NSOIC	JEDEC MS-012			Variation AA		
SYMBOL	Dimensions in Millimeters: Controlling Dimension			Dimensions in Inches Conversion Factor: 1 Inch = 25.40 mm		
	MIN	NOM	MAX	MIN	NOM	MAX
A	1.35	-	1.75	0.053	-	0.069
A1	0.10	-	0.25	0.004	-	0.010
A2	1.25	-	1.65	0.049	-	0.065
b	0.31	-	0.51	0.012	-	0.020
c	0.17	-	0.25	0.007	-	0.010
E	6.00 BSC			0.236 BSC		
E1	3.90 BSC			0.154 BSC		
e	1.27 BSC			0.050 BSC		
h	0.25		0.50	0.010	-	0.020
L	0.40	-	1.27	0.016	-	0.050
L1	1.04 REF			0.041 REF		
L2	0.25 BSC			0.010 BSC		
R	0.07	-	-	0.003	-	-
R1	0.07	-	-	0.003	-	-
ø	0º	-	8º	0º	-	8º
ø1	5º	-	15º	5º	-	15º
ø2	0º	-	-	0º	-	-
D	4.90 BSC			0.193 BSC		
SIPEX Pkg Signoff Date/Rev:				JL Aug16-05 / Rev A		

REVISION HISTORY

Revision	Date	Description
2.0.0	09/27/2010	Reformat of data sheet Corrected V_{CTRL} vs V_{CNTL} and V_{REF} annotations

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