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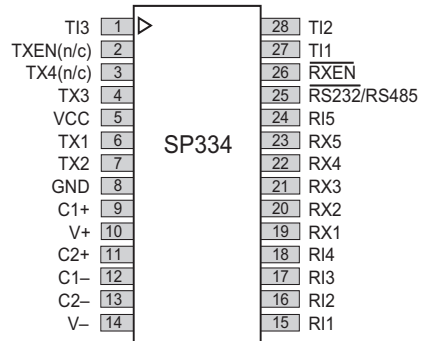
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## Programmable RS-232/RS-485 Transceiver

- +5V Single Supply Operation
- Software Programmable RS-232 or RS-485 Selection
- Three RS-232 Drivers and Five Receivers in RS-232 Mode
- Two RS-485 Full-Duplex Transceivers in RS-485 Mode
- Full Differential Driver Tri-State (Hi-Z) Control
- Receiver Output Tri-State Control



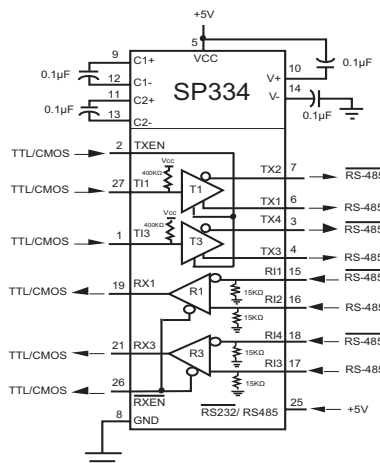
(in RS-232 Mode)

### DESCRIPTION

The **SP334** is a programmable RS-232 and/or RS-485 transceiver IC. The **SP334** contains three drivers and five receivers when selected in RS-232 mode; and two drivers and two receivers when selected in RS-485 mode.

The RS-232 transceivers can typically operate at 230kbps while adhering to the RS-232 specifications. The RS-485 transceivers can operate up to 10Mbps while adhering to the RS-485 specifications. The RS-485 drivers can be disabled (High-Z output) by the TXEN enable pin. The RS-232 and RS-485 receiver outputs can be disabled by the RXEN pin.

### TYPICAL APPLICATIONS CIRCUIT



## ABSOLUTE MAXIMUM RATINGS

These are stress ratings only and functional operation of the device at these ratings or any other above those indicated in the operation sections of the specifications below is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

V<sub>CC</sub>.....+7V  
 Input Voltages  
     Logic.....-0.5V to (V<sub>CC</sub>+0.5V)  
     Drivers.....-0.5V to (V<sub>CC</sub>+0.5V)  
     Receivers.....+/-30V @ ≤100mA  
 Driver Outputs.....+/-15V  
 Maximum Data Rate.....8Mbps (note 1)

Storage Temperature.....-65°C to +150°C  
 Power Dissipation  
     28-pin WSOIC.....1000mW  
 Package Derating:  
     28-pin WSOIC  
     θ<sub>JA</sub>.....40 °C/W

Note 1: Exceeding the maximum data rate of 8Mbps at T<sub>A</sub> = 85°C may permanently damage the device

## SPECIFICATIONS

Limits are specified at T<sub>A</sub> = 25°C and V<sub>CC</sub> = +5.0V unless otherwise noted.

PARAMETER	MIN.	TYP.	MAX.	UNITS	CONDITIONS
<b>Logic Inputs</b>					
V <sub>IL</sub>			0.8	Volts	
V <sub>IH</sub>	2.0			Volts	
<b>LOGIC OUTPUTS</b>					
V <sub>OL</sub>			0.4	Volts	I <sub>OUT</sub> = -3.2mA
V <sub>OH</sub>	2.4			Volts	I <sub>OUT</sub> = 1.0mA
Output Tri-state Leakage		10		µA	0.4V ≤ V <sub>OUT</sub> ≤ +2.4V
<b>RS-232 DRIVER</b>					
<b>DC Characteristics</b>					
HIGH Level Output	+5.0		+15.0	Volts	R <sub>L</sub> = 3kΩ, V <sub>IN</sub> = 0.8V
LOW Level Output	-15.0		-5.0	Volts	R <sub>L</sub> = 3kΩ, V <sub>IN</sub> = 2.0V
Open Circuit Voltage	-15		+15	Volts	
Short Circuit Current			+/-100	mA	V <sub>OUT</sub> = 0V
Power Off Impedance	300			Ω	V <sub>CC</sub> = 0V, V <sub>OUT</sub> = +/-2.0V
<b>AC Characteristics</b>					
Slew Rate			30	V/µs	R <sub>L</sub> = 3kΩ, C <sub>L</sub> = 50pF; V <sub>CC</sub> = +5.0V, T <sub>A</sub> @ 25°C
Transistion Time			1.56	µs	R <sub>L</sub> = 3KΩ, C <sub>L</sub> = 2500pF; between +/-3V, T <sub>A</sub> @ +25°C
Maximum Data Rate	120	235		kbps	R <sub>L</sub> = 3kΩ, C <sub>L</sub> = 2500pF
Propagation Delay t <sub>PHL</sub>		2	8	µs	Measured from 1.5V of V <sub>IN</sub> to 50% of V <sub>OUT</sub> ; R <sub>L</sub> = 3kΩ
Propagation Delay t <sub>PLH</sub>		2	8	µs	
<b>RS-232 RECEIVER</b>					
<b>DC Characteristics</b>					
HIGH Threshold		1.7	3.0	Volts	
LOW Threshold	0.8	1.2		Volts	
Receiver Open Circuit Bias			+2.0	Volts	
Input Impedance	3	5	7	kΩ	V <sub>IN</sub> = +15V to -15V

## SPECIFICATIONS

Limits are specified at  $T_A = 25^\circ\text{C}$  and  $V_{CC} = +5.0\text{V}$  unless otherwise

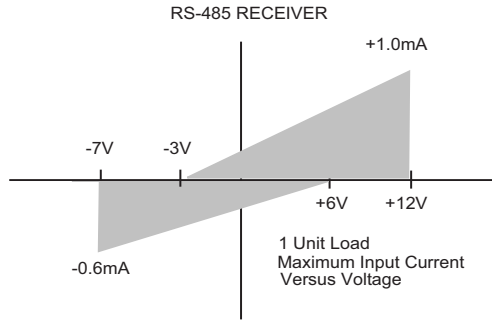
PARAMETER	MIN.	TYP.	MAX.	UNITS	CONDITIONS
<b>RS-232 RECEIVER (continued)</b>					
<b>AC Characteristics</b>					
Maximum Data Rate	120	235		kbps	
Propagation Delay $t_{PHL}$		0.25	1	$\mu\text{s}$	Measured from 50% of $V_{IN}$ to 1.5V of $V_{OUT}$
Propagation Delay $t_{PLH}$		0.25	1	$\mu\text{s}$	
<b>RS-485 DRIVER</b>					
<b>DC Characteristics</b>					
Open circuit Voltage			6.0	Volts	
Differential Output	1.5		5.0	Volts	$R_L = 54\Omega$ , $C_L = 50\text{pF}$
Balance			+/-0.2	Volts	$ V_{T1}  -  \overline{V_{T1}} $
Common-Mode Output			3.0	Volts	
Output Current	28.0			mA	$R_L = 54\Omega$
Short Circuit Current			+/-250	mA	Terminated in -7V to +10V
<b>AC Characteristics</b>					
Maximum Data Rate	10			Mbps	$R_L = 54\Omega$
Maximum Data Rate			8	Mbps	$R_L = 54\Omega$ , $T_A = +85^\circ\text{C}$ , Note 1
Output Transition Time		30		ns	Rise/Fall time, 10%-90%
Propagation Delay $t_{PHL}$		80	120	ns	See Figures 3 & 5, $R_{DIFF} = 54\Omega$ , $C_{L1} = C_{L2} = 100\text{pF}$
Propagation Delay $t_{PLH}$		80	120	ns	
Driver Output Skew		5	20	ns	Per Figure 5, $t_{SKEW} =  t_{DPHL} - t_{DPLH} $
<b>RS-485 RECEIVER</b>					
<b>DC Characteristics</b>					
Common Mode Range	-7.0		+12	Volts	
Receiver Sensitivity			+/-0.2	Volts	$-7\text{V} \leq V_{CM} \leq +12\text{V}$
Input Impedance	12	15		k $\Omega$	$-7\text{V} \leq V_{CM} \leq +12\text{V}$
<b>AC Characteristics</b>					
Maximum Data Rate	10			Mbps	
Maximum Data Rate			8	Mbps	$T_A = +85^\circ\text{C}$ , Note 1
Propagation Delay $t_{PHL}$		130	200	ns	See Figures 3 & 7, $R_{DIFF} = 54\Omega$ , $C_{L1} = C_{L2} = 100\text{pF}$
Propagation Delay $t_{PLH}$		130	200	ns	
Differential Receiver Skew		10	20	ns	$t_{SKEW} =  t_{PHL} - t_{PLH} $ , $R_{DIFF} = 54\Omega$ , $C_{L1} = C_{L2} = 100\text{pF}$ , see Figure 8
<b>ENABLE TIMING</b>					
<b>RS-485 DRIVER</b>					
Enable Time (see Figures 4 and 6)					
Enable to LOW		100	150	ns	$C_L = 15\text{pF}$ , $S_1$ Closed
Enable to HIGH		100	150	ns	$C_L = 15\text{pF}$ , $S_2$ Closed

Note 1: Exceeding the maximum data rate of 8Mbps at  $T_A = 85^\circ\text{C}$  may damage the device.

## SPECIFICATIONS

Limits are specified at  $T_A = 25^\circ\text{C}$  and  $V_{CC} = +5.0\text{V}$  unless otherwise

PARAMETER	MIN.	TYP.	MAX.	UNITS	CONDITIONS
<b>RS-485 Driver Continued</b>					
Disable Time (see Figures 4 and 6)					
Disable from LOW		100	120	ns	$C_L = 15\text{pF}$ , $S_1$ Closed
Disable from HIGH		100	120	ns	$C_L = 15\text{pF}$ , $S_2$ Closed
<b>RS-485 RECEIVER</b>					
Enable Time (see Figures 2 and 8)					
Enable to LOW		100	150	ns	$C_L = 15\text{pF}$ , $S_1$ Closed
Enable to HIGH		100	150	ns	$C_L = 15\text{pF}$ , $S_2$ Closed
Disable Time (see Figures 2 and 8)					
Disable from LOW		100	120	ns	$C_L = 15\text{pF}$ , $S_1$ Closed
Disable from HIGH		100	120	ns	$C_L = 15\text{pF}$ , $S_2$ Closed
<b>POWER REQUIREMENTS</b>					
Supply Voltage $V_{CC}$	+4.75		+5.25	Volts	
Supply Current $I_{CC}$					
No Load ( $T_X$ Disabled)		12	20	mA	$\overline{\text{TXEN}} = 0\text{V}$
No Load (RS-232 Mode)		20	50	mA	$\overline{\text{RS232}}/\text{RS485} = 0\text{V}$
No Load (RS-485 Mode)		15	50	mA	$\overline{\text{RS232}}/\text{RS485} = +5\text{V}$
<b>ENVIRONMENTAL</b>					
Operating Temperature					
Commercial ( $_C$ )	0		70	$^\circ\text{C}$	
Industrial ( $_E$ )	-40		+85	$^\circ\text{C}$	
Storage Temperature	-65		+150	$^\circ\text{C}$	



TEST CIRCUITS

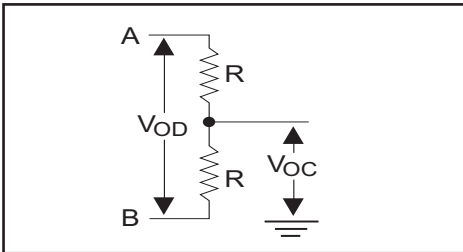


Figure 1. Driver DC Test Load Circuit

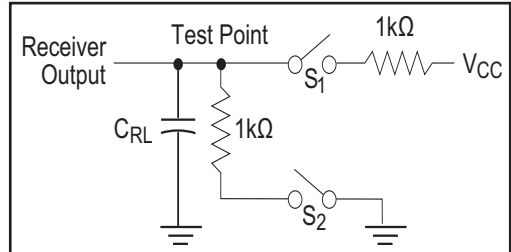


Figure 2. Receiver Timing Test Load Circuit

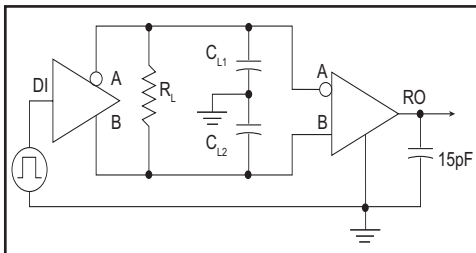


Figure 3. Driver/Receiver Timing Test Circuit

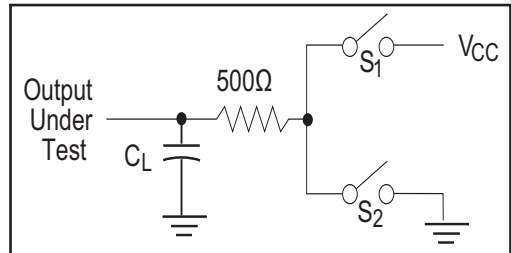


Figure 4. Driver Timing Test Load #2 Circuit

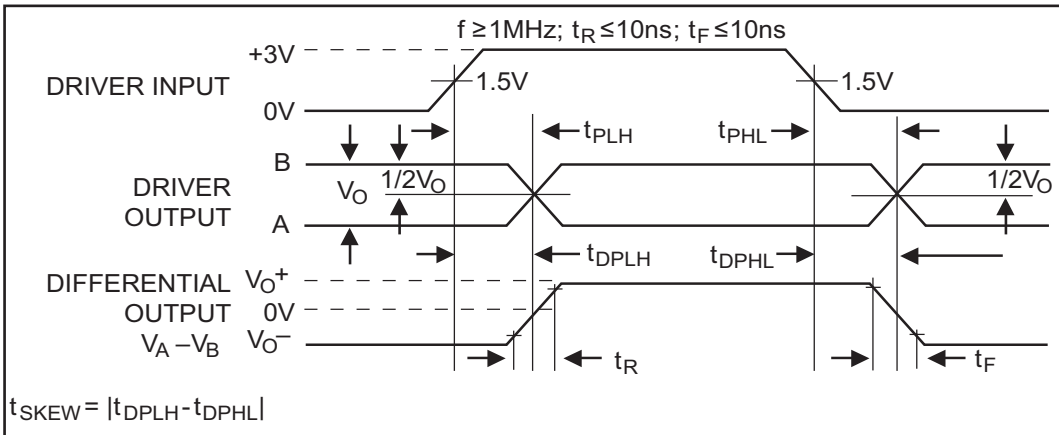


Figure 5. Driver Propagation Delays

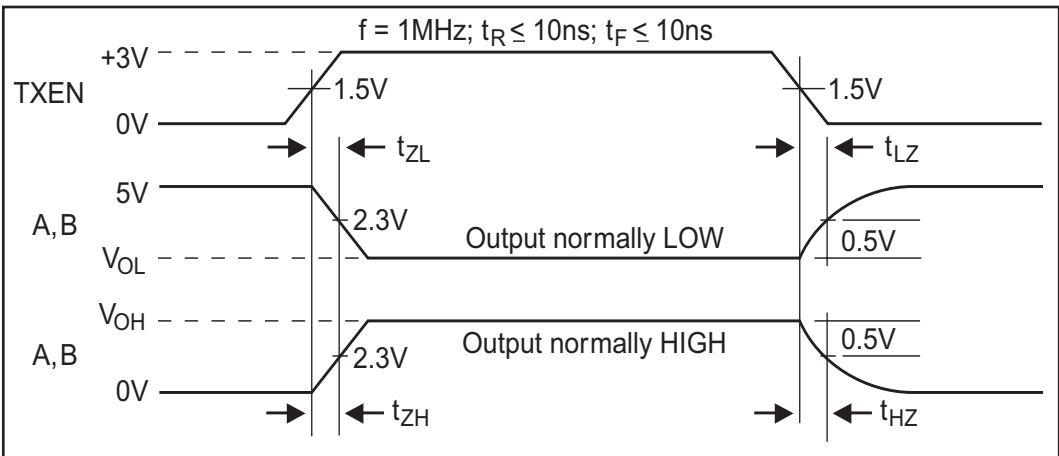


Figure 6. Driver Enable and Disable Times

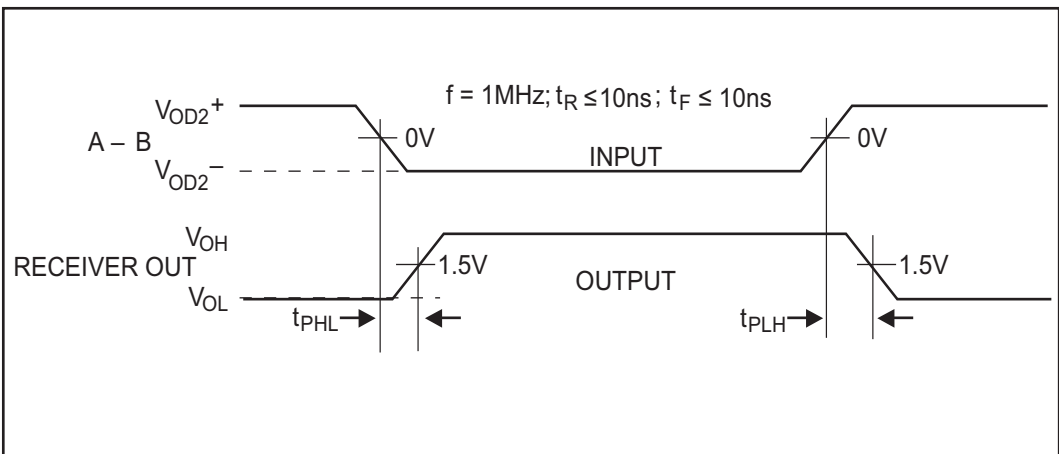


Figure 7. Receiver Propagation Delays

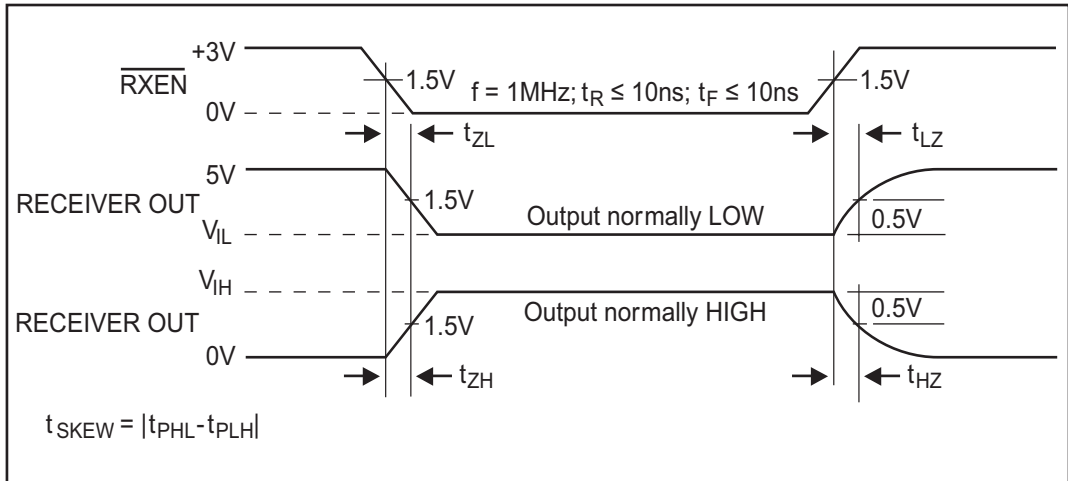


Figure 8. Receiver Enable and Disable Times

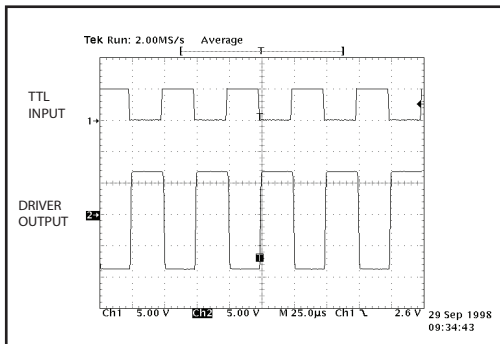


Figure 9. Typical RS-232 Driver Output

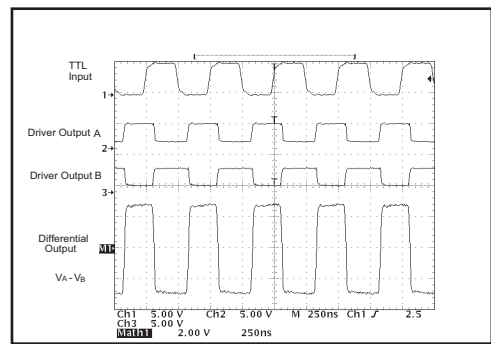


Figure 10. Typical RS-485 Driver Output

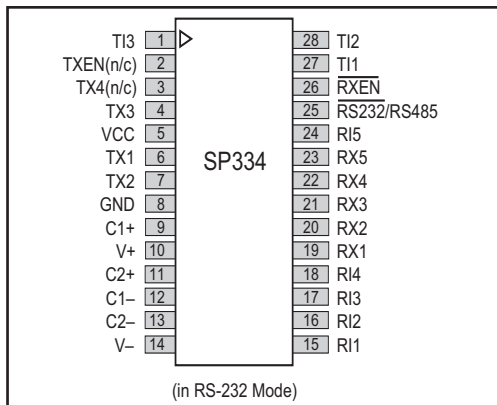


Figure 11. SP334 Pinout



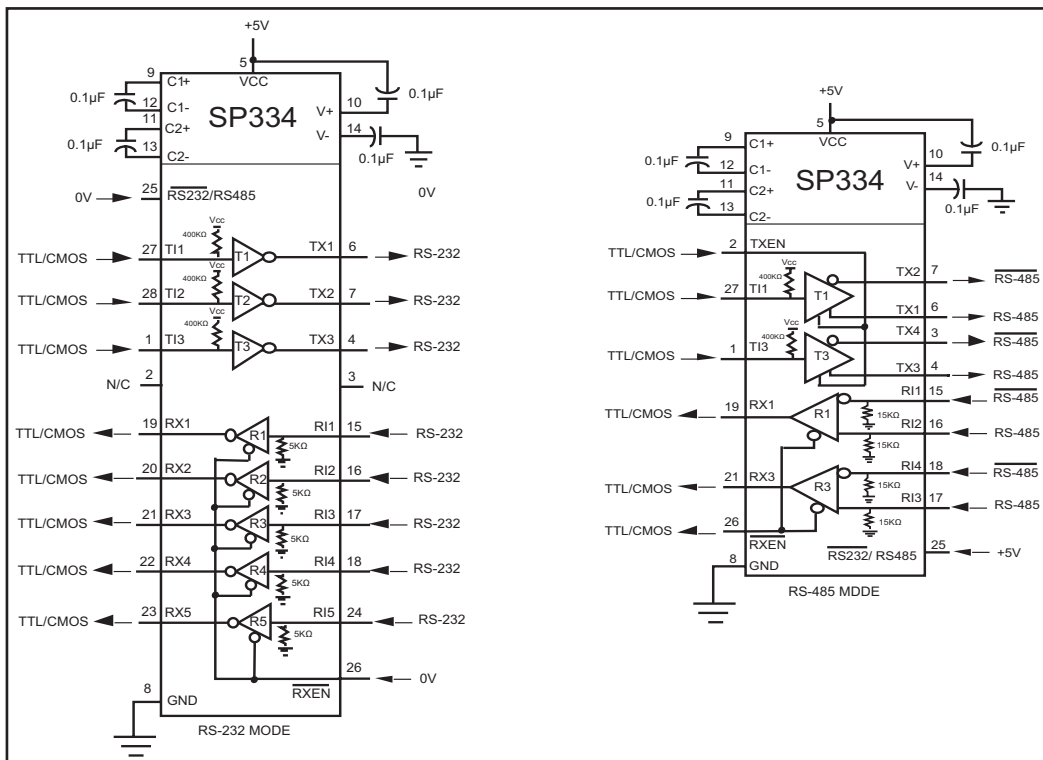


Figure 12. Typical Operating Circuit

## THEORY OF OPERATION

The **SP334** is made up of four separate circuit blocks — the charge pump, drivers, receivers, and decoder. Each of these circuit blocks is described in more detail below.

### Charge-Pump

The charge pump is a **Exar**–patented design (U.S. 5,306,954) and uses a unique approach compared to older less efficient designs. The charge pump still requires four external capacitors, but uses a four–phase voltage shifting technique to attain symmetrical 10V power supplies. Figure 17(a) shows the waveform found on the positive side of capacitor C<sub>2</sub>, and Figure 17(b) shows the negative side of capacitor C<sub>2</sub>. There is a free–running oscillator that controls the four phases of the voltage shifting. A description of each phase follows.

#### Phase 1

—V<sub>SS</sub> charge storage — During this phase of the clock cycle, the positive side of capacitors C<sub>1</sub> and C<sub>2</sub> are initially charged to +5V. C<sub>1</sub><sup>+</sup> is then switched to ground and charge on

C<sub>1</sub><sup>-</sup> is transferred to C<sub>2</sub><sup>-</sup>. Since C<sub>2</sub><sup>+</sup> is connected to +5V, the voltage potential across capacitor C<sub>2</sub> is now 10V.

#### Phase 2

—V<sub>SS</sub> transfer — Phase two of the clock connects the negative terminal of C<sub>2</sub> to the V<sub>SS</sub> storage capacitor and the positive terminal of C<sub>2</sub> to ground, and transfers the generated –10V to C<sub>3</sub>. Simultaneously, the positive side of capacitor C<sub>1</sub> is switched to +5V and the negative side is connected to ground.

#### Phase 3

—V<sub>DD</sub> charge storage — The third phase of the clock is identical to the first phase — the charge transferred in C<sub>1</sub> produces –5V in the negative terminal of C<sub>1</sub>, which is applied to the negative side of capacitor C<sub>2</sub>. Since C<sub>2</sub><sup>+</sup> is at +5V, the voltage potential across C<sub>2</sub> is 10V.

#### Phase 4

—V<sub>DD</sub> transfer — The fourth phase of the clock connects the negative terminal of C<sub>2</sub>

to ground and transfers the generated 10V across  $C_2$  to  $C_4$ , the  $V_{DD}$  storage capacitor. Again, simultaneously with this, the positive side of capacitor  $C_1$  is switched to +5V and the negative side is connected to ground, and the cycle begins again.

Since both  $V^+$  and  $V^-$  are separately generated from  $V_{CC}$  in a no-load condition,  $V^+$  and  $V^-$  will be symmetrical. Older charge pump approaches that generate  $V^-$  from  $V^+$  will show a decrease in the magnitude of  $V^-$  compared to  $V^+$  due to the inherent inefficiencies in the design.

The clock rate for the charge pump typically operates at 15kHz. The external capacitors must be a minimum of  $0.1\mu\text{F}$  with a 16V breakdown rating.

### External Power Supplies

For applications that do not require +5V only, external supplies can be applied at the  $V^+$  and  $V^-$  pins. The value of the external supply voltages must be no greater than  $\pm 10\text{V}$ . The current drain for the  $\pm 10\text{V}$  supplies is used for RS-232. For the RS-232 driver the current requirement will be 3.5mA per driver. The external power supplies should provide a power supply sequence of: +10V, then +5V, followed by -10V.

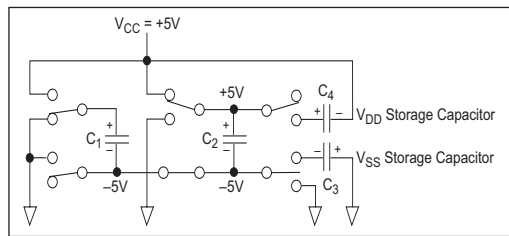


Figure 13. Charge Pump Phase 1.

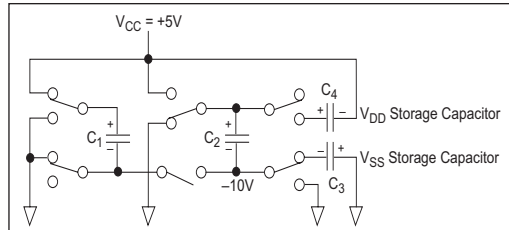


Figure 14. Charge Pump Phase 2.

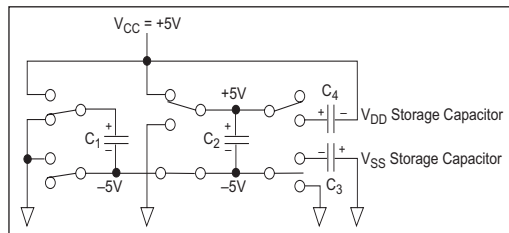


Figure 15. Charge Pump Phase 3.

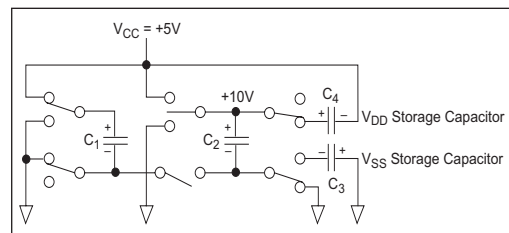


Figure 16. Charge Pump Phase 4.

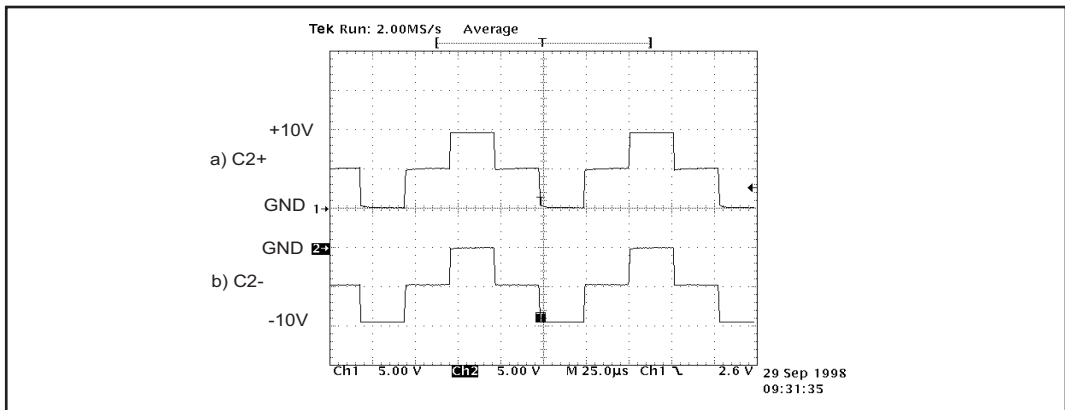


Figure 17. Charge Pump Waveforms

## Drivers

The **SP334** has three independent RS-232 single-ended drivers and two differential RS-485 drivers. Control for the mode selection is done by the RS232/RS485 select pin. The drivers are pre-arranged such that for each mode of operation the relative position and functionality of the drivers are set up to accommodate the selected interface mode. As the mode of the drivers is changed, the electrical characteristics will change to support the requirements of clock, data, and control line signal levels. Unused driver inputs can be left floating; however, to ensure a desired state with no input signal, pull-up resistors to +5V or pull-down resistors to ground are suggested. Since the driver inputs are both TTL or CMOS compatible, any value resistor less than 100k $\Omega$  will suffice.

When in RS-232 mode, the single-ended RS-232 drivers produce compliant RS-232E and ITU V.28 signals. Each of the three drivers output single-ended bipolar signals in access of  $\pm 5V$  with a full load of 3k $\Omega$  and 2500pF applied as specified. These drivers can also operate at least 120kbps.

When programmed to RS-485 mode, the differential RS-485 drivers produce complaint RS-485 signals. Each RS-485 driver outputs a unipolar signal on each output pin with a magnitude of at least 1.5V while loaded with a worst case of 54 $\Omega$  between the driver's two output pins. The signal levels and drive capability of the RS-485 drivers allow the drivers to also comply with RS-422 levels. The transmission rate for the differential drivers is 10Mbps.

## Receivers

The **SP334** has five single-ended receivers when programmed for RS-232 mode and two differential receivers when programmed for RS-485 mode.

Control for the mode selection is done by the same select pin as the drivers. As the operating mode of the receivers is changed, the electrical characteristics will change to support the requirements of the appropriate serial standard. Unused receiver inputs can be left floating without causing oscillation. To ensure a desired state of the receiver

output, a pull-up resistor of 100k $\Omega$  to +5V should be connected to the inverting input for a logic low, or the non-inverting input for a logic high. For single-ended receivers, a pull-down resistor to ground of 5k $\Omega$  is internally connected, which will ensure a logic high output.

The RS-232 receiver has a single-ended input with a threshold of 0.8V to 2.4V. The RS-232 receiver has an operating voltage range of  $\pm 15V$  and can receive signals up to 120kbps. RS-232 receivers are used in RS-232 mode for all signal types include data, clock, and control lines of the RS-232 serial port.

The differential RS-485 receiver has an input impedance of 15k $\Omega$  and a differential threshold of  $\pm 200mV$ . Since the characteristics of an RS-422 receiver are actually subsets of RS-485, the receivers for RS-422 requirements are identical to the RS-485 receivers. All of the differential receivers can receive data up to 10Mbps.

## Enable Pins

The **SP334** drivers can be enabled by use of the TXEN pin. A logic HIGH will enable the driver outputs and a logic LOW will tri-state the outputs. The drivers can only be tri-stated in RS-485 mode. The drivers are always active in RS-232 mode.

The Receiver outputs can also be tri-stated by the use of the RXEN pin. A logic LOW will enable the receiver outputs and a logic HIGH will tri-state the outputs. . The receiver tri-state capability is offered for both RS-232 and RS-485 modes. The input impedance of the receivers during tri-state is at least 12k $\Omega$ .

## Applications

The **SP334** allows the user flexibility in having a RS-232 or RS-485 serial port without using two different discrete active IC's. Figure 18 shows a connection to a standard DB-9 RS-232 connector. In RS-485 mode, the **SP334** is a full duplex transceiver, however, a half duplex configuration can be made by connecting the driver outputs to receiver inputs.

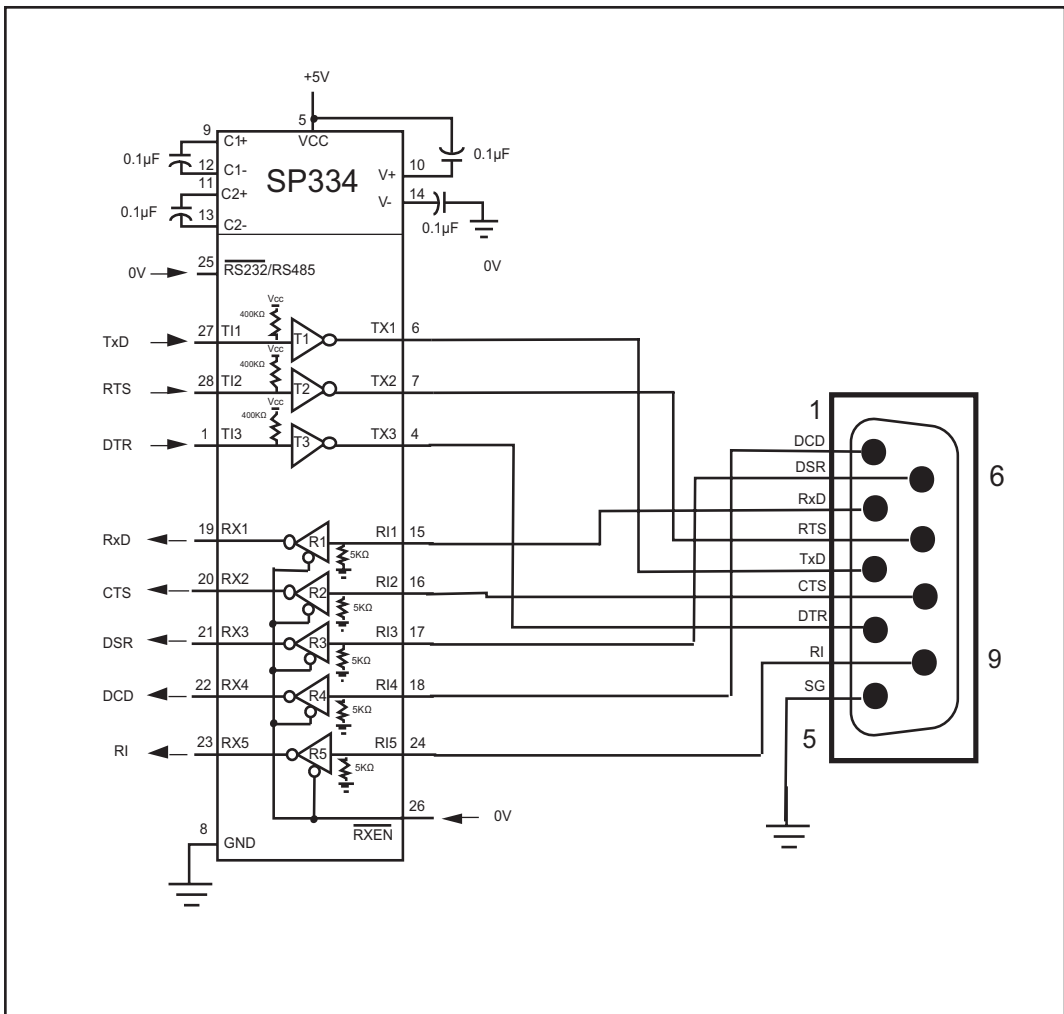
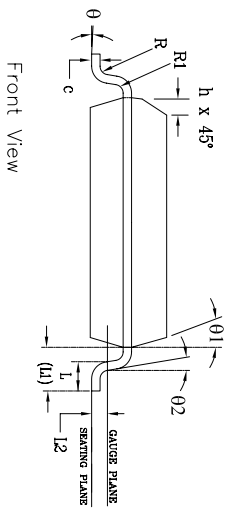
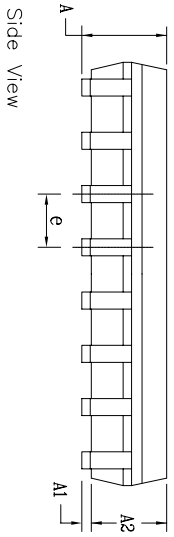
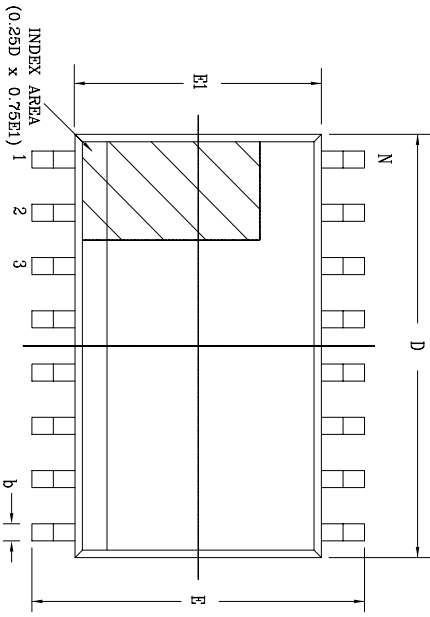


Figure 18. SP334 Configuration to a DB-9 Serial Port

REVISION HISTORY			
REV.	DESCRIPTION	DATE	APP'D
A	DRAWING ORIENTATION	04/24/06	JL
B	CHANGE DRAWING LOGO AND COMPANY NAME	11/28/07	JL



28 Pin SOICW		JEDEC MS-013		Variation AE	
SYMBOLS	DIMENSIONS IN MM (Control Unit)		DIMENSIONS IN INCH (Reference Unit)		MAX
	MIN	MAX	MIN	NOM	
A	2.35	2.65	0.093	—	0.104
A1	0.10	0.30	0.004	—	0.012
A2	2.05	2.55	0.081	—	0.100
b	0.31	0.51	0.012	—	0.020
c	0.20	—	0.008	—	0.013
E	10.30	BSC	0.406	BSC	—
E1	7.50	BSC	0.295	BSC	—
e	1.27	BSC	0.050	BSC	0.030
h	0.25	0.75	0.010	—	0.030
L	0.40	—	1.27	0.016	—
L1	1.40	REF	0.055	REF	—
L2	—	0.25 BSC	—	0.010 BSC	—
R	0.07	—	0.003	—	—
R1	0.07	—	0.003	—	8°
θ	0°	—	8°	0°	—
θ1	5°	—	15°	5°	—
θ2	0°	—	0°	—	15°
D	17.90	BSC	0.705	BSC	—
N	28	—	28	—	—

		<b>EXAR CORPORATION</b>	
		28 PIN SOICW PACKAGE OUTLINE	
Packaging Approver:	By: JL	Date: 11/28/07	Revision: B
Drawing No:	28-PIN SOICW		Sheet: 1 OF 1

## ORDERING INFORMATION

Model	Temperature Range	Package Types
SP334CT-L.....	0°C to +70°C.....	28-pin WSOIC
SP334CT-L/TR.....	0°C to +70°C.....	28-pin WSOIC
SP334ET-L.....	-40°C to +85°C.....	28-pin WSOIC
SP334ET-L/TR.....	-40°C to +85°C.....	28-pin WSOIC

Note: /TR = Tape and Reel

## REVISION HISTORY

DATE	REVISION	DESCRIPTION
2000	SP334/10	Legacy Sipex Datasheet
09/09/09	1.0.0	Convert to Exar Format. Add typical application circuit to page 1 and Revision History table. Remove EOL part numbers and update ordering information per PDN 081126-01. Change revision to 1.0.0. Add Maximum Data Rate to Absolute Maximum Ratings. Add RS-485 Driver and Receiver data rate column for 8Mbps maximum at Tmax and add Note 1.

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