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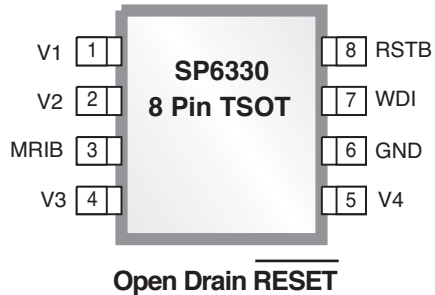
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China



Quad μ Power Supervisory Circuits with Manual Reset & Watchdog

FEATURES

- Low operating voltage of 1.6V
- Low operating current of 20 μ A typical
- Monitors up to four supplies simultaneously
- Adjustable inputs monitor down to 0.5V
- Reset asserted down to 0.9V
- 2% accuracy over temperature range
- Open Drain (OD) or CMOS RSTB output or CMOS RST output
- 4 Reset Timeout Periods: 50ms, 100ms, 200ms and 400ms
- Watch Dog Input Functionality -- WDI
- Manual Reset Input (Active Low) -- MRIB
- 8 Pin TSOT package



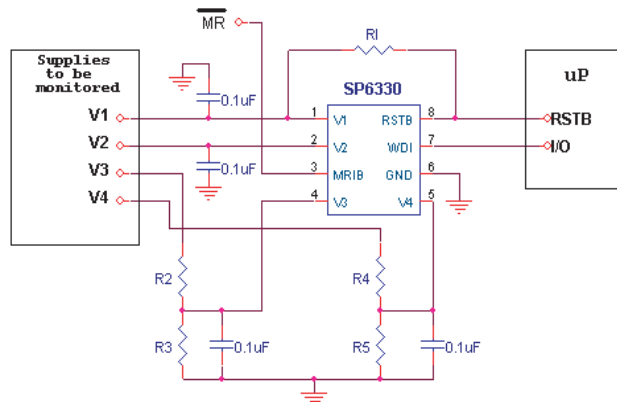
**SEE PAGE 2 FOR OTHER
AVAILABLE PINOUTS**

Available in Lead Free Packaging

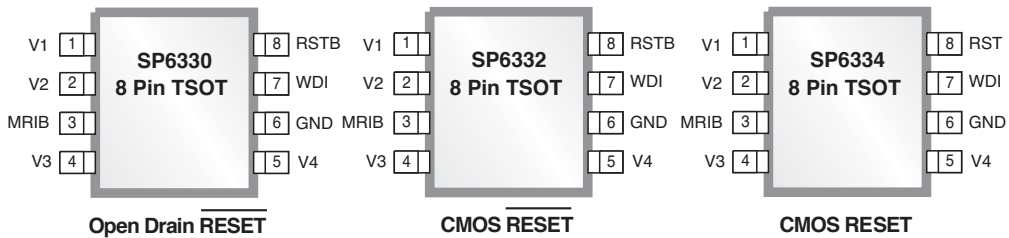
DESCRIPTION

SP6330-SP6332- SP6334 Quad Power Supervisory Circuit Family is a family of microprocessor reset supervisory circuits with multiple reset voltages. The family provides low voltage monitoring ability for up-to four supplies with two precision factory-set thresholds and two user defined custom thresholds. These circuits perform a single function: if any of the input supply voltages drops below its associated threshold, reset outputs are asserted. The SP6330, SP6332, and SP6334 are packaged in an 8-pin TSOT package. All devices are fully specified over -40°C to +85°C temperature range.

TYPICAL APPLICATION CIRCUIT



PINOUT DIAGRAMS



PART NUMBER	V1	V2	V3	V4	Reset	MRIB	WDI
SP6330	√	√	√	√	OD Active Low	√	√
SP6332	√	√	√	√	CMOS Active Low	√	√
SP6334	√	√	√	√	CMOS Active High	√	√

Feature and Pinout Diagram

Representative Samples Available

Sipex Product	Product Description	Package	V1 (Volts)	V2 (Volts)	V3 (Volts)	V4 (Volts)	Reset (ms)	Ordering #
SP6330	Quad Supervisor Open Drain low	8 Pin TSOT	2.925	1.575	0.5	0.5	200	SP6330EK1-L-W-G-C
SP6330	Quad Supervisor Open Drain low	8 Pin TSOT	3.075	2.313	0.5	0.5	200	SP6330EK1-L-X-J-C
SP6330	Quad Supervisor Open Drain low	8 Pin TSOT	4.625	2.313	0.5	0.5	200	SP6330EK1-L-Z-J-C
SP6332	Quad Supervisor CMOS low	8 Pin TSOT	2.625	1.575	0.5	0.5	200	SP6330EK1-L-V-G-C

ABSOLUTE MAXIMUM RATINGS

These are stress ratings only and functional operation of the device at these ratings or any other above those indicated in the operation sections of the specifications below is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability and cause permanent damage to the device.

Terminal Voltage (with respect to GND)

V1, V2..... -0.3 to +6V

Open-Drain RSTB..... -0.3 to +6V

CMOS RST, RSTB, -0.3 to (V1+0.3V)

Input Current/Output

Current.....20mA

V3, V4, MRIB, WDI..... -0.3 to (V1+0.3V)

Operating Temperature

Range.....-40°C to +85 °C

Storage Temperature

Range.....-65°C to 150°C

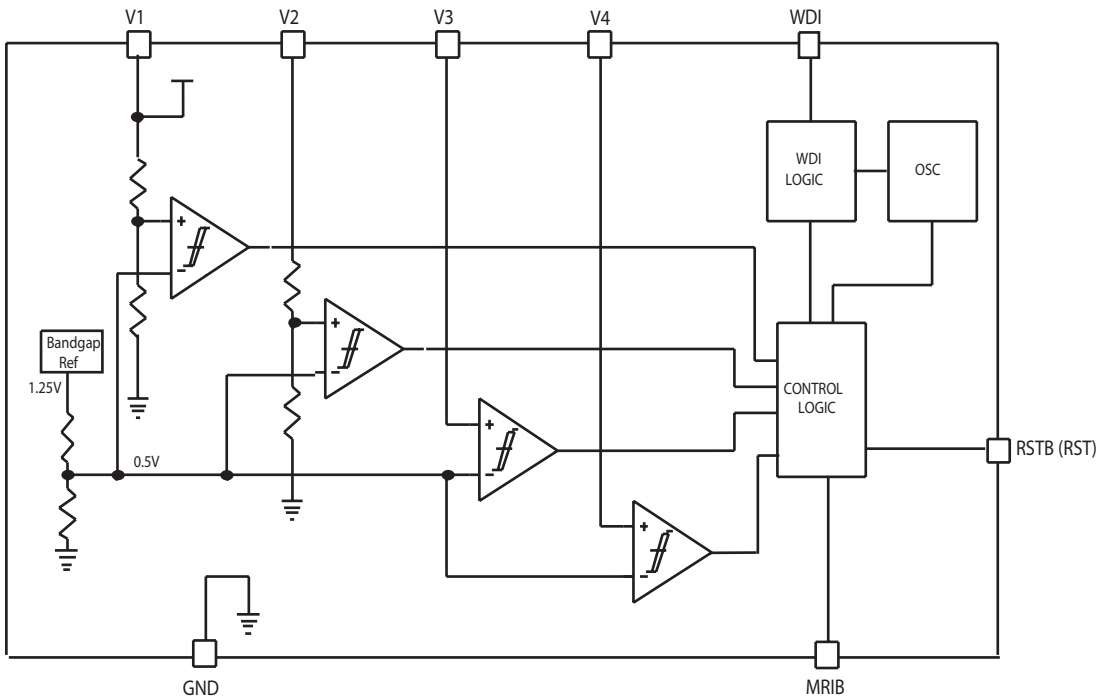
Thermal Resistance θ_{JA}134°C/W

PARAMETER	MIN	TYP	MAX	UNITS	CONDITIONS
V1 = 1.6V to 5.5V; TA = -40°C to +85°C; unless otherwise noted. Typical values are at TA = +25°C					
Operating Voltage Range	0.9		5.5	V	TA = -40°C to +85°C
Supply Current		20	30	μA	V1 < 5.5V, V2 < 3.60V, all I/O pins open
		15	25		V1 < 3.6V, V2 < 2.75V, all I/O pins open
V1 Reset Threshold	4.532	4.625	4.718	V	Z (valid for V1 falling)
	4.287	4.375	4.463		Y (valid for V1 falling)
	3.013	3.075	3.137		X (valid for V1 falling)
	2.866	2.925	2.984		W (valid for V1 falling)
	2.572	2.625	2.678		V (valid for V1 falling)
	2.273	2.320	2.367		U (valid for V1 falling)
	2.146	2.190	2.234		T (valid for V1 falling)
	1.636	1.670	1.704		S (valid for V1 falling)
V2 Reset Threshold	1.548	1.580	1.612	V	R (valid for V1 falling)
	2.266	2.313	2.360		J (valid for V2 falling)
	2.144	2.188	2.232		I (valid for V2 falling)
	1.631	1.665	1.698		H (valid for V2 falling)
	1.543	1.575	1.607		G (valid for V2 falling)
	1.360	1.388	1.416		F (valid for V2 falling)
	1.286	1.313	1.340		E (valid for V2 falling)
	1.087	1.110	1.133		D (valid for V2 falling)
	1.029	1.050	1.071		C (valid for V2 falling)
	0.816	0.833	0.850		B (valid for V2 falling)
0.772	0.788	0.804	A (valid for V2 falling)		
Threshold 1 Tempco		0.06		mV/°C	
Threshold 2 Tempco		0.04		mV/°C	
Threshold 1 Hysteresis		0.65		%	reference to Vth1 typical
Threshold 2 Hysteresis		0.5		%	reference to Vth2 typical
V1 to RST/RSTB Delay		50		us	V1 = Vth1 to (Vth1-0.1V), Vth1 = 3.075
V2 to RST/RSTB Delay		50		us	V2 = Vth2 to (Vth2-0.1V), Vth2 = 1.575
Reset Timeout Period (T1)	37	50	63	ms	TOPT-1
Reset Timeout Period (T2)	74	100	126	ms	TOPT-2
Reset Timeout Period (T3)	148	200	252	ms	TOPT-3
Reset Timeout Period (T4)	296	400	504	ms	TOPT-4

ELECTRICAL CHARACTERISTICS

PARAMETER	MIN	TYP	MAX	UNITS	CONDITIONS
V1 = 1.6V to 5.5V; TA = -40°C to +85°C; unless otherwise noted. Typical values are at TA = +25°C					
V3 RESET COMPARATOR INPUT					
V3 Input Threshold	490	500	510	mV	
V3 Input Current	-50		50	nA	TA = +25°C
V3 Threshold Hysteresis		1.5		mV	
V4 RESET COMPARATOR INPUT					
V4 Input Threshold	490	500	510	mV	
V4 Input Current	-50		50	nA	TA = +25°C
V4 Threshold Hysteresis		1.5		mV	
MRIB - MANUAL RESET INPUT					
MRIB Input Threshold			0.2*V1	V	Vil
MRIB Input Threshold	0.8*V1			V	Vih
MRIB Minimum Input Pulse Width	1			us	
MRIB Glitch Rejection		150		ns	
MRIB to RST/RSTB Delay		100		ns	
MRIB Pull-Up Resistance	30	55	85	kΩ	
WDI - WATCHDOG INPUT					
Watchdog Timeout Period	1.3	1.6	1.9	sec	
WDI Pulse Width	0.1			us	
WDI Input Threshold			0.2*V1	V	Vil
WDI Input Threshold	0.8*V1			V	Vih
WDI Input Current	-500		500	nA	WDI = 0.0V or V1
RESET OUTPUTS RST / RSTB					
RSTB (CMOS or OD)			0.2*V1	V	V1 = Vth1 - 0.1V, Isink = 1mA, output asserted
RSTB (CMOS)	0.8*V1			V	V1 = Vth1 + 0.1V, Isource = 1mA, output not asserted
RST (CMOS)	0.8*V1			V	V1 = Vth1 - 0.1V, Isource = 1mA, output asserted
RST (CMOS)			0.2*V1	V	V1 = Vth1 + 0.1V, V2 > Vth2, V3 > 0.5, V4 > 0.5, Isource = 1mA, output not asserted
RSTB Output OD Leakage Current		2		nA	TA = +25°C

Pin #	Name	Description
1	V1	First supply voltage input. Also powers internal circuitry. Trip threshold voltage internally set.
2	V2	Second supply voltage input. Trip threshold voltage internally set.
3	MRIB	Manual Reset Input pin. Active low. It has an internal pull-up resistor. Reset asserted when MRIB is pulled low and is kept asserted for 200ms after MRIB is released or pulled high. Leave open if not used.
4	V3	Input for the third supply voltage. Trip threshold is 0.5V.
5	V4	Input for the fourth supply voltage. Trip threshold is 0.5V.
6	GND	Common ground reference pin.
7	WDI	Watch-Dog Input pin. When no transition is detected at the WDI pin for the duration of WDI timeout period, reset is asserted. Leave open if not used. RST/RSTB output is used to signal watchdog timeout overflow. RST/RSTB output pulses high/low (depending on the active reset polarity) for the reset timeout period after each watchdog timeout overflow. The watchdog timer clears whenever the reset is asserted or manual reset is asserted or a transition is observed at WDI pin. Watchdog timer functionality can be disabled in parts by leaving this input floating.
8	RST/RSTB	Reset output. Open-Drain or CMOS, active high or low. Reset is asserted when any of the four supply inputs is below its trip threshold. It stays asserted for 200 ms (typical / default) after the last supply input traverses its trip threshold. Reset is guaranteed to be in the correct state for V1>0.9V. RST/RSTB asserts when V1 or V2 or V3 or V4 drop below their corresponding reset thresholds, or MRIB is pulled "LOW" or the watchdog timer triggers a reset (devices without WDOB). RST/RSTB remains asserted for the reset timeout period after V1 and V2 and V3 and V4 exceed their corresponding reset thresholds or MRIB goes "LOW" to "HIGH". Open-drain outputs require an external pull-up resistor. CMOS outputs are referenced to V1.



Block Diagram

The SP6330, SP6332, and SP6334 include a low-voltage precision bandgap reference, four precision comparators, an oscillator, a digital counter chain, a logic control block, trimmed resistor divider chains and additional supporting circuitry. The family is designed to supervise up to 4 independent supply voltages. V1 and V2 supply inputs have their resistor dividers on the chip. Their trip thresholds are factory trimmed. V3 and V4 inputs allow user to customize

two additional supply thresholds to be monitored by means of external resistor dividers. The devices also feature manual reset and watchdog functionalities.

As these devices do not have watchdog outputs, the watchdog timer is serviced internally during the watchdog timeout period when WDI is left unconnected. The watchdog functionality can be disabled by leaving the WDI input floating.

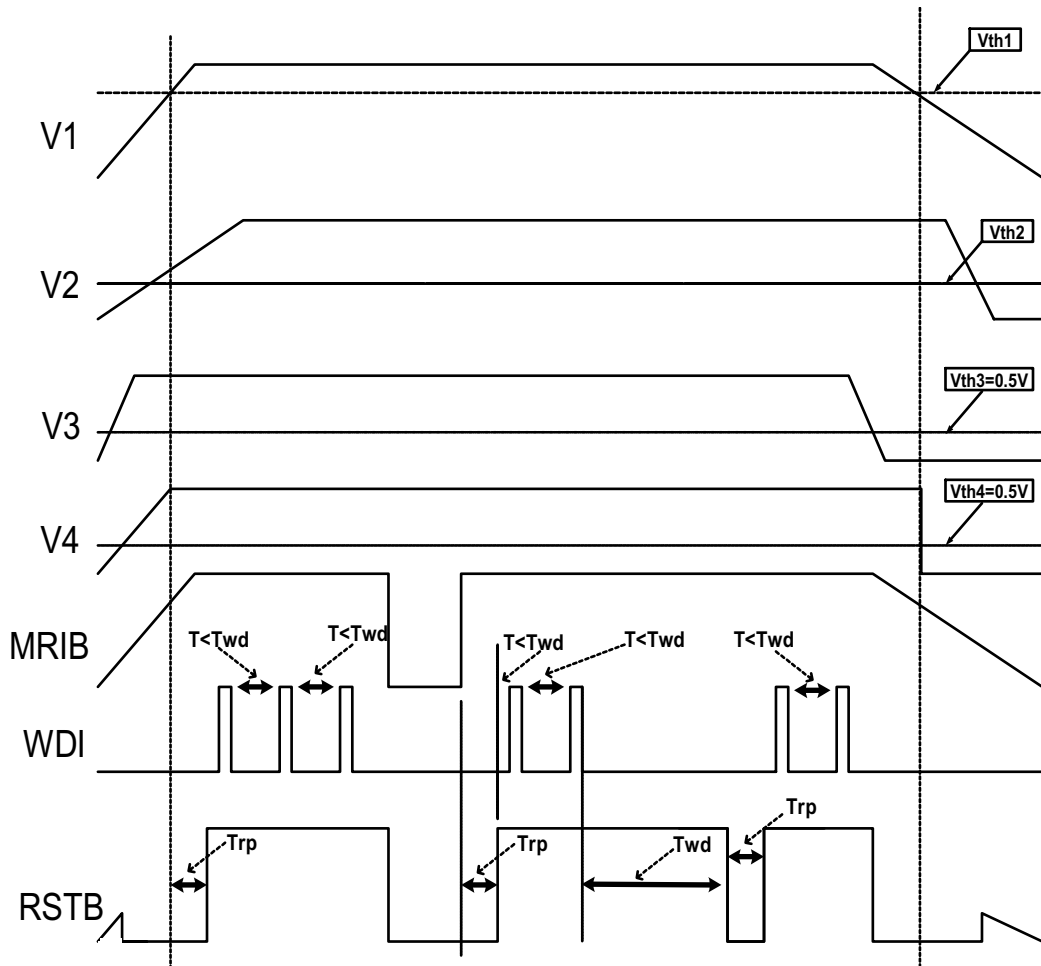
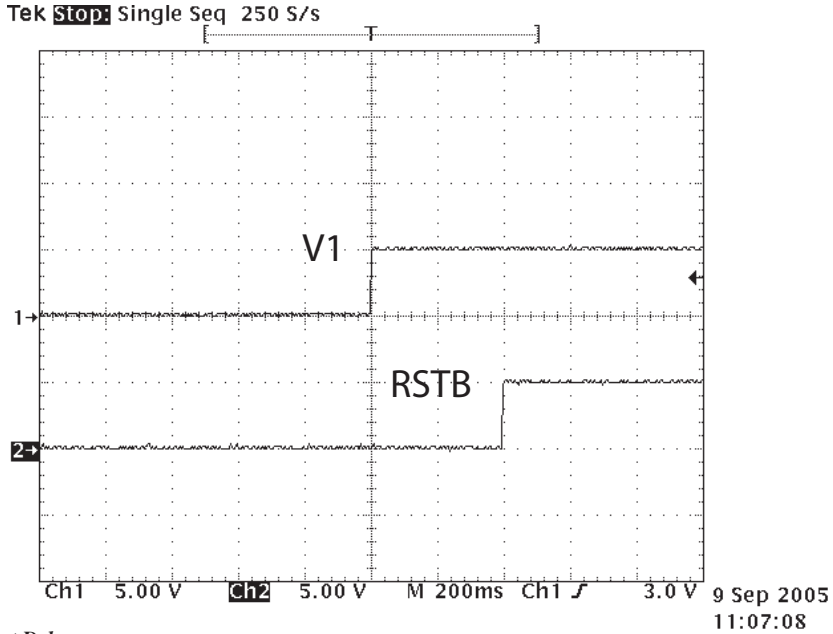
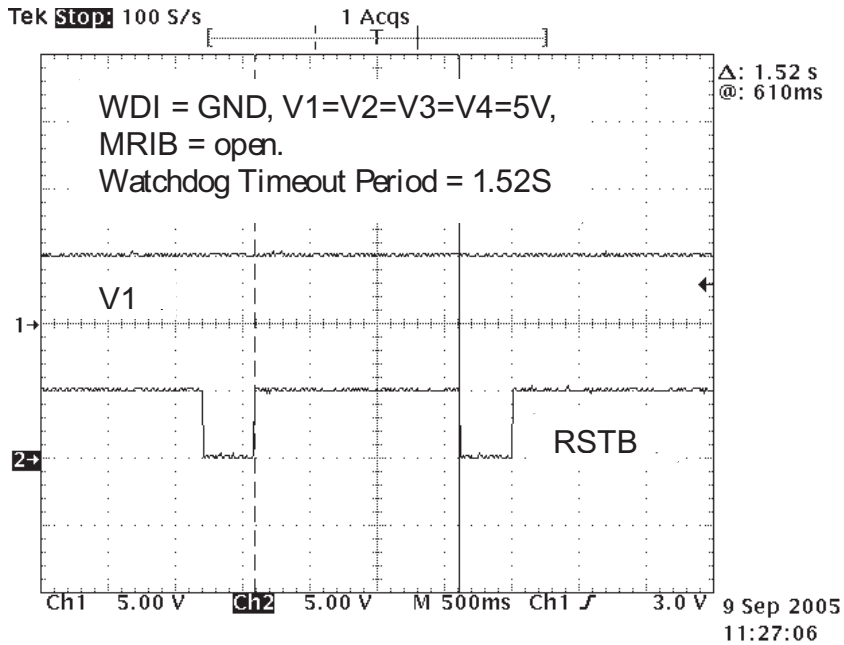


Figure 1: Functionality of a SP63XX family member with manual reset and watchdog capabilities but without WDOB output.

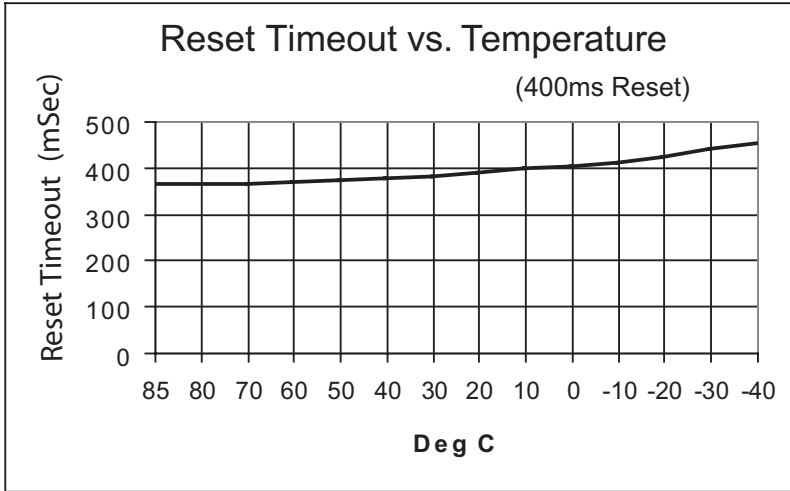
- $V1 > V_{th1}$, $V2 > V_{th2}$, $V3 > V_{th3}$ and $V4 > V_{th4}$ (all supplies over their corresponding thresholds)----> RSTB is de-asserted after reset timeout period (T_{rp}).
- MRIB goes to "LOW" to force "Reset" ----> RSTB is asserted immediately.
- WDI does not make any transition during watchdog timeout period (T_{wd}) ---->RSTB is asserted for a duration of reset timeout period (T_{rp}).
- One of the supplies drops below its corresponding threshold (in this case V3)---->RSTB is asserted immediately.



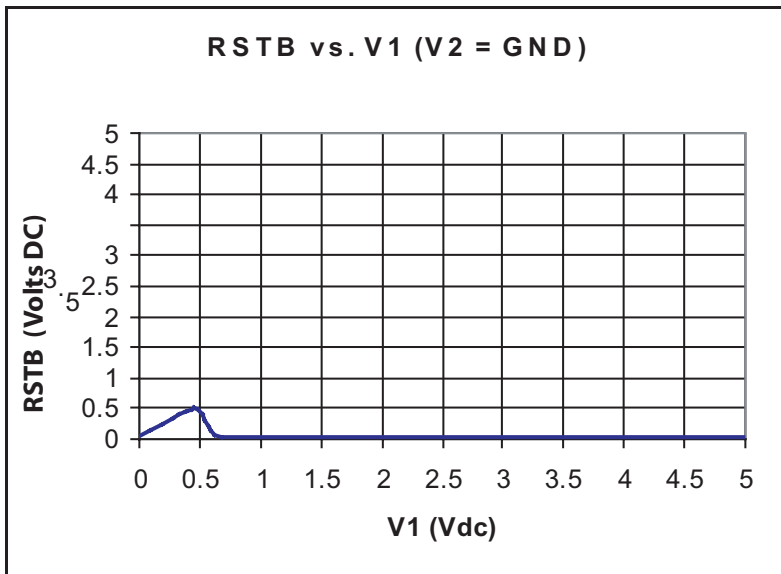
ResetB Timeout Delay



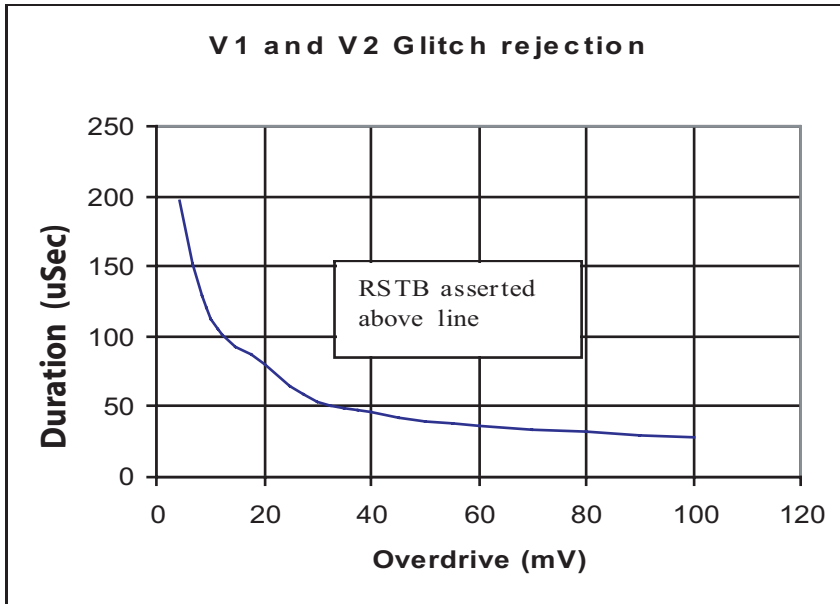
Watchdog Timeout Period



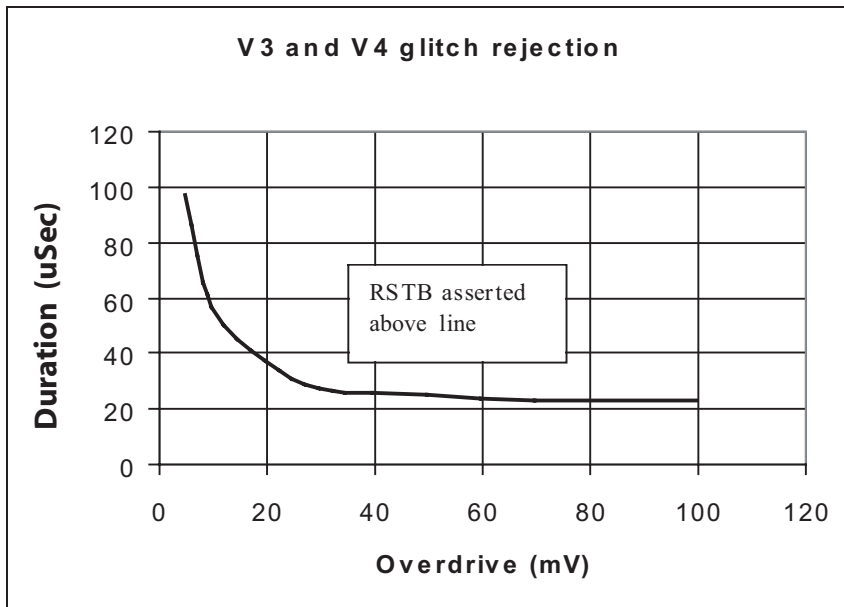
ResetTimeout Delay Vs. Temperature



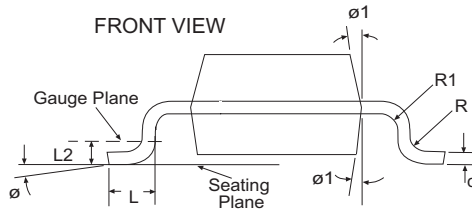
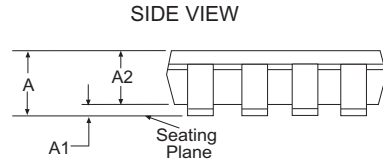
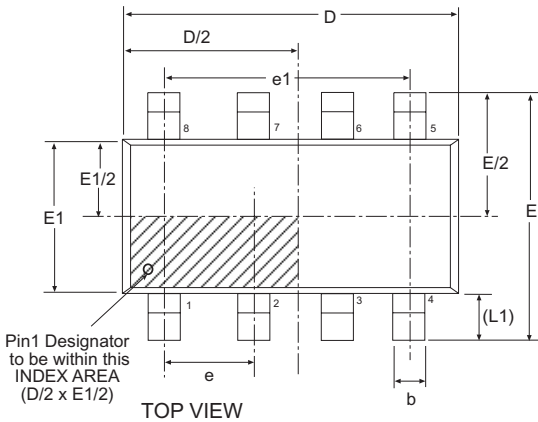
Reset Good



V1 and V2 Glitch Rejection



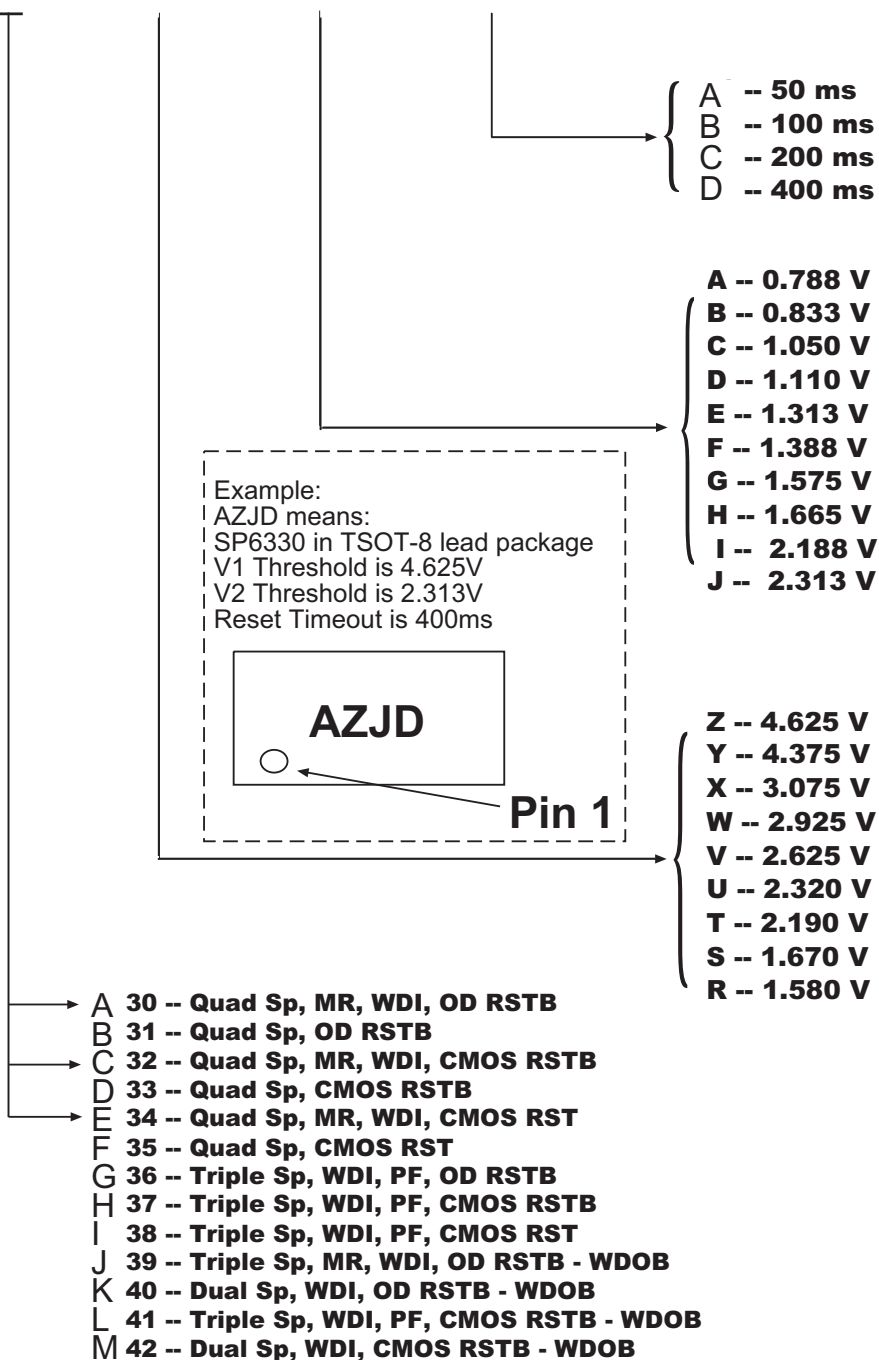
V3 and V4 Glitch Rejection



8 Pin TSOT		JEDEC MO-193			Variation BA		
SYMBOL	Dimensions in Millimeters: Controlling Dimension			Dimensions in Inches Conversion Factor: 1 Inch = 25.40 mm			
	MIN	NOM	MAX	MIN	NOM	MAX	
A	-	-	1.10	-	-	0.043	
A1	0.00	-	0.10	0.000	-	0.004	
A2	0.70	0.90	1.00	0.028	0.036	0.039	
c	0.08	-	0.20	0.003	-	0.008	
D	2.90 BSC			0.114 BSC			
E	2.80 BSC			0.110 BSC			
E1	1.60 BSC			0.063 BSC			
L	0.30	0.45	0.60	0.012	0.018	0.024	
L1	0.60 REF			0.024 REF			
L2	0.25 BSC			0.010 BSC			
Ø	0°	4°	8°	0°	4°	8°	
Ø1	4°	10°	12°	4°	10°	12°	
R	0.10	-	-	0.004	-	-	
R1	0.10	-	0.25	0.004	-	0.010	
b	0.22	-	0.38	0.009	-	0.015	
e	0.65 BSC			0.026 BSC			
e1	1.95 BSC			0.077 BSC			
SIPLEX Pkg Signoff Date/Rev:				JL Oct3-05 / Rev A			

Part Naming Nomenclature

SP63N - Th1 - Th2 - TOPT



Model Package Types	Temperature Range	
SP6330EK1-L-X-X-X.....	-40°C to +85°C.....	Lead Free 8-Pin TSOT
SP6330EK1-L-X-X-X/TR.....	-40°C to +85°C.....	Lead Free 8-Pin TSOT
SP6332EK1-L-X-X-X.....	-40°C to +85°C.....	Lead Free 8-Pin TSOT
SP6332EK1-L-X-X-X/TR.....	-40°C to +85°C.....	Lead Free 8-Pin TSOT
SP6334EK1-L-X-X-X.....	-40°C to +85°C.....	Lead Free 8-Pin TSOT
SP6334EK1-L-X-X-X/TR.....	-40°C to +85°C.....	Lead Free 8-Pin TSOT

Available in lead free packaging only. /TR = Tape and Reel

Pack quantity 2,500 for TSOT-8

Contact Factory for availability of particular voltage threshold and reset timeout options. Note that the Ordering Information denoting those options corresponds to the Part Naming Nomenclature shown on the previous page.

Ordering example: SP6330EK1-L-W-G-C/TR == W -- 2.925V for Voltage Threshold 1; G -- 1.575V for Voltage Threshold 2; and C -- 200ms reset timeout.



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