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**GENERAL DESCRIPTION**

The SP809/SP810 are low power microprocessor ( $\mu$ P) supervisory circuits used to monitor power supplies in  $\mu$ P and digital systems.

They provide applications with benefits of circuit reliability and low cost by eliminating external components. If the VCC supply voltage falls below preset threshold then a reset signal is asserted for at least 140ms after VCC has risen above the reset threshold.

Both the SP809 and SP810 were designed with a reset comparator to help identify invalid signals, which last less than 140ms. The only difference between them is that they have an active-low RESET output and active-high RESET output, respectively. Low supply current (1 $\mu$ A) makes SP809/SP810 ideal for portable equipment.

The devices are available in 3 pin SOT-23 package.

**APPLICATIONS**

- **Portable Electronic Devices**
- **Electrical Power Meters**
- **Digital Still Cameras**
- **$\mu$ P Power Monitoring**

**FEATURES**

- **Ultra Low Supply Current 1 $\mu$ A (typ)**
- **Guaranteed Reset valid to VCC = 0.9V**
- **140ms Power-On Reset Pulse Width**
- **Internally Fixed Threshold 2.3V, 2.6V, 2.9V, 3.1V, 4.4V, 4.6V**
- **1.5% Voltage Threshold Tolerance**
- **3 Pin SOT-23 Package**

Part Number	Output Type
SP809N	Open Drain Active Low
SP809	Push-Pull Low
SP810	Push-Pull Active High

**TYPICAL APPLICATION DIAGRAM**

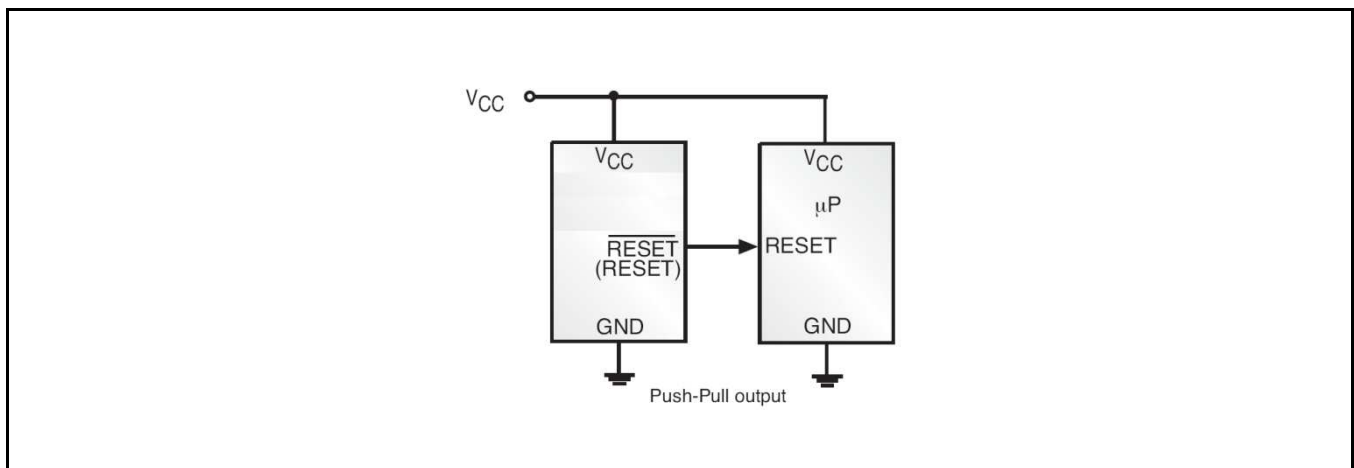


Fig. 1: SP809 / SP810 Application Diagram



**ABSOLUTE MAXIMUM RATINGS**

These are stress ratings only and functional operation of the device at these ratings or any other above those indicated in the operation sections of the specifications below is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

V<sub>CC</sub> ..... -0.3V to 6.5V  
 RESET,  $\overline{\text{RESET}}$  ..... -0.3V to V<sub>CC</sub>+0.3V  
 Output Current (RESET,  $\overline{\text{RESET}}$ ) ..... 20mA  
 Power Dissipation (T<sub>A</sub>=70°C) ..... 320mW  
 Junction Temperature ..... 125°C  
 Storage Temperature ..... -65°C to 150°C

**OPERATING RATINGS**

Input Voltage Range V<sub>CC</sub> ..... 0.9V to 6V  
 Junction Temperature Range ..... -40°C to 85°C

**ELECTRICAL SPECIFICATIONS**

Specifications with standard type are for an Operating Temperature of T<sub>A</sub> = 25°C only; limits applying over the full Operating Temperature range are denoted by a "•". Minimum and Maximum limits are guaranteed through test, design, or statistical correlation. Typical values represent the most likely parametric norm at T<sub>A</sub> = 25°C, and are provided for reference purposes only. Unless otherwise indicated, T<sub>A</sub> = 25°C.

Parameter	Min.	Typ.	Max.	Units	Conditions
Operating Voltage Range V <sub>CC</sub>	0.9		6.0	V	
Supply Current I <sub>CC</sub>		1.0	3.0	μA	V <sub>CC</sub> =V <sub>TH</sub> +0.1V
Reset Threshold V <sub>TH</sub>	2.265	2.3	2.335	V	T <sub>A</sub> =+25°C
	2.254		2.346		• T <sub>A</sub> =-40°C to 85°C
	2.561	2.6	2.639		T <sub>A</sub> =+25°C
	2.548		2.652		• T <sub>A</sub> =-40°C to 85°C
	2.857	2.9	2.944		T <sub>A</sub> =+25°C
	2.842		2.958		• T <sub>A</sub> =-40°C to 85°C
	3.054	3.1	3.147		T <sub>A</sub> =+25°C
	3.038		3.162		• T <sub>A</sub> =-40°C to 85°C
	4.334	4.4	4.466		T <sub>A</sub> =+25°C
	4.312		4.488		• T <sub>A</sub> =-40°C to 85°C
V <sub>CC</sub> Reset Delay V <sub>TRIP</sub>		20		μs	V <sub>CC</sub> =V <sub>TH</sub> to (V <sub>TH</sub> + 0.1V), V <sub>TH</sub> =3.1V
	140	230	560		T <sub>A</sub> =+25°C
Reset Active Timeout Period T <sub>RP</sub>	100		1030	ms	• T <sub>A</sub> =-40°C to 85°C
RESET Output Voltage V <sub>OH</sub>	0.8V <sub>CC</sub>			V	V <sub>CC</sub> =V <sub>TH</sub> - 0.1V, I <sub>SOURCE</sub> = 1.2mA
RESET Output Voltage V <sub>OL</sub>			0.3	V	V <sub>CC</sub> =V <sub>TH</sub> + 0.1V, I <sub>SINK</sub> = 1.2mA
$\overline{\text{RESET}}$ Output Voltage V <sub>OH</sub>	0.8V <sub>CC</sub>			V	V <sub>CC</sub> =V <sub>TH</sub> + 0.1V, I <sub>SOURCE</sub> = 1.2mA
$\overline{\text{RESET}}$ Output Voltage V <sub>OL</sub>			0.3	V	V <sub>CC</sub> =V <sub>TH</sub> - 0.1V, I <sub>SINK</sub> = 1.2mA

Note 1:  $\overline{\text{RESET}}$  output is for SP809; RESET output is for SP810.

**BLOCK DIAGRAM**

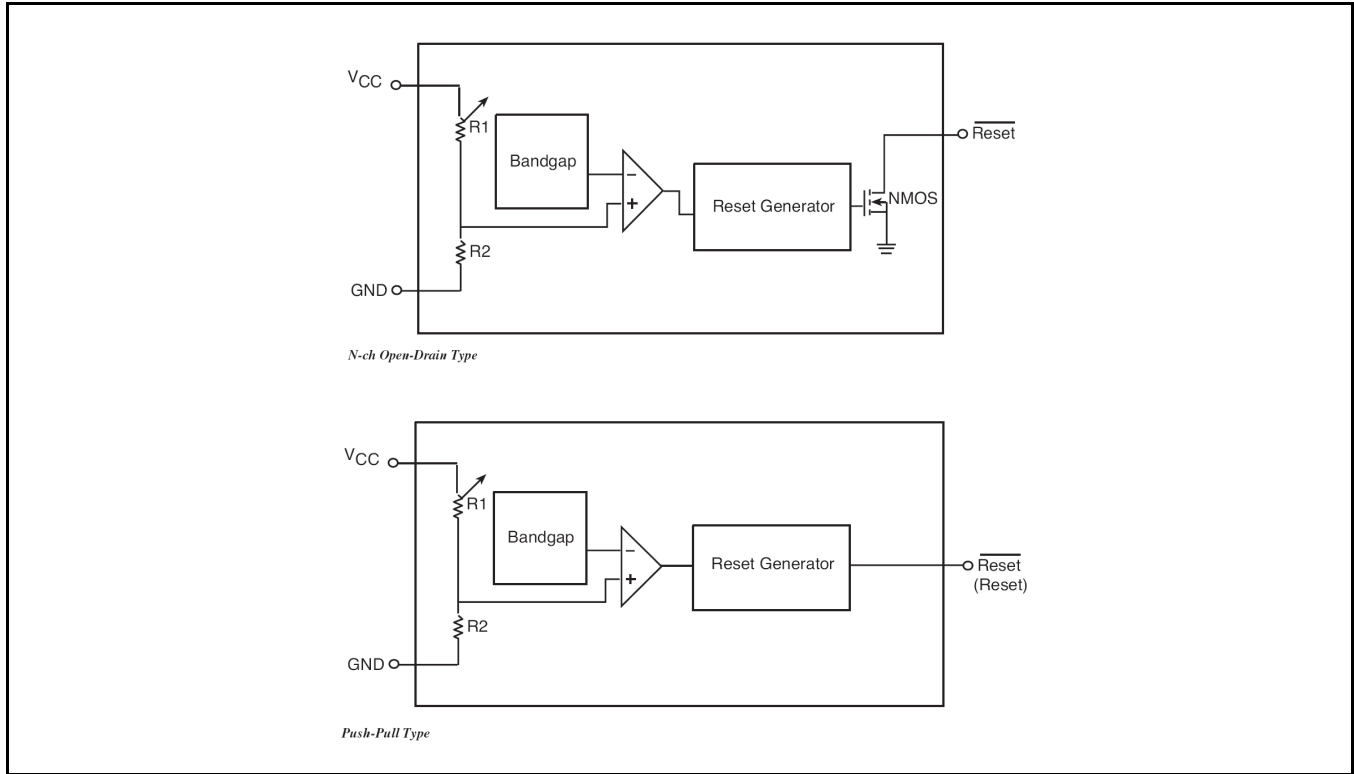


Fig. 2: SP809 / SP810 Block Diagram

**PIN ASSIGNMENT**

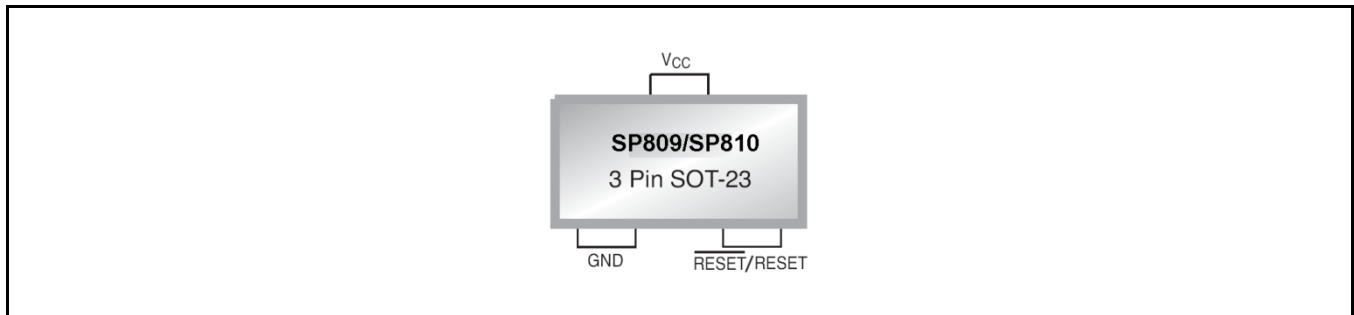


Fig. 3: SP809 / SP810 Pin Assignment

**PIN DESCRIPTION**

Name	Pin Number	Description
GND	1	Ground Signal
RESET	2	Active Low Output Pin. RESET Output remains high while VCC is below the reset threshold
RESET		Active High Output Pin. RESET Output remains high while VCC is below the reset threshold
V <sub>CC</sub>	3	Supply Voltage



# SP809 / SP810

## 3 Pin Microprocessor Supervisor Circuit

### ORDERING INFORMATION

Part Number	Temperature Range	Marking	Package	Packing Quantity	Note 1	Note 2
SP809EK-L-2-3/TR	-40°C ≤ T <sub>A</sub> ≤ +85°C	N4WW	SOT23-3	2.5K/Tape & Reel	Lead Free	
SP809EK-L-2-6/TR	-40°C ≤ T <sub>A</sub> ≤ +85°C	P4WW				
SP809EK-L-2-9/TR	-40°C ≤ T <sub>A</sub> ≤ +85°C	Q4WW				
SP809EK-L-3-1/TR	-40°C ≤ T <sub>A</sub> ≤ +85°C	R4WW				
SP809EK-L-4-6/TR	-40°C ≤ T <sub>A</sub> ≤ +85°C	U4WW				
SP809NEK-L-2-3/TR	-40°C ≤ T <sub>A</sub> ≤ +85°C	V4WW				
SP809NEK-L-2-9/TR	-40°C ≤ T <sub>A</sub> ≤ +85°C	X4WW				
SP809NEK-L-3-1/TR	-40°C ≤ T <sub>A</sub> ≤ +85°C	Y4WW				
SP809NEK-L-4-6/TR	-40°C ≤ T <sub>A</sub> ≤ +85°C	C5WW				
SP810EK-L-2-6/TR	-40°C ≤ T <sub>A</sub> ≤ +85°C	E5WW				
SP810EK-L-4-4/TR	-40°C ≤ T <sub>A</sub> ≤ +85°C	J5WW				

"YY" = Year - "WW" = Work Week - "X" = Lot Number; when applicable.

**TYPICAL PERFORMANCE CHARACTERISTICS**

All data taken at  $T_A = 25^\circ\text{C}$ , unless otherwise specified - Schematic and BOM from Application Information section of this datasheet.

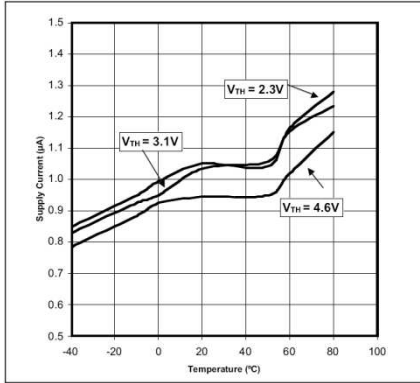


Fig. 4: Supply Current versus Temperature

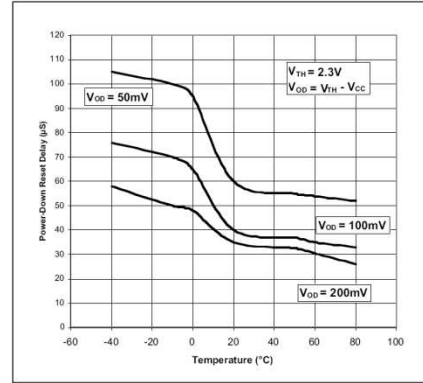


Fig. 5: Power-Down Reset Delay versus Temperature

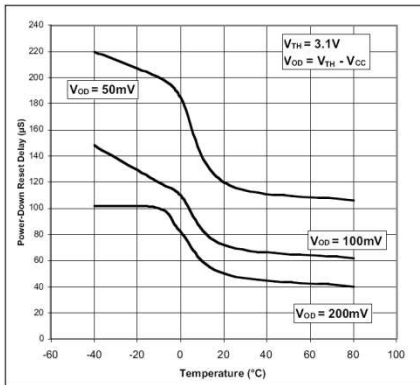


Fig. 6: Power-Down Reset Delay versus Temperature

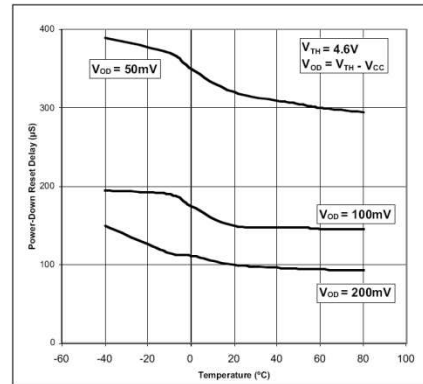


Fig. 7: Power-Down Reset Delay versus Temperature

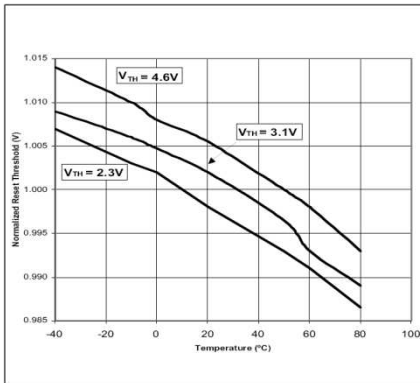


Fig. 8: Normalized Reset Threshold versus Temperature

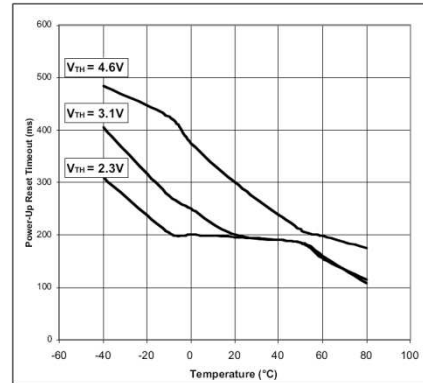


Fig. 9: Power-Up Reset Time-out versus Temperature

**THEORY OF OPERATION**

$\mu P$  will be activated at a valid reset state. These  $\mu P$  supervisory circuits assert reset to prevent code execution errors during power-up, power-down, or brownout conditions.

Reset is guaranteed to be a logic low for  $V_{TH} > V_{CC} > 0.9V$ . Once  $V_{CC}$  exceeded the reset threshold, an internal timer keeps  $\overline{RESET}$  low for the reset timeout period; after this interval,  $\overline{RESET}$  goes high.

If a brownout condition occurs ( $V_{CC}$  drops below the reset threshold),  $\overline{RESET}$  goes low. Any time  $V_{CC}$  goes below the reset threshold, the internal timer resets to zero, and  $\overline{RESET}$  goes low. The internal timer is activated after

$V_{CC}$  returns above the reset threshold, and  $\overline{RESET}$  remains low for the reset timeout period.

**BENEFIT OF HIGHLY ACCURATE RESET THRESHOLD**

SP809/810 with specified voltage as  $5V \pm 10\%$  or  $3V \pm 10\%$  are ideal for systems using a  $5V \pm 5\%$  or  $3V \pm 5\%$  power supply. The reset is guaranteed to assert after the power supply falls below the minimum specified operating voltage range of the system ICs. The pre-trimmed thresholds are reducing the range over which an undesirable reset may occur.

**APPLICATION INFORMATION**

**NEGATIVE GOING  $V_{CC}$  TRANSIENTS**

In addition to issuing a reset to the  $\mu P$  during power-up, power-down, and brownout conditions, SP809 series are relatively resistant to short-duration negative-going  $V_{CC}$  transient.

**ENSURING A VALID RESET OUTPUT DOWN TO  $V_{CC} = 0$**

When  $V_{CC}$  falls below 0.9V, SP809  $\overline{RESET}$  output no longer sinks current; it becomes an open circuit. In this case, high-impedance CMOS logic inputs connecting to  $\overline{RESET}$  can drift to undetermined voltages. Therefore, SP809/810 with CMOS is perfect for most applications of  $V_{CC}$  down to 0.9V.

However in applications where  $\overline{RESET}$  must be valid down to 0V, adding a pull-down resistor to  $\overline{RESET}$  causes any leakage currents to flow to ground, holding  $\overline{RESET}$  low.

**INTERFACING TO  $\mu P$  WITH BIDIRECTIONAL RESET PINS**

The  $\overline{RESET}$  output on the SP809N is open drain, this device interfaces easily with  $\mu Ps$  that have bidirectional reset pins. Connecting the  $\mu P$  supervisor's  $\overline{RESET}$  output directly to the microcontroller's  $\overline{RESET}$  pin with a single pull-up resistor allows either device to assert reset.

**TEST CIRCUIT**

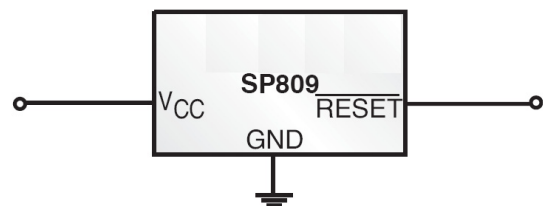
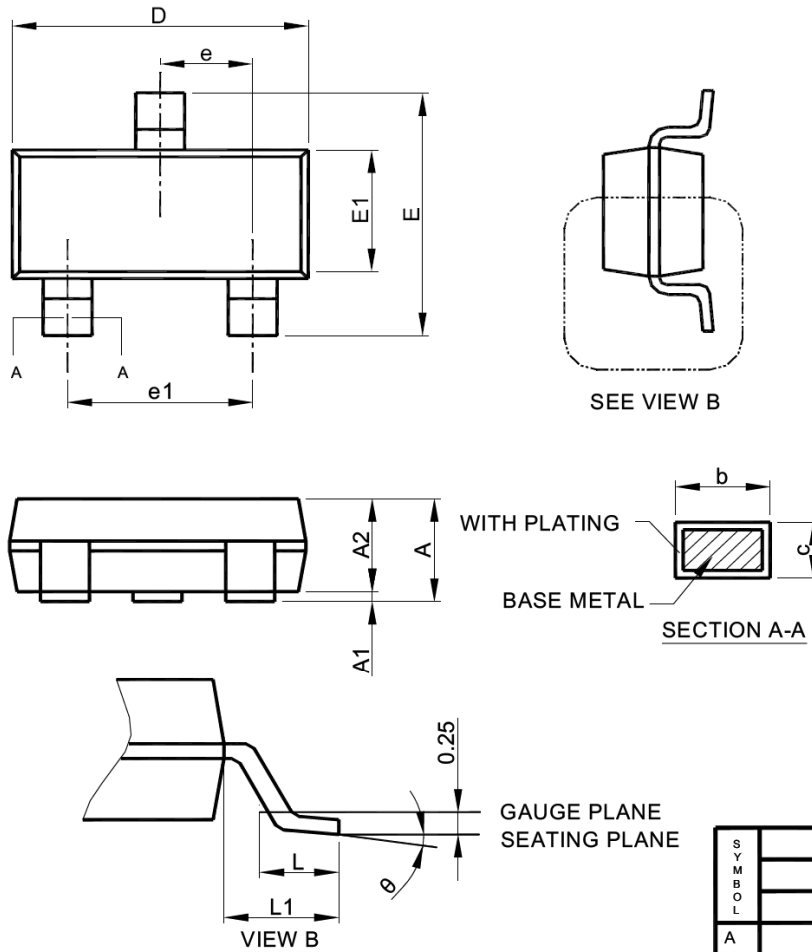


Fig. 10: Test Circuit

**PACKAGE SPECIFICATION**

**3-PIN SOT23**



- Note: 1. Refer to JEDEC MO-178.  
 2. Dimension "D" does not include mold flash, protrusions or gate burrs. Mold flash, protrusion or gate burrs shall not exceed 10 mil per side.  
 3. Dimension "E1" does not include inter-lead flash or protrusions.  
 4. Controlling dimension is millimeter, converted inch dimensions are not necessarily exact.

SYMBOL	SOT-23	
	MILLIMETERS	
	MIN.	MAX.
A	0.95	1.45
A1	0.00	0.15
A2	0.90	1.30
b	0.30	0.50
c	0.08	0.22
D	2.80	3.00
E	2.60	3.00
E1	1.50	1.70
e	0.95 BSC	
e1	1.90 BSC	
L	0.30	0.60
L1	0.60 REF	
θ	0°	8°





# SP809 / SP810

## 3 Pin Microprocessor Supervisor Circuit

### REVISION HISTORY

Revision	Date	Description
2.0.0		Reformat of Datasheet Correction of package drawing

### FOR FURTHER ASSISTANCE

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