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4V Drive Nch+Nch MOSFET SP8K24

Structure

Silicon N-channel MOSFET

Features

- 1) Built-in G-S Protection Diode.
- 2) Small and Surface Mount Package (SOP8).

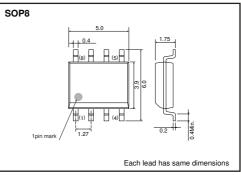
Applications

Power switching , $\ensuremath{\mathsf{DC}}\xspace$ / $\ensuremath{\mathsf{DC}}\xspace$ converter , Inverter

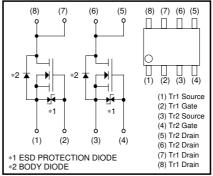
Packaging dimensions

	Package	Taping		
Туре	Code	ТВ		
	Basic ordering unit (pieces)	2500		
SP8K24		0		

•Dimensions (Unit : mm)



Equivalent circuit



A protection diode is included between the gate and the source terminals to protect the diode against static electricity when the product is in use. Use the protection circuit when the fixed voltages are exceeded.

● Absolute maximum ratings (Ta=25°C)

<It is the same ratings for the Tr1 and Tr2.>

Parameter		Symbol	Limits	Unit
Drain-source voltage		V _{DSS}	45	V
Gate-source voltage		V _{GSS}	±20	V
Drain current	Continuous	I _D	±6.0	A
	Pulsed	I _{DP ∗1}	±24	A
Source current (Body diode)	Continuous	ls	1	A
	Pulsed	I _{SP ∗1}	24	А
Total power dissipation		P _D ∗ ₂	2	W / TOTAL
		FD *2	1.4	W / ELEMENT
Chanel temperature		T _{ch}	150	°C
Range of Storage temperature		T _{stg}	-55 to +150	°C

*1 PW ${\leq}10\mu\text{s}$, Duty cycle ${\leq}~1\%$

*2 Mounted on a ceramic board

Transistor

•Electrical characteristics (Ta=25°C)

< It is the same characteristics for the Tr1 and Tr2.>

Parameter	Symbol	Min.	Тур.	Max.	Unit	Conditions
Gate-source leakage	Igss	-	-	±10	μA	$V_{GS}=\pm 20V, V_{DS}=0V$
Drain-source breakdown voltage	V(BR) DSS	45	-	-	V	I _D = 1mA, V _{GS} =0V
Zero gate voltage drain current	IDSS	_	-	1	μA	VDS= 45V, VGS=0V
Gate threshold voltage	V _{GS (th)}	1.0	-	2.5	V	V _{DS} = 10V, I _D = 1mA
	RDS (on)*	-	18	25	mΩ	I _D = 6.0A, V _{GS} = 10V
Static drain-source on-state resistance		-	24	34	mΩ	I _D = 6.0A, V _{GS} = 4.5V
resistance		-	26	37	mΩ	ID= 6.0A, VGS= 4.0V
Forward transfer admittance	Y _{fs} *	6.0	-	-	S	V _{DS} = 10V, I _D = 6.0A
Input capacitance	Ciss	-	1400	-	pF	V _{DS} = 10V
Output capacitance	Coss	-	310	-	pF	V _{GS} =0V
Reverse transfer capacitance	Crss	-	175	-	pF	f=1MHz
Turn-on delay time	td (on) *	-	19	-	ns	VDD≒25V
Rise time	tr *	-	30	-	ns	ID= 3.0A Vgs= 10V
Turn-off delay time	td (off) *	-	72	-	ns	$R_{L} = 8\Omega$
Fall time	tr *	_	27	-	ns	R _G =10Ω
Total gate charge	Qg *	_	15.4	21.6	nC	V _{DD} ≒25V, V _{GS} =5V
Gate-source charge	Q _{gs} *	-	3.7	-	nC	I _D = 6.0A
Gate-drain charge	Q _{gd} *	_	6.5	-	nC	$R_{L}=4\Omega, R_{G}=10\Omega$

*Pulsed

●Body diode characteristics (Source-drain) (Ta=25°C)

< It is the same characteristics for the Tr1 and Tr2.>

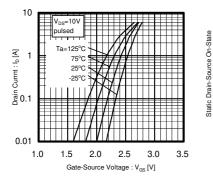
Parameter	Symbol	Min.	Тур.	Max.	Unit	Condition
Forward voltage	V _{SD} *	_	_	1.2	V	I _S =6.0A/V _{GS} =0V

* pulsed

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Transistor

Electrical characteristic curves





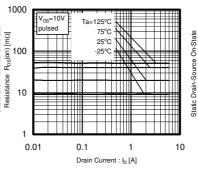


Fig.2 Static Drain-Source On-State Resistance vs. Drain Current (1)

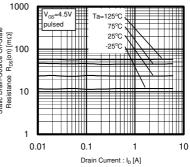


Fig.3 Static Drain-Source On-State Resistance vs. Drain Current (2)

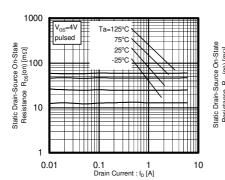


Fig.4 Static Drain-Source On-State Resistance vs. Drain Current (3)

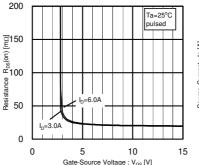
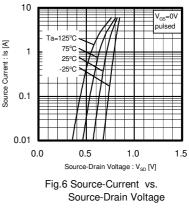
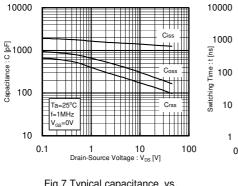
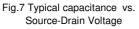
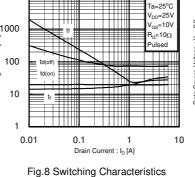


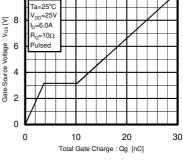
Fig.5 Static Drain-Source On-State Resistance vs. Gate-Source Voltage











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Transistor

Measurement circuits

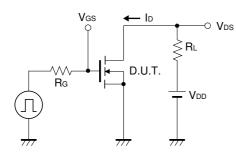


Fig.10 Switching Time Test Circuit

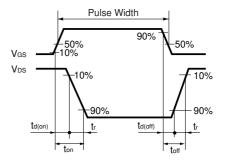


Fig.11 Switching Time Waveforms

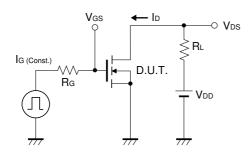
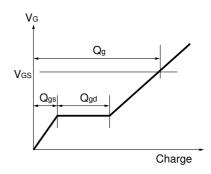


Fig.12 Gate Charge Test Circuit





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Appendix1-Rev2.0

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