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DSP56321

24-Bit Digital Signal Processor

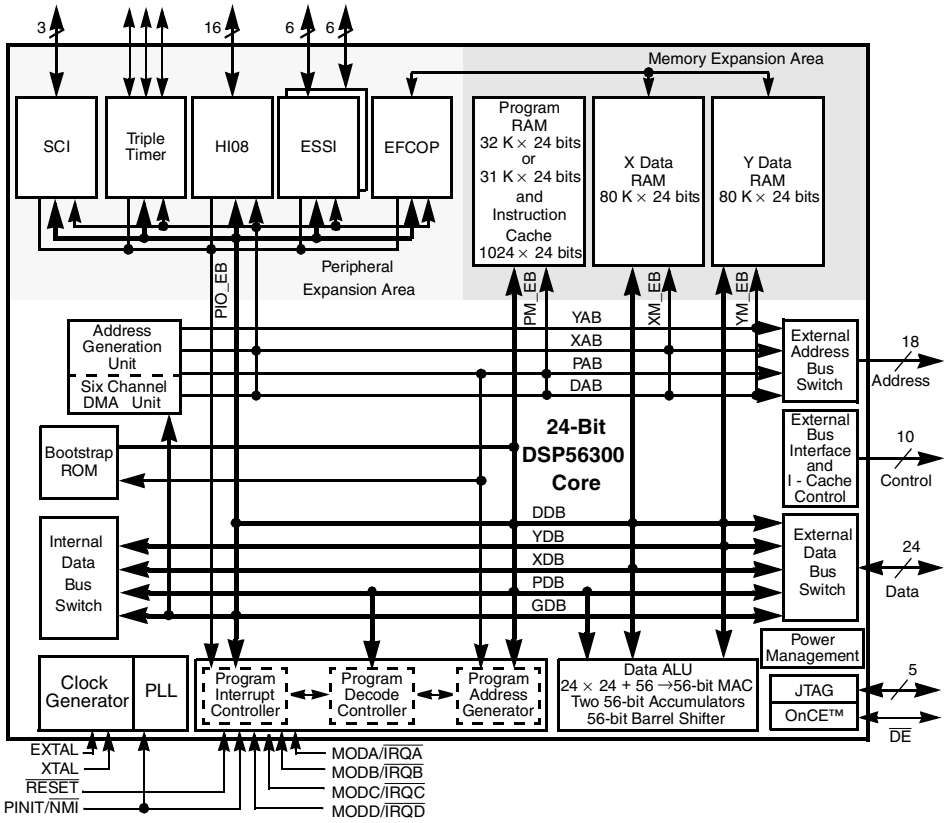


Figure 1. DSP56321 Block Diagram

The DSP56321 is intended for applications requiring a large amount of internal memory, such as networking and wireless infrastructure applications. The onboard EFCOP can accelerate general filtering applications, such as echo-cancellation applications, correlation, and general-purpose convolution-based algorithms.

What's New?

Rev. 11 includes the following changes:

- Adds lead-free packaging and part numbers.

The Freescale DSP56321, a member of the DSP56300 DSP family, supports networking, security encryption, and home entertainment using a high-performance, single-clock-cycle-per- instruction engine (DSP56000 code-compatible), a barrel shifter, 24-bit addressing, an instruction cache, and a direct memory access (DMA) controller (see **Figure 1**).

The DSP56321 offers 275 million multiply- accumulates per second (MMACS) performance, attaining 550 MMACS when the EFCOP is in use. It operates with an internal 275 MHz clock with a 1.6 volt core and independent 3.3 volt input/output (I/O) power. By operating in parallel with the core, the EFCOP provides overall enhanced performance and signal quality with no impact on channel throughput or total channel support. This device is pin-compatible with the Freescale DSP56303, DSP56L307, DSP56309, and DSP56311.

Table of Contents

Data Sheet Conventions

$\overline{\text{OVERBAR}}$	Indicates a signal that is active when pulled low (For example, the $\overline{\text{RESET}}$ pin is active when low.)
“asserted”	Means that a high true (active high) signal is high or that a low true (active low) signal is low
“deasserted”	Means that a high true (active high) signal is low or that a low true (active low) signal is high

Examples:	Signal/Symbol	Logic State	Signal State	Voltage
	$\overline{\text{PIN}}$	True	Asserted	V_{IL}/V_{OL}
	$\overline{\text{PIN}}$	False	Deasserted	V_{IH}/V_{OH}
	PIN	True	Asserted	V_{IH}/V_{OH}
	PIN	False	Deasserted	V_{IL}/V_{OL}

Note: Values for V_{IL}, V_{OL}, V_{IH}, and V_{OH} are defined by individual product specifications.

Features

Table 1 lists the features of the DSP56321 device.

Table 1. DSP56321 Features

Feature	Description
High-Performance DSP56300 Core	• 275 million multiply-accumulates per second (MMACS) (550 MMACS using the EFCOP in filtering applications) with a 275 MHz clock at 1.6 V core and 3.3 V I/O • Object code compatible with the DSP56000 core with highly parallel instruction set • Data arithmetic logic unit (Data ALU) with fully pipelined 24 × 24-bit parallel Multiplier-Accumulator (MAC), 56-bit parallel barrel shifter (fast shift and normalization; bit stream generation and parsing), conditional ALU instructions, and 24-bit or 16-bit arithmetic support under software control • Program control unit (PCU) with position independent code (PIC) support, addressing modes optimized for DSP applications (including immediate offsets), internal instruction cache controller, internal memory-expandable hardware stack, nested hardware DO loops, and fast auto-return interrupts • Direct memory access (DMA) with six DMA channels supporting internal and external accesses; one-, two-, and three-dimensional transfers (including circular buffering); end-of-block-transfer interrupts; and triggering from interrupt lines and all peripherals • Phase-lock loop (PLL) allows change of low-power divide factor (DF) without loss of lock and output clock with skew elimination • Hardware debugging support including on-chip emulation (OnCE) module, Joint Test Action Group (JTAG) test access port (TAP)

Enhanced Filter Coprocessor (EFCOP)	• Internal 24 × 24-bit filtering and echo-cancellation coprocessor that runs in parallel to the DSP core
	• Operation at the same frequency as the core (up to 275 MHz)
	• Support for a variety of filter modes, some of which are optimized for cellular base station applications:
	  • Real finite impulse response (FIR) with real taps
	  • Complex FIR with complex taps
	  • Complex FIR generating pure real or pure imaginary outputs alternately
	  • A 4-bit decimation factor in FIR filters, thus providing a decimation ratio up to 16
	  • Direct form 1 (DFI) Infinite Impulse Response (IIR) filter
	  • Direct form 2 (DFII) IIR filter
	  • Four scaling factors (1, 4, 8, 16) for IIR output
	  • Adaptive FIR filter with true least mean square (LMS) coefficient updates
	  • Adaptive FIR filter with delayed LMS coefficient updates

Internal Peripherals	• Enhanced 8-bit parallel host interface (HI08) supports a variety of buses (for example, ISA) and provides glueless connection to a number of industry-standard microcomputers, microprocessors, and DSPs • Two enhanced synchronous serial interfaces (ESSI), each with one receiver and three transmitters (allows six-channel home theater) • Serial communications interface (SCI) with baud rate generator • Triple timer module • Up to 34 programmable general-purpose input/output (GPIO) pins, depending on which peripherals are enabled

Table 1. DSP56321 Features (Continued)

<table>
<tr><th>Feature</th><th>Description</th></tr>
<tr><td>Internal Memories</td><td>
• 192 × 24-bit bootstrap ROM
• 192 K × 24-bit RAM total
• Program RAM, instruction cache, X data RAM, and Y data RAM sizes are programmable:
<table>
<tr><th>Program RAM Size</th><th>Instruction Cache Size</th><th>X Data RAM Size*</th><th>Y Data RAM Size*</th><th>Instruction Cache</th><th>MSW2</th><th>MSW1</th><th>MSW0</th></tr>
<tr><td>32 K × 24-bit</td><td>0</td><td>80 K × 24-bit</td><td>80 K × 24-bit</td><td>disabled</td><td>0</td><td>0</td><td>0</td></tr>
<tr><td>31 K × 24-bit</td><td>1024 × 24-bit</td><td>80 K × 24-bit</td><td>80 K × 24-bit</td><td>enabled</td><td>0</td><td>0</td><td>0</td></tr>
<tr><td>40 K × 24-bit</td><td>0</td><td>76 K × 24-bit</td><td>76 K × 24-bit</td><td>disabled</td><td>0</td><td>0</td><td>1</td></tr>
<tr><td>39 K × 24-bit</td><td>1024 × 24-bit</td><td>76 K × 24-bit</td><td>76 K × 24-bit</td><td>enabled</td><td>0</td><td>0</td><td>1</td></tr>
<tr><td>48 K × 24-bit</td><td>0</td><td>72 K × 24-bit</td><td>72 K × 24-bit</td><td>disabled</td><td>0</td><td>1</td><td>0</td></tr>
<tr><td>47 K × 24-bit</td><td>1024 × 24-bit</td><td>72 K × 24-bit</td><td>72 K × 24-bit</td><td>enabled</td><td>0</td><td>1</td><td>0</td></tr>
<tr><td>64 K × 24-bit</td><td>0</td><td>64 K × 24-bit</td><td>64 K × 24-bit</td><td>disabled</td><td>0</td><td>1</td><td>1</td></tr>
<tr><td>63 K × 24-bit</td><td>1024 × 24-bit</td><td>64 K × 24-bit</td><td>64 K × 24-bit</td><td>enabled</td><td>0</td><td>1</td><td>1</td></tr>
<tr><td>72 K × 24-bit</td><td>0</td><td>60 K × 24-bit</td><td>60 K × 24-bit</td><td>disabled</td><td>1</td><td>0</td><td>0</td></tr>
<tr><td>71 K × 24-bit</td><td>1024 × 24-bit</td><td>60 K × 24-bit</td><td>60 K × 24-bit</td><td>enabled</td><td>1</td><td>0</td><td>0</td></tr>
<tr><td>80 K × 24-bit</td><td>0</td><td>56 K × 24-bit</td><td>56 K × 24-bit</td><td>disabled</td><td>1</td><td>0</td><td>1</td></tr>
<tr><td>79 K × 24-bit</td><td>1024 × 24-bit</td><td>56 K × 24-bit</td><td>56 K × 24-bit</td><td>enabled</td><td>1</td><td>0</td><td>1</td></tr>
<tr><td>96 K × 24-bit</td><td>0</td><td>48 K × 24-bit</td><td>48 K × 24-bit</td><td>disabled</td><td>1</td><td>1</td><td>0</td></tr>
<tr><td>95 K × 24-bit</td><td>1024 × 24-bit</td><td>48 K × 24-bit</td><td>48 K × 24-bit</td><td>enabled</td><td>1</td><td>1</td><td>0</td></tr>
<tr><td>112 K × 24-bit</td><td>0</td><td>40 K × 24-bit</td><td>40 K × 24-bit</td><td>disabled</td><td>1</td><td>1</td><td>1</td></tr>
<tr><td>111 K × 24-bit</td><td>1024 × 24-bit</td><td>40 K × 24-bit</td><td>40 K × 24-bit</td><td>enabled</td><td>1</td><td>1</td><td>1</td></tr>
<tr><td colspan="8">*Includes 12 K × 24-bit shared memory (that is, 24 K total memory shared by the core and the EFCOP)</td></tr>
</table>
</td></tr>
<tr><td>External Memory Expansion</td><td>
• Data memory expansion to two 256 K × 24-bit word memory spaces using the standard external address lines
• Program memory expansion to one 256 K × 24-bit words memory space using the standard external address lines
• External memory expansion port
• Chip select logic for glueless interface to static random access memory (SRAMs)
</td></tr>
<tr><td>Power Dissipation</td><td>
• Very low-power CMOS design
• Wait and Stop low-power standby modes
• Fully static design specified to operate down to 0 Hz (dc)
• Optimized power management circuitry (instruction-dependent, peripheral-dependent, and mode-dependent)
</td></tr>
<tr><td>Packaging</td><td>
• Molded array plastic-ball grid array (MAP-BGA) package in lead-free or lead-bearing versions.
</td></tr>
</table>

Target Applications

DSP56321 applications require high performance, low power, small packaging, and a large amount of internal memory. The EFCOP can accelerate general filtering applications. Examples include:

- Wireless and wireline infrastructure applications
- Multi-channel wireless local loop systems
- Security encryption systems
- Home entertainment systems
- DSP resource boards
- High-speed modem banks
- IP telephony

Product Documentation

The documents listed in **Table 2** are required for a complete description of the DSP56321 device and are necessary to design properly with the part. Documentation is available from a local Freescale distributor, a Freescale semiconductor sales office, or a Freescale Semiconductor Literature Distribution Center. For documentation updates, visit the Freescale DSP website. See the contact information on the back cover of this document.

Table 2. DSP56321 Documentation

Name	Description	Order Number
DSP56321 Reference Manual	Detailed functional description of the DSP56321 memory configuration, operation, and register programming	DSP56321RM
DSP56300 Family Manual	Detailed description of the DSP56300 family processor core and instruction set	DSP56300FM
Application Notes	Documents describing specific applications or optimized device operation including code examples	See the DSP56321 product website

Signals/Connections 1

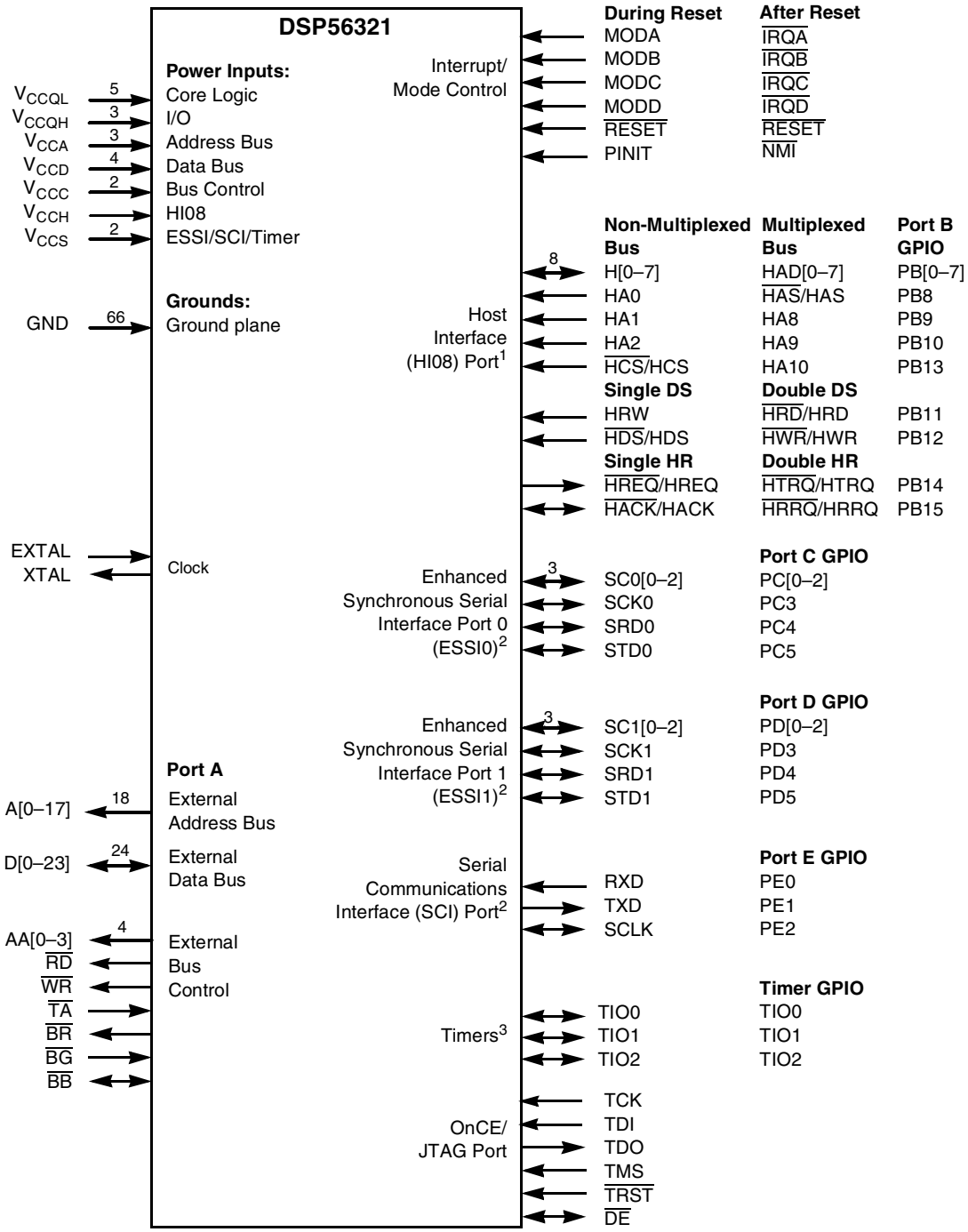
The DSP56321 input and output signals are organized into functional groups as shown in **Table 1-1**. **Figure 1-1** diagrams the DSP56321 signals by functional group. The remainder of this chapter describes the signal pins in each functional group.

Table 1-1. DSP56321 Functional Signal Groupings

Functional Group		Number of Signals
Power (V_{CC})		20
Ground (GND)		66
Clock		2
Address bus	Port A[1]	18
Data bus		24
Bus control		10
Interrupt and mode control		6
Host interface (HI08)	Port B[2]	16
Enhanced synchronous serial interface (ESSI)	Ports C and D[3]	12
Serial communication interface (SCI)	Port E[4]	3
Timer		3
OnCE/JTAG Port		6

Notes:
1. Port A signals define the external memory interface port, including the external address bus, data bus, and control signals.
2. Port B signals are the HI08 port signals multiplexed with the GPIO signals.
3. Port C and D signals are the two ESSI port signals multiplexed with the GPIO signals.
4. Port E signals are the SCI port signals multiplexed with the GPIO signals.
5. Eight signal lines are not connected internally. These are designated as no connect (NC) in the package description (see **Chapter 3**). There are also two reserved lines.

Note: This chapter refers to a number of configuration registers used to select individual multiplexed signal functionality. See the *DSP56321 Reference Manual* for details on these configuration registers.



Notes:
1. The HI08 port supports a non-multiplexed or a multiplexed bus, single or double data strobe (DS), and single or double host request (HR) configurations. Since each of these modes is configured independently, any combination of these modes is possible. These HI08 signals can also be configured alternatively as GPIO signals (PB[0–15]). Signals with dual designations (for example, HAS/HAS) have configurable polarity.
2. The ESSI0, ESSI1, and SCI signals are multiplexed with the Port C GPIO signals (PC[0–5]), Port D GPIO signals (PD[0–5]), and Port E GPIO signals (PE[0–2]), respectively.
3. TIO[0–2] can be configured as GPIO signals.

Figure 1-1. Signals Identified by Functional Group

1.1 Power

Table 1-2. Power Inputs

Power Name	Description
V_{CCQL}	**Quiet Core (Low) Power**—An isolated power for the core processing and clock logic. This input must be isolated externally from all other chip power inputs.
V_{CCQH}	**Quiet External (High) Power**—A quiet power source for I/O lines. This input must be tied externally to all other chip power inputs, *except* V_{CCQL}.
V_{CCA}	**Address Bus Power**—An isolated power for sections of the address bus I/O drivers. This input must be tied externally to all other chip power inputs, *except* V_{CCQL}.
V_{CCD}	**Data Bus Power**—An isolated power for sections of the data bus I/O drivers. This input must be tied externally to all other chip power inputs, *except* V_{CCQL}.
V_{CCC}	**Bus Control Power**—An isolated power for the bus control I/O drivers. This input must be tied externally to all other chip power inputs, *except* V_{CCQL}.
V_{CCH}	**Host Power**—An isolated power for the HI08 I/O drivers. This input must be tied externally to all other chip power inputs, *except* V_{CCQL}.
V_{CCS}	**ESSI, SCI, and Timer Power**—An isolated power for the ESSI, SCI, and timer I/O drivers. This input must be tied externally to all other chip power inputs, *except* V_{CCQL}.
Note: The user must provide adequate external decoupling capacitors for all power connections.	

1.2 Ground

Table 1-3. Grounds

Name	Description
GND	**Ground**—Connected to an internal device ground plane.
Note: The user must provide adequate external decoupling capacitors for all GND connections.	

1.3 Clock

Table 1-4. Clock Signals

Signal Name	Type	State During Reset	Signal Description
EXTAL	Input	Input	**External Clock/Crystal Input**—Interfaces the internal crystal oscillator input to an external crystal or an external clock.
XTAL	Output	Chip-driven	**Crystal Output**—Connects the internal crystal oscillator output to an external crystal. If an external clock is used, leave XTAL unconnected.

1.4 External Memory Expansion Port (Port A)

Note: When the DSP56321 enters a low-power standby mode (stop or wait), it releases bus mastership and tri-states the relevant Port A signals: A[0–17], D[0–23], AA[0–3], $\overline{RD}$, $\overline{WR}$, $\overline{BB}$.

1.4.1 External Address Bus

Table 1-5. External Address Bus Signals

Signal Name	Type	State During Reset, Stop, or Wait	Signal Description
A[0–17]	Output	Tri-stated	**Address Bus**—When the DSP is the bus master, A[0–17] are active-high outputs that specify the address for external program and data memory accesses. Otherwise, the signals are tri-stated. To minimize power dissipation, A[0–17] do not change state when external memory spaces are not being accessed.

1.4.2 External Data Bus

Table 1-6. External Data Bus Signals

Signal Name	Type	State During Reset	State During Stop or Wait	Signal Description
D[0–23]	Input/ Output	Ignored Input	Last state: *Input*: Ignored *Output*: Last value	**Data Bus**—When the DSP is the bus master, D[0–23] are active-high, bidirectional input/outputs that provide the bidirectional data bus for external program and data memory accesses. Otherwise, D[0–23] drivers are tri-stated. If the last state is output, these lines have weak keepers to maintain the last output state if all drivers are tri-stated.

1.4.3 External Bus Control

Table 1-7. External Bus Control Signals

Signal Name	Type	State During Reset, Stop, or Wait	Signal Description
AA[0–3]	Output	Tri-stated	**Address Attribute**—When defined as AA, these signals can be used as chip selects or additional address lines. The default use defines a priority scheme under which only one AA signal can be asserted at a time. Setting the AA priority disable (APD) bit (Bit 14) of the Operating Mode Register, the priority mechanism is disabled and the lines can be used together as four external lines that can be decoded externally into 16 chip select signals.
$\overline{RD}$	Output	Tri-stated	**Read Enable**—When the DSP is the bus master, $\overline{RD}$ is an active-low output that is asserted to read external memory on the data bus (D[0–23]). Otherwise, $\overline{RD}$ is tri-stated.
$\overline{WR}$	Output	Tri-stated	**Write Enable**—When the DSP is the bus master, $\overline{WR}$ is an active-low output that is asserted to write external memory on the data bus (D[0–23]). Otherwise, the signals are tri-stated.

Table 1-7. External Bus Control Signals (Continued)

Signal Name	Type	State During Reset, Stop, or Wait	Signal Description
$\overline{TA}$	Input	Ignored Input	**Transfer Acknowledge**—If the DSP56321 is the bus master and there is no external bus activity, or the DSP56321 is not the bus master, the $\overline{TA}$ input is ignored. The $\overline{TA}$ input is a data transfer acknowledge (DTACK) function that can extend an external bus cycle indefinitely. Any number of wait states (1, 2. . .infinity) can be added to the wait states inserted by the bus control register (BCR) by keeping $\overline{TA}$ deasserted. In typical operation, $\overline{TA}$ is deasserted at the start of a bus cycle, is asserted to enable completion of the bus cycle, and is deasserted before the next bus cycle. The current bus cycle completes one clock period after $\overline{TA}$ is asserted synchronous to CLKOUT. The number of wait states is determined by the $\overline{TA}$ input or by the BCR, whichever is longer. The BCR can be used to set the minimum number of wait states in external bus cycles. To use the $\overline{TA}$ functionality, the BCR must be programmed to at least one wait state. A zero wait state access cannot be extended by $\overline{TA}$ deassertion; otherwise, improper operation may result.
$\overline{BR}$	Output	Reset: Output (deasserted) State during Stop/Wait depends on BRH bit setting: • BRH = 0: Output (deasserted) • BRH = 1: Maintains last state (that is, if asserted, remains asserted)	**Bus Request**—Asserted when the DSP requests bus mastership. $\overline{BR}$ is deasserted when the DSP no longer needs the bus. $\overline{BR}$ may be asserted or deasserted independently of whether the DSP56321 is a bus master or a bus slave. Bus “parking” allows $\overline{BR}$ to be deasserted even though the DSP56321 is the bus master. (See the description of bus “parking” in the $\overline{BB}$ signal description.) The bus request hold (BRH) bit in the BCR allows $\overline{BR}$ to be asserted under software control even though the DSP does not need the bus. $\overline{BR}$ is typically sent to an external bus arbitrator that controls the priority, parking, and tenure of each master on the same external bus. $\overline{BR}$ is affected only by DSP requests for the external bus, never for the internal bus. During hardware reset, $\overline{BR}$ is deasserted and the arbitration is reset to the bus slave state.
$\overline{BG}$	Input	Ignored Input	**Bus Grant**—Asserted by an external bus arbitration circuit when the DSP56321 becomes the next bus master. When $\overline{BG}$ is asserted, the DSP56321 must wait until $\overline{BB}$ is deasserted before taking bus mastership. When $\overline{BG}$ is deasserted, bus mastership is typically given up at the end of the current bus cycle. This may occur in the middle of an instruction that requires more than one external bus cycle for execution. To ensure proper operation, the user must set the asynchronous bus arbitration enable (ABE) bit (Bit 13) in the Operating Mode Register. When this bit is set, $\overline{BG}$ and $\overline{BB}$ are synchronized internally. This adds a required delay between the deassertion of an initial $\overline{BG}$ input and the assertion of a subsequent $\overline{BG}$ input.
$\overline{BB}$	Input/ Output	Ignored Input	**Bus Busy**—Indicates that the bus is active. Only after $\overline{BB}$ is deasserted can the pending bus master become the bus master (and then assert the signal again). The bus master may keep $\overline{BB}$ asserted after ceasing bus activity regardless of whether $\overline{BR}$ is asserted or deasserted. Called “bus parking,” this allows the current bus master to reuse the bus without rearbitration until another device requires the bus. $\overline{BB}$ is deasserted by an “active pull-up” method (that is, $\overline{BB}$ is driven high and then released and held high by an external pull-up resistor). **Notes:** **1.** See $\overline{BG}$ for additional information. **2.** $\overline{BB}$ requires an external pull-up resistor.

1.5 Interrupt and Mode Control

The interrupt and mode control signals select the chip operating mode as it comes out of hardware reset. After $\overline{\text{RESET}}$ is deasserted, these inputs are hardware interrupt request lines.

Table 1-8. Interrupt and Mode Control

Signal Name	Type	State During Reset	Signal Description
MODA	Input	Schmitt-trigger Input	**Mode Select A**—MODA, MODB, MODC, and MODD select one of 16 initial chip operating modes, latched into the Operating Mode Register when the $\overline{\text{RESET}}$ signal is deasserted.
$\overline{\text{IRQA}}$	Input		**External Interrupt Request A**—After reset, this input becomes a level-sensitive or negative-edge-triggered, maskable interrupt request input during normal instruction processing. If the processor is in the STOP or WAIT standby state and $\overline{\text{IRQA}}$ is asserted, the processor exits the STOP or WAIT state.
MODB	Input	Schmitt-trigger Input	**Mode Select B**—MODA, MODB, MODC, and MODD select one of 16 initial chip operating modes, latched into the Operating Mode Register when the $\overline{\text{RESET}}$ signal is deasserted.
$\overline{\text{IRQB}}$	Input		**External Interrupt Request B**—After reset, this input becomes a level-sensitive or negative-edge-triggered, maskable interrupt request input during normal instruction processing. If the processor is in the WAIT standby state and $\overline{\text{IRQB}}$ is asserted, the processor exits the WAIT state.
MODC	Input	Schmitt-trigger Input	**Mode Select C**—MODA, MODB, MODC, and MODD select one of 16 initial chip operating modes, latched into the Operating Mode Register when the $\overline{\text{RESET}}$ signal is deasserted.
$\overline{\text{IRQC}}$	Input		**External Interrupt Request C**—After reset, this input becomes a level-sensitive or negative-edge-triggered, maskable interrupt request input during normal instruction processing. If the processor is in the WAIT standby state and $\overline{\text{IRQC}}$ is asserted, the processor exits the WAIT state.
MODD	Input	Schmitt-trigger Input	**Mode Select D**—MODA, MODB, MODC, and MODD select one of 16 initial chip operating modes, latched into the Operating Mode Register when the $\overline{\text{RESET}}$ signal is deasserted.
$\overline{\text{IRQD}}$	Input		**External Interrupt Request D**—After reset, this input becomes a level-sensitive or negative-edge-triggered, maskable interrupt request input during normal instruction processing. If the processor is in the WAIT standby state and $\overline{\text{IRQD}}$ is asserted, the processor exits the WAIT state.
$\overline{\text{RESET}}$	Input	Schmitt-trigger Input	**Reset**—Places the chip in the Reset state and resets the internal phase generator. The Schmitt-trigger input allows a slowly rising input (such as a capacitor charging) to reset the chip reliably. When the $\overline{\text{RESET}}$ signal is deasserted, the initial chip operating mode is latched from the MODA, MODB, MODC, and MODD inputs. The $\overline{\text{RESET}}$ signal must be asserted after powerup.
PINIT	Input	Schmitt-trigger Input	**PLL Initial**—During assertion of $\overline{\text{RESET}}$, the value of PINIT determines whether the DPLL is enabled or disabled.
$\overline{\text{NMI}}$	Input		**Nonmaskable Interrupt**—After $\overline{\text{RESET}}$ deassertion and during normal instruction processing, this Schmitt-trigger input is the negative-edge-triggered $\overline{\text{NMI}}$ request.

1.6 Host Interface (HI08)

The HI08 provides a fast, 8-bit, parallel data port that connects directly to the host bus. The HI08 supports a variety of standard buses and connects directly to a number of industry-standard microcomputers, microprocessors, DSPs, and DMA hardware.

1.6.1 Host Port Usage Considerations

Careful synchronization is required when the system reads multiple-bit registers that are written by another asynchronous system. This is a common problem when two asynchronous systems are connected (as they are in the Host port). The considerations for proper operation are discussed in **Table 1-9**.

Table 1-9. Host Port Usage Considerations

Action	Description
Asynchronous read of receive byte registers	When reading the receive byte registers, Receive register High (RXH), Receive register Middle (RXM), or Receive register Low (RXL), the host interface programmer should use interrupts or poll the Receive register Data Full (RXDF) flag that indicates data is available. This assures that the data in the receive byte registers is valid.
Asynchronous write to transmit byte registers	The host interface programmer should not write to the transmit byte registers, Transmit register High (TXH), Transmit register Middle (TXM), or Transmit register Low (TXL), unless the Transmit register Data Empty (TXDE) bit is set indicating that the transmit byte registers are empty. This guarantees that the transmit byte registers transfer valid data to the Host Receive (HRX) register.
Asynchronous write to host vector	The host interface programmer must change the Host Vector (HV) register only when the Host Command bit (HC) is clear. This practice guarantees that the DSP interrupt control logic receives a stable vector.

1.6.2 Host Port Configuration

HI08 signal functions vary according to the programmed configuration of the interface as determined by the 16 bits in the HI08 Port Control Register.

Table 1-10. Host Interface

Signal Name	Type	State During Reset[1,2]	Signal Description
H[0–7]	Input/Output	Ignored Input	**Host Data—**When the HI08 is programmed to interface with a non-multiplexed host bus and the HI function is selected, these signals are lines 0–7 of the bidirectional Data bus.
HAD[0–7]	Input/Output		**Host Address—**When the HI08 is programmed to interface with a multiplexed host bus and the HI function is selected, these signals are lines 0–7 of the bidirectional multiplexed Address/Data bus.
PB[0–7]	Input or Output		**Port B 0–7—**When the HI08 is configured as GPIO through the HI08 Port Control Register, these signals are individually programmed as inputs or outputs through the HI08 Data Direction Register.

Table 1-10. Host Interface (Continued)

Signal Name	Type	State During Reset[1,2]	Signal Description
HA0	Input	Ignored Input	**Host Address Input 0**—When the HI08 is programmed to interface with a nonmultiplexed host bus and the HI function is selected, this signal is line 0 of the host address input bus.
$\overline{\text{HAS}}$/HAS	Input		**Host Address Strobe—**When the HI08 is programmed to interface with a multiplexed host bus and the HI function is selected, this signal is the host address strobe (HAS) Schmitt-trigger input. The polarity of the address strobe is programmable but is configured active-low ($\overline{\text{HAS}}$) following reset.
PB8	Input or Output		**Port B 8**—When the HI08 is configured as GPIO through the HI08 Port Control Register, this signal is individually programmed as an input or output through the HI08 Data Direction Register.
HA1	Input	Ignored Input	**Host Address Input 1**—When the HI08 is programmed to interface with a nonmultiplexed host bus and the HI function is selected, this signal is line 1 of the host address (HA1) input bus.
HA8	Input		**Host Address 8**—When the HI08 is programmed to interface with a multiplexed host bus and the HI function is selected, this signal is line 8 of the host address (HA8) input bus.
PB9	Input or Output		**Port B 9**—When the HI08 is configured as GPIO through the HI08 Port Control Register, this signal is individually programmed as an input or output through the HI08 Data Direction Register.
HA2	Input	Ignored Input	**Host Address Input 2**—When the HI08 is programmed to interface with a nonmultiplexed host bus and the HI function is selected, this signal is line 2 of the host address (HA2) input bus.
HA9	Input		**Host Address 9**—When the HI08 is programmed to interface with a multiplexed host bus and the HI function is selected, this signal is line 9 of the host address (HA9) input bus.
PB10	Input or Output		**Port B 10**—When the HI08 is configured as GPIO through the HI08 Port Control Register, this signal is individually programmed as an input or output through the HI08 Data Direction Register.
$\overline{\text{HCS}}$/HCS	Input	Ignored Input	**Host Chip Select**—When the HI08 is programmed to interface with a nonmultiplexed host bus and the HI function is selected, this signal is the host chip select (HCS) input. The polarity of the chip select is programmable but is configured active-low ($\overline{\text{HCS}}$) after reset.
HA10	Input		**Host Address 10**—When the HI08 is programmed to interface with a multiplexed host bus and the HI function is selected, this signal is line 10 of the host address (HA10) input bus.
PB13	Input or Output		**Port B 13**—When the HI08 is configured as GPIO through the HI08 Port Control Register, this signal is individually programmed as an input or output through the HI08 Data Direction Register.
HRW	Input	Ignored Input	**Host Read/Write**—When the HI08 is programmed to interface with a single-data-strobe host bus and the HI function is selected, this signal is the Host Read/$\overline{\text{Write}}$ (HRW) input.
$\overline{\text{HRD}}$/HRD	Input		**Host Read Data**—When the HI08 is programmed to interface with a double-data-strobe host bus and the HI function is selected, this signal is the HRD strobe Schmitt-trigger input. The polarity of the data strobe is programmable but is configured as active-low ($\overline{\text{HRD}}$) after reset.
PB11	Input or Output		**Port B 11**—When the HI08 is configured as GPIO through the HI08 Port Control Register, this signal is individually programmed as an input or output through the HI08 Data Direction Register.

Table 1-10. Host Interface (Continued)

Signal Name	Type	State During Reset[1,2]	Signal Description
$\overline{\text{HDS}}$/HDS	Input	Ignored Input	**Host Data Strobe**—When the HI08 is programmed to interface with a single-data-strobe host bus and the HI function is selected, this signal is the host data strobe (HDS) Schmitt-trigger input. The polarity of the data strobe is programmable but is configured as active-low ($\overline{\text{HDS}}$) following reset.
$\overline{\text{HWR}}$/HWR	Input		**Host Write Data**—When the HI08 is programmed to interface with a double-data-strobe host bus and the HI function is selected, this signal is the host write data strobe (HWR) Schmitt-trigger input. The polarity of the data strobe is programmable but is configured as active-low ($\overline{\text{HWR}}$) following reset.
PB12	Input or Output		**Port B 12**—When the HI08 is configured as GPIO through the HI08 Port Control Register, this signal is individually programmed as an input or output through the HI08 Data Direction Register.
$\overline{\text{HREQ}}$/HREQ	Output	Ignored Input	**Host Request**—When the HI08 is programmed to interface with a single host request host bus and the HI function is selected, this signal is the host request (HREQ) output. The polarity of the host request is programmable but is configured as active-low ($\overline{\text{HREQ}}$) following reset. The host request may be programmed as a driven or open-drain output.
$\overline{\text{HTRQ}}$/HTRQ	Output		**Transmit Host Request**—When the HI08 is programmed to interface with a double host request host bus and the HI function is selected, this signal is the transmit host request (HTRQ) output. The polarity of the host request is programmable but is configured as active-low ($\overline{\text{HTRQ}}$) following reset. The host request may be programmed as a driven or open-drain output.
PB14	Input or Output		**Port B 14**—When the HI08 is configured as GPIO through the HI08 Port Control Register, this signal is individually programmed as an input or output through the HI08 Data Direction Register.
$\overline{\text{HACK}}$/HACK	Input	Ignored Input	**Host Acknowledge**—When the HI08 is programmed to interface with a single host request host bus and the HI function is selected, this signal is the host acknowledge (HACK) Schmitt-trigger input. The polarity of the host acknowledge is programmable but is configured as active-low ($\overline{\text{HACK}}$) after reset.
$\overline{\text{HRRQ}}$/HRRQ	Output		**Receive Host Request**—When the HI08 is programmed to interface with a double host request host bus and the HI function is selected, this signal is the receive host request (HRRQ) output. The polarity of the host request is programmable but is configured as active-low ($\overline{\text{HRRQ}}$) after reset. The host request may be programmed as a driven or open-drain output.
PB15	Input or Output		**Port B 15**—When the HI08 is configured as GPIO through the HI08 Port Control Register, this signal is individually programmed as an input or output through the HI08 Data Direction Register.

Notes: 1. In the Stop state, the signal maintains the last state as follows:
- If the last state is input, the signal is an ignored input.
- If the last state is output, these lines have weak keepers that maintain the last output state even if the drivers are tri-stated.

2. The Wait processing state does not affect the signal state.

1.7 Enhanced Synchronous Serial Interface 0 (ESSI0)

Two synchronous serial interfaces (ESSI0 and ESSI1) provide a full-duplex serial port for serial communication with a variety of serial devices, including one or more industry-standard codecs, other DSPs, microprocessors, and peripherals that implement the Freescale serial peripheral interface (SPI).

Table 1-11. Enhanced Synchronous Serial Interface 0

Signal Name	Type	State During Reset[1,2]	Signal Description
SC00	Input or Output	Ignored Input	**Serial Control 0**—For asynchronous mode, this signal is used for the receive clock I/O (Schmitt-trigger input). For synchronous mode, this signal is used either for transmitter 1 output or for serial I/O flag 0.
PC0	Input or Output		**Port C 0**—The default configuration following reset is GPIO input PC0. When configured as PC0, signal direction is controlled through the Port C Direction Register. The signal can be configured as ESSI signal SC00 through the Port C Control Register.
SC01	Input/Output	Ignored Input	**Serial Control 1**—For asynchronous mode, this signal is the receiver frame sync I/O. For synchronous mode, this signal is used either for transmitter 2 output or for serial I/O flag 1.
PC1	Input or Output		**Port C 1**—The default configuration following reset is GPIO input PC1. When configured as PC1, signal direction is controlled through the Port C Direction Register. The signal can be configured as an ESSI signal SC01 through the Port C Control Register.
SC02	Input/Output	Ignored Input	**Serial Control Signal 2**—The frame sync for both the transmitter and receiver in synchronous mode, and for the transmitter only in asynchronous mode. When configured as an output, this signal is the internally generated frame sync signal. When configured as an input, this signal receives an external frame sync signal for the transmitter (and the receiver in synchronous operation).
PC2	Input or Output		**Port C 2**—The default configuration following reset is GPIO input PC2. When configured as PC2, signal direction is controlled through the Port C Direction Register. The signal can be configured as an ESSI signal SC02 through the Port C Control Register.
SCK0	Input/Output	Ignored Input	**Serial Clock**—Provides the serial bit rate clock for the ESSI. The SCK0 is a clock input or output, used by both the transmitter and receiver in synchronous modes or by the transmitter in asynchronous modes. Although an external serial clock can be independent of and asynchronous to the DSP system clock, it must exceed the minimum clock cycle time of 6T (that is, the system clock frequency must be at least three times the external ESSI clock frequency). The ESSI needs at least three DSP phases inside each half of the serial clock.
PC3	Input or Output		**Port C 3**—The default configuration following reset is GPIO input PC3. When configured as PC3, signal direction is controlled through the Port C Direction Register. The signal can be configured as an ESSI signal SCK0 through the Port C Control Register.
SRD0	Input	Ignored Input	**Serial Receive Data**—Receives serial data and transfers the data to the ESSI Receive Shift Register. SRD0 is an input when data is received.
PC4	Input or Output		**Port C 4**—The default configuration following reset is GPIO input PC4. When configured as PC4, signal direction is controlled through the Port C Direction Register. The signal can be configured as an ESSI signal SRD0 through the Port C Control Register.

Table 1-11. Enhanced Synchronous Serial Interface 0 (Continued)

Signal Name	Type	State During Reset[1,2]	Signal Description
STD0	Output	Ignored Input	**Serial Transmit Data**—Transmits data from the Serial Transmit Shift Register. STD0 is an output when data is transmitted.
PC5	Input or Output		**Port C 5**—The default configuration following reset is GPIO input PC5. When configured as PC5, signal direction is controlled through the Port C Direction Register. The signal can be configured as an ESSI signal STD0 through the Port C Control Register.

Notes: 1. In the Stop state, the signal maintains the last state as follows:
- If the last state is input, the signal is an ignored input.
- If the last state is output, these lines have weak keepers that maintain the last output state even if the drivers are tri-stated.

2. The Wait processing state does not affect the signal state.

1.8 Enhanced Synchronous Serial Interface 1 (ESSI1)

Table 1-12. Enhanced Serial Synchronous Interface 1

Signal Name	Type	State During Reset[1,2]	Signal Description
SC10	Input or Output	Ignored Input	**Serial Control 0**—For asynchronous mode, this signal is used for the receive clock I/O (Schmitt-trigger input). For synchronous mode, this signal is used either for transmitter 1 output or for serial I/O flag 0.
PD0	Input or Output		**Port D 0**—The default configuration following reset is GPIO input PD0. When configured as PD0, signal direction is controlled through the Port D Direction Register. The signal can be configured as an ESSI signal SC10 through the Port D Control Register.
SC11	Input/Output	Ignored Input	**Serial Control 1**—For asynchronous mode, this signal is the receiver frame sync I/O. For synchronous mode, this signal is used either for Transmitter 2 output or for Serial I/O Flag 1.
PD1	Input or Output		**Port D 1**—The default configuration following reset is GPIO input PD1. When configured as PD1, signal direction is controlled through the Port D Direction Register. The signal can be configured as an ESSI signal SC11 through the Port D Control Register.
SC12	Input/Output	Ignored Input	**Serial Control Signal 2**—The frame sync for both the transmitter and receiver in synchronous mode and for the transmitter only in asynchronous mode. When configured as an output, this signal is the internally generated frame sync signal. When configured as an input, this signal receives an external frame sync signal for the transmitter (and the receiver in synchronous operation).
PD2	Input or Output		**Port D 2**—The default configuration following reset is GPIO input PD2. When configured as PD2, signal direction is controlled through the Port D Direction Register. The signal can be configured as an ESSI signal SC12 through the Port D Control Register.

Table 1-12. Enhanced Serial Synchronous Interface 1 (Continued)

Signal Name	Type	State During Reset[1,2]	Signal Description
SCK1	Input/Output	Ignored Input	**Serial Clock**—Provides the serial bit rate clock for the ESSI. The SCK1 is a clock input or output used by both the transmitter and receiver in synchronous modes or by the transmitter in asynchronous modes. Although an external serial clock can be independent of and asynchronous to the DSP system clock, it must exceed the minimum clock cycle time of 6T (that is, the system clock frequency must be at least three times the external ESSI clock frequency). The ESSI needs at least three DSP phases inside each half of the serial clock.
PD3	Input or Output		**Port D 3**—The default configuration following reset is GPIO input PD3. When configured as PD3, signal direction is controlled through the Port D Direction Register. The signal can be configured as an ESSI signal SCK1 through the Port D Control Register.
SRD1	Input	Ignored Input	**Serial Receive Data**—Receives serial data and transfers the data to the ESSI Receive Shift Register. SRD1 is an input when data is being received.
PD4	Input or Output		**Port D 4**—The default configuration following reset is GPIO input PD4. When configured as PD4, signal direction is controlled through the Port D Direction Register. The signal can be configured as an ESSI signal SRD1 through the Port D Control Register.
STD1	Output	Ignored Input	**Serial Transmit Data**—Transmits data from the Serial Transmit Shift Register. STD1 is an output when data is being transmitted.
PD5	Input or Output		**Port D 5**—The default configuration following reset is GPIO input PD5. When configured as PD5, signal direction is controlled through the Port D Direction Register. The signal can be configured as an ESSI signal STD1 through the Port D Control Register.

Notes: 1. In the Stop state, the signal maintains the last state as follows:
- If the last state is input, the signal is an ignored input.
- If the last state is output, these lines have weak keepers that maintain the last output state even if the drivers are tri-stated.

2. The Wait processing state does not affect the signal state.

1.9 Serial Communication Interface (SCI)

The SCI provides a full duplex port for serial communication with other DSPs, microprocessors, or peripherals such as modems.

Table 1-13. Serial Communication Interface

Signal Name	Type	State During Reset[1,2]	Signal Description
RXD	Input	Ignored Input	**Serial Receive Data**—Receives byte-oriented serial data and transfers it to the SCI Receive Shift Register.
PE0	Input or Output		**Port E 0**—The default configuration following reset is GPIO input PE0. When configured as PE0, signal direction is controlled through the Port E Direction Register. The signal can be configured as an SCI signal RXD through the Port E Control Register.
TXD	Output	Ignored Input	**Serial Transmit Data**—Transmits data from the SCI Transmit Data Register.
PE1	Input or Output		**Port E 1**—The default configuration following reset is GPIO input PE1. When configured as PE1, signal direction is controlled through the Port E Direction Register. The signal can be configured as an SCI signal TXD through the Port E Control Register.

Table 1-13. Serial Communication Interface (Continued)

Signal Name	Type	State During Reset[1,2]	Signal Description
SCLK	Input/Output	Ignored Input	**Serial Clock**—Provides the input or output clock used by the transmitter and/or the receiver.
PE2	Input or Output		**Port E 2**—The default configuration following reset is GPIO input PE2. When configured as PE2, signal direction is controlled through the Port E Direction Register. The signal can be configured as an SCI signal SCLK through the Port E Control Register.

Notes: 1. In the Stop state, the signal maintains the last state as follows:
- If the last state is input, the signal is an ignored input.
- If the last state is output, these lines have weak keepers that maintain the last output state even if the drivers are tri-stated.

2. The Wait processing state does not affect the signal state.

1.10 Timers

The DSP56321 has three identical and independent timers. Each timer can use internal or external clocking and can either interrupt the DSP56321 after a specified number of events (clocks) or signal an external device after counting a specific number of internal events.

Table 1-14. Triple Timer Signals

Signal Name	Type	State During Reset[1,2]	Signal Description
TIO0	Input or Output	Ignored Input	**Timer 0 Schmitt-Trigger Input/Output**— When Timer 0 functions as an external event counter or in measurement mode, TIO0 is used as input. When Timer 0 functions in watchdog, timer, or pulse modulation mode, TIO0 is used as output. The default mode after reset is GPIO input. TIO0 can be changed to output or configured as a timer I/O through the Timer 0 Control/Status Register (TCSR0).
TIO1	Input or Output	Ignored Input	**Timer 1 Schmitt-Trigger Input/Output**— When Timer 1 functions as an external event counter or in measurement mode, TIO1 is used as input. When Timer 1 functions in watchdog, timer, or pulse modulation mode, TIO1 is used as output. The default mode after reset is GPIO input. TIO1 can be changed to output or configured as a timer I/O through the Timer 1 Control/Status Register (TCSR1).
TIO2	Input or Output	Ignored Input	**Timer 2 Schmitt-Trigger Input/Output**— When Timer 2 functions as an external event counter or in measurement mode, TIO2 is used as input. When Timer 2 functions in watchdog, timer, or pulse modulation mode, TIO2 is used as output. The default mode after reset is GPIO input. TIO2 can be changed to output or configured as a timer I/O through the Timer 2 Control/Status Register (TCSR2).

Notes: 1. In the Stop state, the signal maintains the last state as follows:
- If the last state is input, the signal is an ignored input.
- If the last state is output, these lines have weak keepers that maintain the last output state even if the drivers are tri-stated.

2. The Wait processing state does not affect the signal state.

1.11 JTAG and OnCE Interface

The DSP56300 family and in particular the DSP56321 support circuit-board test strategies based on the **IEEE® Std.** 1149.1™ test access port and boundary scan architecture, the industry standard developed under the sponsorship of the Test Technology Committee of IEEE and the JTAG. The OnCE module provides a means to interface nonintrusively with the DSP56300 core and its peripherals so that you can examine registers, memory, or on-chip peripherals. Functions of the OnCE module are provided through the JTAG TAP signals. For programming models, see the chapter on debugging support in the *DSP56300 Family Manual*.

Table 1-15. JTAG/OnCE Interface

Signal Name	Type	State During Reset	Signal Description
TCK	Input	Input	**Test Clock**—A test clock input signal to synchronize the JTAG test logic.
TDI	Input	Input	**Test Data Input**—A test data serial input signal for test instructions and data. TDI is sampled on the rising edge of TCK and has an internal pull-up resistor.
TDO	Output	Tri-stated	**Test Data Output**—A test data serial output signal for test instructions and data. TDO is actively driven in the shift-IR and shift-DR controller states. TDO changes on the falling edge of TCK.
TMS	Input	Input	**Test Mode Select**—Sequences the test controller's state machine. TMS is sampled on the rising edge of TCK and has an internal pull-up resistor.
$\overline{\text{TRST}}$	Input	Input	**Test Reset**—Initializes the test controller asynchronously. $\overline{\text{TRST}}$ has an internal pull-up resistor. $\overline{\text{TRST}}$ must be asserted during and after power-up (see EB610/D for details).
$\overline{\text{DE}}$	Input/ Output	Input	**Debug Event**—As an input, initiates Debug mode from an external command controller, and, as an open-drain output, acknowledges that the chip has entered Debug mode. As an input, $\overline{\text{DE}}$ causes the DSP56300 core to finish executing the current instruction, save the instruction pipeline information, enter Debug mode, and wait for commands to be entered from the debug serial input line. This signal is asserted as an output for three clock cycles when the chip enters Debug mode as a result of a debug request or as a result of meeting a breakpoint condition. The $\overline{\text{DE}}$ has an internal pull-up resistor. This signal is not a standard part of the JTAG TAP controller. The signal connects directly to the OnCE module to initiate debug mode directly or to provide a direct external indication that the chip has entered Debug mode. All other interface with the OnCE module must occur through the JTAG port.

Specifications 2

The DSP56321 is fabricated in high-density CMOS with Transistor-Transistor Logic (TTL) compatible inputs and outputs.

2.1 Maximum Ratings

CAUTION

This device contains circuitry protecting against damage due to high static voltage or electrical fields; however, normal precautions should be taken to avoid exceeding maximum voltage ratings. Reliability is enhanced if unused inputs are tied to an appropriate logic voltage level (for example, either GND or V_{CC}).

In the calculation of timing requirements, adding a maximum value of one specification to a minimum value of another specification does not yield a reasonable sum. A maximum specification is calculated using a worst case variation of process parameter values in one direction. The minimum specification is calculated using the worst case for the same parameters in the opposite direction. Therefore, a "maximum" value for a specification never occurs in the same device that has a "minimum" value for another specification; adding a maximum to a minimum represents a condition that can never exist.

Table 2-1. Absolute Maximum Ratings

Rating[1]	Symbol	Value[1, 2]	Unit
Supply Voltage[3]	V_{CCQL}	–0.1 to 2.25	V
Input/Output Supply Voltage[3]	V_{CCQH}	–0.3 to 4.35	V
All input voltages	V_{IN}	GND – 0.3 to V_{CCQH} + 0.3	V
Current drain per pin excluding V_{CC} and GND	I	10	mA
Operating temperature range	T_J	–40 to +100	°C
Storage temperature	T_{STG}	–55 to +150	°C

Notes:
1. GND = 0 V, V_{CCQL} = 1.6 V ± 0.1 V, V_{CCQH} = 3.3 V ± 0.3 V, T_J = –40°C to +100°C, CL = 50 pF
2. Absolute maximum ratings are stress ratings only, and functional operation at the maximum is not guaranteed. Stress beyond the maximum rating may affect device reliability or cause permanent damage to the device.
3. Power-up sequence: During power-up, and throughout the DSP56321 operation, V_{CCQH} voltage must always be higher or equal to V_{CCQL} voltage.

2.2 Thermal Characteristics

Table 2-2. Thermal Characteristics

Thermal Resistance Characteristic	Symbol	MAP-BGA Value	Unit
Junction-to-ambient, natural convection, single-layer board (1s)[1,2]	$R_{\theta JA}$	44	°C/W
Junction-to-ambient, natural convection, four-layer board (2s2p)[1,3]	$R_{\theta JMA}$	25	°C/W
Junction-to-ambient, @200 ft/min air flow, single-layer board (1s)[1,3]	$R_{\theta JMA}$	35	°C/W
Junction-to-ambient, @200 ft/min air flow, four-layer board (2s2p)[1,3]	$R_{\theta JMA}$	22	°C/W
Junction-to-board[4]	$R_{\theta JB}$	13	°C/W
Junction-to-case thermal resistance[5]	$R_{\theta JC}$	7	°C/W

Notes:
1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
2. Per SEMI G38-87 and JEDEC JESD51-2 with the single-layer board horizontal.
3. Per JEDEC JESD51-6 with the board horizontal.
4. Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
5. Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).

2.3 DC Electrical Characteristics

Table 2-3. DC Electrical Characteristics[7]

Characteristics	Symbol	Min	Typ	Max	Unit
Supply voltage[1]:					
• Core (V_{CCQL})		1.5	1.6	1.7	V
• I/O (V_{CCQH}, V_{CCA}, V_{CCD}, V_{CCC}, V_{CCH}, and V_{CCS})		3.0	3.3	3.6	V
Input high voltage					
• D[0–23], $\overline{BG}$, $\overline{BB}$, $\overline{TA}$	V_{IH}	2.0	—	V_{CCQH} + 0.3	V
• MOD/$\overline{IRQ}$[2] $\overline{RESET}$, PINIT/$\overline{NMI}$ and all JTAG/ESSI/SCI/Timer/HI08 pins	V_{IHP}	2.0	—	V_{CCQH} + 0.3	V
• EXTAL[9]	V_{IHX}	0.8 × V_{CCQH}	—	V_{CCQH}	V
Input low voltage					
• D[0–23], $\overline{BG}$, $\overline{BB}$, $\overline{TA}$, MOD/$\overline{IRQ}$[2], $\overline{RESET}$, PINIT	V_{IL}	–0.3	—	0.8	V
• All JTAG/ESSI/SCI/Timer/HI08 pins	V_{ILP}	–0.3	—	0.8	V
• EXTAL[9]	V_{ILX}	–0.3	—	0.2 × V_{CCQH}	V
Input leakage current	I_{IN}	–10	—	10	µA
High impedance (off-state) input current (@ 2.4 V / 0.4 V)	I_{TSI}	–10	—	10	µA
Output high voltage[8]	V_{OH}				
• TTL (I_{OH} = –0.4 mA)[6]		2.4	—	—	V
• CMOS (I_{OH} = –10 µA)[6]		V_{CCQH} – 0.01	—	—	V
Output low voltage[8]	V_{OL}				
• TTL (I_{OL} = 3.0 mA)[6]		—	—	0.4	V
• CMOS (I_{OL} = 10 µA)[6]		—	—	0.01	V

Table 2-3. DC Electrical Characteristics[7]

Characteristics	Symbol	Min	Typ	Max	Unit
Internal supply current:					
• In Normal mode[3]	I_{CCI}				
— at 200 MHz		—	190	—	mA
— at 220 MHz		—	200	—	mA
— at 240 MHz		—	210	—	mA
— at 275 MHz		—	235	—	mA
• In Wait mode[4]	I_{CCW}	—	25	—	mA
• In Stop mode[5]	I_{CCS}	—	15	—	mA
Input capacitance[6]	C_{IN}	—	—	10	pF

Notes:
1. Power-up sequence: During power-up, and throughout the DSP56321 operation, V_{CCQH} voltage must always be higher or equal to V_{CCQL} voltage.
2. Refers to MODA/$\overline{\text{IRQA}}$, MODB/$\overline{\text{IRQB}}$, MODC/$\overline{\text{IRQC}}$, and MODD/$\overline{\text{IRQD}}$ pins.
3. **Section 4.3** provides a formula to compute the estimated current requirements in Normal mode. To obtain these results, all inputs must be terminated (that is, not allowed to float). Measurements are based on synthetic intensive DSP benchmarks (see **Appendix A**). The power consumption numbers in this specification are 90 percent of the measured results of this benchmark. This reflects typical DSP applications.
4. To obtain these results, all inputs must be terminated (that is, not allowed to float).
5. To obtain these results, all inputs not disconnected at Stop mode must be terminated (that is, not allowed to float), and the DPLL and on-chip crystal oscillator must be disabled.
6. Periodically sampled and not 100 percent tested.
7. V_{CCQH} = 3.3 V ±0.3 V, V_{CQLC} = 1.6 V ±0.1 V; T_J = –40°C to +100 °C, C_L = 50 pF
8. This characteristic does not apply to XTAL.
9. Driving EXTAL to the low V_{IHX} or the high V_{ILX} value may cause additional power consumption (DC current). To minimize power consumption, the minimum V_{IHX} should be no lower than 0.9 × V_{CCQH} and the maximum V_{ILX} should be no higher than 0.1 × V_{CCQH}.

2.4 AC Electrical Characteristics

The timing waveforms shown in the AC electrical characteristics section are tested with a V_{IL} maximum of 0.3 V and a V_{IH} minimum of 2.4 V for all pins except EXTAL, which is tested using the input levels shown in Notes 7 and 9 of the previous table. AC timing specifications, which are referenced to a device input signal, are measured in production with respect to the 50 percent point of the respective input signal's transition. DSP56321 output levels are measured with the production test machine V_{OL} and V_{OH} reference levels set at 0.4 V and 2.4 V, respectively.

Note: Although the minimum value for the frequency of EXTAL is 0 MHz, the device AC test conditions are 16 MHz and rated speed with the DPLL enabled.

2.4.1 Internal Clocks

Table 2-4. Internal Clocks

Characteristics	Symbol	Expression		
		Min	Typ	Max
Internal operating frequency	f			
• With DPLL disabled		—	Ef/2	—
• With DPLL enabled		—	(Ef × MF)/(PDF × DF)	—
Internal clock cycle time	T_C			
• With DPLL disabled		—	2 × ET_C	—
• With DPLL enabled		—	ET_C × PDF × DF/MF	—
Internal clock high period	T_H			
• With DPLL disabled		—	ET_C	—
• With DPLL enabled		0.49 × T_C	—	0.51 × T_C

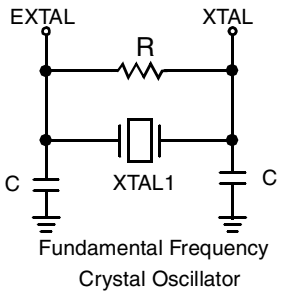
Table 2-4. Internal Clocks (Continued)

Characteristics	Symbol	Expression		
		Min	Typ	Max
Internal clock low period • With DPLL disabled • With DPLL enabled	T_L	— 0.49 × T_C	ET_C —	— 0.51 × T_C

Note: Ef = External frequency; MF = Multiplication Factor = MFI + MFN/MFD; PDF = Predivision Factor; DF = Division Factor; T_C = Internal clock cycle; ET_C = External clock cycle; T_H = Internal clock high; T_L = Internal clock low

2.4.2 External Clock Operation

The DSP56321 system clock is derived from the on-chip oscillator or is externally supplied. To use the on-chip oscillator, connect a crystal and associated resistor/capacitor components to EXTAL and XTAL; an example is shown in **Figure 2-1**.



Suggested Component Values:
f_{OSC} = 16–32 MHz
R = 1 MΩ±10%
C = 10 pF ±10%

Calculations are for a 16–32 MHz crystal with the following parameters:
- shunt capacitance (C_0) of 5.2–7.3 pF,
- series resistance of 5–15 Ω, and
- drive level of 2 mW.

Note: Make sure that in the PCTL Register:
- XTLD (bit 2) = 0

Figure 2-1. Crystal Oscillator Circuits

Table 2-5. External Clock Operation

No.	Characteristics	Symbol	200 MHz		220 MHz		240 MHz		275 MHz	
			Min	Max	Min	Max	Min	Max	Min	Max
1	Frequency of EXTAL (EXTAL Pin Frequency)[1] • With DPLL disabled • With DPLL enabled[2]	Ef DEFR = PDF × PDFR	0 MHz 16 MHz	200 MHz 200 MHz	0 MHz 16 MHz	220 MHz 220 MHz	0 MHz 16 MHz	240 MHz 240 MHz	0 MHz 16 MHz	275 MHz 275 MHz
2	EXTAL input high[3] • With DPLL disabled (46.7%–53.3% duty cycle[4]) • With DPLL enabled (42.5%–57.5% duty cycle[4])	ET_H	2.34 ns 2.13 ns	∞ 35.9 ns	2.12 ns 1.93 ns	∞ 35.9 ns	1.95 ns 1.77 ns	∞ 35.9 ns	1.70 ns 1.55 ns	∞ 35.9 ns
3	EXTAL input low[4] • With DPLL disabled (46.7%–53.3% duty cycle[4]) • With DPLL enabled (42.5%–57.5% duty cycle[4])	ET_L	2.34 ns 2.13 ns	∞ 35.9 ns	2.12ns 1.93 ns	∞ 35.9 ns	1.95 ns 1.77 ns	∞ 35.9 ns	1.70 ns 1.55 ns	∞ 35.9 ns

Table 2-5. External Clock Operation (Continued)

No.	Characteristics	Symbol	200 MHz		220 MHz		240 MHz		275 MHz	
			Min	Max	Min	Max	Min	Max	Min	Max
4	EXTAL cycle time[3] • With DPLL disabled • With DPLL enabled	ET_C	 5.0 ns 5.0 ns	 ∞ 62.5 ns	 4.55 ns 4.55 ns	 ∞ 62.5 ns	 4.17 ns 4.17 ns	 ∞ 62.5 ns	 3.64 ns 3.64 ns	 ∞ 62.5 ns
7	Instruction cycle time = $I_{CYC} = ET_C$ • With DPLL disabled • With DPLL enabled	I_{CYC}	 10 ns 5.0 ns	 ∞ 1.6 µs	 9.09 ns 4.55 ns	 ∞ 1.6 µs	 8.33 ns 4.17 ns	 ∞ 1.6 µs	 7.28 ns 3.64 ns	 ∞ 1.6 µs

Notes:
1. The rise and fall time of this external clock should be 2 ns maximum.
2. Refer to **Table 2-6** for a description of PDF and PDFR.
3. Measured at 50 percent of the input transition.
4. The indicated duty cycle is for the specified maximum frequency for which a part is rated. The minimum clock high or low time required for correction operation, however, remains the same at lower operating frequencies; therefore, when a lower clock frequency is used, the signal symmetry may vary from the specified duty cycle as long as the minimum high time and low time requirements are met.

Note: If an externally-supplied square wave voltage source is used, disable the internal oscillator circuit after boot-up by setting XTLD (PCTL Register bit 2 = 1—see the *DSP56321 Reference Manual*). The external square wave source connects to EXTAL and XTAL is not used. **Figure 2-2** shows the EXTAL input signal.

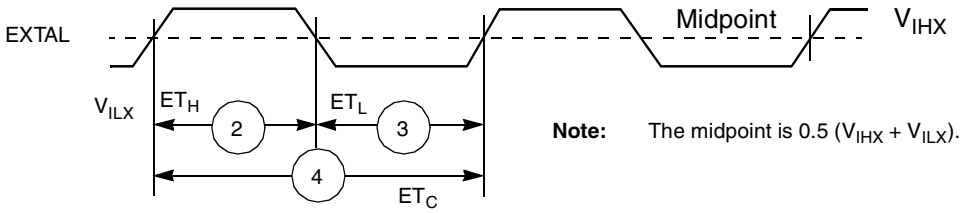


Figure 2-2. External Input Clock Timing

2.4.3 Clock Generator (CLKGEN) and Digital PLL (DPLL) Characteristics

Table 2-6. CLKGEN and DPLL Characteristics

Characteristics	Symbol	200 MHz		220 MHz		240 MHz		275 MHz		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
Predivision factor	PDF[1]	1	16	1	16	1	16	1	16	—
Predivider output clock frequency range	PDFR	16	32	16	32	16	32	16	32	MHz
Total multiplication factor[2]	MF	5	15	5	15	5	15	5	15	—
Multiplication factor integer part	MFI[1]	5	15	5	15	5	15	5	15	—
Multiplication factor numerator[3]	MFN	0	127	0	127	0	127	0	127	—
Multiplication factor denominator	MFD	1	128	1	128	1	128	1	128	—
Double clock frequency range	DDFR	160	400	160	440	160	480	160	550	MHz
Phase lock-in time[4]	DPLT	6.8[5]	150[6]	6.8[5]	150[6]	6.8[5]	150[6]	6.8[5]	150[6]	µs