



Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!



Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832

Email & Skype: info@chipsmall.com Web: www.chipsmall.com

Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China



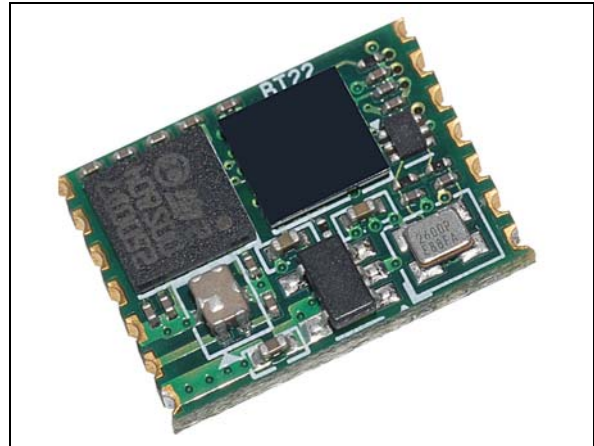


Bluetooth® V2.1 + EDR module class 2 embedding SPP and AT commands

Datasheet – production data

Features

- Bluetooth® radio
 - Fully embedded Bluetooth v2.1 + EDR with profiles
 - Class 2 module
 - Complete RF ready module
- ST micro Cortex-M3 microprocessor up to 72 MHz
- Memory
 - 256 kb Flash memory
 - 48 kb RAM memory
- Data rate
 - 1.5 Mbps maximum data rate
- Serial interface
 - UART up to 2.0 Mbps
- General I/O
 - 4 general purpose I/Os
- User interface
 - AT2 command set (abSerial)
 - Firmware upgrade over UART
- CE and Bluetooth qualified
- EPL (end product listing) fulfilled
- Single voltage supply: 3.3 V typical
- Micro-sized form factor: 10.5 x 13.5 x 2.5 mm
- Operating temperature range: -40 °C to 85 °C



Contents

1	Description	6
2	RoHS compliance	7
3	Applications	7
4	Software architecture	8
	4.1 Lower layer stack	8
	4.2 Upper layer stack: Amp'ed UP	8
	4.3 AT command set: abSerial	8
	4.4 Bluetooth firmware implementation	9
5	Hardware specifications	10
	5.1 Recommended operating conditions	10
	5.2 Absolute maximum ratings	10
	5.3 High speed CPU mode current consumption	11
	5.4 Standard CPU mode current consumption	11
	5.5 I/O operating characteristics	12
	5.6 Selected RF characteristics	12
	5.7 Pin assignment	13
	5.8 Pin placement	14
	5.9 Layout drawing	15
6	Hardware block diagram	16
7	Hardware design	17
	7.1 Module reflow installation	17
	7.2 GPIO interface	18
	7.3 UART interface	18
8	Application information	20
	8.1 Antenna choice	20
	8.2 Antenna coupling	22

8.3	Example of trace calculation	22
8.4	Reset circuit	23
8.4.1	External reset circuit	23
8.4.2	Internal reset circuit	23
9	Regulatory compliance	24
10	Ordering information	25
11	Revision history	26

List of tables

Table 1.	Recommended operating conditions	10
Table 2.	Absolute maximum ratings	10
Table 3.	High speed CPU mode current consumption	11
Table 4.	Standard CPU mode current consumption	11
Table 5.	I/O operating characteristics	12
Table 6.	Selected RF characteristics	12
Table 7.	Pin assignment	13
Table 8.	Soldering	17
Table 9.	Ordering information	25
Table 10.	Document revision history	26

List of figures

Figure 1.	FW architecture	9
Figure 2.	Pin placement	14
Figure 3.	Ground plane diagram	14
Figure 4.	Layout drawing	15
Figure 5.	SPBT2532C2.AT2 module block diagram	16
Figure 6.	Soldering profile	18
Figure 7.	Connection to host device	18
Figure 8.	Typical RS232 circuit	19
Figure 9.	Example of antenna integration on the STEVAL-SPBT2ATV3.	20
Figure 10.	Antenna printed on PCB	21
Figure 11.	SMD antenna	21
Figure 12.	SMA connector for external antenna	21
Figure 13.	Parameters for trace matching	22
Figure 14.	External reset circuit	23
Figure 15.	Internal reset circuit	23

1 Description

The SPBT2532C2.AT2 is an easy to use Bluetooth module, compliant with Bluetooth v2.1 + EDR.

The module is the smallest form factor available which provides a complete RF platform. The SPBT2532C2.AT2 enables electronic devices with wireless connectivity, not requiring any RF experience or expertise for integration into the final product. The SPBT2532C2.AT2 module, being a certified solution, optimizes the time to market of the final application.

The module is designed for maximum performance in the minimum possible size including fast speed UART and 4 general purpose I/O lines, several serial interface options, and up to 1.5 Mbps data throughput.

The SPBT2532C2.AT2 is a surface mount PCB module that provides fully embedded, ready-to-use Bluetooth wireless technology. The reprogrammable Flash memory contains embedded firmware for serial cable replacement using the Bluetooth SPP profile. Embedded Bluetooth AT2 command firmware is a friendly interface, which realizes a simple control for cable replacement, enabling communication with most Bluetooth enabled devices, provided that the devices support the SPP profile. The SPBT2532C2.AT2, supporting iAP profile, provides communication with Android™, smartphones, and Apple® iOS Bluetooth enabled devices.

An Apple authentication IC is required to exchange data with an Apple device or access an Apple device application. The AT2 FW includes the Bluetooth SPP profile capable of recognizing the Apple authentication chip.

Customers using the Apple authentication IC must register as developers to become an Apple certified MFI member. License fees may apply, for additional information visit: <http://developer.apple.com/programs/which-program/index.html>.

Certified MFI developers developing electronic accessories that connect to the iPod®, iPhone®, and iPad® gain access to technical documentation, hardware components, technical support and certification logos.

Customized firmware for peripheral device interaction, power optimization, security, and other proprietary features may be supported and can be ordered pre-loaded and configured.

2 RoHS compliance

ST modules are RoHS compliant and comply with ECOPACK® norms.

3 Applications

- Serial cable replacement
- M2M industrial control
- Service diagnostic
- Data acquisition equipment
- Machine control
- Sensor monitoring
- Security system
- Mobile health.

4 Software architecture

4.1 Lower layer stack

- Bluetooth v2.1 + EDR
- Device power modes: active, sleep and deep sleep
- Wake-on Bluetooth feature optimized power consumption of host CPU
- Authentication and encryption
- Encryption key length from 8 bits to 128 bits
- Persistent Flash memory for BD address and user parameter storage
- All ACL (asynchronous connection less) packet types
- Point-to-point supported
- Master/slave switch supported during connection and post connection
- Dedicated inquiry access code for improved inquiry scan performance
- Dynamic packet selection channel quality driven data rate to optimize link performance
- Dynamic power control
- 802.11b co-existence AFH.

4.2 Upper layer stack: Amp'ed UP

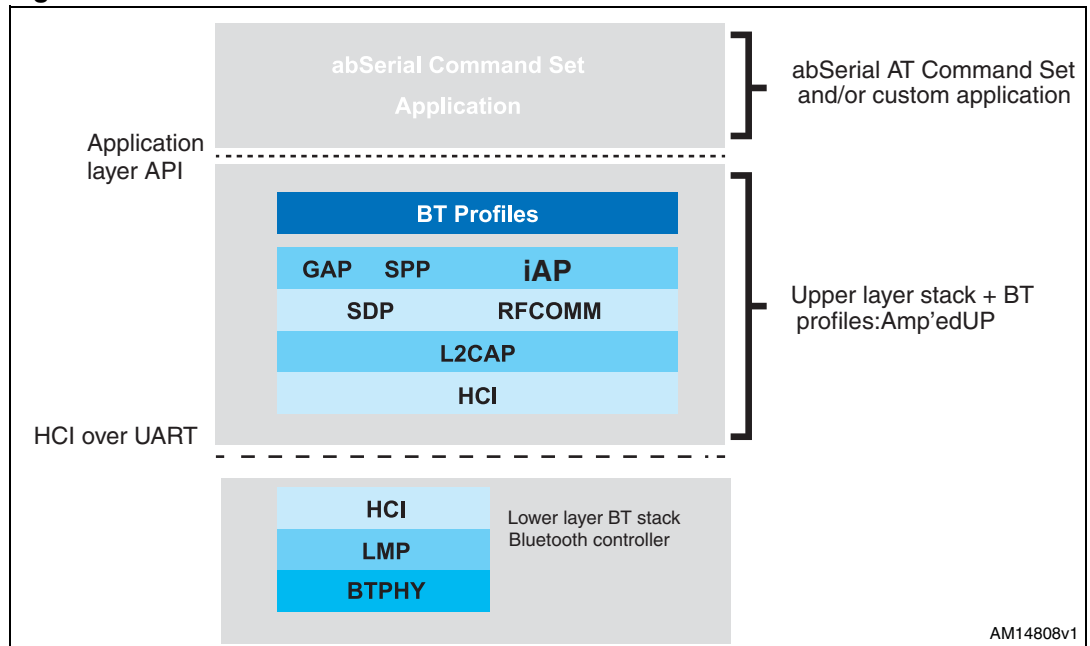
- SPP, IAP, SDAP and GAP protocols
- RFCOMM, SDP, and L2CAP supported
- Multipoint with simultaneous slaves.

4.3 AT command set: abSerial

The complete command list including the iAP commands is reported in the UM1547 user manual.

4.4 Bluetooth firmware implementation

Figure 1. FW architecture



5 Hardware specifications

General conditions ($V_{IN} = 3.3\text{ V}$ and 25 °C).

5.1 Recommended operating conditions

Table 1. Recommended operating conditions

Rating	Min.	Typ.	Max.	Unit
Operating temperature range ⁽¹⁾	-40	-	85	°C
Supply voltage V_{IN}	2.8	3.3	3.6	V
Signal pin voltage	-	3.0	-	V
RF frequency	2400	-	2483.5	MHz

1. @ CPU 8MHz, @ CPU 32MHz - 16 MHz max. operating temperature is 55 °C.

5.2 Absolute maximum ratings

Table 2. Absolute maximum ratings

Rating	Min.	Typ.	Max.	Unit
Storage temperature range	-55	-	+105	°C
Supply voltage, V_{IN}	-0.3		+ 5.0	V
I/O pin voltage, V_{IO}	-0.3		+ 5.5	V
RF input power	-		-5	dBm
Input voltage on non-5 V tolerant pin	0.3		+4.0	V

5.3 High speed CPU mode current consumption

- High speed CPU mode
 - CPU 32 MHz, maximum operating temperature 55 °C
 - UART supports up to 921 Kbps
 - Data throughput up to 1.5 Mbps
 - Shallow sleep enabled.

Table 3. High speed CPU mode current consumption

Modes (typical power consumption)	Avg.	Unit
ACL data 115 K baud UART at max. throughput (master)	41	mA
ACL data 115 K baud UART at max. throughput (slave)	41	mA
Connection, no data traffic, master	28.9	mA
Connection, no data traffic, slave	34.5	mA
Standby, without deep sleep	28	mA
Standby, with deep sleep	3.1	mA
Bluetooth power down / CPU standby	25	µA

5.4 Standard CPU mode current consumption

- Standard CPU mode
 - CPU 8 MHz, maximum operating temperature 85 °C
 - UART supports up to 115 Kbps
 - Data throughput up to 200 Kbps
 - Shallow sleep enabled.

Table 4. Standard CPU mode current consumption

Mode (typical power consumption)	Avg.	Unit
ACL data 115 K baud UART at max. throughput (master)	25.8	mA
ACL data 115 K baud UART at max. throughput (slave)	25.8	mA
Connection, no data traffic, master	11.9	mA
Connection, no data traffic, slave	16.9	mA
Standby, without deep sleep	11.2	mA
Standby, with deep sleep	2.6	mA
Bluetooth power down / CPU standby	25	µA

5.5 I/O operating characteristics

Table 5. I/O operating characteristics

Symbol	Parameter	Min.	Max.	Unit	Conditions
V _{IL}	Low-level input voltage	-	0.9	V	V _{IN} , 3.0 V
V _{IH}	High-level input voltage	2.1	-	V	V _{IN} , 3.0 V
V _{OL}	Low-level output voltage	-	0.4	V	V _{IN} , 3.0 V
V _{OH}	High-level output voltage	2.2	-	V	V _{IN} , 3.0 V
I _{OL}	Low-level output current	-	4.0	mA	V _{OL} = 0.4 V
I _{OH}	High-level output current	-	4.0	mA	V _{OH} = 2.2 V
R _{PU}	Pull-up resistor	80	120	kΩ	Resistor turned on
R _{PD}	Pull-down resistor	80	120	kΩ	Resistor turned on

5.6 Selected RF characteristics

Table 6. Selected RF characteristics

Parameter	Conditions	Typ.	Unit
Antenna load		50	ohm
Radio receiver			
Sensitivity level	BER < .001 with DH5	-85	dBm
Maximum usable level	BER < .001 with DH1	+8	dBm
Input VSWR		2.5:1	
Radio transmitter			
Maximum output power	50 Ω load	+2	dBm
Initial carrier frequency tolerance		± 30	kHz
20 dB bandwidth for modulated carrier		935	kHz

5.7 Pin assignment

Table 7. Pin assignment

Name	Type	Pin#	Description	ALT function ^{(1) (2)}	5 V tolerant	Initial state
UART interface						
RXD	I	13	Receive data	ADC 3	Y	
TXD	O	14	Transmit data	ADC 2	Y	
RTS	O	12	Request to send (active low)	ADC 0 I ² C clock/aux UART Rx	Y	
CTS	I	11	Clear to send (active low)	ADC 1 I ² C data/aux UART Tx	Y	
Boot loader						
Boot 0	I	9	Boot 0			
Power and ground						
V _{in}		8	V _{in}			
GND		5,7	GND			
Reset						
RESETN	I	10	Reset input (active low for 5 ms)			
Antenna						
ANT	RF I/O	6	50 Ω Rx/Tx antenna port			
GPIO - general purpose input/output						
GPIO [1]	I/O	1	General purpose input/output	SPI MISO	Y	Input pull-down
GPIO [2]	I/O	2	General purpose input/output	SPI MOSI/I2S_SD	Y	Floating
GPIO [3]	I/O	3	General purpose input/output	SPI SCLK/I2S_CK	Y	Input pull-down
GPIO [4]	I/O	4	General purpose input/output	SPI SS/I2S_WS	Y	Input pull-down

1. ADC pin functions are not 5 V tolerant when used as ALT pin function. Otherwise the I/O pins are all 5 V tolerant.
2. Please note that the usage of ALT function is dependant upon the firmware that is loaded into the module, and is beyond the scope of this document. The AT command interface uses the main UART by default.

5.8 Pin placement

Figure 2. Pin placement

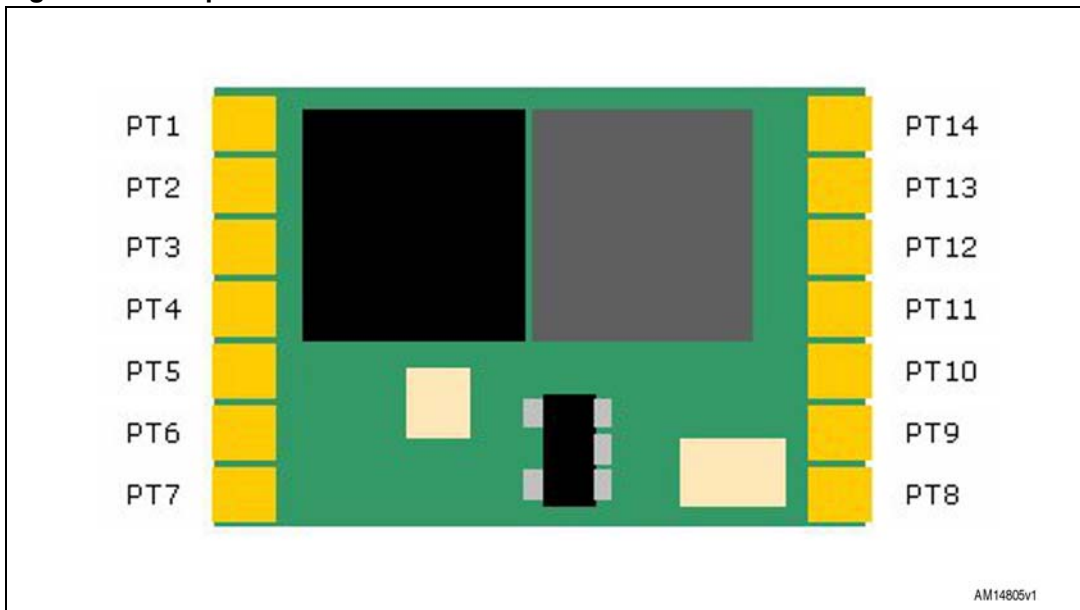
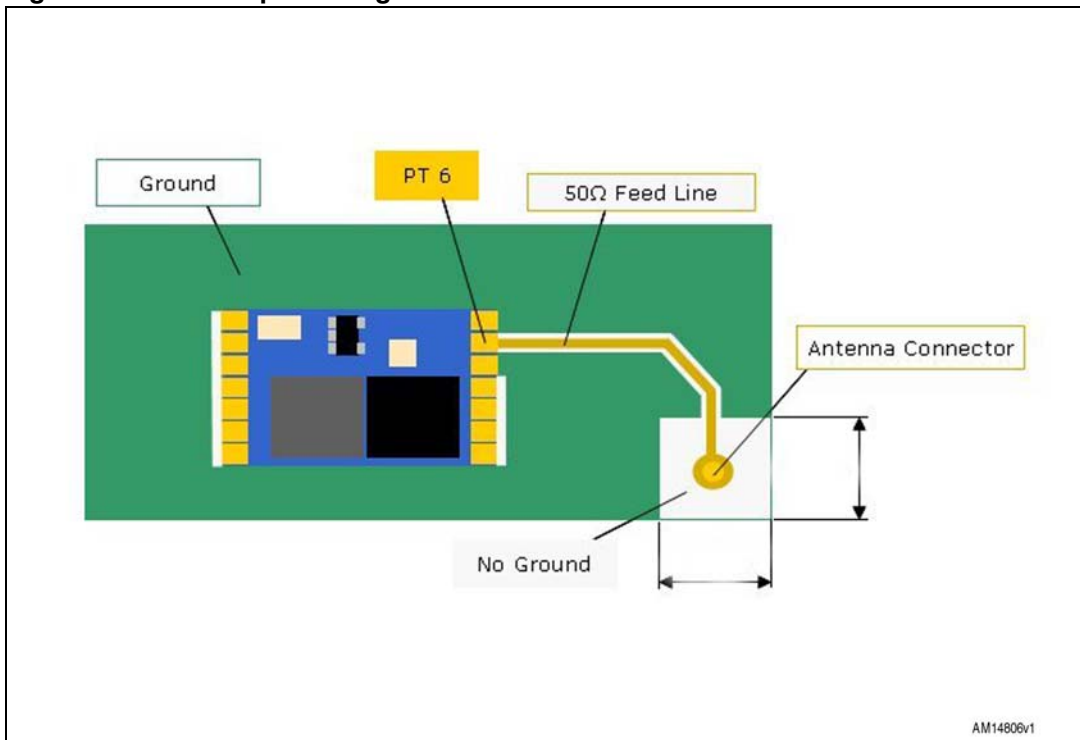
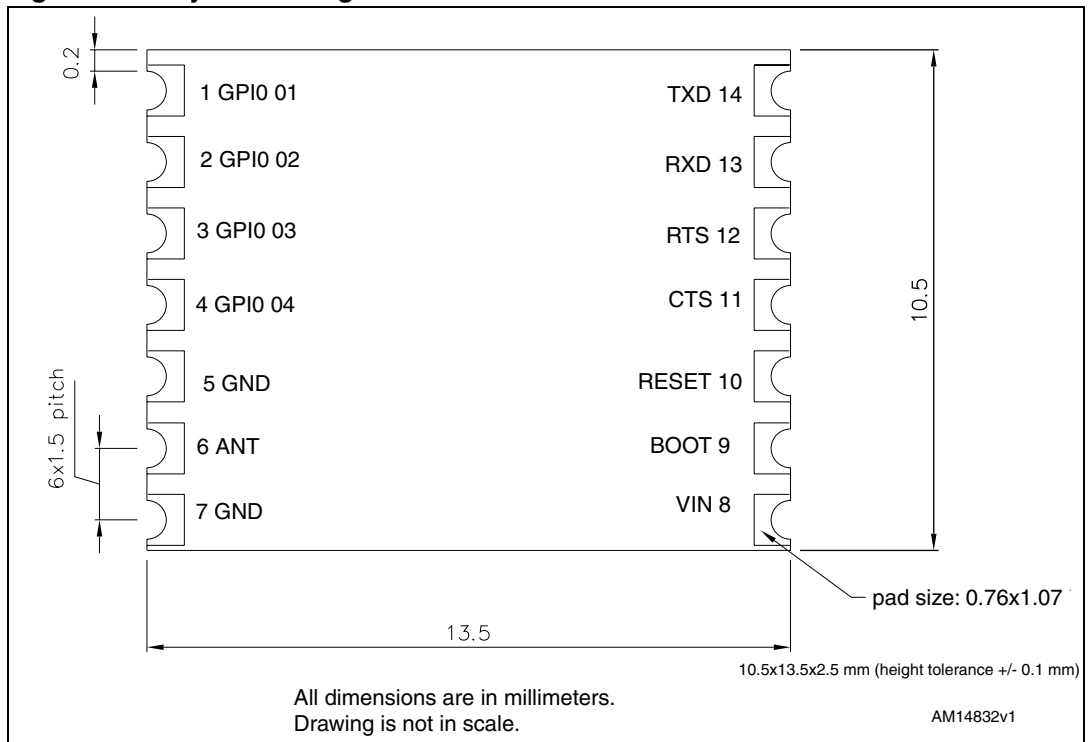


Figure 3. Ground plane diagram



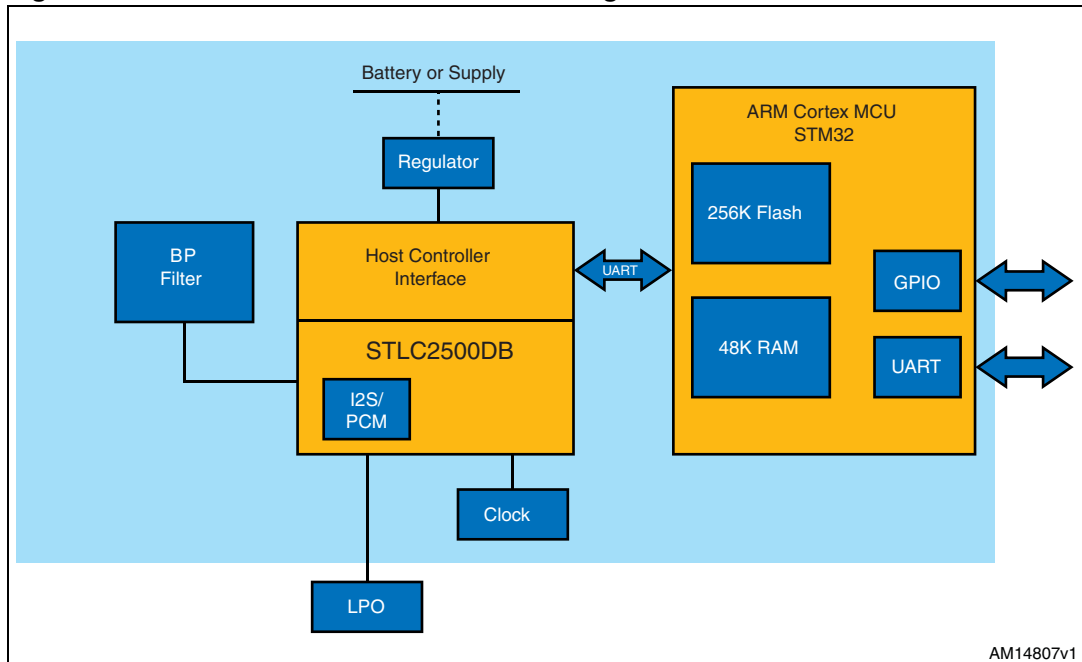
5.9 Layout drawing

Figure 4. Layout drawing



6 Hardware block diagram

Figure 5. SPBT2532C2.AT2 module block diagram



7 Hardware design

The SPBT2532C2.AT2 module with AT2 command embedded FW supports UART and GPIO hardware interfaces. Note that the usage of these interfaces is dependent upon the firmware that is loaded into the module, and is beyond the scope of this document. The AT2 command interface uses the main UART by default.

- Note:*
- 1 All unused pins should be left floating; do not ground.
 - 2 All GND pins must be well grounded.
 - 3 The area around the module should be free of any ground planes, power planes, trace routings, or metal, for 6 mm from the antenna in all directions.
 - 4 Traces should not be routed underneath the module.

7.1 Module reflow installation

The SPB2532C2.AT2 is a surface mount Bluetooth module supplied on a 14-pin, 6-layer PCB. The final assembly recommended reflow profiles are indicated here below.

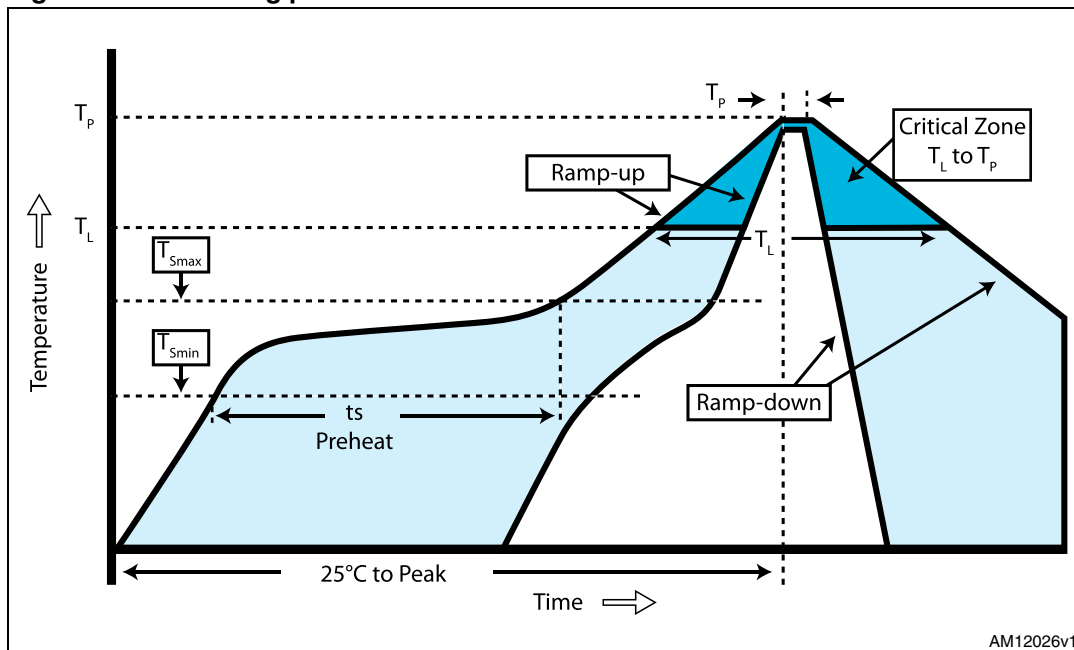
The soldering phase must be executed with care: in order to avoid undesired melting phenomenon, particular attention must be paid to the setup of the peak temperature.

The following are some suggestions for the temperature profile based on IPC/JEDEC J-STD-020C, July 2004 recommendations.

Table 8. Soldering

Profile feature	PB-free assembly
Average ramp-up rate ($T_{S_{MAX}}$ to T_P)	3 °C/sec max.
Preheat:	
– Temperature min. (T_S min.)	150 °C
– Temperature max. (T_S max.)	200 °C
– Time (t_s min. to t_s max.)(t_s)	60-100 sec
Time maintained above:	
– Temperature T_L	217 °C
– Temperature T_L	60-70 sec
Peak temperature (T_P)	240 + 0 °C
Time within 5 °C of actual peak temperature (T_P)	10-20 sec
Ramp-down rate	6 °C/sec
Time from 25 °C to peak temperature	8 minutes max.

Figure 6. Soldering profile



7.2 GPIO interface

All GPIOs are capable of sinking and sourcing 4 mA of I/O current. GPIO [1] is internally pulled down with 100 kΩ (nominal) resistors.

7.3 UART interface

The UART is compatible with the 16550 industry standard. Four signals are provided with the UART interface. The TXD and RXD pins are used for data while the CTS and RTS pins are used for flow control.

Figure 7. Connection to host device

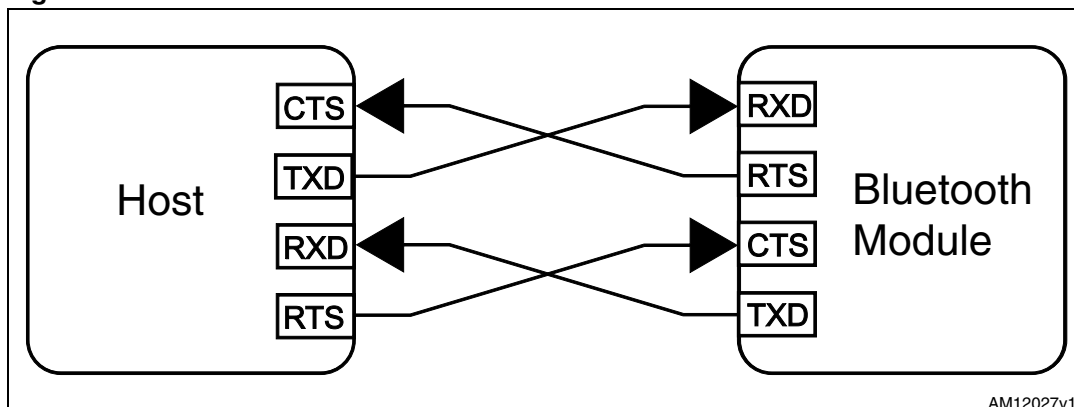
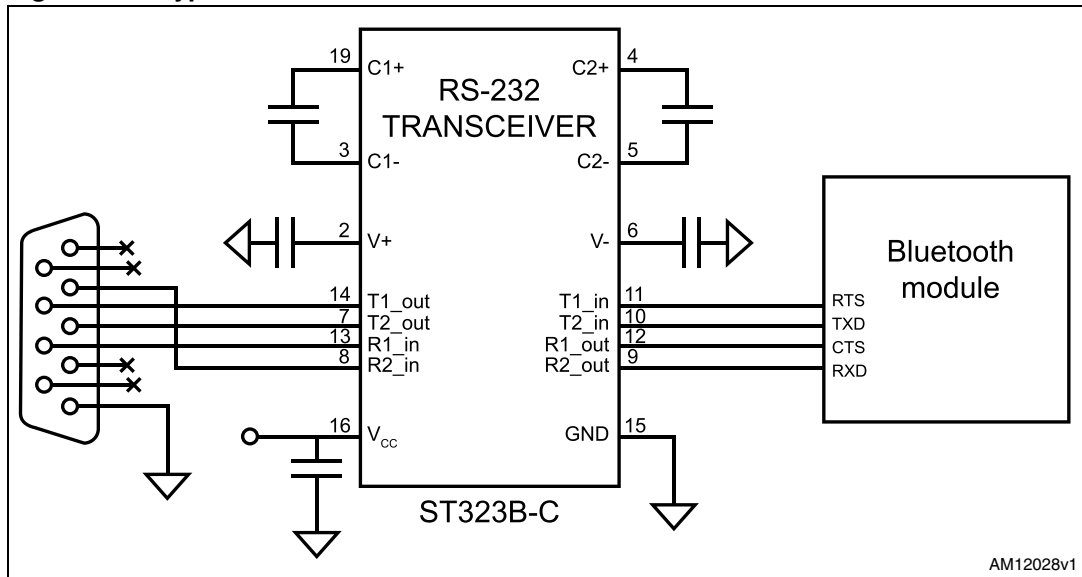


Figure 8. Typical RS232 circuit



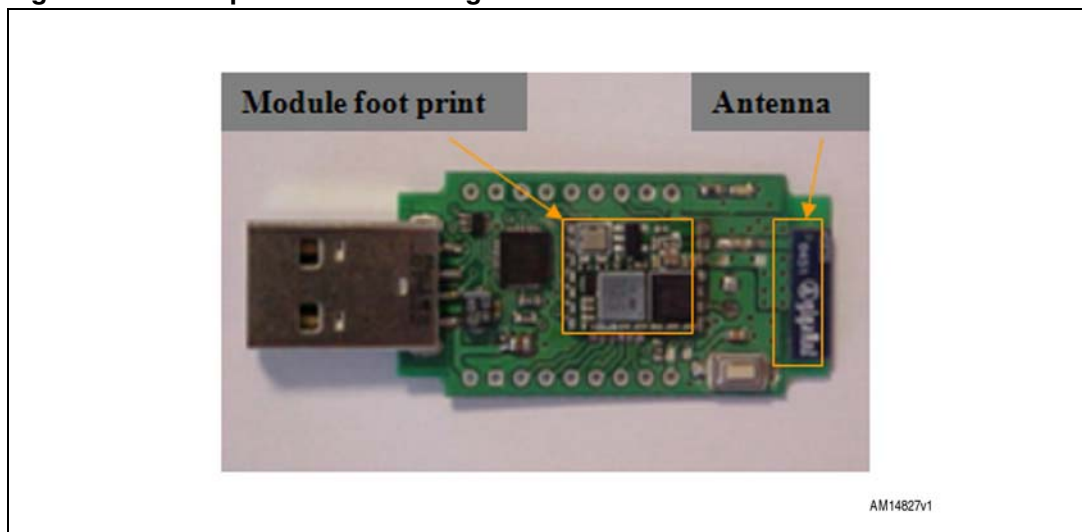
8 Application information

Here below there are some suggestions to better implement the module in the final application.

- Avoid that traces with switching signals are routed on the motherboard below the module. The best condition would be to have a ground plane underneath the module
- Connect the supply voltage ground of the module with the other grounds present on the motherboard in a star ground configuration.

Keep the RF ground separate from the module supply voltage ground; the two grounds are already connected inside the module in one point, a possible implementation can be seen in [Figure 9](#).

Figure 9. Example of antenna integration on the STEVAL-SPBT2ATV3



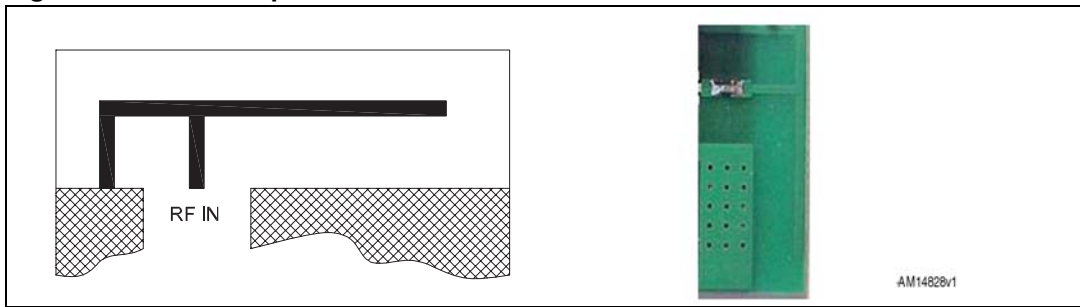
8.1 Antenna choice

The RF output pin must be connected to an antenna which may be:

- Antenna directly printed on the PCB ([Figure 10](#))
- Integrated SMD antenna, including but not limited to the following examples ([Figure 11](#)):
 - Johanson Technology 2450T18A100S
 - Antenova 30-30-A5839-01
 - Murata ANCV12G44SAA127
 - Pulse W3008
 - Yageo CAN4311153002451K.

The external antenna connected by means of an SMA connector ([Figure 12](#)).

Figure 10. Antenna printed on PCB



Note: This is an antenna design indication. Since antenna dimension depends on PCB material, thickness, ϵr constant and design, among other parameters, to dimension it correctly, please refer to antenna calculator literature.

Figure 11. SMD antenna

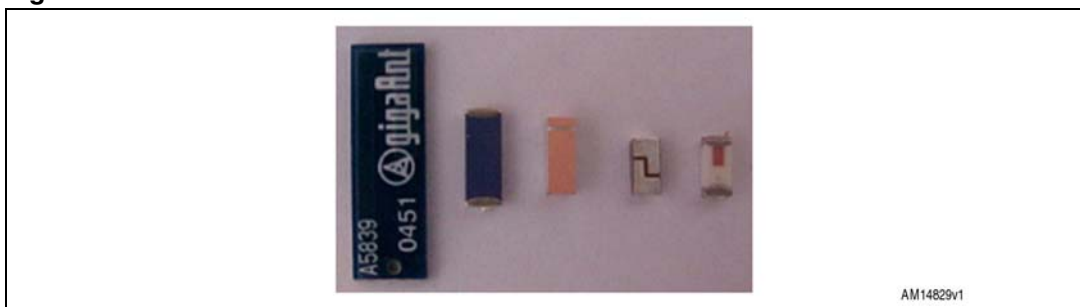
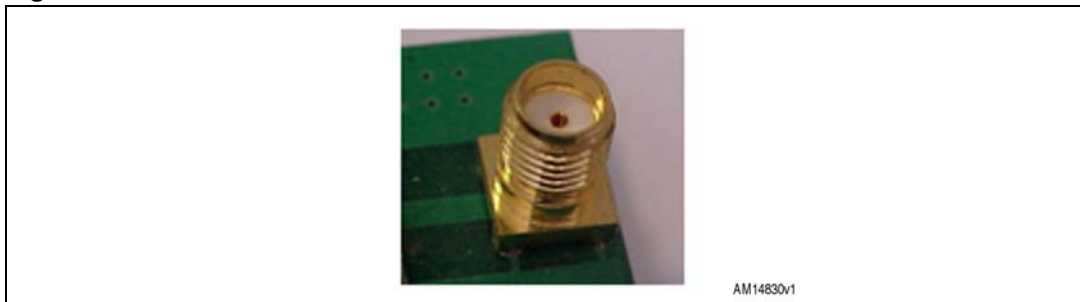


Figure 12. SMA connector for external antenna



8.2 Antenna coupling

Despite the type of antenna chosen, the connection between the RF out pin and the antenna must be realized to get the maximum power transfer.

As a general rule, the characteristic impedance (Z_0) of the connection must be fixed at the value of $50\ \Omega$. The connection trace must be matched to respect such a condition.

$50\ \Omega$ matching depends on various factors and elements that must be taken into consideration:

- Type of material, i.e. FR4 or others
- The electrical characteristics of the material, among them the electric constant, ϵ_r , at 2.4 GHz
- PCB and traces mechanical dimensions:
 - PCB thickness
 - Reference ground thickness
 - Trace width
 - Trace thickness.

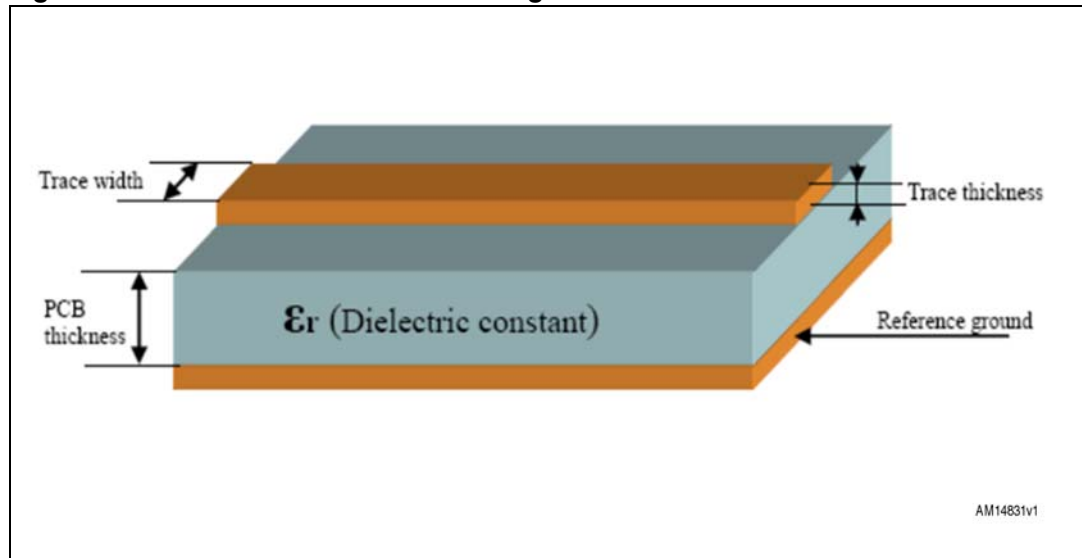
8.3 Example of trace calculation

Example of strip line calculation:

- To get a strip line of $50\ \Omega$, using a 1 mm thick FR4 board, with an $\epsilon_r = 4.3$ at 2.4 GHz, with Cu thickness of $41\ \mu\text{m}$, the strip line width must be 1.9 mm (micro strip type calculation).

Tools for calculating the characteristic impedance, based on the physical and mechanical characteristics of the PCB, can be easily found online.

Figure 13. Parameters for trace matching

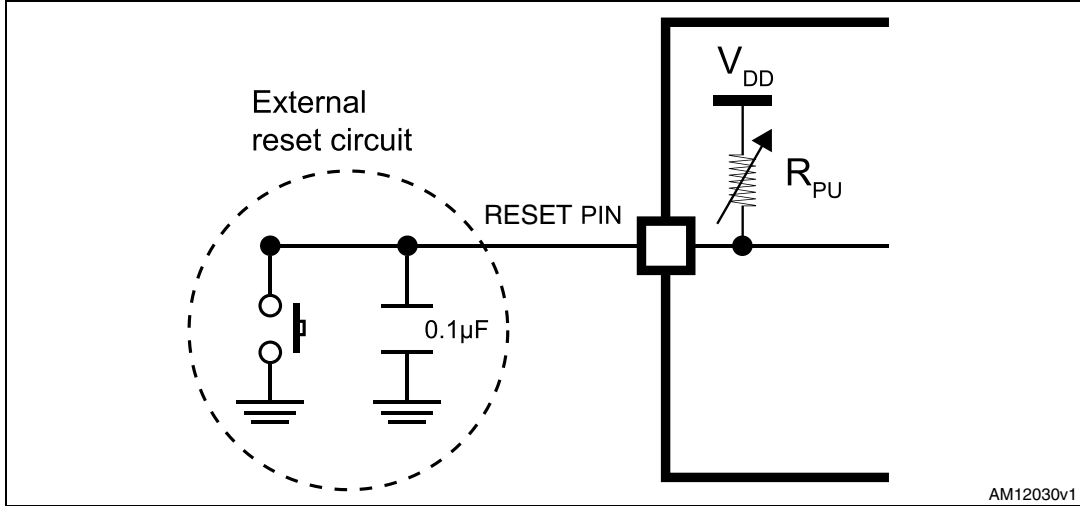


8.4 Reset circuit

Two types of system reset circuits are detailed below.

8.4.1 External reset circuit

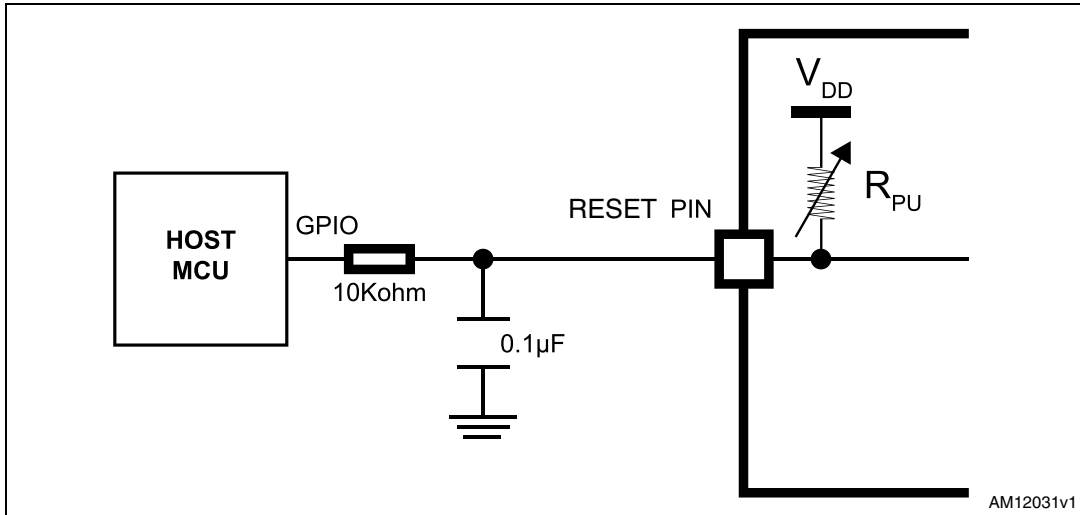
Figure 14. External reset circuit



Note: R_{PU} ranges from 30 kΩ to 50 kΩ internally.

8.4.2 Internal reset circuit

Figure 15. Internal reset circuit



- Note:
- 1 R_{PU} ranges from 30 kΩ to 50 kΩ internally.
 - 2 R_{RST} should be from 1 kΩ to 10 kΩ

9 Regulatory compliance

- BQB
 - BQB qualified design, QD ID: B016360
 - Product type: End Product
 - TGP version: Core 2.1/2.1 + EDR TCRL-2009-1
 - Core spec version: 2.1/2.1 + EDR
 - Product descriptions: Bluetooth module

 - CE
 - CE Expert opinion: 307-ARAJ00079
 - Measurements have been performed in accordance with (report available on request):
 - EN 300 328 V 1.7.1 (2006-10) ^(a)
 - EN 301 489-17 V 2.1.1 (2009) ^(b)
 - EN60950-1:2006 +A11:2009+A1:2010 ^(c)
- CE certified:



-
- a. EN 300 328 V 1.7.1 (2006-10): “electromagnetic compatibility and radio spectrum matters (ERM); wideband transmission systems; data transmission equipment operating in the 2.4 GHz ISM band and using wideband modulation techniques; harmonized EN covering essential requirements under article 3.2 of the R&TTE directive”.
- b. EN 301 489-17 V 2.1.1 (2009): “electromagnetic compatibility and radio spectrum matters (ERM); electromagnetic compatibility (EMC) standard for radio equipment and services; part 17: specific condition for 2.4 GHz wideband transmission systems and 5 GHz high performance RLAN equipment”.
- c. EN60950-1:2006 +A11:2009+A1:2010: “Information technology equipment - safety”.

10 Ordering information

Table 9. Ordering information

Order code	Description
SPBT2532C2.AT2	Class 2 OEM Bluetooth antenna module