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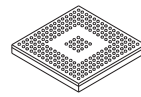
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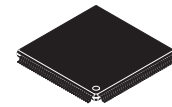
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MPC5510



MAPBGA-208
17 mm x 17 mm



LQFP-144
20 mm x 20 mm

LQFP-176
24 mm x 24 mm

MPC5510 Microcontroller Family Data Sheet

MPC5510 Family Features

- Single issue, 32-bit CPU core complex (e200z1)
 - Compliant with the Power Architecture™ embedded category
 - Includes an instruction set enhancement allowing variable length encoding (VLE) for code size footprint reduction. With the optional encoding of mixed 16-bit and 32-bit instructions, it is possible to achieve significant code size footprint reduction.
- Up to 1.5-Mbyte on-chip flash with flash control unit (FCU)
- Up to 80 Kbytes on-chip SRAM
- Memory protection unit (MPU) with up to sixteen region descriptors and 32-byte region granularity
- Interrupt controller (INTC) capable of handling selectable-priority interrupt sources
- Frequency modulated Phase-locked loop (FMPLL)
- Crossbar switch architecture for concurrent access to peripherals, flash, or RAM from multiple bus masters
- 16-channel enhanced direct memory access controller (eDMA)
- Boot assist module (BAM) supports internal flash programming via a serial link (CAN or SCI)
- Timer supports input/output channels providing a range of 16-bit input capture, output compare, and pulse width modulation functions (eMIOS200)
- Up to 40-channel 12-bit analog-to-digital converter (ADC)
- Up to four serial peripheral interface (DSPI) modules
- Media Local Bus (MLB) emulation logic (works with two DSPIs, the e200z0, the eDMA, and system RAM to create a 3-pin or 5-pin 256Fs MLB protocol)
- Up to eight serial communication interface (eSCI) modules
- Up to six enhanced full CAN (FlexCAN) modules with configurable buffers
- One inter IC communication interface (I²C) module
- Up to 144 configurable general purpose pins supporting input and output operations and 3.0V through 5.5V supply levels
- Real-time counter (RTC_API) with clock source from external 32-kHz crystal oscillator, internal 32-kHz or 16-MHz oscillator and supporting wake-up with selectable 1-second resolution and > 1-hour timeout, or 1-millisecond resolution with maximum timeout of one second
- Up to eight periodic interrupt timers (PIT) with 32-bit counter resolution
- Nexus development interface (NDI) per IEEE-ISTO 5001-2003 Class Two Plus standard
- Device/board test support per Joint Test Action Group (JTAG) of IEEE (IEEE 1149.1)
- On-chip voltage regulator (VREG) for regulation of 5V input to 1.5V and 3.3V internal supply levels
- Optional e200z0, second Power Architecture based I/O processor with VLE instruction set
- Optional FlexRAY controller
- Optional external bus interface (EBI) module

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Table of Contents

1	Pin Assignments and Reset States	4
1.1	Signal Properties and Multiplexing Summary	4
1.2	Power and Ground Supply Summary	15
1.3	Pinout – 144 LQFP	17
1.4	Pinout – 176 LQFP	18
1.5	Pinout – 208 PBGA	19
2	Electrical Characteristics	20
2.1	Maximum Ratings	20
2.2	Thermal Characteristics	21
2.2.1	General Notes for Specifications at Maximum Junction Temperature	21
2.3	ESD Characteristics	24
2.4	DC Electrical Specifications	25
2.5	Operating Current Specifications	27
2.6	I/O Pad Current Specifications	29
2.7	Low Voltage Characteristics	30
2.8	Oscillators Electrical Characteristics	31
2.9	FMPLL Electrical Characteristics	33
2.10	eQADC Electrical Characteristics	34
2.11	Flash Memory Electrical Characteristics	35
2.12	Pad AC Specifications	36
2.13	AC Timing	37
2.13.1	Reset and Boot Configuration Pins	37
2.13.2	External Interrupt (IRQ) and Non-Maskable Interrupt (NMI) Pins	37
2.13.3	JTAG (IEEE 1149.1) Interface	38
2.13.4	Nexus Debug Interface	41
2.13.5	External Bus Interface (EBI)	43
2.13.6	Enhanced Modular I/O Subsystem (eMIOS)	46
2.13.7	Deserial Serial Peripheral Interface (DSPI)	47
3	Package Information	52
4	Product Documentation	52
4.1	Revision History	53

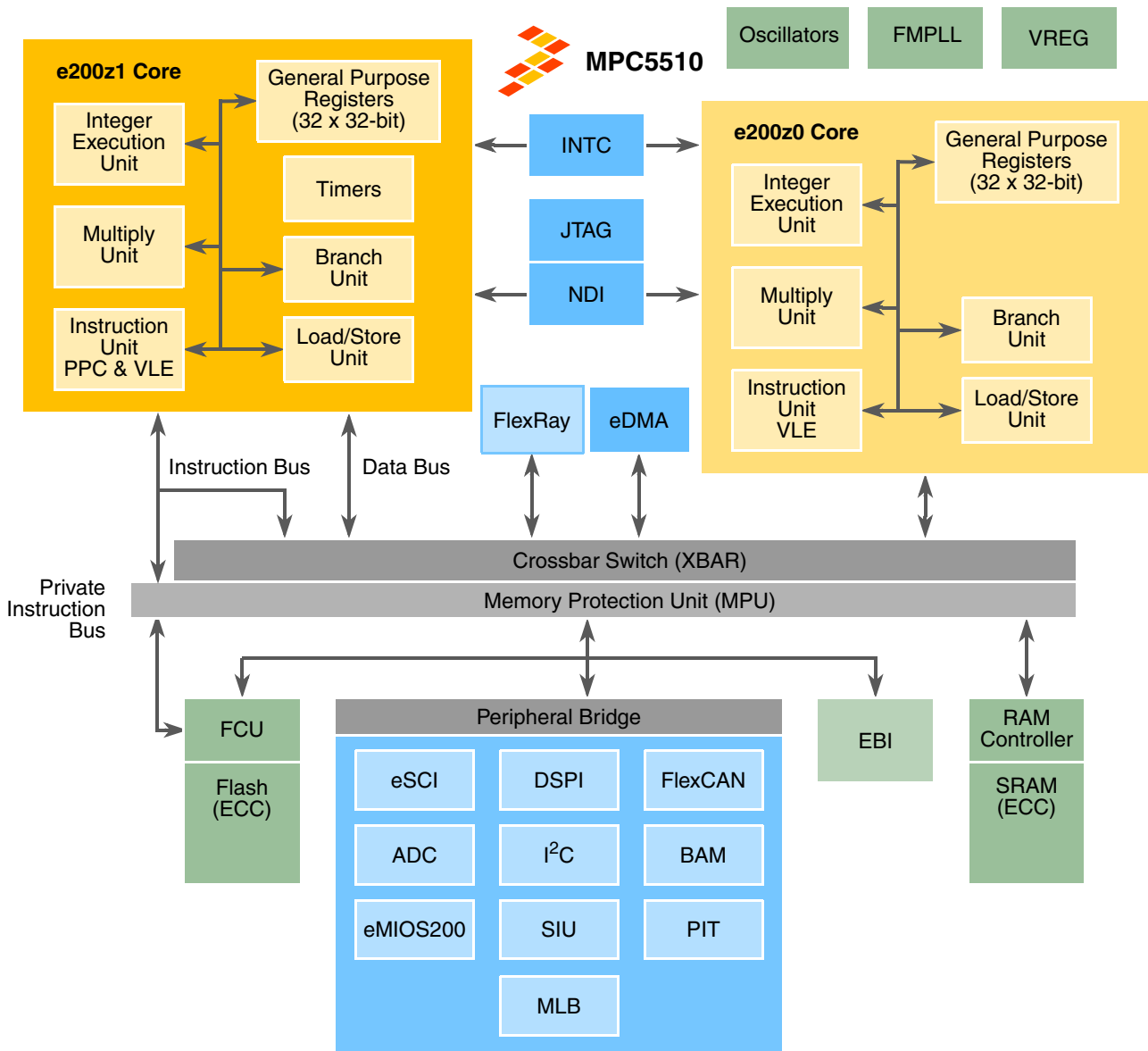
List of Tables

Table 1.	MPC5510 Signal Properties	4
Table 2.	MPC5510 Power/Ground	15
Table 3.	Absolute Maximum Ratings	20
Table 4.	Thermal Characteristics	21
Table 5.	ESD Ratings	24
Table 6.	DC Electrical Specifications	25
Table 7.	Operating Currents	27
Table 8.	I/O Pad Average DC Current	29
Table 9.	Low Voltage Monitors	30
Table 10.	3.3V High Frequency External Oscillator	31
Table 11.	5V Low Frequency (32 kHz) External Oscillator	31
Table 12.	5V High Frequency (16 MHz) Internal RC Oscillator	32

Table 13.	5V Low Frequency (32 kHz) Internal RC Oscillator	32
Table 14.	FMPLL Electrical Specifications	33
Table 15.	eQADC Conversion Specifications (Operating)	34
Table 16.	Flash Program and Erase Specifications	35
Table 17.	Flash EEPROM Module Life (Full Temperature Range)	35
Table 18.	Pad AC Specifications (VDDE = 3.0V - 5.5V)	36
Table 19.	Reset and Boot Configuration Timing	37
Table 20.	IRQ/NMI Timing	37
Table 21.	JTAG Interface Timing	38
Table 22.	Nexus Debug Port Timing	41
Table 23.	External Bus Operation Timing	43
Table 24.	eMIOS Timing	46
Table 25.	DSPI Timing	47
Table 26.	Package Information	52
Table 27.	Revision History of MPC5510 Data Sheet	53

List of Figures

Figure 1.	MPC5510 Family Block Diagram	3
Figure 2.	MPC5510 Pinout – 144 LQFP	17
Figure 3.	MPC5510 Pinout – 176 LQFP	18
Figure 4.	MPC5510 Pinout – 208 PBGA	19
Figure 5.	Pad Output Delay	36
Figure 6.	Reset and Boot Configuration Timing	37
Figure 7.	IRQ and NMI Timing	37
Figure 8.	JTAG Test Clock Input Timing	38
Figure 9.	JTAG Test Access Port Timing	39
Figure 10.	JTAG JCOMP Timing	39
Figure 11.	JTAG Boundary Scan Timing	40
Figure 12.	Nexus Output Timing	41
Figure 13.	Nexus TDI, TMS, TDO Timing	42
Figure 14.	CLKOUT Timing	43
Figure 15.	Synchronous Output Timing	44
Figure 16.	Synchronous Input Timing	45
Figure 17.	Address Latch Enable (ALE) Timing	46
Figure 18.	DSPI Classic SPI Timing — Master, CPHA = 0	48
Figure 19.	DSPI Classic SPI Timing — Master, CPHA = 1	48
Figure 20.	DSPI Classic SPI Timing — Slave, CPHA = 0	49
Figure 21.	DSPI Classic SPI Timing — Slave, CPHA = 1	49
Figure 22.	DSPI Modified Transfer Format Timing — Master, CPHA = 0	50
Figure 23.	DSPI Modified Transfer Format Timing — Master, CPHA = 1	50
Figure 24.	DSPI Modified Transfer Format Timing — Slave, CPHA = 0	51
Figure 25.	DSPI Modified Transfer Format Timing — Slave, CPHA = 1	51
Figure 26.	DSPI PCS Strobe (PCSS) Timing	51



LEGEND

- | | |
|--|---|
| ADC – Analog to Digital Converter modules | FlexRay – Dual Channel FlexRay controller |
| BAM – Boot Assist Module | FMPLL – Frequency Modulated Phase Locked Loop module |
| EBI – External Bus Interface module | I²C – Inter IC Controller modules |
| ECC – Error Correction Code | INTC – Interrupt Controller module |
| DSPI – Serial Peripherals Interface controller module | JTAG – Joint Test Action Group interface |
| eDMA – enhanced Direct Memory Controller module | MLB – Media Local Bus emulation logic |
| eMIOS200 – Timed Input Output module | NDI – Nexus Debug Interface module |
| eSCI – Serial Communications Interface modules | PIT – Periodic Interrupt Timer module |
| FCU – Flash Controller Unit | SIU – System Integration module |
| FlexCAN – Controller Area Network controller modules | VREG – Voltage Regulator |

Figure 1. MPC5510 Family Block Diagram

1 Pin Assignments and Reset States

1.1 Signal Properties and Multiplexing Summary

Table 1 shows the signal properties for each pin on the MPC5510. For all port pins, which have an associated pad configuration register (SIU_PCR n register) to control its pin properties, the “Supported Pin Functions” column lists the functions associated with the programming of the SIU_PCR n [PA] bit field in the following order: GPIO, Function1, Function2 and Function3. If fewer than three functions plus GPIO are supported by a given pin, then the unused functions begin with Function3, then Function2, then Function1. Note that the GPIO number is the same number as the corresponding pad configuration register (SIU_PCR n) number.

Table 1. MPC5510 Signal Properties

Pin Name	GPIO (PCR) Num ¹	Supported Functions ²	Description	I/O Type	Voltage ³	Pad ⁴ Type	Status During Reset ⁵	Status After Reset ⁵	Package Pin Locations		
									144	176	208
Port A (16)											
PA0	0	PA0 AN0	GPI eQADC Analog Input	I I	V _{DDA}	AE + IH	—	—	9	9	E3
PA1	1	PA1 AN1	GPI eQADC Analog Input	I I	V _{DDA}	AE + IH	—	—	8	8	E2
PA2	2	PA2 AN2	GPI eQADC Analog Input	I I	V _{DDA}	AE + IH	—	—	7	7	E1
PA3	3	PA3 AN3	GPI eQADC Analog Input	I I	V _{DDA}	AE + IH	—	—	6	6	D3
PA4	4	PA4 AN4	GPI eQADC Analog Input	I I	V _{DDA}	AE + IH	—	—	5	5	D2
PA5	5	PA5 AN5	GPI eQADC Analog Input	I I	V _{DDA}	AE + IH	—	—	4	4	D1
PA6	6	PA6 AN6	GPI eQADC Analog Input	I I	V _{DDA}	AE + IH	—	—	3	3	C2
PA7	7	PA7 AN7	GPI eQADC Analog Input	I I	V _{DDA}	AE + IH	—	—	2	2	C1
PA8	8	PA8 AN8/ANW	GPI eQADC Analog Input	I I	V _{DDA}	AE + IH	—	—	143	175	A3
PA9	9	PA9 AN9/ANX	GPI eQADC Analog Input	I I	V _{DDA}	AE + IH	—	—	142	174	C4
PA10	10	PA10 AN10/ANY	GPI eQADC Analog Input	I I	V _{DDA}	AE + IH	—	—	140	172	D5
PA11	11	PA11 AN11/ANZ	GPI eQADC Analog Input	I I	V _{DDA}	AE + IH	—	—	139	171	C5
PA12	12	PA12 AN12	GPI eQADC Analog Input	I I	V _{DDA}	AE + IH	—	—	138	170	B5
PA13	13	PA13 AN13	GPI eQADC Analog Input	I I	V _{DDA}	AE + IH	—	—	137	169	A5
PA14	14	PA14 AN14 EXTAL32 ⁶	GPI eQADC Analog Input 32 kHz Crystal Oscillator Input	I I I	V _{DDA}	AE + IH	—	—	136	167	D6

Table 1. MPC5510 Signal Properties (continued)

Pin Name	GPIO (PCR) Num ¹	Supported Functions ²	Description	I/O Type	Voltage ³	Pad ⁴ Type	Status During Reset ⁵	Status After Reset ⁵	Package Pin Locations		
									144	176	208
PA15	15	PA15 AN15 XTAL32 ⁶	GPI eQADC Analog Input 32 kHz Crystal Oscillator Output	I I O	V _{DDE1}	AE + IH	—	—	135	165	C6
Port B (16)											
PB0	16	PB0 AN28 eMIOS16 PCS_C5	GPIO eQADC Analog Input ⁷ eMIOS Channel DSPI_C Peripheral Chip Select	I/O I O O	V _{DDE1}	A + SH	—	—	134	162	C7
PB1	17	PB1 AN29 eMIOS17 PCS_C4	GPIO eQADC Analog Input ⁷ eMIOS Channel DSPI_C Peripheral Chip Select	I/O I O O	V _{DDE1}	A + SH	—	—	133	161	D7
PB2	18	PB2 AN30 eMIOS18 PCS_C3	GPIO eQADC Analog Input ⁷ eMIOS Channel DSPI_C Peripheral Chip Select	I/O I O O	V _{DDE1}	A + SH	—	—	132	160	A8
PB3	19	PB3 AN31 PCS_C2	GPIO eQADC Analog Input ⁷ DSPI_C Peripheral Chip Select	I/O I O	V _{DDE1}	A + SH	—	—	131	159	B8
PB4	20	PB4 AN32 PCS_C1	GPIO eQADC Analog Input ⁷ DSPI_C Peripheral Chip Select	I/O I O	V _{DDE1}	A + SH	—	—	130	158	C8
PB5	21	PB5 AN33 PCS_C0	GPIO eQADC Analog Input ⁷ DSPI_C Peripheral Chip Select	I/O I I/O	V _{DDE1}	A + SH	—	—	129	157	D8
PB6	22	PB6 AN34 SCK_C	GPIO eQADC Analog Input ⁷ DSPI_C Clock	I/O I I/O	V _{DDE1}	A + SH	—	—	128	156	A9
PB7	23	PB7 AN35 SOUT_C	GPIO eQADC Analog Input ⁷ DSPI_C Data Output	I/O I O	V _{DDE1}	A + SH	—	—	127	153	B9
PB8	24	PB8 AN36 SIN_C	GPIO eQADC Analog Input ⁷ DSPI_C Data Input	I/O I I	V _{DDE1}	A + SH	—	—	126	152	C9
PB9	25	PB9 AN37 CNTX_D PCS_B4	GPIO eQADC Analog Input ⁷ CAN_D Transmit DSPI_B Peripheral Chip Select	I/O I O O	V _{DDE1}	A + SH	—	—	125	151	D9
PB10	26	PB10 AN38 CNRX_D PCS_B3	GPIO eQADC Analog Input ⁷ CAN_D Receive DSPI_B Peripheral Chip Select	I/O I I O	V _{DDE1}	A + SH	—	—	124	150	A10
PB11	27	PB11 AN39 eMIOS19 PCS_B5	GPIO eQADC Analog Input ⁷ eMIOS Channel DSPI_B Peripheral Chip Select	I/O I O O	V _{DDE1}	A + SH	—	—	123	149	B10

Table 1. MPC5510 Signal Properties (continued)

Pin Name	GPIO (PCR) Num ¹	Supported Functions ²	Description	I/O Type	Voltage ³	Pad ⁴ Type	Status During Reset ⁵	Status After Reset ⁵	Package Pin Locations		
									144	176	208
PB12	28	PB12 TXD_G PCS_B4	GPIO SCI_G Transmit DSPI_B Peripheral Chip Select	I/O O O	V _{DDE1}	SH	—	—	—	164	A7
PB13	29	PB13 RXD_G PCS_B3	GPIO SCI_G Receive DSPI_B Peripheral Chip Select	I/O I O	V _{DDE1}	SH	—	—	—	163	B7
PB14	30	PB14 TXD_H	GPIO SCI_H Transmit	I/O O	V _{DDE1}	SH	—	—	—	148	C10
PB15	31	PB15 RXD_H	GPIO SCI_H Receive	I/O I	V _{DDE1}	SH	—	—	—	147	A11
Port C (16)											
PC0	32	PC0 eMIOS0 FR_A_TX_EN AD24	GPIO eMIOS Channel FlexRay Channel A Transmit Enable EBI Muxed Address/Data	I/O I/O O I/O	V _{DDE1}	MH	—	—	122	146	B11
PC1	33	PC1 eMIOS1 FR_A_TX AD16	GPIO eMIOS Channel FlexRay Channel A Transmit EBI Muxed Address/Data	I/O I/O O I/O	V _{DDE1}	MH	—	—	121	145	C11
PC2	34	PC2 eMIOS2 FR_A_RX TS	GPIO eMIOS Channel FlexRay Channel A Receive EBI Transfer Start	I/O I/O I I/O	V _{DDE1}	MH	—	—	120	144	D11
PC3	35	PC3 eMIOS3 FR_DBG0	GPIO eMIOS Channel FlexRay Debug	I/O I/O O	V _{DDE1}	MH	—	—	117	141	A12
PC4	36	PC4 eMIOS4 FR_DBG1	GPIO eMIOS Channel FlexRay Debug	I/O I/O O	V _{DDE1}	SH	—	—	116	140	B12
PC5	37	PC5 eMIOS5 FR_DBG2	GPIO eMIOS Channel FlexRay Debug	I/O I/O O	V _{DDE1}	SH	—	—	115	139	C12
PC6	38	PC6 eMIOS6 FR_DBG3	GPIO eMIOS Channel FlexRay Debug	I/O I/O O	V _{DDE1}	SH	—	—	114	138	D12
PC7	39	PC7 eMIOS7 FR_B_RX	GPIO eMIOS Channel FlexRay Channel B Receive	I/O I/O I	V _{DDE1}	SH	—	—	113	137	A13
PC8	40	PC8 eMIOS8 FR_B_TX AD15	GPIO eMIOS Channel FlexRay Channel B Transmit EBI Muxed Address/Data	I/O I/O O I/O	V _{DDE1}	MH	—	—	112	136	B13
PC9	41	PC9 eMIOS9 FR_B_TX_EN AD14	GPIO eMIOS Channel FlexRay Channel B Transmit Enable EBI Muxed Address/Data	I/O I/O O I/O	V _{DDE1}	MH	—	—	111	135	C13

Table 1. MPC5510 Signal Properties (continued)

Pin Name	GPIO (PCR) Num ¹	Supported Functions ²	Description	I/O Type	Voltage ³	Pad ⁴ Type	Status During Reset ⁵	Status After Reset ⁵	Package Pin Locations		
									144	176	208
PC10	42	PC10 eMIOS10 PCS_C5 SCK_D	GPIO eMIOS Channel DSPI_C Peripheral Chip Select DSPI_D Clock	I/O I/O O I/O	V _{DDE1}	SH	—	—	110	134	A14
PC11	43	PC11 eMIOS11 PCS_C4 SOUT_D	GPIO eMIOS Channel DSPI_C Peripheral Chip Select DSPI_D Serial Out	I/O I/O O O	V _{DDE1}	SH	—	—	109	133	B14
PC12	44	PC12 eMIOS12 PSC_C3 SIN_D	GPIO eMIOS Channel DSPI_C Peripheral Chip Select DSPI_D Serial In	I/O I/O O I	V _{DDE1}	SH	—	—	108	132	B16
PC13	45	PC13 eMIOS13 PCS_A5 PCS_D0	GPIO eMIOS Channel DSPI_A Peripheral Chip Select DSPI_D Peripheral Chip Select	I/O I/O O O	V _{DDE1}	SH	—	—	107	131	C15
PC14	46	PC14 eMIOS14 PCS_A4 PCS_D1	GPIO eMIOS Channel DSPI_A Peripheral Chip Select DSPI_D Peripheral Chip Select	I/O I/O O O	V _{DDE1}	SH	—	—	106	130	C16
PC15	47	PC15 eMIOS15 PCS_A3 PCS_D2	GPIO eMIOS Channel DSPI_A Peripheral Chip Select DSPI_D Peripheral Chip Select	I/O I/O O O	V _{DDE1}	SH	—	—	105	129	D14
Port D (16)											
PD0	48	PD0 CNTX_A PCS_D3	GPIO CAN_A Transmit DSPI_D Peripheral Chip Select	I/O O O	V _{DDE1}	SH	—	—	104	128	D15
PD1	49	PD1 CNRX_A PCS_D4	GPIO CAN_A Receive DSPI_D Peripheral Chip Select	I/O I O	V _{DDE1}	SH	—	—	103	127	D16
PD2	50	PD2 CNRX_B eMIOS10 BOOTCFG PCS_D5	GPIO CAN_B Receive eMIOS Channel Boot Configuration DSPI_D Peripheral Chip Select	I/O I O I O	V _{DDE1}	SH	BOOTCFG (Pulldown)	GPI (Pulldown)	102	126	E14
PD3	51	PD3 CNTX_B eMIOS11	GPIO CAN_B Transmit eMIOS Channel	I/O O O	V _{DDE1}	SH	—	—	101	125	E15
PD4	52	PD4 CNTX_C eMIOS12	GPIO CAN_C Transmit eMIOS Channel	I/O O O	V _{DDE1}	SH	—	—	100	124	E16
PD5	53	PD5 CNRX_C eMIOS13	GPIO CAN_C Receive eMIOS Channel	I/O I O	V _{DDE1}	SH	—	—	99	123	F13

Table 1. MPC5510 Signal Properties (continued)

Pin Name	GPIO (PCR) Num ¹	Supported Functions ²	Description	I/O Type	Voltage ³	Pad ⁴ Type	Status During Reset ⁵	Status After Reset ⁵	Package Pin Locations		
									144	176	208
PD6	54	PD6 TXD_A eMIOS14	GPIO SCI_A Transmit eMIOS Channel	I/O O O	V _{DDE1}	SH	—	—	98	122	F14
PD7	55	PD7 RXD_A eMIOS15	GPIO SCI_A Receive eMIOS Channel	I/O I O	V _{DDE1}	SH	—	—	97	121	F15
PD8	56	PD8 TXD_B SCL_A	GPIO SCI_B Transmit I ² C Serial Clock Line	I/O O I/O	V _{DDE1}	SH	—	—	94	118	G13
PD9	57	PD9 RXD_B SDA_A	GPIO SCI_B Receive I ² C Serial Data Line	I/O I I/O	V _{DDE1}	SH	—	—	93	117	F16
PD10	58	PD10 PCS_B2 CNTX_F NMIO	GPIO DSPI_B Peripheral Chip Select CAN_F Transmit NMI Input for Z1 Core	I/O O O I	V _{DDE1}	SH	—	—	92	116	G14
PD11	59	PD11 PCS_B1 CNRX_F NMI1	GPIO DSPI_B Peripheral Chip Select CAN_F Receive NMI Input for Z0 Core	I/O O I I	V _{DDE1}	SH	—	—	91	115	G15
PD12	60	PD12 PCS_B0 eMIOS9	GPIO DSPI_B Peripheral Chip Select eMIOS Channel	I/O I/O O	V _{DDE1}	SH	—	—	90	114	H14
PD13	61	PD13 SCK_B eMIOS8	GPIO DSPI_B Clock eMIOS Channel	I/O I/O O	V _{DDE1}	SH	—	—	89	113	H15
PD14	62	PD14 SOUT_B eMIOS7	GPIO DSPI_B Data Output eMIOS Channel	I/O O O	V _{DDE1}	SH	—	—	88	110	J14
PD15	63	PD15 SIN_B eMIOS6	GPIO DSPI_B Data Input eMIOS Channel	I/O I O	V _{DDE1}	SH	—	—	87	107	K14
Port E (16)											
PE0	64	PE0 PCS_A2 eMIOS5 MLBCLK	GPIO DSPI_A Peripheral Chip Select eMIOS Channel MLB Clock	I/O O O I	V _{DDE1}	SH	—	—	86	106	K16
PE1	65	PE1 PCS_A1 eMIOS4 MLBSI / MLBSIG	GPIO DSPI_A Peripheral Chip Select eMIOS Channel MLB Signal In (5-pin) / MLB Bi-directional Signal (3-pin)	I/O O O I I/O	V _{DDE1}	MH	—	—	85	103	L14
PE2	66	PE2 PCS_A0 eMIOS3 MLBDI / MLBDAT	GPIO DSPI_A Peripheral Chip Select eMIOS Channel MLB Data In (5-pin) / MLB Bi-directional Data (3-pin)	I/O I/O O I I/O	V _{DDE1}	MH	—	—	84	101	L15

Table 1. MPC5510 Signal Properties (continued)

Pin Name	GPIO (PCR) Num ¹	Supported Functions ²	Description	I/O Type	Voltage ³	Pad ⁴ Type	Status During Reset ⁵	Status After Reset ⁵	Package Pin Locations		
									144	176	208
PE3	67	PE3 SCK_A eMIOS2 MLBSO / MLBSIG_BUFEN	GPIO DSPI_A Clock eMIOS Channel MLB Signal Out (5-pin) / MLB Signal Level Shifter Enable (3-pin)	I/O I/O O O O	V _{DDE1}	MH	—	—	83	100	M13
PE4	68	PE4 SOUT_A eMIOS1 MLBDO / MLBDAT_BUFEN	GPIO DSPI_A Data Out eMIOS Channel MLB Data Out (5-pin) / MLB Data Level Shifter Enable (3-pin)	I/O O O O O	V _{DDE1}	MH	—	—	82	98	N14
PE5	69	PE5 SIN_A eMIOS0 MLB_SLOT / MLB_SIGOBS / MLB_DATOBS	GPIO DSPI_A Data In eMIOS Channel MLB Slot Debug / MLB Clock Adjust Observe Signal / MLB Clock Adjust Observe Data	I/O I O O O O	V _{DDE1}	MH	—	—	81	97	M15
PE6	70	PE6 CLKOUT	GPIO System Clock Output	I/O O	V _{DDE3}	MH	—	—	67	83	P13
PE7	71	PE7	GPIO	I/O	V _{DDE1}	SH	—	—	—	—	H13
PE8	72	PE8	GPIO	I/O	V _{DDE1}	SH	—	—	—	—	H16
PE9	72	PE9	GPIO	I/O	V _{DDE1}	SH	—	—	—	—	J13
PE10	74	PE10	GPIO	I/O	V _{DDE1}	SH	—	—	—	112	J16
PE11	75	PE11	GPIO	I/O	V _{DDE1}	SH	—	—	—	111	J15
PE12	76	PE12	GPIO	I/O	V _{DDE1}	SH	—	—	—	109	K13
PE13	77	PE13	GPIO	I/O	V _{DDE1}	SH	—	—	—	108	L13
PE14	78	PE14	GPIO	I/O	V _{DDE1}	SH	—	—	—	102	L16
PE15	79	PE15	GPIO	I/O	V _{DDE1}	SH	—	—	—	99	M14
Port F (16)											
PF0	80	PF0 RD_W \overline{R} EVTI ⁸	GPIO EBI Read/Write Nexus Event In	I/O I/O I	V _{DDE3}	MH	—	—	66	82	N12
PF1	81	PF1 T \overline{A} MLBCLK EVTO ⁸	GPIO EBI Transfer Acknowledge MLB Clock Nexus Event Out	I/O I/O I O	V _{DDE3}	MH	—	—	65	81	P12
PF2	82	PF2 AD8 ADDR8 MLBSI / MLBSIG MSEO ⁸	GPIO EBI Muxed Address/Data EBI Non Muxed Address MLB Signal In (5-pin) / MLB Bi-Directional Signal (3-pin) Nexus Message Start/End Out	I/O I/O O I I/O O	V _{DDE3}	MH	—	—	64	80	R12

Table 1. MPC5510 Signal Properties (continued)

Pin Name	GPIO (PCR) Num ¹	Supported Functions ²	Description	I/O Type	Voltage ³	Pad ⁴ Type	Status During Reset ⁵	Status After Reset ⁵	Package Pin Locations		
									144	176	208
PF3	83	PF3 AD9 ADDR9 MLBDI / MLBDAT MCKO ⁸	GPIO EBI Muxed Address/Data EBI Non Muxed Address MLB Data In (5-pin) / MLB Bi-directional Data (3-pin) Nexus Message Clock Out	I/O I/O O I I/O O	V _{DDE3}	MH	—	—	63	79	T12
PF4	84	PF4 AD10 ADDR10 MLBSO / MLBSIG_BUFEN MDO0 ⁸	GPIO EBI Muxed Address/Data EBI Non Muxed Address MLB Signal Out (5-pin) / MLB Signal Level Shifter Enable (3-pin) Nexus Message Data Out	I/O I/O O O O O	V _{DDE3}	MH	—	—	59	74	T10
PF5	85	PF5 AD11 ADDR11 MLBDO / MLBDAT_BUFEN MDO1 ⁸	GPIO EBI Muxed Address/Data EBI Non Muxed Address MLB Data Out (5-pin) / MLB Data Level Shifter Enable (3-pin) Nexus Message Data Out	I/O I/O O O O O	V _{DDE3}	MH	—	—	58	72	R9
PF6	86	PF6 AD12 ADDR12 MLB_SLOT / MLB_SIGOBS / MLB_DATOBS MDO2 ⁸	GPIO EBI Muxed Address/Data EBI Non Muxed Address MLB Slot Debug / MLB Clock Adjust Observe Signal / MLB Clock Adjust Observe Data Nexus Message Data Out	I/O I/O O O O O O	V _{DDE3}	MH	—	—	57	68	T8
PF7	87	PF7 AD13 ADDR13 MDO3 ⁸	GPIO EBI Muxed Address/Data EBI Non Muxed Address Nexus Message Data Out	I/O I/O O O	V _{DDE3}	MH	—	—	56	66	P8
PF8	88	PF8 AD14 ADDR14 MDO4 ⁸	GPIO EBI Muxed Address/Data EBI Non Muxed Address Nexus Message Data Out	I/O I/O O O	V _{DDE2}	MH	—	—	55	65	N8
PF9	89	PF9 AD15 ADDR15 MDO5 ⁸	GPIO EBI Muxed Address/Data EBI Non Muxed Address Nexus Message Data Out	I/O I/O O O	V _{DDE2}	MH	—	—	54	64	T7
PF10	90	PF10 $\overline{CS1}$ TXD_C MDO6 ⁸	GPIO EBI Chip Select SCI_C Transmit Nexus Message Data Out	I/O O O O	V _{DDE2}	MH	—	—	52	62	R7
PF11	91	PF11 $\overline{CS0}$ RXD_C MDO7 ⁸	GPIO EBI Chip Select SCI_C Receive Nexus Message Data Out	I/O O I O	V _{DDE2}	MH	—	—	51	61	P7
PF12	92	PF12 \overline{TS} TXD_D ALE	GPIO EBI Transfer Start SCI_D Transmit EBI Address Latch Enable	I/O I/O O O	V _{DDE2}	MH	—	—	50	60	N7

Table 1. MPC5510 Signal Properties (continued)

Pin Name	GPIO (PCR) Num ¹	Supported Functions ²	Description	I/O Type	Voltage ³	Pad ⁴ Type	Status During Reset ⁵	Status After Reset ⁵	Package Pin Locations		
									144	176	208
PF13	93	PF13 \overline{OE} RXD_D	GPIO EBI Output Enable SCI_D Receive	I/O O I	V _{DDE2}	MH	—	—	49	59	R6
PF14	94	PF14 $\overline{WE0}$ BDIP CNTX_D	GPIO EBI Write Enable EBI Burst Data In Progress CAN_D Transmit	I/O O O O	V _{DDE2}	MH	—	—	45	55	P6
PF15	95	PF15 $\overline{WE1}$ TEA CNRX_D	GPIO EBI Write Enable EBI Transfer Error Acknowledge CAN_D Receive	I/O O I/O I	V _{DDE2}	MH	—	—	44	54	N6
Port G (16)											
PG0	96	PG0 AD16 eMIOS16	GPIO EBI Muxed Address/Data eMIOS Channel	I/O I/O I/O	V _{DDE2}	MH	—	—	43	51	P5
PG1	97	PG1 AD17 eMIOS17 SIN_C	GPIO EBI Muxed Address/Data eMIOS Channel DSPI_C Serial In	I/O I/O I/O I	V _{DDE2}	MH	—	—	42	50	T4
PG2	98	PG2 AD18 eMIOS18 SOUT_C	GPIO EBI Muxed Address/Data eMIOS Channel DSPI_C Serial Out	I/O I/O I/O O	V _{DDE2}	MH	—	—	41	49	R4
PG3	99	PG3 AD19 eMIOS19 SCK_C	GPIO EBI Muxed Address/Data eMIOS Channel DSPI_C Serial Clock	I/O I/O I/O I/O	V _{DDE2}	MH	—	—	40	48	P4
PG4	100	PG4 AD20 eMIOS20 PCS_C0	GPIO EBI Muxed Address/Data eMIOS Channel DSPI_C Peripheral Chip Select	I/O I/O I/O I/O	V _{DDE2}	MH	—	—	39	47	T3
PG5	101	PG5 AD21 eMIOS21	GPIO EBI Muxed Address/Data eMIOS Channel	I/O I/O I/O	V _{DDE2}	MH	—	—	38	46	R3
PG6	102	PG6 AD22 eMIOS22	GPIO EBI Muxed Address/Data eMIOS Channel	I/O I/O I/O	V _{DDE2}	MH	—	—	37	45	T2
PG7	103	PG7 AD23 eMIOS23 RXD_C	GPIO EBI Muxed Address/Data eMIOS Channel SCI_C Receive	I/O I/O I/O I	V _{DDE2}	MH	—	—	36	44	R1
PG8	104	PG8 AD24 PCS_A4	GPIO EBI Muxed Address/Data DSPI_A Peripheral Chip Select	I/O I/O O	V _{DDE2}	MH	—	—	35	43	P2

Table 1. MPC5510 Signal Properties (continued)

Pin Name	GPIO (PCR) Num ¹	Supported Functions ²	Description	I/O Type	Voltage ³	Pad ⁴ Type	Status During Reset ⁵	Status After Reset ⁵	Package Pin Locations		
									144	176	208
PG9	105	PG9 AD25 PCS_A3 TXD_C	GPIO EBI Muxed Address/Data DSPI_A Peripheral Chip Select SCI_C Transmit	I/O I/O O O	V _{DDE2}	MH	—	—	34	42	N3
PG10	106	PG10 AD26 PCS_A2	GPIO EBI Muxed Address/Data DSPI_A Peripheral Chip Select	I/O I/O O	V _{DDE2}	MH	—	—	30	38	N2
PG11	107	PG11 AD27 PCS_A1	GPIO EBI Muxed Address/Data DSPI_A Peripheral Chip Select	I/O I/O O	V _{DDE2}	MH	—	—	29	37	N1
PG12	108	PG12 AD28 PCS_A0	GPIO EBI Muxed Address/Data DSPI_A Peripheral Chip Select	I/O I/O I/O	V _{DDE2}	MH	—	—	28	36	M4
PG13	109	PG13 AD29 SCK_A	GPIO EBI Muxed Address/Data DSPI_A Clock	I/O I/O I/O	V _{DDE2}	MH	—	—	27	35	M3
PG14	110	PG14 AD30 SOUT_A	GPIO EBI Muxed Address/Data DSPI_A Data Out	I/O I/O O	V _{DDE2}	MH	—	—	26	34	M2
PG15	111	PG15 AD31 SIN_A	GPIO EBI Muxed Address/Data DSPI_A Data In	I/O I/O I	V _{DDE2}	MH	—	—	25	33	M1
Port H (16)											
PH0	112	PH0 AN27 eMIOS20 SCL_A	GPIO eQADC Analog Input ⁷ eMIOS Channel I ² C_A Serial Clock	I/O I O I/O	V _{DDE2}	A + SH	—	—	24	32	L3
PH1	113	PH1 AN26 eMIOS21 SDA_A	GPIO eQADC Analog Input ⁷ eMIOS Channel I ² C_A Serial Data	I/O I O I/O	V _{DDE2}	A + SH	—	—	23	31	L2
PH2	114	PH2 AN25 eMIOS22 CS3	GPIO eQADC Analog Input ⁷ eMIOS Channel EBI Chip Select	I/O I O O	V _{DDE2}	A + MH	—	—	22	30	L1
PH3	115	PH3 AN24 eMIOS23 CS2	GPIO eQADC Analog Input ⁷ eMIOS Channel EBI Chip Select	I/O I O O	V _{DDE2}	A + MH	—	—	21	29	K4
PH4	116	PH4 AN23 TXD_E MA2	GPIO eQADC Analog Input ⁷ SCI_E Transmit eQADC External Mux Address	I/O I O O	V _{DDE2}	A + SH	—	—	20	28	K3
PH5	117	PH5 AN22 RXD_E MA1	GPIO eQADC Analog Input ⁷ SCI_E Receive eQADC External Mux Address	I/O I I O	V _{DDE2}	A + SH	—	—	19	24	J3

Table 1. MPC5510 Signal Properties (continued)

Pin Name	GPIO (PCR) Num ¹	Supported Functions ²	Description	I/O Type	Voltage ³	Pad ⁴ Type	Status During Reset ⁵	Status After Reset ⁵	Package Pin Locations		
									144	176	208
PH6	118	PH6 AN21 TXD_F	GPIO eQADC Analog Input ⁷ SCI_F Transmit	I/O I O	V _{DDE2}	A + SH	—	—	18	23	J2
PH7	119	PH7 AN20 RXD_F	GPIO eQADC Analog Input ⁷ SCI_F Receive	I/O I I	V _{DDE2}	A + SH	—	—	17	22	J1
PH8	120	PH8 AN19 CNTX_E MA0	GPIO eQADC Analog Input ⁷ CAN_E Transmit eQADC External Mux Address	I/O I O O	V _{DDE2}	A + SH	—	—	14	17	H1
PH9	121	PH9 AN18/ANT CNRX_E	GPIO eQADC Analog Input ⁷ CAN_E Receive	I/O I I	V _{DDE2}	A + SH	—	—	13	14	G2
PH10	122	PH10 AN17/ANS CNRX_F	GPIO eQADC Analog Input ⁷ CAN_F Receive	I/O I I	V _{DDE2}	A + SH	—	—	12	12	F4
PH11	123	PH11 AN16/ANR CNTX_F	GPIO eQADC Analog Input ⁷ CAN_F Transmit	I/O I O	V _{DDE2}	A + SH	—	—	11	11	F3
PH12	124	PH12 PCS_D5	GPIO DSPI_D Peripheral Chip Select	I/O O	V _{DDE2}	SH	—	—	—	—	F2
PH13	125	PH13	GPIO	I/O	V _{DDE2}	SH	—	—	—	—	F1
PH14	126	PH14 WE2	GPIO EBI Write Enable	I/O O	V _{DDE2}	MH	—	—	—	53	T5
PH15	127	PH15 WE3	GPIO EBI Write Enable	I/O O	V _{DDE2}	MH	—	—	—	52	R5
Port J (16)											
PJ0	128	PJ0 AD0	GPIO EBI Muxed Address/Data	I/O I/O	V _{DDE3}	MH	—	—	—	—	N11
PJ1	129	PJ1 AD1	GPIO EBI Muxed Address/Data	I/O I/O	V _{DDE3}	MH	—	—	—	—	P11
PJ2	130	PJ2 AD2	GPIO EBI Muxed Address/Data	I/O I/O	V _{DDE3}	MH	—	—	—	—	N10
PJ3	131	PJ3 AD3	GPIO EBI Muxed Address/Data	I/O I/O	V _{DDE3}	MH	—	—	—	—	R10
PJ4	132	PJ4 AD4	GPIO EBI Muxed Address/Data	I/O I/O	V _{DDE3}	MH	—	—	—	75	P10
PJ5	133	PJ5 AD5	GPIO EBI Muxed Address/Data	I/O I/O	V _{DDE3}	MH	—	—	—	73	T9
PJ6	134	PJ6 AD6	GPIO EBI Muxed Address/Data	I/O I/O	V _{DDE3}	MH	—	—	—	69	P9
PJ7	135	PJ7 AD7	GPIO EBI Muxed Address/Data	I/O I/O	V _{DDE3}	MH	—	—	—	67	R8

Table 1. MPC5510 Signal Properties (continued)

Pin Name	GPIO (PCR) Num ¹	Supported Functions ²	Description	I/O Type	Voltage ³	Pad ⁴ Type	Status During Reset ⁵	Status After Reset ⁵	Package Pin Locations			
									144	176	208	
PJ8	136	PJ8 PCS_D4	GPIO DSPI_D Peripheral Chip Select	I/O I/O	V _{DDE2}	SH	—	—	—	27	K2	
PJ9	137	PJ9 PCS_D3	GPIO DSPI_D Peripheral Chip Select	I/O I/O	V _{DDE2}	SH	—	—	—	26	K1	
PJ10	138	PJ10 PCS_D2	GPIO DSPI_D Peripheral Chip Select	I/O I/O	V _{DDE2}	SH	—	—	—	25	J4	
PJ11	139	PJ11 PCS_D1	GPIO DSPI_D Peripheral Chip Select	I/O I/O	V _{DDE2}	SH	—	—	—	19	H3	
PJ12	140	PJ12 PCS_D0	GPIO DSPI_D Peripheral Chip Select	I/O I/O	V _{DDE2}	SH	—	—	—	18	H2	
PJ13	141	PJ13 SCK_D	GPIO DSPI_D Clock	I/O I/O	V _{DDE2}	SH	—	—	—	16	G4	
PJ14	142	PJ14 SOUT_D	GPIO DSPI_D Serial Out	I/O O	V _{DDE2}	SH	—	—	—	15	G3	
PJ15	143	PJ15 SIN_D	GPIO DSPI_D Serial In	I/O I	V _{DDE2}	SH	—	—	—	13	G1	
Port K (2)												
PK0	144	PK0 EXTAL32	GPIO 32 kHz Crystal Oscillator Input	I I	V _{DDA}	AE + IH	—	—	—	168	B6	
PK1	145	PK1 XTAL32	GPIO 32 kHz Crystal Oscillator Output	I O	V _{DDA}	AE + IH	—	—	—	166	A6	
Miscellaneous Pins (9)												
EXTAL	—	EXTAL EXTCLK	Main Crystal Oscillator Input External Clock Input	I I	V _{DDSYN}	AE	EXTAL			75	91	N16
XTAL	—	XTAL	Main Crystal Oscillator Output	O	V _{DDSYN}	AE	XTAL			74	90	P16
TMS	—	TMS	JTAG Test Mode Select Input	I	V _{DDE3}	SH	TMS (Pull Up)			72	88	T15
TCK	—	TCK	JTAG Test Clock Input	I	V _{DDE3}	IH	TCK (Pull Down)			71	87	R14
TDO	—	TDO	JTAG Test Data Output	O	V _{DDE3}	MH	TDO (Pull Up ⁹)			70	86	T14
TDI	—	TDI	JTAG Test Data Input	I	V _{DDE3}	IH	TDI (Pull Up)			69	85	R13
JCOMP	—	JCOMP	JTAG Compliancy	I	V _{DDE3}	IH	JCOMP (Pull Down)			68	84	T13
TEST ¹⁰	—	TEST	Test Mode Select	I	V _{DDE3}	IH	TEST			62	78	R11
$\overline{\text{RESET}}$	—	$\overline{\text{RESET}}$	External Reset	I/O	V _{DDE2}	SH	$\overline{\text{RESET}}$ (Pull Up)			10	10	E4

¹ The GPIO number is the same as the corresponding pad configuration register (SIU_PCR*n*) number.

² This column lists the functions associated with the programming of the SIU_PCR*n*[PA] bit field in the following order: GPIO, function 1, function 2, and function 3. The unused functions by a given pin begin with function 3, then function 2, then function 1.

³ These are nominal voltages. Each segment provides the power and ground for the given set of I/O pins.

⁴ Pad types: SH - Bi-directional slow speed pad with input hysteresis; MH - Bi-directional medium speed pad with input hysteresis; IH - Input only pad with input hysteresis; AE/A - Analog pad.

⁵ A dash for the function in this column denotes the input and output buffer are turned off.

- ⁶ Port A[14:15]—EXTAL32 and XTAL32 functions only apply on the 144LQFP. These functions are on PortK[0:1] for the 176LQFP and 208BGA. In the 176 LQFP and 208 BGA packages, activity on PA14 should be minimized if the 32kHz XTAL is enabled.
- ⁷ This analog input pin has reduced analog-to-digital conversion accuracy compared to PA0–PA15. See eQADC spec #11 (Total Unadjusted Error for single ended conversions with calibration) for further notes on this.
- ⁸ The NEXUS function is selected when the JTAG TAP controller is enabled via the JCOMP pin and the appropriate bits in the NP PCR register. The value of the PA field in the associated PCR register has no effect on the pin function when the NEXUS function is selected.
- ⁹ Pullup is enabled only when JCOMP is negated.
- ¹⁰ Always connect the TEST pin to Ground (V_{SS}).

1.2 Power and Ground Supply Summary

Table 2. MPC5510 Power/Ground

Pin Name	Function Description	Voltage ¹	Package Pin Locations		
			144	176	208
V _{DDR}	Voltage Regulator Supply	5.0 V	46	56	T6
V _{DDA}	Analog Power	5.0 V	144	176	A2
V _{RH} ²	eQADC Voltage Reference High	5.0 V			B3
V _{SSA}	Analog Ground	–	141	173	A4
V _{RL} ³	eQADC Voltage Reference Low	–			B4
REFBYPC	eQADC Reference Bypass Capacitor	V _{SSA}	1	1	B1
V _{PP} ⁴	Flash Program/Erase Power	5.0 V	78	94	P15
V _{DDSYN} ⁵	Clock Synthesizer Power	3.3 V	73	89	R16
V _{SSSYN}	Clock Synthesizer Ground	–	76	92	M16
V _{DDE1}	External I/O Power	3.3 V – 5.0 V	96,119	105,120, 143,155	A15,D10,E13, G16,K15
V _{DDE2}			16,33,48	21,41,58	H4,L4,N5,P1
V _{DDE3}			61	71,77	N9,T11
V _{SSE1}	External I/O Ground	–	95,118	104,119, 142,154	Shorted to V _{SS} in the package
V _{SSE2}			15,32,47	20,40,57	Shorted to V _{SS} in the package
V _{SSE3}			60	70,76	Shorted to V _{SS} in the package
V _{DD33} ⁵	3.3 V I/O Power	3.3 V	77	93	N15
V _{FLASH} ^{5,6}	Flash Read Power				
V _{DD} ⁵	Internal Logic Power	1.5 V	31,53,79	39,63,95	A1,A16,B2,B15, R2,R15,T1,T16
V _{DDF} ⁵	Flash Internal Logic Power				79
V _{SS}	Ground	–	80	96	C3,C14,D4,D13, G7-G10,H7-H10, J7-J10,K7-K10, N4,N13,P3,P14
V _{SSF}	Flash Internal Logic Ground				Shorted to V _{SS} in the package

¹ These are nominal voltages.

² V_{RH} is shorted to V_{DDA} in the 144LQFP and 176 LQFP packages.

Pin Assignments and Reset States

- ³ V_{RL} is shorted to V_{SSA} in the 144LQFP and 176 LQFP packages.
- ⁴ V_{PP} requires 5V for program/erase operations, but may be 0-5V otherwise. V_{PP} should not go high or low when the device is in Sleep mode.
- ⁵ Voltage generated from internal voltage regulator and no external connection or load allowed except the required bypass capacitors.
- ⁶ V_{FLASH} is shorted to V_{DD33} in the package.

1.3 Pinout – 144 LQFP

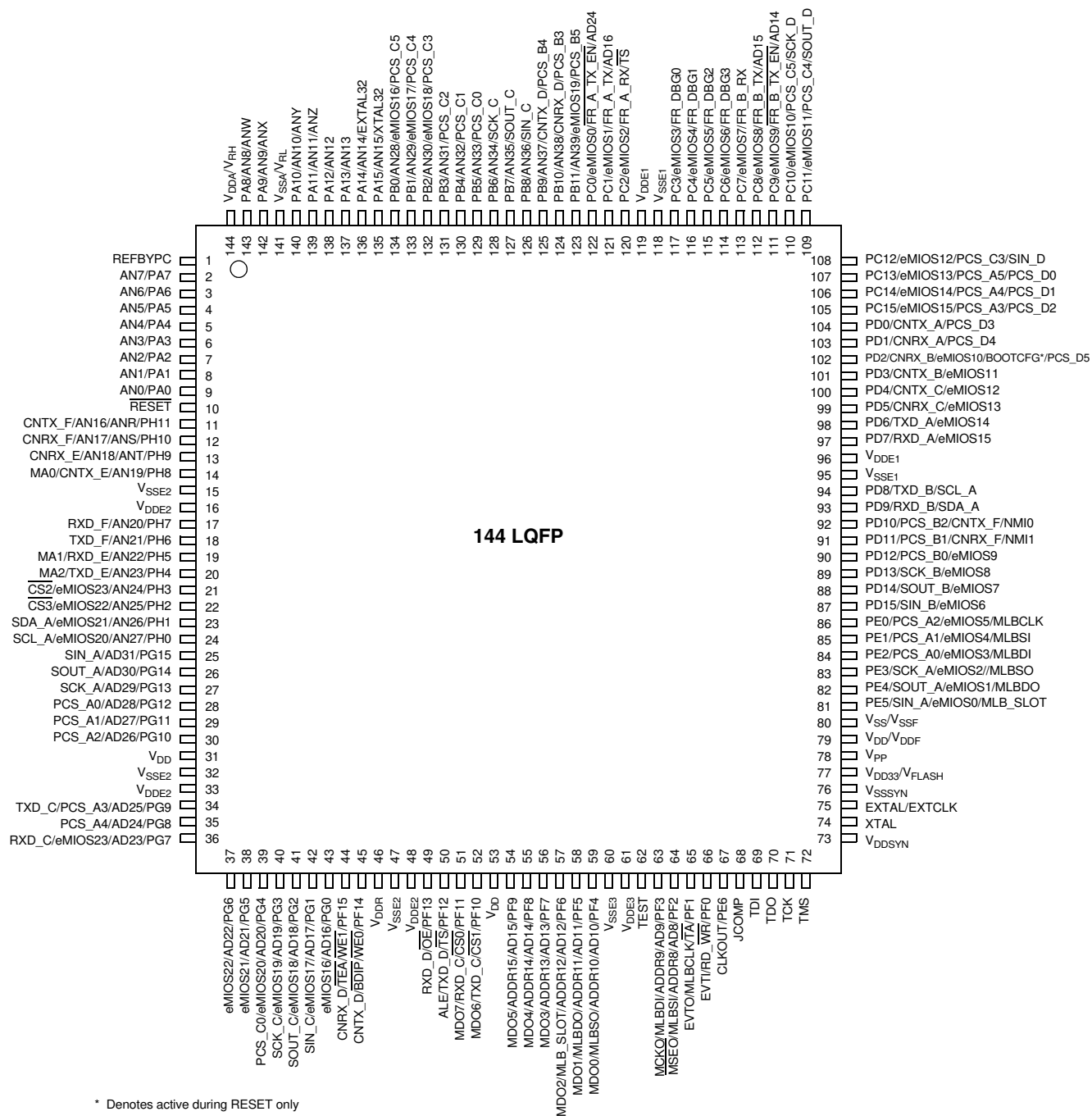


Figure 2. MPC5510 Pinout – 144 LQFP

1.4 Pinout – 176 LQFP

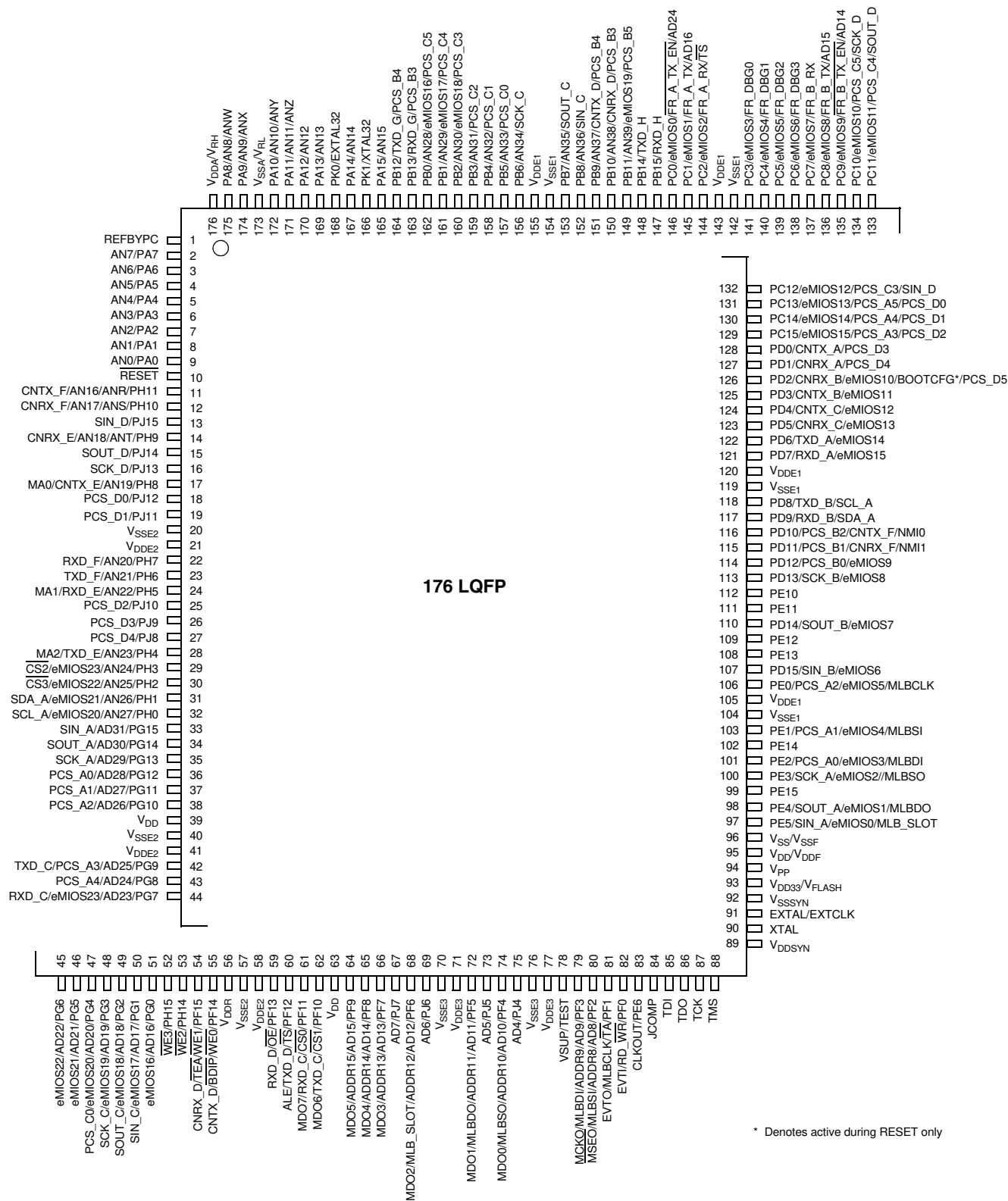


Figure 3. MPC5510 Pinout – 176 LQFP

1.5 Pinout – 208 PBGA

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16																	
A	V _{DD}	V _{DDA}	PA8	V _{SSA}	PA13	PK1	PB12	PB2	PB6	PB10	PB15	PC3	PC7	PC10	V _{DDE1}	V _{DD}	A																
B	REF BYPC	V _{DD}	V _{RH}	V _{RL}	PA12	PK0	PB13	PB3	PB7	PB11	PC0	PC4	PC8	PC11	V _{DD}	PC12	B																
C	PA7	PA6	V _{SS}	PA9	PA11	PA15	PB0	PB4	PB8	PB14	PC1	PC5	PC9	V _{SS}	PC13	PC14	C																
D	PA5	PA4	PA3	V _{SS}	PA10	PA14	PB1	PB5	PB9	V _{DDE1}	PC2	PC6	V _{SS}	PC15	PD0	PD1	D																
E	PA2	PA1	PA0	RESET	<p style="text-align: center;">208 PBGA Ball Map (as viewed from top through the package)</p> <table border="1" style="margin: auto;"> <tr><td>V_{SS}</td><td>V_{SS}</td><td>V_{SS}</td><td>V_{SS}</td></tr> <tr><td>V_{SS}</td><td>V_{SS}</td><td>V_{SS}</td><td>V_{SS}</td></tr> <tr><td>V_{SS}</td><td>V_{SS}</td><td>V_{SS}</td><td>V_{SS}</td></tr> <tr><td>V_{SS}</td><td>V_{SS}</td><td>V_{SS}</td><td>V_{SS}</td></tr> </table>								V _{SS}	V _{SS}	V _{SS}	V _{SS}	V _{SS}	V _{SS}	V _{SS}	V _{SS}	V _{SS}	V _{SS}	V _{SS}	V _{SS}	V _{SS}	V _{SS}	V _{SS}	V _{SS}	V _{DDE1}	PD2	PD3	PD4	E
V _{SS}	V _{SS}	V _{SS}	V _{SS}																														
V _{SS}	V _{SS}	V _{SS}	V _{SS}																														
V _{SS}	V _{SS}	V _{SS}	V _{SS}																														
V _{SS}	V _{SS}	V _{SS}	V _{SS}																														
F	PH13	PH12	PH11	PH10																	PD5	PD6	PD7	PD9	F								
G	PJ15	PH9	PJ14	PJ13																	PD8	PD10	PD11	V _{DDE1}	G								
H	PH8	PJ12	PJ11	V _{DDE2}																	PE7	PD12	PD13	PE8	H								
J	PH7	PH6	PH5	PJ10																	PE9	PD14	PE11	PE10	J								
K	PJ9	PJ8	PH4	PH3																	PE12	PD15	V _{DDE1}	PE0	K								
L	PH2	PH1	PH0	V _{DDE2}									PE13	PE1	PE2	PE14	L																
M	PG15	PG14	PG13	PG12									PE3	PE15	PE5	V _{SSSYN}	M																
N	PG11	PG10	PG9	V _{SS}	V _{DDE2}	PF15	PF12	PF8	V _{DDE3}	PJ2	PJ0	PF0	V _{SS}	PE4	V _{DD33}	EXTAL	N																
P	V _{DDE2}	PG8	V _{SS}	PG3	PG0	PF14	PF11	PF7	PJ6	PJ4	PJ1	PF1	PE6	V _{SS}	V _{PP}	XTAL	P																
R	PG7	V _{DD}	PG5	PG2	PH15	PF13	PF10	PJ7	PF5	PJ3	TEST	PF2	TDI	TCK	V _{DD}	V _{DDSYN}	R																
T	V _{DD}	PG6	PG4	PG1	PH14	V _{DDR}	PF9	PF6	PJ5	PF4	V _{DDE3}	PF3	JCOMP	TDO	TMS	V _{DD}	T																

Figure 4. MPC5510 Pinout – 208 PBGA

2 Electrical Characteristics

This section contains detailed information on power considerations, DC/AC electrical characteristics, and AC timing specifications for the MCU.

2.1 Maximum Ratings

Table 3. Absolute Maximum Ratings¹

Num	Characteristic	Symbol	Min	Max ²	Unit
1	5.0V Voltage Regulator Reference Voltage	V_{DDR}	-0.3	6.5	V
2	5.0V Analog Supply Voltage (reference to V_{SSA})	V_{DDA}	-0.3	6.5	V
3	5.0V Flash Program/Erase Voltage	V_{PP}	-0.3	6.5	V
4	3.3V – 5.0V External I/O Supply Voltage ³	V_{DDE1}^4 V_{DDE2}^4 V_{DDE3}^4	-0.3 -0.3 -0.3	6.5 6.5 6.5	V
5	DC Input Voltage ⁵	V_{IN}	-1.0 ⁶	6.5 ⁷	V
6	V_{REF} Differential Voltage	$V_{RH} - V_{RL}$	-0.3	5.5	V
7	V_{RH} to V_{DDA} Differential Voltage	$V_{RH} - V_{DDA}$	-5.5	5.5	V
8	V_{RL} to V_{SSA} Differential Voltage	$V_{RL} - V_{SSA}$	-0.3	0.3	V
9	V_{DDR} to V_{DDA} Differential Voltage	$V_{DDR} - V_{DDA}$	- V_{DDA}	0.3	V
10	Maximum DC Digital Input Current ⁸ (per pin, applies to all digital MH, SH, and IH pins)	I_{MAXD}	-2	2	mA
11	Maximum DC Analog Input Current ⁹ (per pin, applies to all analog AE and A pins)	I_{MAXA}	-3	3	mA
12	Storage Temperature Range	T_{STG}	-55.0	150.0	°C
13	Maximum Solder Temperature ¹⁰	T_{SDR}	—	260.0	°C
14	Moisture Sensitivity Level ¹¹	MSL	—	3	

¹ Functional operating conditions are given in the DC electrical specifications. Absolute maximum ratings are stress ratings only, and functional operation at the maxima is not guaranteed. Stress beyond the listed maxima may affect device reliability or cause permanent damage to the device.

² Absolute maximum voltages are currently maximum burn-in voltages. Absolute maximum specifications for device stress have not yet been determined.

³ All functional non-supply I/O pins are clamped to V_{SS} and V_{DDE} .

⁴ V_{DDE1} , V_{DDE2} , and V_{DDE3} are separate power segments and may be powered independently with no differential voltage constraints between the power segments.

⁵ AC signal over and undershoot of the input voltages of up to +/- 2.0 volts is permitted for a cumulative duration of 60 hours over the complete lifetime of the device (injection current does not need to be limited for this duration).

⁶ Internal structures will hold the input voltage above -1.0 volt if the injection current limit of 2mA is met.

⁷ Internal structures hold the input voltage below this maximum voltage on all pads powered by V_{DDE} supplies, if the maximum injection current specification is met (2 mA for all pins) and V_{DDE} is within Operating Voltage specifications.

⁸ Total injection current for all pins (including both digital and analog) must not exceed 25mA.

⁹ Total injection current for all analog input pins must not exceed 15mA.

¹⁰ Solder profile per CDF-AEC-Q100.

¹¹ Moisture sensitivity per JEDEC test method A112.

2.2 Thermal Characteristics

Table 4. Thermal Characteristics

Num	Characteristic	Symbol	Unit	Value		
				208 MAPBGA	176 LQFP	144 LQFP
1	Junction to Ambient ^{1, 2} Natural Convection (Single layer board)	$R_{\theta JA}$	°C/W	44	38	43
2	Junction to Ambient ^{1, 3} Natural Convection (Four layer board 2s2p)	$R_{\theta JA}$	°C/W	27	31	34
3	Junction to Ambient ^{1, 3} (@200 ft./min., Single layer board)	$R_{\theta JMA}$	°C/W	35	30	34
4	Junction to Ambient ^{1, 3} (@200 ft./min., Four layer board 2s2p)	$R_{\theta JMA}$	°C/W	24	25	28
5	Junction to Board ⁴	$R_{\theta JB}$	°C/W	16	20	22
6	Junction to Case ⁵	$R_{\theta JC}$	°C/W	8	6	7
7	Junction to Package Top ⁶ Natural Convection	Ψ_{JT}	°C/W	2	2	2

¹ Junction temperature is a function of on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.

² Per SEMI G38-87 and JEDEC JESD51-2 with the single layer board horizontal.

³ Per JEDEC JESD51-6 with the board horizontal.

⁴ Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.

⁵ Indicates the average thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1) with the cold plate temperature used for the case temperature.

⁶ Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2.

2.2.1 General Notes for Specifications at Maximum Junction Temperature

An estimation of the chip junction temperature, T_J , can be obtained from the equation:

$$T_J = T_A + (R_{\theta JA} \times P_D) \quad \text{Eqn. 1}$$

where:

$$T_A = \text{ambient temperature for the package (}^\circ\text{C)} \quad \text{Eqn. 2}$$

$$R_{\theta JA} = \text{junction to ambient thermal resistance (}^\circ\text{C/W)} \quad \text{Eqn. 3}$$

$$P_D = \text{power dissipation in the package (W)} \quad \text{Eqn. 4}$$

The supplied thermal resistances are provided based on JEDEC JESD51 series of standards to provide consistent values for estimations and comparisons. The difference between the values determined on the single-layer (1s) board and on the four-layer board with two signal layers and a power and a ground plane (2s2p) clearly demonstrate that the effective thermal resistance of

Electrical Characteristics

the component is not a constant. It depends on the construction of the application board (number of planes), the effective size of the board which cools the component, how well the component is thermally and electrically connected to the planes, and the power being dissipated by adjacent components.

Connect all the ground and power balls to the respective planes with one via per ball. Using fewer vias to connect the package to the planes reduces the thermal performance. Thinner planes also reduce the thermal performance. When the clearance between through vias leave the planes virtually disconnected, the thermal performance is also greatly reduced.

As a general rule, the value obtained on a single layer board is appropriate for the tightly packed printed circuit board. The value obtained on the board with the internal planes is usually appropriate if the application board has one oz (35 micron nominal thickness) internal planes, the components are well separated, and the overall power dissipation on the board is less than 0.02 W/cm².

The thermal performance of any component depends strongly on the power dissipation of surrounding components. In addition, the ambient temperature varies widely within the application. For many natural convection and especially closed box applications, the board temperature at the perimeter (edge) of the package is approximately the same as the local air temperature near the device. Specifying the local ambient conditions explicitly as the board temperature provides a more precise description of the local ambient conditions that determine the temperature of the device.

At a known board temperature, the junction temperature is estimated using the following equation:

$$T_J = T_B + (R_{\theta JB} \times P_D) \quad \text{Eqn. 5}$$

where:

$$T_J = \text{junction temperature (}^\circ\text{C)} \quad \text{Eqn. 6}$$

$$T_B = \text{board temperature at the package perimeter (}^\circ\text{C/W)} \quad \text{Eqn. 7}$$

$$R_{\theta JB} = \text{junction to board thermal resistance (}^\circ\text{C/W) per JESD51-8} \quad \text{Eqn. 8}$$

$$P_D = \text{power dissipation in the package (W)} \quad \text{Eqn. 9}$$

When the heat loss from the package case to the air can be ignored, acceptable predictions of junction temperature can be made. The application board should be similar to the thermal test condition, with the component soldered to a board with internal planes.

Historically, the thermal resistance has frequently been expressed as the sum of a junction to case thermal resistance and a case to ambient thermal resistance:

$$R_{\theta JA} = R_{\theta JC} + R_{\theta CA} \quad \text{Eqn. 10}$$

where:

$$R_{\theta JA} = \text{junction to ambient thermal resistance (}^\circ\text{C/W)} \quad \text{Eqn. 11}$$

$$R_{\theta JC} = \text{junction to case thermal resistance (}^\circ\text{C/W)} \quad \text{Eqn. 12}$$

$$R_{\theta CA} = \text{case to ambient thermal resistance (}^\circ\text{C/W)} \quad \text{Eqn. 13}$$

$R_{\theta JC}$ is device related and cannot be influenced by the user. The user controls the thermal environment to change the case to ambient thermal resistance, $R_{\theta CA}$. For instance, the user can change the air flow around the device, add a heat sink, change the mounting arrangement on printed circuit board, or change the thermal dissipation on the printed circuit board surrounding the

device. This description is most useful for packages with heat sinks where some 90% of the heat flow is through the case to the heat sink to ambient. For most packages, a better model is required.

A more accurate two-resistor thermal model can be constructed from the junction to board thermal resistance and the junction to case thermal resistance. The junction to case covers the situation where a heat sink will be used or where a substantial amount of heat is dissipated from the top of the package. The junction to board thermal resistance describes the thermal performance when most of the heat is conducted to the printed circuit board. This model can be used for either hand estimations or for a computational fluid dynamics (CFD) thermal model.

To determine the junction temperature of the device in the application after prototypes are available, the Thermal Characterization Parameter (Ψ_{JT}) can be used to determine the junction temperature with a measurement of the temperature at the top center of the package case using the following equation:

$$T_J = T_T + (\Psi_{JT} \times P_D) \quad \text{Eqn. 14}$$

where:

$$T_T = \text{thermocouple temperature on top of the package (}^\circ\text{C)} \quad \text{Eqn. 15}$$

$$\Psi_{JT} = \text{thermal characterization parameter (}^\circ\text{C/W)} \quad \text{Eqn. 16}$$

$$P_D = \text{power dissipation in the package (W)} \quad \text{Eqn. 17}$$

The thermal characterization parameter is measured per JESD51-2 specification using a 40-gauge type T thermocouple epoxied to the top center of the package case. The thermocouple should be positioned so that the thermocouple junction rests on the package. A small amount of epoxy is placed over the thermocouple junction and over about 1 mm of wire extending from the junction. The thermocouple wire is placed flat against the package case to avoid measurement errors caused by cooling effects of the thermocouple wire.

References:

Semiconductor Equipment and Materials International
 805 East Middlefield Rd
 Mountain View, CA 94043
 (415) 964-5111

MIL-SPEC and EIA/JESD (JEDEC) specifications are available from Global Engineering Documents at 800-854-7179 or 303-397-7956.

JEDEC specifications are available on the WEB at <http://www.jedec.org>.

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2.3 ESD Characteristics

Table 5. ESD Ratings^{1, 2}

Characteristic	Symbol	Value	Unit
ESD for Human Body Model (HBM)		2000	V
HBM Circuit Description	R1	1500	Ohm
	C	100	pF
ESD for Field Induced Charge Model (FDCM)		500 (all pins)	V
		750 (corner pins)	
Number of Pulses per pin:			
Positive Pulses (HBM)	—	1	—
Negative Pulses (HBM)	—	1	—
Interval of Pulses	—	1	second

¹ All ESD testing is in conformity with CDF-AEC-Q100 Stress Test Qualification for Automotive Grade Integrated Circuits.

² A device will be defined as a failure if after exposure to ESD pulses the device no longer meets the device specification requirements. Complete DC parametric and functional testing shall be performed per applicable device specification at room temperature followed by hot temperature, unless specified otherwise in the device specification

2.4 DC Electrical Specifications

Table 6. DC Electrical Specifications

Num	Characteristic	Symbol	Min	Max	Unit
1a	C parts Operating junction temperature range Operating ambient temperature range ¹	T_J T_A	-40 -40	105 85	°C °C
1b	V parts Operating junction temperature range Operating ambient temperature range ¹	T_J T_A	-40 -40	120 105	°C °C
1c	M parts² Operating junction temperature range Operating ambient temperature range ¹	T_J T_A	-40 -40	145 125	°C °C
2	5.0V Voltage Regulator Reference Voltage	V_{DDR}	4.5	5.25	V
3	5.0V Analog Supply Voltage	V_{DDA}	4.5	5.25	V
4	5.0V Flash Program/Erase Voltage ³	V_{PP}	4.5	5.25	V
5	3.3V – 5.0V External I/O Supply Voltage	$V_{DDE1}^{4,5}$ V_{DDE2}^4 V_{DDE3}^4	3.0 3.0 3.0	5.5 5.5 5.5	V
6	Pad (SH/MH/IH) Input High Voltage	V_{IH}	$0.65 \times V_{DDE}$	$V_{DDE} + 0.3$	V
7	Pad (SH/MH/IH) Input Low Voltage	V_{IL}	$V_{SS} - 0.3$	$0.35 \times V_{DDE}$	V
8	Pad (SH/MH/IH) Input Hysteresis	V_{HYS}	$0.1 \times V_{DDE}$	$0.2 \times V_{DDE}$	V
9	Analog (AE/A) Input Voltage	V_{INDC}	$V_{SSA} - 0.3$	$V_{DDA} + 0.3$ see note ⁵	V
10	Slow/Medium I/O Output High Voltage $I_{OH} = -1.0$ mA $I_{OH} = -0.2$ mA	V_{OH}	$0.80 \times V_{DDE}$ $0.95 \times V_{DDE}$	—	V
11	Slow/Medium I/O Output Low Voltage $I_{OL} = 1.0$ mA $I_{OH} = 0.2$ mA	V_{OL}	—	$0.20 \times V_{DDE}$ $0.05 \times V_{DDE}$	V
12	Input Capacitance (Digital Pins: Pad type MH,SH, IH with no A or AE)	C_{IN}	—	7	pF
13	Input Capacitance (Analog Pins: Pad type A, AE, and AE+IH)	C_{IN_A}	—	10	pF
14	Input Capacitance (Shared digital and analog pins: A with SH or MH)	C_{IN_M}	—	12	pF
15	Slow/Medium I/O Weak Pull Up/Down Absolute Current ⁶	I_{ACT}	10	170	μA
16	I/O Input Leakage Current ⁷	I_{INACT_D}	-1.5	1.5	μA
17	DC Injection Current (per pin)	I_{IC}	-2.0	2.0	mA
18	Analog Input Current, Channel Off ⁸ (Analog pins AE and AE+IH)	I_{INACT_A}	-200	200	nA
19	Analog Input Current (Shared digital and analog pins: A with SH or MH)	I_{INACT_AD}	-1.5	1.5	μA
20	V_{RH} to V_{DDA} Differential Voltage	$V_{RH} - V_{DDA}$	-100	100	mV