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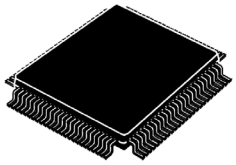
Freescale Semiconductor
Data Sheet: Advance Information

Document Number: MPC5602P
Rev. 6,12/2012

MPC5602P

MPC5602P Microcontroller Data Sheet



100 LQFP (14 mm x 14 mm)

64 LQFP (10 mm x 10 mm)

- Up to 64 MHz, single issue, 32-bit CPU core complex (e200z0h)
  - Compliant with Power Architecture embedded category
  - Variable Length Encoding (VLE)
- Memory organization
  - Up to 256 KB on-chip code flash memory with ECC and erase/program controller
  - Optional: additional 64 (4 × 16) KB on-chip data flash memory with ECC for EEPROM emulation
  - Up to 20 KB on-chip SRAM with ECC
- Fail-safe protection
  - Programmable watchdog timer
  - Non-maskable interrupt
  - Fault collection unit
- Nexus Class 1 interface
- Interrupts and events
  - 16-channel eDMA controller
  - 16 priority level controller
  - Up to 25 external interrupts
  - PIT implements four 32-bit timers
  - 120 interrupts are routed via INTC
- General purpose I/Os
  - Individually programmable as input, output or special function
  - 37 on 64 LQFP
  - 64 on 100 LQFP
- 1 general purpose eTimer unit
  - 6 timers each with up/down capabilities
  - 16-bit resolution, cascadeable counters
  - Quadrature decode with rotation direction flag
  - Double buffer input capture and output compare
- Communications interfaces
  - Up to 2 LINFlex modules (1× Master/Slave, 1× Master only)
  - Up to 3 DSPI channels with automatic chip select generation (up to 8/4/4 chip selects)
  - 1 FlexCAN interface (2.0B Active) with 32 message buffers
  - 1 safety port based on FlexCAN with 32 message buffers and up to 8 Mbit/s at 64 MHz capabilitym usable as second CAN when not used as safety port
- One 10-bit analog-to-digital converter (ADC)
  - Up to 16 input channels (16 ch on 100 LQFP and 12 ch on 64 LQFP)
  - Conversion time < 1 µs including sampling time at full precision
  - Programmable Cross Triggering Unit (CTU)
  - 4 analog watchdogs with interrupt capability
- On-chip CAN/UART bootstrap loader with Boot Assist Module (BAM)
- 1 FlexPWM unit
  - 8 complementary or independent outputs with ADC synchronization signals
  - Polarity control, reload unit
  - Integrated configurable dead time unit and inverter fault input pins
  - 16-bit resolution
  - Lockable configuration
- Clock generation
  - 4–40 MHz main oscillator
  - 16 MHz internal RC oscillator
  - Software-controlled FMPLL capable of up to 64 MHz
- Voltage supply
  - 3.3 V or 5 V supply for I/Os and ADC
  - On-chip single supply voltage regulator with external ballast transistor
- Operating temperature ranges: –40 to 125 °C or –40 to 105 °C

This document contains information on a product under development. Freescale reserves the right to change or discontinue this product without notice.

Table of Contents

1 Introduction

1.1 Document overview

This document provides electrical specifications, pin assignments, and package diagrams for the MPC5601P/2P series of microcontroller units (MCUs). It also describes the device features and highlights important electrical and physical characteristics. For functional characteristics, refer to the device reference manual.

1.2 Description

This 32-bit system-on-chip (SoC) automotive microcontroller family is the latest achievement in integrated automotive application controllers. It belongs to an expanding range of automotive-focused products designed to address chassis applications—specifically, electrical hydraulic power steering (EHPS) and electric power steering (EPS)—as well as airbag applications.

This family is one of a series of next-generation integrated automotive microcontrollers based on the Power Architecture® technology.

The advanced and cost-efficient host processor core of this automotive controller family complies with the Power Architecture embedded category. It operates at speeds of up to 64 MHz and offers high performance processing optimized for low power consumption. It capitalizes on the available development infrastructure of current Power Architecture devices and is supported with software drivers, operating systems and configuration code to assist with users implementations.

1.3 Device comparison

Table 1 provides a summary of different members of the MPC5602P family and their features to enable a comparison among the family members and an understanding of the range of functionality offered within this family.

Table 1. MPC5602P device comparison

Feature	MPC5601P	MPC5602P
Code flash memory (with ECC)	192 KB	256 KB
Data flash memory / EE option (with ECC)	64 KB (optional feature)	
SRAM (with ECC)	12 KB	20 KB
Processor core	32-bit e200z0h	
Instruction set	VLE (variable length encoding)	
CPU performance	0–64 MHz	
FMPLL (frequency-modulated phase-locked loop) module	1	
INTC (interrupt controller) channels	120	
PIT (periodic interrupt timer)	1 (with four 32-bit timers)	
eDMA (enhanced direct memory access) channels	16	
FlexCAN (controller area network)	1[1,2]	2[1,2]
Safety port	Yes (via FlexCAN module)	Yes (via second FlexCAN module)
FCU (fault collection unit)	Yes	
CTU (cross triggering unit)	No	Yes
eTimer	1 (16-bit, 6 channels)	

Table 1. MPC5602P device comparison (continued)

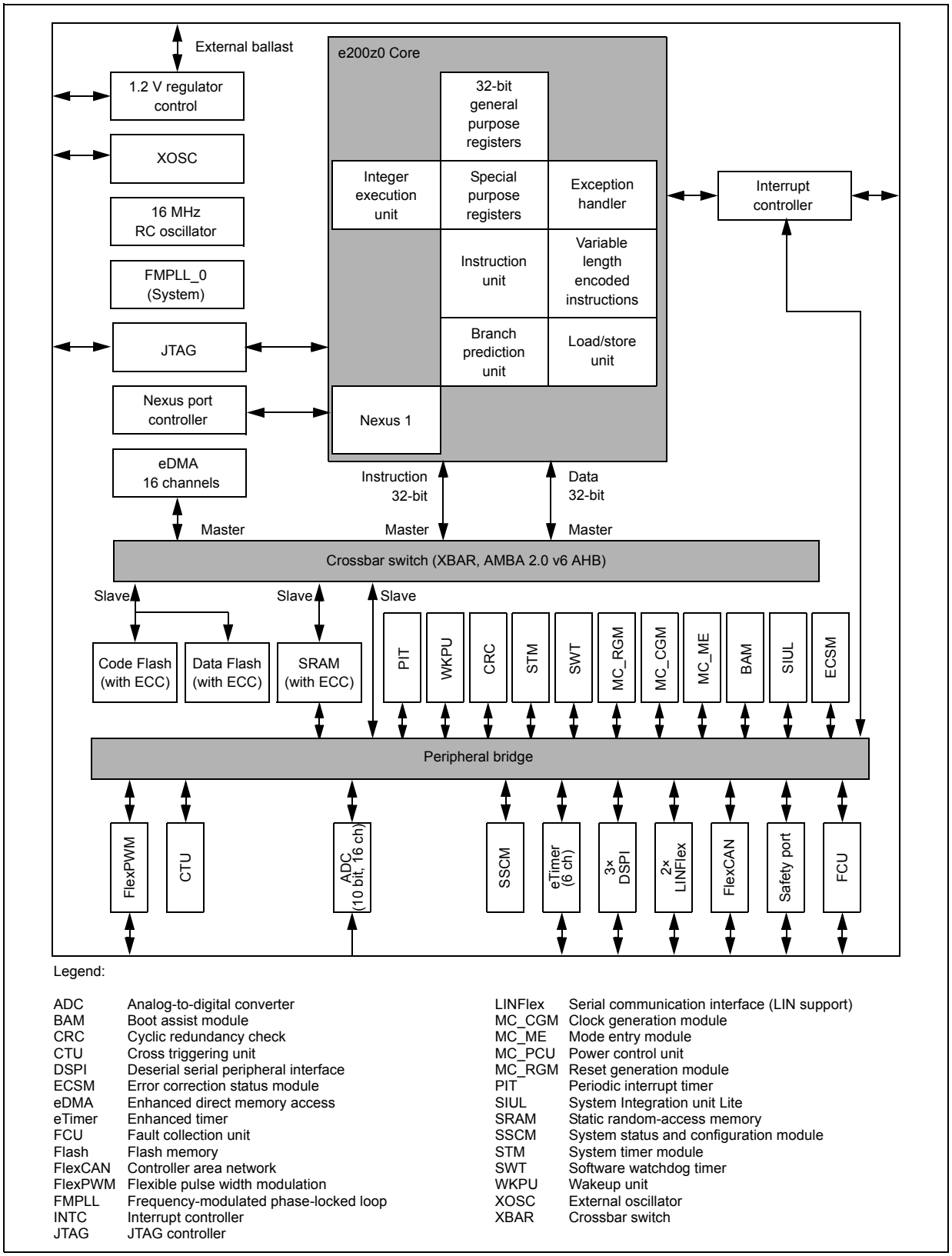
Feature		MPC5601P	MPC5602P
FlexPWM (pulse-width modulation) channels		No	8 (capture capability not supported)
Analog-to-digital converter (ADC)		1 (10-bit, 16 channels)	
LINFlex		1 (1 × Master/Slave)	2 (1 × Master/Slave, 1 × Master only)
DSPI (deserial serial peripheral interface)		1	3
CRC (cyclic redundancy check) unit		Yes	
Junction temperature sensor		No	
JTAG controller		Yes	
Nexus port controller (NPC)		Yes (Nexus Class 1)	
Supply	Digital power supply	3.3 V or 5 V single supply with external transistor	
	Analog power supply	3.3 V or 5 V	
	Internal RC oscillator	16 MHz	
	External crystal oscillator	4–40 MHz	
Packages		64 LQFP 100 LQFP	
Temperature	Standard ambient temperature	–40 to 125 °C	

1 Each FlexCAN module has 32 message buffers.

2 One FlexCAN module can act as a safety port with a bit rate as high as 8 Mbit/s at 64 MHz.

1.4 Block diagram

Figure 1 shows a top-level block diagram of the MPC5602P MCU. Table 1 summarizes the functions of the blocks.



Legend:

ADC	Analog-to-digital converter
BAM	Boot assist module
CRC	Cyclic redundancy check
CTU	Cross triggering unit
DSPI	Deserial serial peripheral interface
ECSM	Error correction status module
eDMA	Enhanced direct memory access
eTimer	Enhanced timer
FCU	Fault collection unit
Flash	Flash memory
FlexCAN	Controller area network
FlexPWM	Flexible pulse width modulation
FMPLL	Frequency-modulated phase-locked loop
INTC	Interrupt controller
JTAG	JTAG controller
LINFlex	Serial communication interface (LIN support)
MC_CGM	Clock generation module
MC_ME	Mode entry module
MC_PCU	Power control unit
MC_RGM	Reset generation module
PIT	Periodic interrupt timer
SIUL	System Integration unit Lite
SRAM	Static random-access memory
SSCM	System status and configuration module
STM	System timer module
SWT	Software watchdog timer
WKPU	Wakeup unit
XOSC	External oscillator
XBAR	Crossbar switch

Figure 1. MPC5602P block diagram

Table 2. MPC5602P series block summary

Block	Function
Analog-to-digital converter (ADC)	Multi-channel, 10-bit analog-to-digital converter
Boot assist module (BAM)	Block of read-only memory containing VLE code which is executed according to the boot mode of the device
Clock generation module (MC_CGM)	Provides logic and control required for the generation of system and peripheral clocks
Controller area network (FlexCAN)	Supports the standard CAN communications protocol
Cross triggering unit (CTU)	Enables synchronization of ADC conversions with a timer event from the eMIOS or from the PIT
Crossbar switch (XBAR)	Supports simultaneous connections between two master ports and three slave ports; supports a 32-bit address bus width and a 32-bit data bus width
Cyclic redundancy check (CRC)	CRC checksum generator
Deserial serial peripheral interface (DSPI)	Provides a synchronous serial interface for communication with external devices
Enhanced direct memory access (eDMA)	Performs complex data transfers with minimal intervention from a host processor via "*n*" programmable channels
Enhanced timer (eTimer)	Provides enhanced programmable up/down modulo counting
Error correction status module (ECSM)	Provides a myriad of miscellaneous control functions for the device including program-visible information about configuration and revision levels, a reset status register, wakeup control for exiting sleep modes, and optional features such as information on memory errors reported by error-correcting codes
External oscillator (XOSC)	Provides an output clock used as input reference for FMPLL_0 or as reference clock for specific modules depending on system needs
Fault collection unit (FCU)	Provides functional safety to the device
Flash memory	Provides non-volatile storage for program code, constants and variables
Frequency-modulated phase-locked loop (FMPLL)	Generates high-speed system clocks and supports programmable frequency modulation
Interrupt controller (INTC)	Provides priority-based preemptive scheduling of interrupt requests
JTAG controller	Provides the means to test chip functionality and connectivity while remaining transparent to system logic when not in test mode
LINFlex controller	Manages a high number of LIN (Local Interconnect Network protocol) messages efficiently with a minimum of CPU load
Mode entry module (MC_ME)	Provides a mechanism for controlling the device operational mode and mode transition sequences in all functional states; also manages the power control unit, reset generation module and clock generation module, and holds the configuration, control and status registers accessible for applications
Periodic interrupt timer (PIT)	Produces periodic interrupts and triggers
Peripheral bridge (PBRIDGE)	Is the interface between the system bus and on-chip peripherals
Power control unit (MC_PCU)	Reduces the overall power consumption by disconnecting parts of the device from the power supply via a power switching device; device components are grouped into sections called "power domains" which are controlled by the PCU

Table 2. MPC5602P series block summary (continued)

Block	Function
Pulse width modulator (FlexPWM)	Contains four PWM submodules, each of which capable of controlling a single half-bridge power stage and two fault input channels
Reset generation module (MC_RGM)	Centralizes reset sources and manages the device reset sequence of the device
Static random-access memory (SRAM)	Provides storage for program code, constants, and variables
System integration unit lite (SIUL)	Provides control over all the electrical pad controls and up 32 ports with 16 bits of bidirectional, general-purpose input and output signals and supports up to 32 external interrupts with trigger event configuration
System status and configuration module (SSCM)	Provides system configuration and status data (such as memory size and status, device mode and security status), device identification data, debug status port enable and selection, and bus and peripheral abort enable/disable
System timer module (STM)	Provides a set of output compare events to support AUTOSAR[1] and operating system tasks
System watchdog timer (SWT)	Provides protection from runaway code
Wakeup unit (WKPU)	Supports up to 18 external sources that can generate interrupts or wakeup events, of which 1 can cause non-maskable interrupt requests or wakeup events

1 AUTOSAR: AUTomotive Open System ARchitecture (see http://www.autosar.org)

1.5 Feature details

1.5.1 High performance e200z0 core processor

The e200z0 Power Architecture core provides the following features:

- High performance e200z0 core processor for managing peripherals and interrupts
- Single issue 4-stage pipeline in-order execution 32-bit Power Architecture CPU
- Harvard architecture
- Variable length encoding (VLE), allowing mixed 16- and 32-bit instructions
  - Results in smaller code size footprint
  - Minimizes impact on performance
- Branch processing acceleration using lookahead instruction buffer
- Load/store unit
  - 1-cycle load latency
  - Misaligned access support
  - No load-to-use pipeline bubbles
- Thirty-two 32-bit general purpose registers (GPRs)
- Separate instruction bus and load/store bus Harvard architecture
- Hardware vectored interrupt support
- Reservation instructions for implementing read-modify-write constructs
- Long cycle time instructions, except for guarded loads, do not increase interrupt latency
- Extensive system development support through Nexus debug port
- Non-maskable interrupt support

1.5.2 Crossbar switch (XBAR)

The XBAR multi-port crossbar switch supports simultaneous connections between three master ports and three slave ports. The crossbar supports a 32-bit address bus width and a 32-bit data bus width.

The crossbar allows for two concurrent transactions to occur from any master port to any slave port; but one of those transfers must be an instruction fetch from internal flash memory. If a slave port is simultaneously requested by more than one master port, arbitration logic will select the higher priority master and grant it ownership of the slave port. All other masters requesting that slave port will be stalled until the higher priority master completes its transactions. Requesting masters will be treated with equal priority and will be granted access a slave port in round-robin fashion, based upon the ID of the last master to be granted access.

The crossbar provides the following features:

- 3 master ports:
  - e200z0 core complex instruction port
  - e200z0 core complex Load/Store Data port
  - eDMA
- 3 slave ports:
  - Flash memory (Code and Data)
  - SRAM
  - Peripheral bridge
- 32-bit internal address, 32-bit internal data paths
- Fixed Priority Arbitration based on Port Master
- Temporary dynamic priority elevation of masters

1.5.3 Enhanced direct memory access (eDMA)

The enhanced direct memory access (eDMA) controller is a second-generation module capable of performing complex data movements via 16 programmable channels, with minimal intervention from the host processor. The hardware micro architecture includes a DMA engine which performs source and destination address calculations, and the actual data movement operations, along with an SRAM-based memory containing the transfer control descriptors (TCD) for the channels.

The eDMA module provides the following features:

- 16 channels support independent 8-, 16- or 32-bit single value or block transfers
- Supports variable-sized queues and circular queues
- Source and destination address registers are independently configured to either post-increment or to remain constant
- Each transfer is initiated by a peripheral, CPU, or eDMA channel request
- Each eDMA channel can optionally send an interrupt request to the CPU on completion of a single value or block transfer
- DMA transfers possible between system memories, DSPIs, ADC, FlexPWM, eTimer and CTU
- Programmable DMA channel multiplexer allows assignment of any DMA source to any available DMA channel with as many as 30 request sources
- eDMA abort operation through software

1.5.4 Flash memory

The MPC5602P provides 320 KB of programmable, non-volatile, flash memory. The non-volatile memory (NVM) can be used for instruction and/or data storage. The flash memory module is interfaced to the system bus by a dedicated flash memory controller. It supports a 32-bit data bus width at the system bus port, and a 128-bit read data interface to flash memory. The module contains four 128-bit wide prefetch buffers. Prefetch buffer hits allow no-wait responses. Normal flash memory array accesses are registered and are forwarded to the system bus on the following cycle, incurring two wait-states.

The flash memory module provides the following features:

- As much as 320 KB flash memory
  - 6 blocks (32 KB + 2×16 KB + 32 KB + 32 KB + 128 KB) code flash memory
  - 4 blocks (16 KB + 16 KB + 16 KB + 16 KB) data flash memory
  - Full Read-While-Write (RWW) capability between code flash memory and data flash memory
- Four 128-bit wide prefetch buffers to provide single cycle in-line accesses (prefetch buffers can be configured to prefetch code or data or both)
- Typical flash memory access time: no wait-state for buffer hits, 2 wait-states for page buffer miss at 64 MHz
- Hardware managed flash memory writes handled by 32-bit RISC Krypton engine
- Hardware and software configurable read and write access protections on a per-master basis
- Configurable access timing allowing use in a wide range of system frequencies
- Multiple-mapping support and mapping-based block access timing (up to 31 additional cycles) allowing use for emulation of other memory types
- Software programmable block program/erase restriction control
- Erase of selected block(s)
- Read page sizes
  - Code flash memory: 128 bits (4 words)
  - Data flash memory: 32 bits (1 word)
- ECC with single-bit correction, double-bit detection for data integrity
  - Code flash memory: 64-bit ECC
  - Data flash memory: 32-bit ECC
- Embedded hardware program and erase algorithm
- Erase suspend and program abort
- Censorship protection scheme to prevent flash memory content visibility
- Hardware support for EEPROM emulation

1.5.5 Static random access memory (SRAM)

The MPC5602P SRAM module provides up to 20 KB of general-purpose memory.

ECC handling is done on a 32-bit boundary and is completely software compatible with MPC55xx family devices containing an e200z6 core and 64-bit wide ECC.

The SRAM module provides the following features:

- Supports read/write accesses mapped to the SRAM from any master
- Up to 20 KB general purpose SRAM
- Supports byte (8-bit), half word (16-bit), and word (32-bit) writes for optimal use of memory
- Typical SRAM access time: no wait-state for reads and 32-bit writes; 1 wait-state for 8- and 16-bit writes if back-to-back with a read to same memory block

1.5.6 Interrupt controller (INTC)

The interrupt controller (INTC) provides priority-based preemptive scheduling of interrupt requests, suitable for statically scheduled hard real-time systems. The INTC handles 128 selectable-priority interrupt sources.

For high-priority interrupt requests, the time from the assertion of the interrupt request by the peripheral to the execution of the interrupt service routine (ISR) by the processor has been minimized. The INTC provides a unique vector for each interrupt request source for quick determination of which ISR has to be executed. It also provides a wide number of priorities so that

lower priority ISRs do not delay the execution of higher priority ISRs. To allow the appropriate priorities for each source of interrupt request, the priority of each interrupt request is software configurable.

When multiple tasks share a resource, coherent accesses to that resource need to be supported. The INTC supports the priority ceiling protocol (PCP) for coherent accesses. By providing a modifiable priority mask, the priority can be raised temporarily so that all tasks which share the same resource can not preempt each other.

The INTC provides the following features:

- Unique 9-bit vector for each separate interrupt source
- 8 software triggerable interrupt sources
- 16 priority levels with fixed hardware arbitration within priority levels for each interrupt source
- Ability to modify the ISR or task priority: modifying the priority can be used to implement the priority ceiling protocol for accessing shared resources.
- 1 external high priority interrupt (NMI) directly accessing the main core and I/O processor (IOP) critical interrupt mechanism

1.5.7 System status and configuration module (SSCM)

The system status and configuration module (SSCM) provides central device functionality.

The SSCM includes these features:

- System configuration and status
  - Memory sizes/status
  - Device mode and security status
  - Determine boot vector
  - Search code flash for bootable sector
  - DMA status
- Debug status port enable and selection
- Bus and peripheral abort enable/disable

1.5.8 System clocks and clock generation

The following list summarizes the system clock and clock generation on the MPC5602P:

- Lock detect circuitry continuously monitors lock status
- Loss of clock (LOC) detection for PLL outputs
- Programmable output clock divider (÷1, ÷2, ÷4, ÷8)
- FlexPWM module and eTimer module running at the same frequency as the e200z0h core
- Internal 16 MHz RC oscillator for rapid start-up and safe mode: supports frequency trimming by user application

1.5.9 Frequency-modulated phase-locked loop (FMPLL)

The FMPLL allows the user to generate high speed system clocks from a 4–40 MHz input clock. Further, the FMPLL supports programmable frequency modulation of the system clock. The PLL multiplication factor, output clock divider ratio are all software configurable.

The FMPLL has the following major features:

- Input clock frequency: 4–40 MHz
- Maximum output frequency: 64 MHz
- Voltage controlled oscillator (VCO)—frequency 256–512 MHz
- Reduced frequency divider (RFD) for reduced frequency operation without forcing the FMPLL to relock

- Frequency-modulated PLL
  - Modulation enabled/disabled through software
  - Triangle wave modulation
- Programmable modulation depth (±0.25% to ±4% deviation from center frequency): programmable modulation frequency dependent on reference frequency
- Self-clocked mode (SCM) operation

1.5.10 Main oscillator

The main oscillator provides these features:

- Input frequency range: 4–40 MHz
- Crystal input mode or oscillator input mode
- PLL reference

1.5.11 Internal RC oscillator

This device has an RC ladder phase-shift oscillator. The architecture uses constant current charging of a capacitor. The voltage at the capacitor is compared by the stable bandgap reference voltage.

The RC oscillator provides these features:

- Nominal frequency 16 MHz
- ±5% variation over voltage and temperature after process trim
- Clock output of the RC oscillator serves as system clock source in case loss of lock or loss of clock is detected by the PLL
- RC oscillator is used as the default system clock during startup

1.5.12 Periodic interrupt timer (PIT)

The PIT module implements these features:

- 4 general-purpose interrupt timers
- 32-bit counter resolution
- Clocked by system clock frequency
- Each channel usable as trigger for a DMA request

1.5.13 System timer module (STM)

The STM implements these features:

- One 32-bit up counter with 8-bit prescaler
- Four 32-bit compare channels
- Independent interrupt source for each channel
- Counter can be stopped in debug mode

1.5.14 Software watchdog timer (SWT)

The SWT has the following features:

- 32-bit time-out register to set the time-out period
- Programmable selection of window mode or regular servicing

- Programmable selection of reset or interrupt on an initial time-out
- Master access protection
- Hard and soft configuration lock bits
- Reset configuration inputs allow timer to be enabled out of reset

1.5.15 Fault collection unit (FCU)

The FCU provides an independent fault reporting mechanism even if the CPU is malfunctioning.

The FCU module has the following features:

- FCU status register reporting the device status
- Continuous monitoring of critical fault signals
- User selection of critical signals from different fault sources inside the device
- Critical fault events trigger 2 external pins (user selected signal protocol) that can be used externally to reset the device and/or other circuitry (for example, a safety relay)
- Faults are latched into a register

1.5.16 System integration unit – Lite (SIUL)

The MPC5602P SIUL controls MCU pad configuration, external interrupt, general purpose I/O (GPIO), and internal peripheral multiplexing.

The pad configuration block controls the static electrical characteristics of I/O pins. The GPIO block provides uniform and discrete input/output control of the I/O pins of the MCU.

The SIUL provides the following features:

- Centralized general purpose input output (GPIO) control of up to 49 input/output pins and 16 analog input-only pads (package dependent)
- All GPIO pins can be independently configured to support pull-up, pull-down, or no pull
- Reading and writing to GPIO supported both as individual pins and 16-bit wide ports
- All peripheral pins, except ADC channels, can be alternatively configured as both general purpose input or output pins
- ADC channels support alternative configuration as general purpose inputs
- Direct readback of the pin value is supported on all pins through the SIUL
- Configurable digital input filter that can be applied to some general purpose input pins for noise elimination
- Up to 4 internal functions can be multiplexed onto 1 pin

1.5.17 Boot and censorship

Different booting modes are available in the MPC5602P: booting from internal flash memory and booting via a serial link.

The default booting scheme uses the internal flash memory (an internal pull-down resistor is used to select this mode). Optionally, the user can boot via FlexCAN or LINFlex (using the boot assist module software).

A censorship scheme is provided to protect the content of the flash memory and offer increased security for the entire device.

A password mechanism is designed to grant the legitimate user access to the non-volatile memory.

1.5.17.1 Boot assist module (BAM)

The BAM is a block of read-only memory that is programmed once and is identical for all MPC560xP devices that are based on the e200z0h core. The BAM program is executed every time the device is powered on if the alternate boot mode has been selected by the user.

The BAM provides the following features:

- Serial bootloading via FlexCAN or LINFlex
- Ability to accept a password via the used serial communication channel to grant the legitimate user access to the non-volatile memory

1.5.18 Error correction status module (ECSM)

The ECSM provides a myriad of miscellaneous control functions regarding program-visible information about the platform configuration and revision levels, a reset status register, a software watchdog timer, wakeup control for exiting sleep modes, and information on platform memory errors reported by error-correcting codes and/or generic access error information for certain processor cores.

The Error Correction Status Module supports a number of miscellaneous control functions for the platform. The ECSM includes these features:

- Registers for capturing information on platform memory errors if error-correcting codes (ECC) are implemented
- For test purposes, optional registers to specify the generation of double-bit memory errors are enabled on the MPC5602P.

The sources of the ECC errors are:

- Flash memory
- SRAM

1.5.19 Peripheral bridge (PBRIDGE)

The PBRIDGE implements the following features:

- Duplicated periphery
- Master access privilege level per peripheral (per master: read access enable; write access enable)
- Write buffering for peripherals
- Checker applied on PBRIDGE output toward periphery
- Byte endianess swap capability

1.5.20 Controller area network (FlexCAN)

The MPC5602P MCU contains one controller area network (FlexCAN) module. This module is a communication controller implementing the CAN protocol according to Bosch Specification version 2.0B. The CAN protocol was designed to be used primarily as a vehicle serial data bus, meeting the specific requirements of this field: real-time processing, reliable operation in the EMI environment of a vehicle, cost-effectiveness and required bandwidth. The FlexCAN module contains 32 message buffers.

The FlexCAN module provides the following features:

- Full implementation of the CAN protocol specification, version 2.0B
  - Standard data and remote frames
  - Extended data and remote frames
  - Up to 8-bytes data length
  - Programmable bit rate up to 1 Mbit/s
- 32 message buffers of up to 8-bytes data length
- Each message buffer configurable as Rx or Tx, all supporting standard and extended messages
- Programmable loop-back mode supporting self-test operation
- 3 programmable mask registers

- Programmable transmit-first scheme: lowest ID or lowest buffer number
- Time stamp based on 16-bit free-running timer
- Global network time, synchronized by a specific message
- Maskable interrupts
- Independent of the transmission medium (an external transceiver is assumed)
- High immunity to EMI
- Short latency time due to an arbitration scheme for high-priority messages
- Transmit features
  - Supports configuration of multiple mailboxes to form message queues of scalable depth
  - Arbitration scheme according to message ID or message buffer number
  - Internal arbitration to guarantee no inner or outer priority inversion
  - Transmit abort procedure and notification
- Receive features
  - Individual programmable filters for each mailbox
  - 8 mailboxes configurable as a 6-entry receive FIFO
  - 8 programmable acceptance filters for receive FIFO
- Programmable clock source
  - System clock
  - Direct oscillator clock to avoid PLL jitter

1.5.21 Safety port (FlexCAN)

The MPC5602P MCU has a second CAN controller synthesized to run at high bit rates to be used as a safety port. The CAN module of the safety port provides the following features:

- Identical to the FlexCAN module
- Bit rate up to 8 Mbit/s at 64 MHz CPU clock using direct connection between CAN modules (no physical transceiver required)
- 32 message buffers of up to 8-bytes data length
- Can be used as a second independent CAN module

1.5.22 Serial communication interface module (LINFlex)

The LINFlex (local interconnect network flexible) on the MPC5602P features the following:

- Supports LIN Master mode (both instances), LIN Slave mode (only one instance) and UART mode
- LIN state machine compliant to LIN1.3, 2.0 and 2.1 specifications
- Handles LIN frame transmission and reception without CPU intervention
- LIN features
  - Autonomous LIN frame handling
  - Message buffer to store Identifier and up to 8 data bytes
  - Supports message length of up to 64 bytes
  - Detection and flagging of LIN errors (sync field, delimiter, ID parity, bit framing, checksum, and time-out)
  - Classic or extended checksum calculation
  - Configurable Break duration of up to 36-bit times
  - Programmable baud rate prescalers (13-bit mantissa, 4-bit fractional)
  - Diagnostic features: Loop back; Self Test; LIN bus stuck dominant detection
  - Interrupt-driven operation with 16 interrupt sources

- LIN slave mode features:
  - Autonomous LIN header handling
  - Autonomous LIN response handling
  - Optional discarding of irrelevant LIN responses using ID filter
- UART mode:
  - Full-duplex operation
  - Standard non return-to-zero (NRZ) mark/space format
  - Data buffers with 4-byte receive, 4-byte transmit
  - Configurable word length (8-bit or 9-bit words)
  - Error detection and flagging
  - Parity, Noise and Framing errors
  - Interrupt-driven operation with four interrupt sources
  - Separate transmitter and receiver CPU interrupt sources
  - 16-bit programmable baud-rate modulus counter and 16-bit fractional
  - 2 receiver wake-up methods

1.5.23 Deserial serial peripheral interface (DSPI)

The deserial serial peripheral interface (DSPI) module provides a synchronous serial interface for communication between the MPC5602P MCU and external devices.

The DSPI modules provide these features:

- Full duplex, synchronous transfers
- Master or slave operation
- Programmable master bit rates
- Programmable clock polarity and phase
- End-of-transmission interrupt flag
- Programmable transfer baud rate
- Programmable data frames from 4 to 16 bits
- Up to 8 chip select lines available:
  - 8 on DSPI_0
  - 4 each on DSPI_1 and DSPI_2
- 8 clock and transfer attributes registers
- Chip select strobe available as alternate function on one of the chip select pins for deglitching
- FIFOs for buffering up to 4 transfers on the transmit and receive side
- Queueing operation possible through use of the I/O processor or eDMA
- General purpose I/O functionality on pins when not used for SPI

1.5.24 Pulse width modulator (FlexPWM)

The pulse width modulator module (PWM) contains four PWM submodules each of which is set up to control a single half-bridge power stage. There are also three fault channels.

This PWM is capable of controlling most motor types: AC induction motors (ACIM), permanent magnet AC motors (PMAC), both brushless (BLDC) and brush DC motors (BDC), switched (SRM) and variable reluctance motors (VRM), and stepper motors.

The FlexPWM block implements the following features:

- 16-bit resolution for center, edge-aligned, and asymmetrical PWMs

- Clock frequency same as that used for e200z0h core
- PWM outputs can operate as complementary pairs or independent channels
- Can accept signed numbers for PWM generation
- Independent control of both edges of each PWM output
- Synchronization to external hardware or other PWM supported
- Double buffered PWM registers
  - Integral reload rates from 1 to 16
  - Half cycle reload capability
- Multiple ADC trigger events can be generated per PWM cycle via hardware
- Write protection for critical registers
- Fault inputs can be assigned to control multiple PWM outputs
- Programmable filters for fault inputs
- Independently programmable PWM output polarity
- Independent top and bottom deadtime insertion
- Each complementary pair can operate with its own PWM frequency and deadtime values
- Individual software-control for each PWM output
- All outputs can be programmed to change simultaneously via a “Force Out” event
- PWMX pin can optionally output a third PWM signal from each submodule
- Channels not used for PWM generation can be used for buffered output compare functions
- Channels not used for PWM generation can be used for input capture functions
- Enhanced dual-edge capture functionality
- eDMA support with automatic reload
- 2 fault inputs
- Capture capability for PWMA, PWMB, and PWMX channels not supported

1.5.25 eTimer

The MPC5602P includes one eTimer module which provides six 16-bit general purpose up/down timer/counter units with the following features:

- Clock frequency same as that used for the e200z0h core
- Individual channel capability
  - Input capture trigger
  - Output compare
  - Double buffer (to capture rising edge and falling edge)
  - Separate prescaler for each counter
  - Selectable clock source
  - 0–100% pulse measurement
  - Rotation direction flag (quad decoder mode)
- Maximum count rate
  - External event counting: max. count rate = peripheral clock/2
  - Internal clock counting: max. count rate = peripheral clock
- Counters are:
  - Cascadable
  - Preloadable
- Programmable count modulo
- Quadrature decode capabilities

- Counters can share available input pins
- Count once or repeatedly
- Pins available as GPIO when timer functionality not in use

1.5.26 Analog-to-digital converter (ADC) module

The ADC module provides the following features:

Analog part:

- 1 on-chip analog-to-digital converter
  - 10-bit AD resolution
  - 1 sample and hold unit
  - Conversion time, including sampling time, less than 1 µs (at full precision)
  - Typical sampling time is 150 ns minimum (at full precision)
  - DNL/INL ±1 LSB
  - TUE < 1.5 LSB
  - Single-ended input signal up to 3.3 V/5.0 V
  - 3.3 V/5.0 V input reference voltage
  - ADC and its reference can be supplied with a voltage independent from V_{DDIO}
  - ADC supply can be equal or higher than V_{DDIO}
  - ADC supply and ADC reference are not independent from each other (both internally bonded to same pad)
  - Sample times of 2 (default), 8, 64 or 128 ADC clock cycles

Digital part:

- 16 input channels
- 4 analog watchdogs comparing ADC results against predefined levels (low, high, range) before results are stored in the appropriate ADC result location
- 2 modes of operation: Motor Control mode or Regular mode
- Regular mode features
  - Register based interface with the CPU: control register, status register and 1 result register per channel
  - ADC state machine managing 3 request flows: regular command, hardware injected command and software injected command
  - Selectable priority between software and hardware injected commands
  - DMA compatible interface
- CTU-controlled mode features
  - Triggered mode only
  - 4 independent result queues (1×16 entries, 2×8 entries, 1×4 entries)
  - Result alignment circuitry (left justified and right justified)
  - 32-bit read mode allows to have channel ID on one of the 16-bit part
  - DMA compatible interfaces

1.5.27 Cross triggering unit (CTU)

The cross triggering unit allows automatic generation of ADC conversion requests on user selected conditions without CPU load during the PWM period and with minimized CPU load for dynamic configuration.

It implements the following features:

- Double buffered trigger generation unit with up to 8 independent triggers generated from external triggers

- Trigger generation unit configurable in sequential mode or in triggered mode
- Each trigger can be appropriately delayed to compensate the delay of external low pass filter
- Double buffered global trigger unit allowing eTimer synchronization and/or ADC command generation
- Double buffered ADC command list pointers to minimize ADC-trigger unit update
- Double buffered ADC conversion command list with up to 24 ADC commands
- Each trigger capable of generating consecutive commands
- ADC conversion command allows to control ADC channel, single or synchronous sampling, independent result queue selection

1.5.28 Nexus Development Interface (NDI)

The NDI (Nexus Development Interface) block is compliant with Nexus Class 1 of the IEEE-ISTO 5001-2003 standard. This development support is supplied for MCUs without requiring external address and data pins for internal visibility. The NDI block is an integration of several individual Nexus blocks that are selected to provide the development support interface for this device. The NDI block interfaces to the host processor and internal busses to provide development support as per the IEEE-ISTO 5001-2003 Nexus Class 1 standard. The development support provided includes access to the MCU's internal memory map and access to the processor's internal registers.

The NDI provides the following features:

- Configured via the IEEE 1149.1
- All Nexus port pins operate at V_{DDIO} (no dedicated power supply)
- Nexus Class 1 supports Static debug

1.5.29 Cyclic redundancy check (CRC)

The CRC computing unit is dedicated to the computation of CRC off-loading the CPU. The CRC module features:

- Support for CRC-16-CCITT ($x25$ protocol):
  - $x^{16} + x^{12} + x^5 + 1$
- Support for CRC-32 (Ethernet protocol):
  - $x^{32} + x^{26} + x^{23} + x^{22} + x^{16} + x^{12} + x^{11} + x^{10} + x^8 + x^7 + x^5 + x^4 + x^2 + x + 1$
- Zero wait states for each write/read operations to the CRC_CFG and CRC_INP registers at the maximum frequency

1.5.30 IEEE 1149.1 JTAG controller

The JTAG controller (JTAGC) block provides the means to test chip functionality and connectivity while remaining transparent to system logic when not in test mode. All data input to and output from the JTAGC block is communicated in serial format. The JTAGC block is compliant with the IEEE standard.

The JTAG controller provides the following features:

- IEEE test access port (TAP) interface 4 pins (TDI, TMS, TCK, TDO)
- Selectable modes of operation include JTAGC/debug or normal system operation.
- 5-bit instruction register that supports the following IEEE 1149.1-2001 defined instructions:
  - BYPASS
  - IDCODE
  - EXTEST
  - SAMPLE
  - SAMPLE/PRELOAD
- 5-bit instruction register that supports the additional following public instructions:
  - ACCESS_AUX_TAP_NPC

— ACCESS_AUX_TAP_ONCE

- 3 test data registers:
  - Bypass register
  - Boundary scan register (size parameterized to support a variety of boundary scan chain lengths)
  - Device identification register
- TAP controller state machine that controls the operation of the data registers, instruction register and associated circuitry

1.5.31 On-chip voltage regulator (VREG)

The on-chip voltage regulator module provides the following features:

- Uses external NPN (negative-positive-negative) transistor
- Regulates external 3.3 V/5.0 V down to 1.2 V for the core logic
- Low voltage detection on the internal 1.2 V and I/O voltage 3.3 V

2 Package pinouts and signal descriptions

2.1 Package pinouts

The LQFP pinouts are shown in the following figures. For pin signal descriptions, please refer to Table 5.

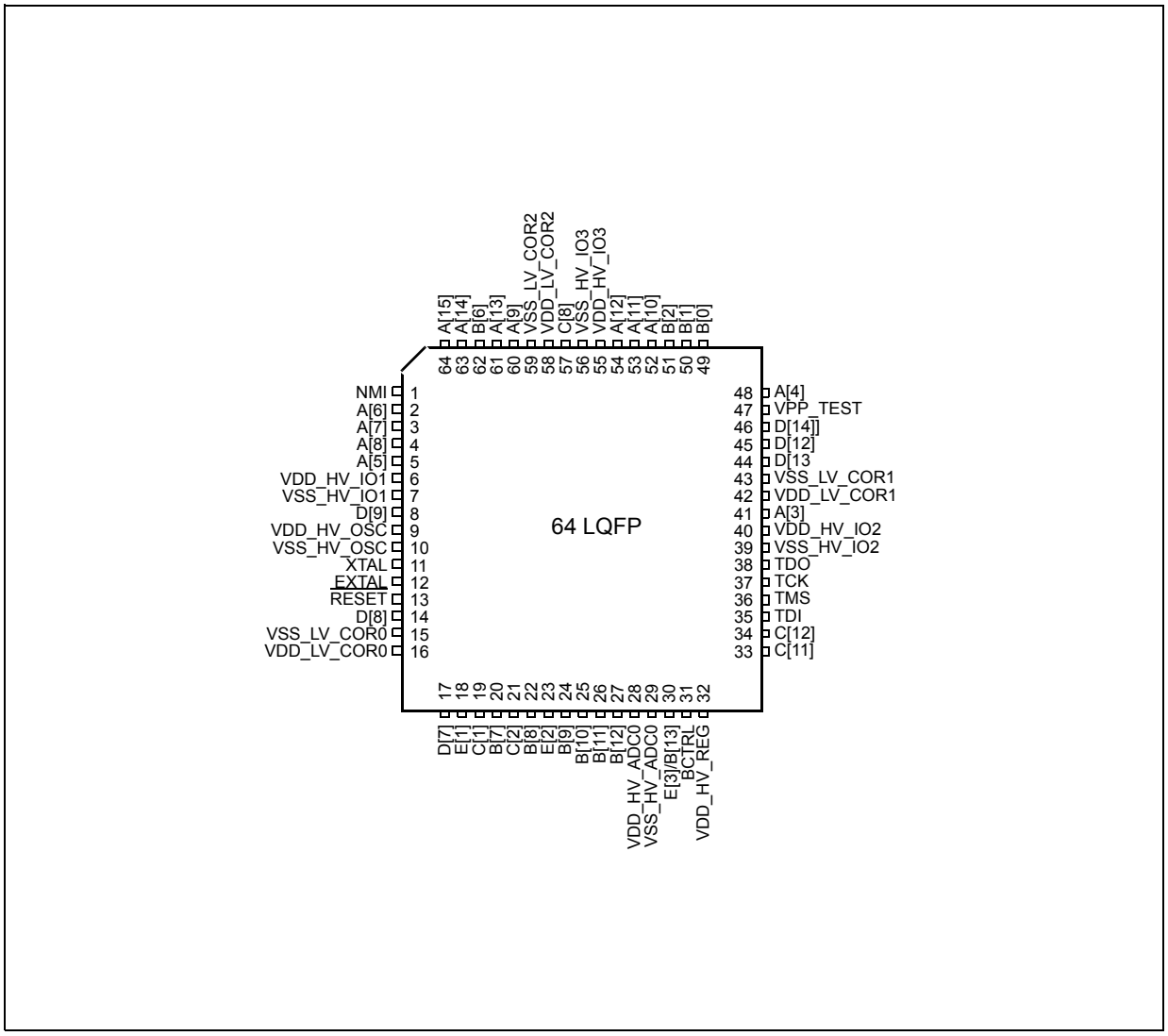


Figure 2. 64-pin LQFP pinout(top view)

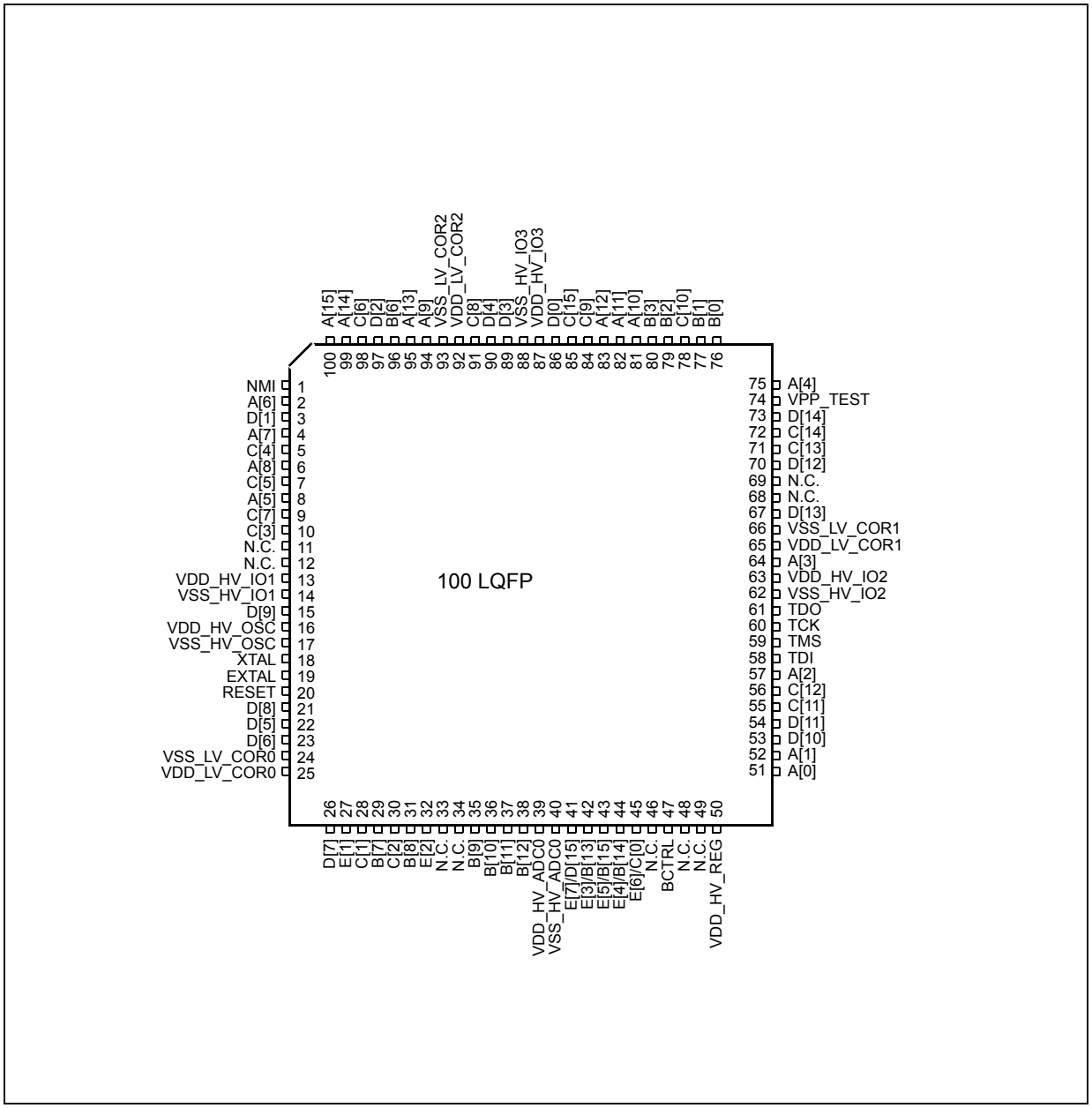


Figure 3. 100-pin LQFP pinout (top view)

2.2 Pin description

The following sections provide signal descriptions and related information about the functionality and configuration of the MPC5602P devices.

2.2.1 Power supply and reference voltage pins

Table 3 lists the power supply and reference voltage for the MPC5602P devices.

Table 3. Supply pins

Supply		Pin	
Symbol	**Description**	**64-pin**	**100-pin**
VREG control and power supply pins. Pins available on 64-pin and 100-pin packages			
BCTRL	Voltage regulator external NPN ballast base control pin	31	47
$V_{DD\_HV\_REG}$ (3.3 V or 5.0 V)	Voltage regulator supply voltage	32	50
ADC_0 reference and supply voltage. Pins available on 64-pin and 100-pin packages			
$V_{DD\_HV\_ADC0}$[1]	ADC_0 supply and high reference voltage	28	39
$V_{SS\_HV\_ADC0}$	ADC_0 ground and low reference voltage	29	40
Power supply pins (3.3 V or 5.0 V). Pins available on 64-pin and 100-pin packages			
$V_{DD\_HV\_IO1}$	Input/output supply voltage	6	13
$V_{SS\_HV\_IO1}$	Input/output ground	7	14
$V_{DD\_HV\_IO2}$	Input/output supply voltage and data Flash memory supply voltage	40	63
$V_{SS\_HV\_IO2}$	Input/output ground and Flash memory HV ground	39	62
$V_{DD\_HV\_IO3}$	Input/output supply voltage and code Flash memory supply voltage	55	87
$V_{SS\_HV\_IO3}$	Input/output ground and code Flash memory HV ground	56	88
$V_{DD\_HV\_OSC}$	Crystal oscillator amplifier supply voltage	9	16
$V_{SS\_HV\_OSC}$	Crystal oscillator amplifier ground	10	17
Power supply pins (1.2 V). Pins available on 64-pin and 100-pin packages			
$V_{DD\_LV\_COR0}$	1.2 V supply pins for core logic and PLL. Decoupling capacitor must be connected between these pins and the nearest $V_{SS\_LV\_COR}$ pin.	16	25
$V_{SS\_LV\_COR0}$	1.2 V supply pins for core logic and PLL. Decoupling capacitor must be connected between these pins and the nearest $V_{DD\_LV\_COR}$ pin.	15	24
$V_{DD\_LV\_COR1}$	1.2 V supply pins for core logic and data Flash. Decoupling capacitor must be connected between these pins and the nearest $V_{SS\_LV\_COR}$ pin.	42	65
$V_{SS\_LV\_COR1}$	1.2 V supply pins for core logic and data Flash. Decoupling capacitor must be connected between these pins and the nearest $V_{DD\_LV\_COR}$ pin.	43	66
$V_{DD\_LV\_COR2}$	1.2 V supply pins for core logic and code Flash. Decoupling capacitor must be connected between these pins and the nearest $V_{SS\_LV\_COR}$ pin.	58	92
$V_{SS\_LV\_COR2}$	1.2 V supply pins for core logic and code Flash. Decoupling capacitor must be connected betwee.n these pins and the nearest $V_{DD\_LV\_COR}$ pin.	59	93

[1] Analog supply/ground and high/low reference lines are internally physically separate, but are shorted via a double-bonding connection on $V_{DD\_HV\_ADCx}$/$V_{SS\_HV\_ADCx}$ pins.

2.2.2 System pins

Table 4 and Table 5 contain information on pin functions for the MPC5602P devices. The pins listed in Table 4 are single-function pins. The pins shown in Table 5 are multi-function pins, programmable via their respective pad configuration register (PCR) values.

Table 4. System pins

Symbol	Description	Direction	Pad speed[1]		Pin	
			SRC = 0	SRC = 1	64-pin	100-pin
Dedicated pins						
NMI	Non-maskable Interrupt	Input only	Slow	—	1	1
XTAL	Analog output of the oscillator amplifier circuit—needs to be grounded if oscillator is used in bypass mode	—	—	—	11	18
EXTAL	Analog input of the oscillator amplifier circuit, when the oscillator is not in bypass mode Analog input for the clock generator when the oscillator is in bypass mode	—	—	—	12	19
TDI	JTAG test data input	Input only	Slow	—	35	58
TMS	JTAG state machine control	Input only	Slow	—	36	59
TCK	JTAG clock	Input only	Slow	—	37	60
TDO	JTAG test data output	Output only	Slow	Fast	38	61
Reset pin						
$\overline{\text{RESET}}$	Bidirectional reset with Schmitt trigger characteristics and noise filter	Bidirectional	Medium	—	13	20
Test pin						
VPP_TEST	Pin for testing purpose only. To be tied to ground in normal operating mode.	—	—	—	47	74

1 SRC values refer to the value assigned to the Slew Rate Control bits of the pad configuration register.

2.2.3 Pin multiplexing

Table 5 defines the pin list and muxing for the MPC5602P devices.

Each row of Table 5 shows all the possible ways of configuring each pin, via alternate functions. The default function assigned to each pin after reset is the ALT0 function.

MPC5602P devices provide three main I/O pad types, depending on the associated functions:

- *Slow pads* are the most common, providing a compromise between transition time and low electromagnetic emission.
- *Medium pads* provide fast enough transition for serial communication channels with controlled current to reduce electromagnetic emission.
- *Fast pads* provide maximum speed. They are used for improved NEXUS debugging capability.

Medium and Fast pads can use slow configuration to reduce electromagnetic emission, at the cost of reducing AC performance. For more information, see “Pad AC Specifications” in the device data sheet.

Table 5. Pin muxing

Port pin	PCR register	Alternate function[1,2]	Functions	Peripheral[3]	I/O direction[4]	Pad speed[5]		Pin	
						SRC = 0	SRC = 1	64-pin	100-pin
Port A (16-bit)									
A[0]	PCR[0]	ALT0 ALT1 ALT2 ALT3 —	GPIO[0] ETC[0] SCK F[0] EIRQ[0]	SIUL eTimer_0 DSPI_2 FCU_0 SIUL	I/O I/O I/O O I	Slow	Medium	—	51
A[1]	PCR[1]	ALT0 ALT1 ALT2 ALT3 —	GPIO[1] ETC[1] SOUT F[1] EIRQ[1]	SIUL eTimer_0 DSPI_2 FCU_0 SIUL	I/O I/O O O I	Slow	Medium	—	52
A[2]	PCR[2]	ALT0 ALT1 ALT2 ALT3 — — —	GPIO[2] ETC[2] — A[3] SIN ABS[0] EIRQ[2]	SIUL eTimer_0 — FlexPWM_0 DSPI_2 MC_RGM SIUL	I/O I/O — O I I I	Slow	Medium	—	57
A[3]	PCR[3]	ALT0 ALT1 ALT2 ALT3 — —	GPIO[3] ETC[3] CS0 B[3] ABS[1] EIRQ[3]	SIUL eTimer_0 DSPI_2 FlexPWM_0 MC_RGM SIUL	I/O I/O I/O O I I	Slow	Medium	41	64
A[4]	PCR[4]	ALT0 ALT1 ALT2 ALT3 — —	GPIO[4] — CS1 ETC[4] FAB EIRQ[4]	SIUL — DSPI_2 eTimer_0 MC_RGM SIUL	I/O — O I/O I I	Slow	Medium	48	75
A[5]	PCR[5]	ALT0 ALT1 ALT2 ALT3 —	GPIO[5] CS0 — CS7 EIRQ[5]	SIUL DSPI_1 — DSPI_0 SIUL	I/O I/O — O I	Slow	Medium	5	8
A[6]	PCR[6]	ALT0 ALT1 ALT2 ALT3 —	GPIO[6] SCK — — EIRQ[6]	SIUL DSPI_1 — — SIUL	I/O I/O — — I	Slow	Medium	2	2
A[7]	PCR[7]	ALT0 ALT1 ALT2 ALT3 —	GPIO[7] SOUT — — EIRQ[7]	SIUL DSPI_1 — — SIUL	I/O O — — I	Slow	Medium	3	4

Table 5. Pin muxing (continued)

Port pin	PCR register	Alternate function[1,2]	Functions	Peripheral[3]	I/O direction[4]	Pad speed[5]		Pin	
						SRC = 0	SRC = 1	64-pin	100-pin
A[8]	PCR[8]	ALT0 ALT1 ALT2 ALT3 — —	GPIO[8] — — — SIN EIRQ[8]	SIUL — — — DSPI_1 SIUL	I/O — — — I I	Slow	Medium	4	6
A[9]	PCR[9]	ALT0 ALT1 ALT2 ALT3 —	GPIO[9] CS1 — B[3] FAULT[0]	SIUL DSPI_2 — FlexPWM_0 FlexPWM_0	I/O O — O I	Slow	Medium	60	94
A[10]	PCR[10]	ALT0 ALT1 ALT2 ALT3 —	GPIO[10] CS0 B[0] X[2] EIRQ[9]	SIUL DSPI_2 FlexPWM_0 FlexPWM_0 SIUL	I/O I/O O O I	Slow	Medium	52	81
A[11]	PCR[11]	ALT0 ALT1 ALT2 ALT3 —	GPIO[11] SCK A[0] A[2] EIRQ[10]	SIUL DSPI_2 FlexPWM_0 FlexPWM_0 SIUL	I/O I/O O O I	Slow	Medium	53	82
A[12]	PCR[12]	ALT0 ALT1 ALT2 ALT3 —	GPIO[12] SOUT A[2] B[2] EIRQ[11]	SIUL DSPI_2 FlexPWM_0 FlexPWM_0 SIUL	I/O O O O I	Slow	Medium	54	83
A[13]	PCR[13]	ALT0 ALT1 ALT2 ALT3 — — —	GPIO[13] — B[2] — SIN FAULT[0] EIRQ[12]	SIUL — FlexPWM_0 — DSPI_2 FlexPWM_0 SIUL	I/O — O — I I I	Slow	Medium	61	95
A[14]	PCR[14]	ALT0 ALT1 ALT2 ALT3 —	GPIO[14] TXD — — EIRQ[13]	SIUL Safety Port_0 — — SIUL	I/O O — — I	Slow	Medium	63	99
A[15]	PCR[15]	ALT0 ALT1 ALT2 ALT3 — —	GPIO[15] — — — RXD EIRQ[14]	SIUL — — — Safety Port_0 SIUL	I/O — — — I I	Slow	Medium	64	100